Field Effect Transistor (FET)

Although BJT are used for amplification: it has some diadvantages like

1. Very low Input Resistance
2. Unstability $(I_C = \beta I_B + (\beta+1) I_{CO})$

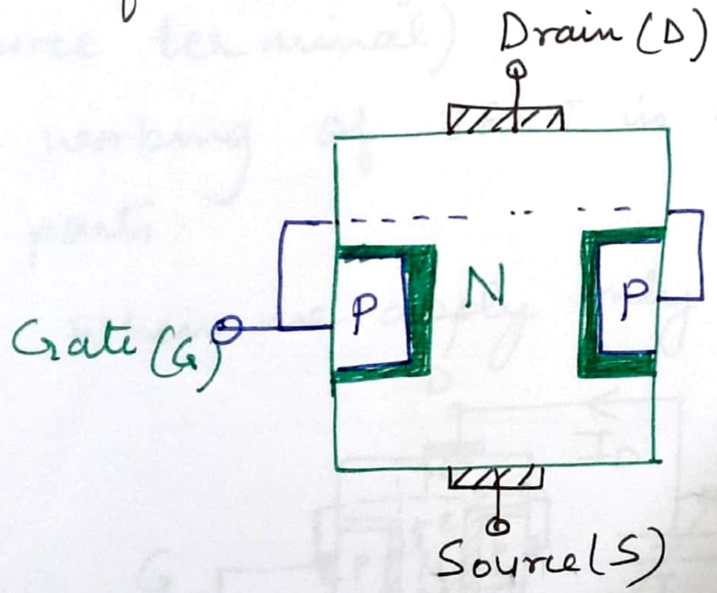
Thus, we make a device which has high input resistance as well as in which the output current does not depends upon the leakage ~~current~~ current named as Field Effect Transistor (FET).

FET

- JFET
  - N-channel
  - P-channel
- MOSFET
  - Enhancement MOSFET
    - N-channel
    - P-channel
  - Depletion MOSFET
    - N-channel
    - P-Channel

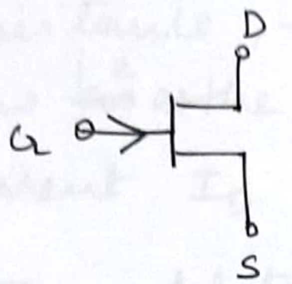
N-Channel JFET (Junction Field Effect Transistor).

Construction :- For N-channel JFET, we have an N-type S/C bar and made two metallic contacts with its named as drain (D) and ~~Gate (G)~~ Source (S). On the other side we dope two p-type S/C. into the N-type which are connected together to form a terminal Gate (G).

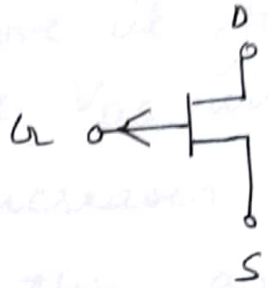


* The path b/w the two P type S/Cs is called channel and since it is made of N-type S/C, therefore it is called N-channel JFET.
* There is a depletion layer b/w the P and N-type and hence no current flows when there is no biasing.

Symbol.



N-channel JFET



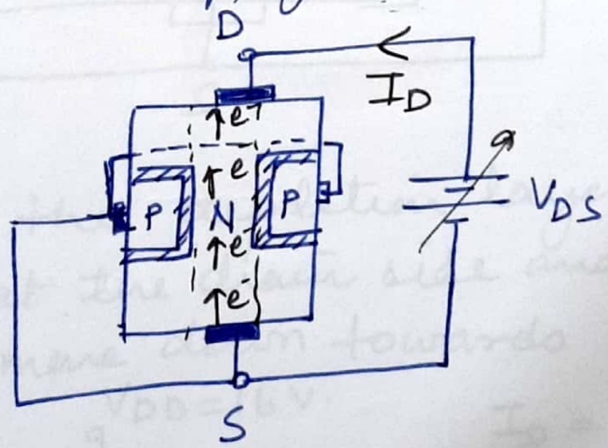
p-channel JFET.

Working.

We apply two voltage V_{GS} (voltage source between Gate and Source terminal) and V_{DS} (voltage source b/w Drain and Source terminal).

The working of JFET is divided into two parts.

1) when we apply only V_{DS} ($V_{GS} = 0$).

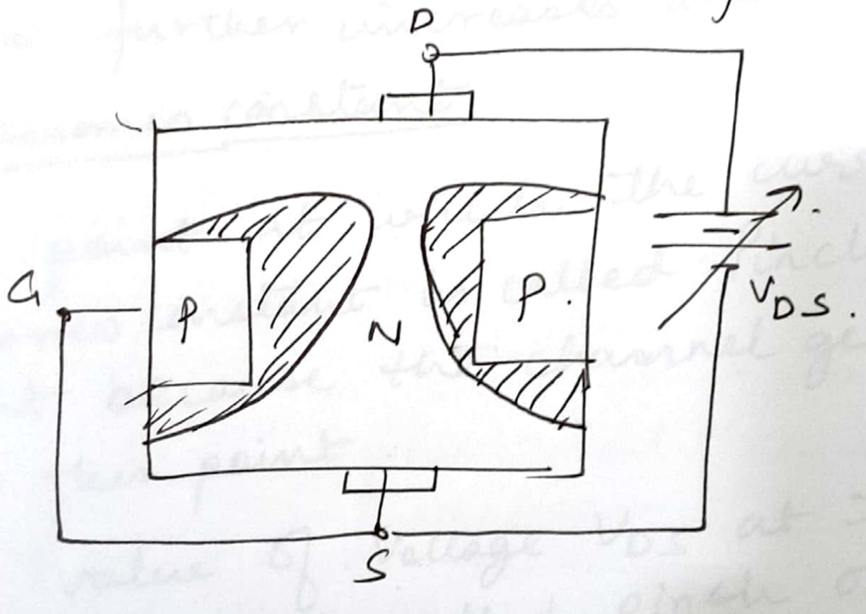


(* Note → +ve terminal is Drain and -ve terminal is source for N-channel.)

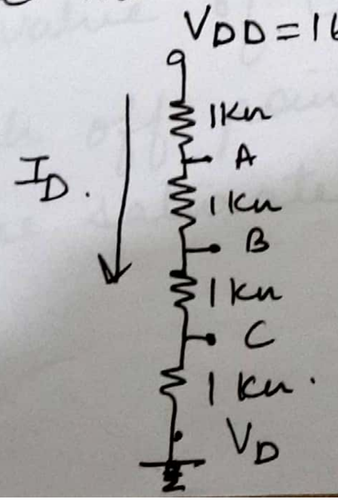
* The negative terminal of the ~~drain~~ source will emit the electrons which travel through the channel and reaches drain, hence we will say that a current I_D will flow through the channel from Drain to Source.

* Since the n-type S/c acts as a resistance, therefore it follows Ohm's law i.e ~~as~~ as the voltage V_{DS} increases the current I_D also increases.

* In addition to this, as we are increasing positive voltage (V_{DS}) in the N-type S/c bar, thus the ~~P-N junction~~ depletion layer at the junction of P-N type S/c also increases as it reverse bias the P-N junction.



Note:- the depletion layer width is higher at the drain side and gets narrower as we move down towards source.



$I_D = \frac{16}{4} = 4mA$.

$V_A = 16 - 4 \times 1 = 12$

$V_B = 16 - 4 \times 2 = 8$

$V_C = 16 - 4 \times 3 = 4$

$V_D = 16 - 4 \times 4 = 0$.

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Thus it shows that as we move down the positive voltage decreases, Hence the depletion layer width is higher at drain side and lower at the source side.

* In this manner, as we keep on increasing V_{DS}, I_D will increase and also the depletion layer width is increasing and a point will come at which the depletion layer from both sides touch each other. and the current will no further increases and hence it <u>becomes constant</u>

The point at which the current becomes constant is called Pinch off point because the channel gets pinched at this point.

* The value of Voltage V_{DS} at the pinch off point is called pinch off Voltage (V_P).

* The value of current I_D at the pinch off point is called Drain to source saturated current (I_{DSS}).

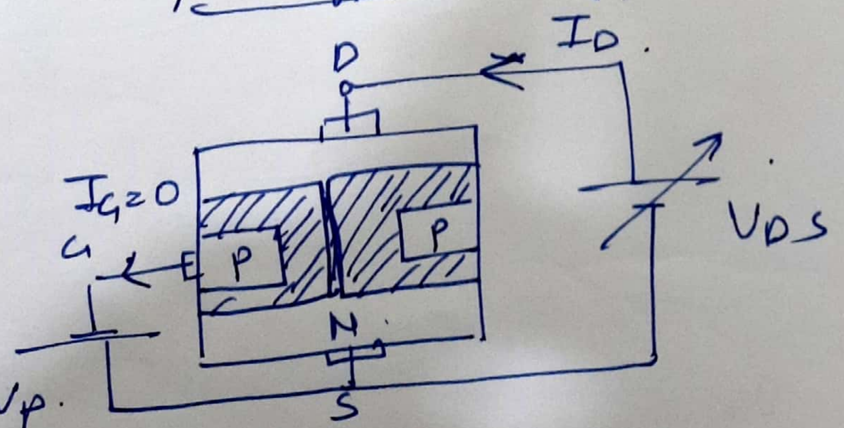
2) <u>when $V_{GS} \neq 0$ V.</u>

* Here, V_{GS} is always (−ve) voltage; ~~so that~~ [Since Gate is made up of p-type S/C].
Thus. P-N junction will always be reverse bias and hence, the input resistance will be very large.

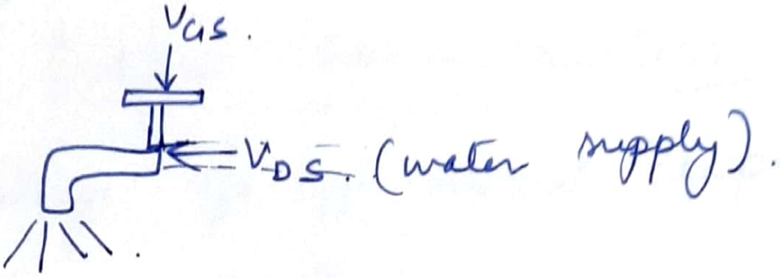
When, we apply negative voltage to the Gate, it will promote the formation of depletion layer. at the P-N junction along with V_{DS} and due to this the pinch-off condition becomes at the less voltage of V_{DS} than the earlier (when $V_{GS} = 0$V) or we can say that the value of I_{DSS} decreases.

As we keep on increasing −ve voltage on the Gate, a point will come at which I_D becomes zero. <u>This is known as cut-off point</u> and the value of V_{GS} is denoted as ($V_{GS\,off}$.)

Note that. $\boxed{V_{GS\,off} = -V_P}$



* The working of JFET is similar to a Tap.



As the tap control the intensity of water coming out. Similarly V_{GS} control the amount of I_D (drain current) and hence FET is known as Voltage Control device.

Relation b/w current and voltage

The relation is given by shockley equation

$$\boxed{I_D = I_{DSS}\left(1 - \left|\frac{V_{GS}}{V_P}\right|\right)^2}$$

where $I_D \rightarrow$ drain Current

$I_{DSS} \rightarrow$ Maximum drain current.

$V_{GS} \rightarrow$ Applied gate to source voltage

$V_P \rightarrow$ Pinch off voltage.

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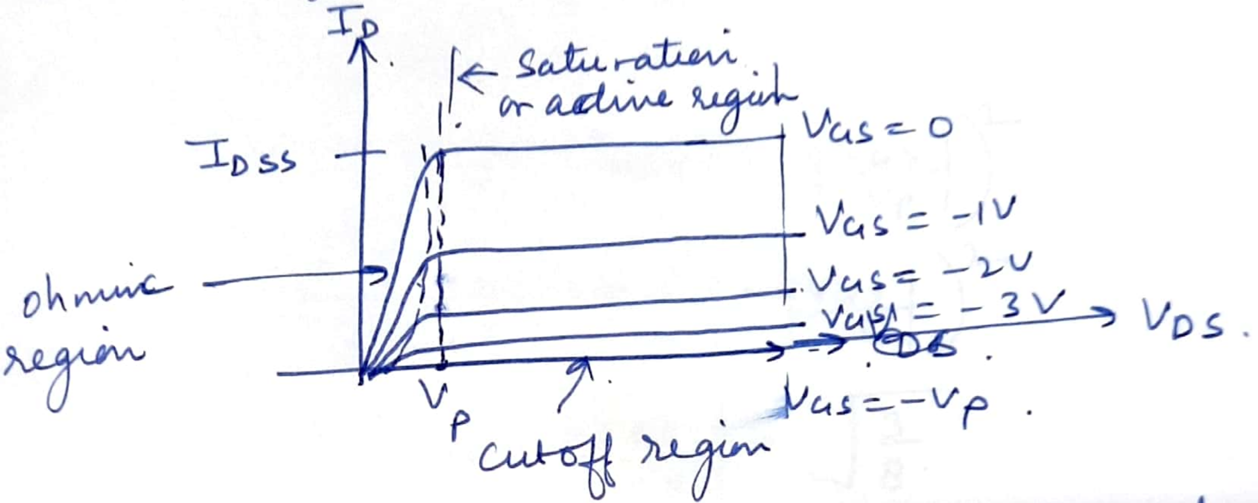
Characteristics of JFET (N-channel)

1) ~~Trans~~ Output characteristics

O/p voltage V/s o/p current keeping input voltage as constant

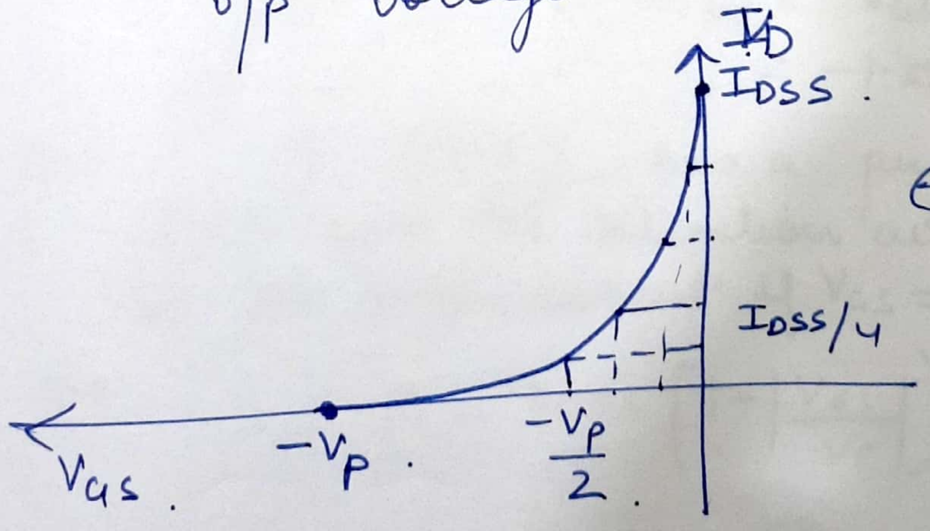


2) Transfer characteristics (Transconductance)

O/p voltage V/s O/p current keeping O/p voltage constant.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$y = mx^2$$



Numericals.

Q1. An n-channel JFET has $I_{DSS} = 8\,mA$ and $V_p = -4\,V$.

(a) if $I_D = 3\,mA$ Calculate the value of V_{GS}

(b) Calculate $V_{DS(sat)}$ for $I_D = 3\,mA$.

Solⁿ. we have

(a) $$I_D = I_{DSS}\left(1 - \left|\frac{V_{GS}}{V_P}\right|\right)^2$$

$$\Rightarrow \quad 3 = 8\left(1 - \left|\frac{V_{GS}}{-4}\right|\right)^2.$$

$$\Rightarrow \quad 1 - \left|\frac{V_{GS}}{-4}\right| = \sqrt{\frac{3}{8}}.$$

$$V_{GS} = -4\left(1 - \sqrt{\frac{3}{8}}\right)$$

$$= -1.55\ V.$$

(b) To Calculate $(V_{DS})_{sat}$

$$(V_{DS})_{sat} = V_{GS} - V_P.$$

$$= -1.55 + 4 = 2.45\ V.$$

Q2 :- A JFET has a pinch-off voltage of $-4V$. and the saturation current of $9\,mA$. Calculate the drain current if $V_{GS} = -2\,V$.

Ans. $$I_D = I_{DSS}\left(1 - \left|\frac{V_{GS}}{V_P}\right|\right)^2 = 9\left[1 - \frac{2}{4}\right]^2$$

$$= \frac{9}{4} = 2.25\,mA$$

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Q3. A certain JFET has $I_{DSS} = 12 mA$ and $V_P = -6V$. Calculate g_m (transconductance) for $V_{GS} = -1V$.

Sol^n we have $g_m = g_{mo}\left(1 - \left|\frac{V_{GS}}{V_P}\right|\right)$

where

$$g_{mo} = -\frac{2 I_{DSS}}{V_P}.$$

$$= \frac{-\cancel{2} \times 12}{-\cancel{6}\ 3} = 4\ mA/V.$$

$$g_m = 4\left[1 - \left(\frac{-1}{-6}\right)\right] = \frac{4 \times 5}{6}.$$

$$= 3.33\ mS.$$

Parameters of JFET

1. Dynamic drain resistance (r_d) → It is the AC resistance of a JFET. It is defined as ratio of change in output voltage (drain voltage) to change in output current (drain current) I_D at a constant value of gate to source voltage (V_{gs}).

$$\boxed{r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{\text{const. } V_{GS}}}$$

2. Transconductance (g_m).

It is ratio of change in ~~o/p voltage~~ o/p current (I_D) to change in i/p voltage (V_{gs}).

$$\boxed{g_m = \frac{\Delta I_D}{\Delta V_{GS}}}\Bigg|_{\text{const. } V_{DS}}$$

Derivation for g_m:

we have $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.

differentiate w.r.t V_{GS}.

$$\frac{dI_D}{dV_{GS}} = \frac{-2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right).$$

or $\boxed{g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right)}$.

where $\boxed{g_{mo} = \left|\frac{-2I_{DSS}}{V_P}\right|}$

3. Amplification factor (μ)

Ratio of change in o/p voltage to change in i/p voltage

$$\boxed{\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}} \quad I_D = \text{Const.}$$

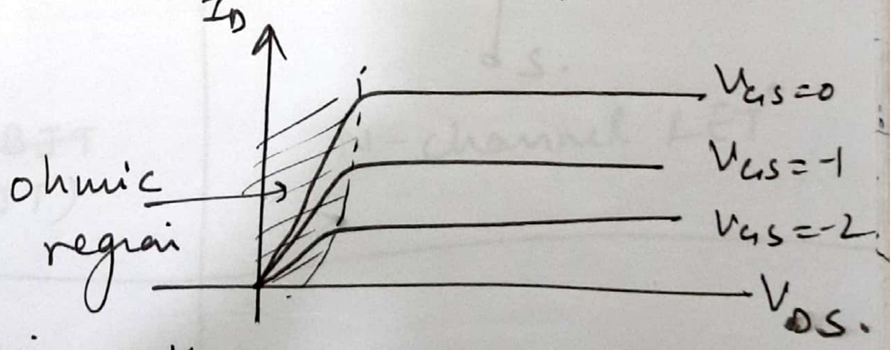
Relation b/w. μ, g_m and r_d.

we have $\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \cdot \frac{\Delta I_D}{\Delta I_D}$

$$= \left(\frac{\Delta V_{DS}}{\Delta I_D}\right) \cdot \left(\frac{\Delta I_D}{\Delta V_{GS}}\right)$$

$$\boxed{\mu = r_d \times g_m}$$

* Note FET is ~~ab~~ also known as voltage variable Resistor (VVR).



In ohmic region, the JFET acts as resistance and its value changes as we change the value of V_{GS}.

$$\boxed{r_d = \frac{r_{do}}{\left(1 - \frac{V_{GS}}{V_P}\right)^2}}$$