

# VHDL ASSIGNMENT

## ASYNCHRONOUS RIPPLE UP COUNTER USING J K FLIP FLOP

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### J K FLIP FLOP PROGRAM

The screenshot displays the ISE Project Navigator interface with the following components:

- Design Panel:** Shows the project hierarchy with components like 'hello', 'xc7a100t-3csg324', 'ripple - Behavioral (ripple)', 'u0 - jk - Behavioral (jk)', 'u1 - jk - Behavioral (jk)', and 'u2 - jk - Behavioral (jk)'. It also indicates 'No Processes Running' and lists 'Processes: u0 - jk - Behavioral' with options like 'ISim Simulator', 'Behavioral Check Syn...', and 'Simulate Behavioral ...'.
- Files Panel:** Lists files 'jk.vhd' and 'ripple...' with types 'VH...' and associations 'All'.
- Source Panel:** Contains the VHDL code for the JK Flip-Flop, which is as follows:

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 entity jk is
4     Port (
5         clk : in  STD_LOGIC;
6         q : inout STD_LOGIC:= '1';
7         j : in  STD_LOGIC:= '1';
8         k : in  STD_LOGIC:= '1';
9         qbar :inout STD_LOGIC:= '0'
10    );
11 end jk;
12 architecture Behavioral of jk is
13     signal sig:std_logic := '1';
14 begin
15     process(clk)
16     begin
17         if(rising_edge(clk)) then
18             if(j='0' and k='0') then
19                 sig<=sig;
20             elsif(j='0' and k='1') then
21                 sig<='0';
22             elsif(j='1' and k='0') then
23                 sig<='1';
24             elsif(j='1' and k='1') then
25                 sig<=not(sig);
26             end if;
27         end if;
28         qbar <= not(sig);
29     end process;
30 end Behavioral;
```
- Console Panel:** Shows the output of the compilation process:

```
Parsing VHDL file "/home/vishal/vish/hello/jk.vhd" into library isim_temp
Parsing VHDL file "/home/vishal/vish/hello/ripple.vhd" into library isim_temp
Process "Behavioral Check Syntax" completed successfully
```

## RIPPLE UP COUNTER PROGRAM USING 3 J K FLIP FLOP

The screenshot displays the ISE Project Navigator interface for a project named 'hello'. The main window shows the VHDL code for a ripple up counter using three JK flip-flops. The code is as follows:

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3
4
5
6 entity ripple is
7     Port ( clk_main : in  STD_LOGIC;
8           q0 : inout STD_LOGIC;
9           q1 : inout STD_LOGIC;
10          q2 : inout STD_LOGIC;
11          J : in  STD_LOGIC:= '1';
12          K : in  STD_LOGIC:= '1';
13          q0bar : inout STD_LOGIC;
14          q1bar : inout STD_LOGIC;
15          q2bar : inout STD_LOGIC
16        );
17 end ripple;
18
19 architecture Behavioral of ripple is
20
21 component jk
22     Port ( clk : in  STD_LOGIC;
23           q : inout STD_LOGIC:= '1';
24           j : in  STD_LOGIC:= '1';
25           k : in  STD_LOGIC:= '1';
26           qbar : inout STD_LOGIC:= '0' );
27 end component;
28
29 begin
30
31     u0:jk port map(clk_main,q0,J,K,q0bar);
32     u1:jk port map(q0bar,q1,J,K,q1bar);
33     u2:jk port map(q1bar,q2,J,K,q2bar);
34 end Behavioral;
35
36
```

The left pane shows the Design Hierarchy with the following structure:

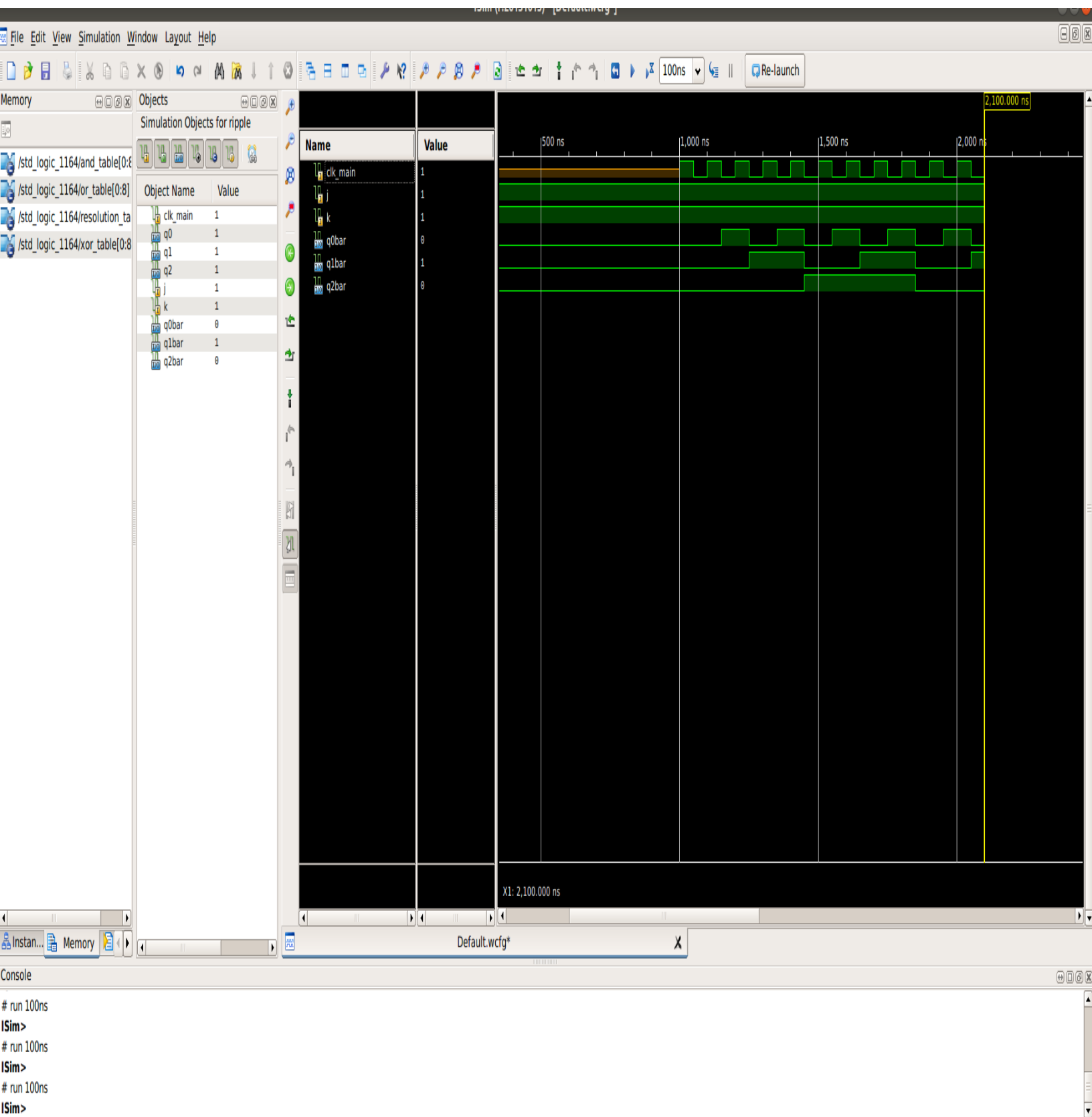
- hello
- xc7a100t-3csg324
- ripple - Behavioral (ripple.vhd)
- u0 - jk - Behavioral (jk.vhd)
- u1 - jk - Behavioral (jk.vhd)
- u2 - jk - Behavioral (jk.vhd)

The bottom pane shows the Console output:

```
"/home/vishal/vish/hello/ripple_isim_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "/home/vishal/vish/hello/ripple_isim_beh.wdb"
ISim simulation engine GUI launched successfully

Process "Simulate Behavioral Model" completed successfully
```

PULSE WAVEFORM (OUTPUT )



## SCHEMATICS(OUTPUT)

