VHDL ASSIGNMENT

ASYNCHRONOUS RIPPLE UP COUNTER USING J K FLIP FLOP

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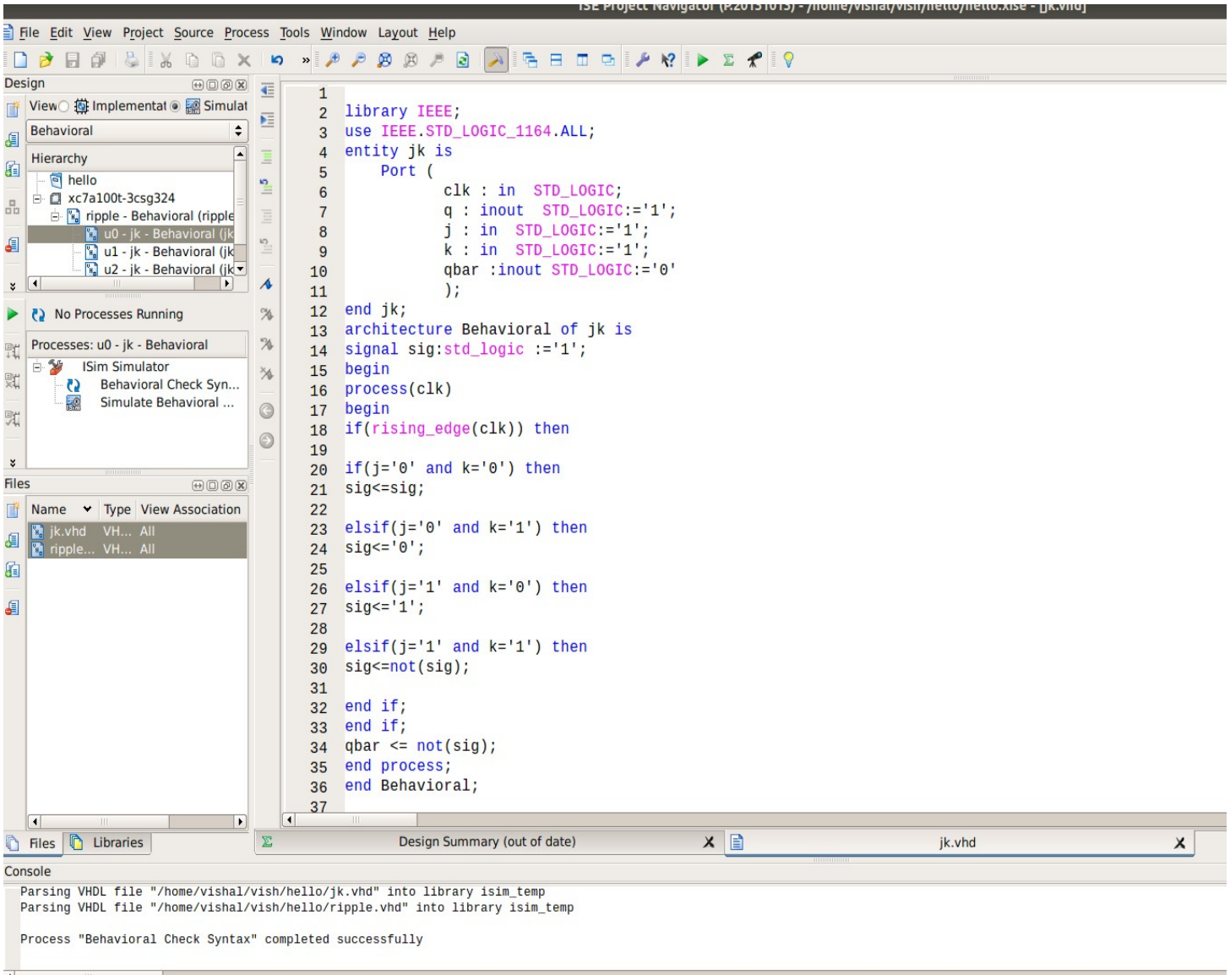
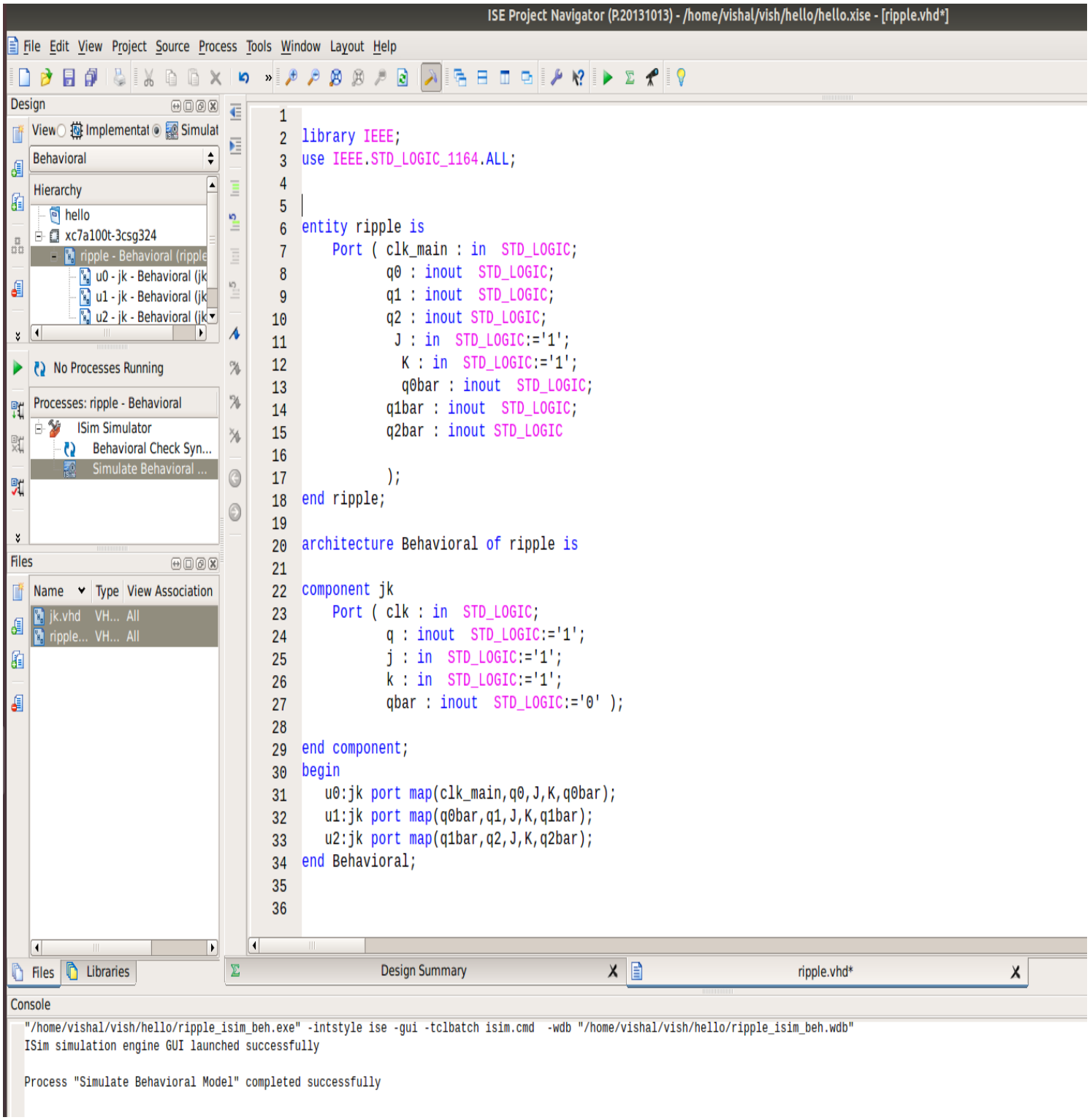
J K FLIP FLOP PROGRAM

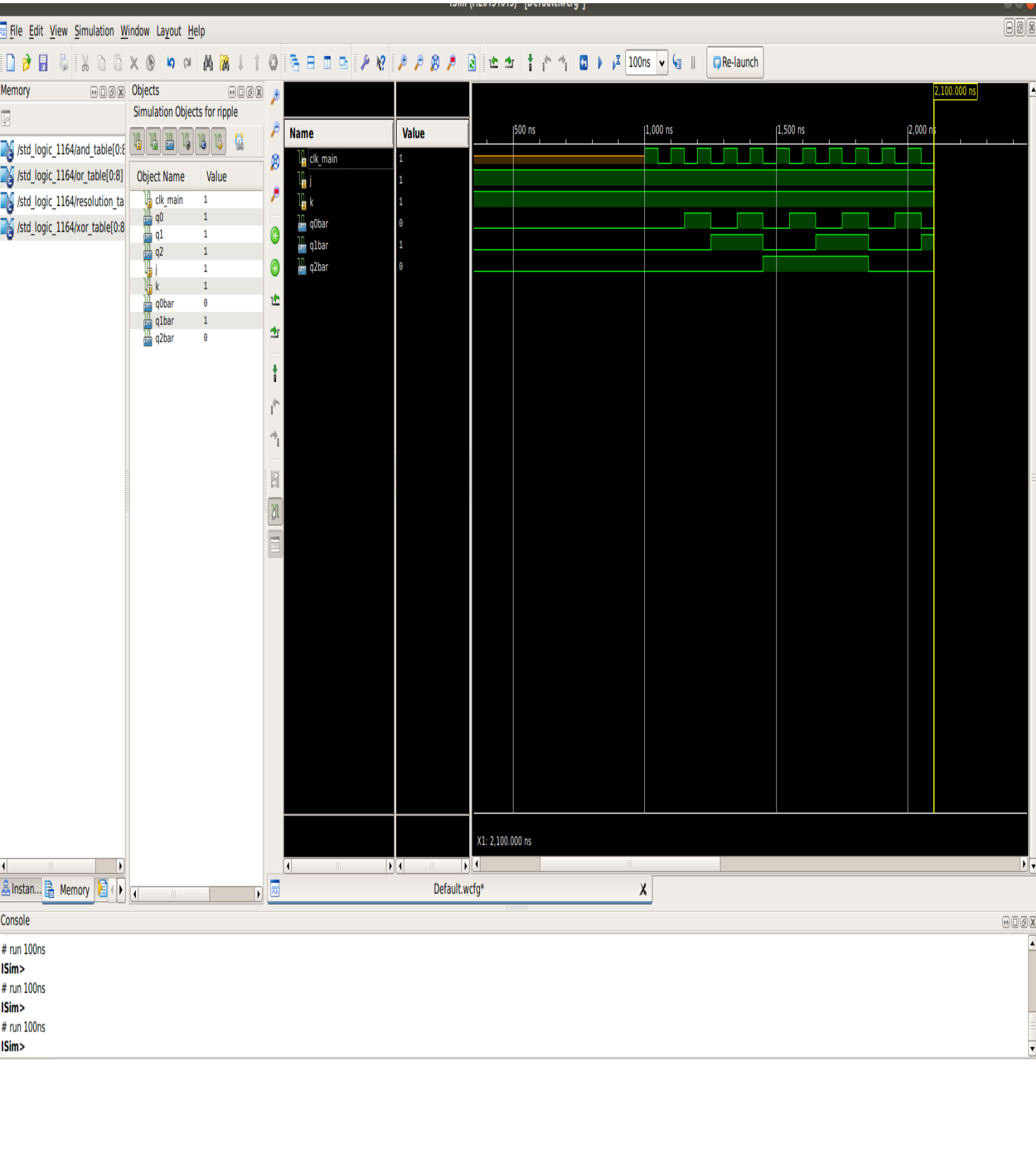


RIPPLE UP COUNTER PROGRAM USING 3 J K FLIP FLOP




```
1
2  library IEEE;
3  use IEEE.STD_LOGIC_1164.ALL;
4
5
6  entity ripple is
7      Port ( clk_main : in  STD_LOGIC;
8             q0 : inout  STD_LOGIC;
9             q1 : inout  STD_LOGIC;
10            q2 : inout STD_LOGIC;
11             J : in  STD_LOGIC:='1';
12              K : in  STD_LOGIC:='1';
13              q0bar : inout  STD_LOGIC;
14            q1bar : inout  STD_LOGIC;
15            q2bar : inout STD_LOGIC
16
17            );
18 end ripple;
19
20 architecture Behavioral of ripple is
21
22 component jk
23     Port ( clk : in  STD_LOGIC;
24            q : inout  STD_LOGIC:='1';
25            j : in  STD_LOGIC:='1';
26            k : in  STD_LOGIC:='1';
27            qbar : inout  STD_LOGIC:='0' );
28
29 end component;
30 begin
31    u0:jk port map(clk_main,q0,J,K,q0bar);
32    u1:jk port map(q0bar,q1,J,K,q1bar);
33    u2:jk port map(q1bar,q2,J,K,q2bar);
34 end Behavioral;
35
36
```

PULSE WAVEFORM (OUTPUT)



SCHEMATICS(OUTPUT)