VHDL ASSIGNMENT 3
4 BIT MAGNITUDE COMPARATOR
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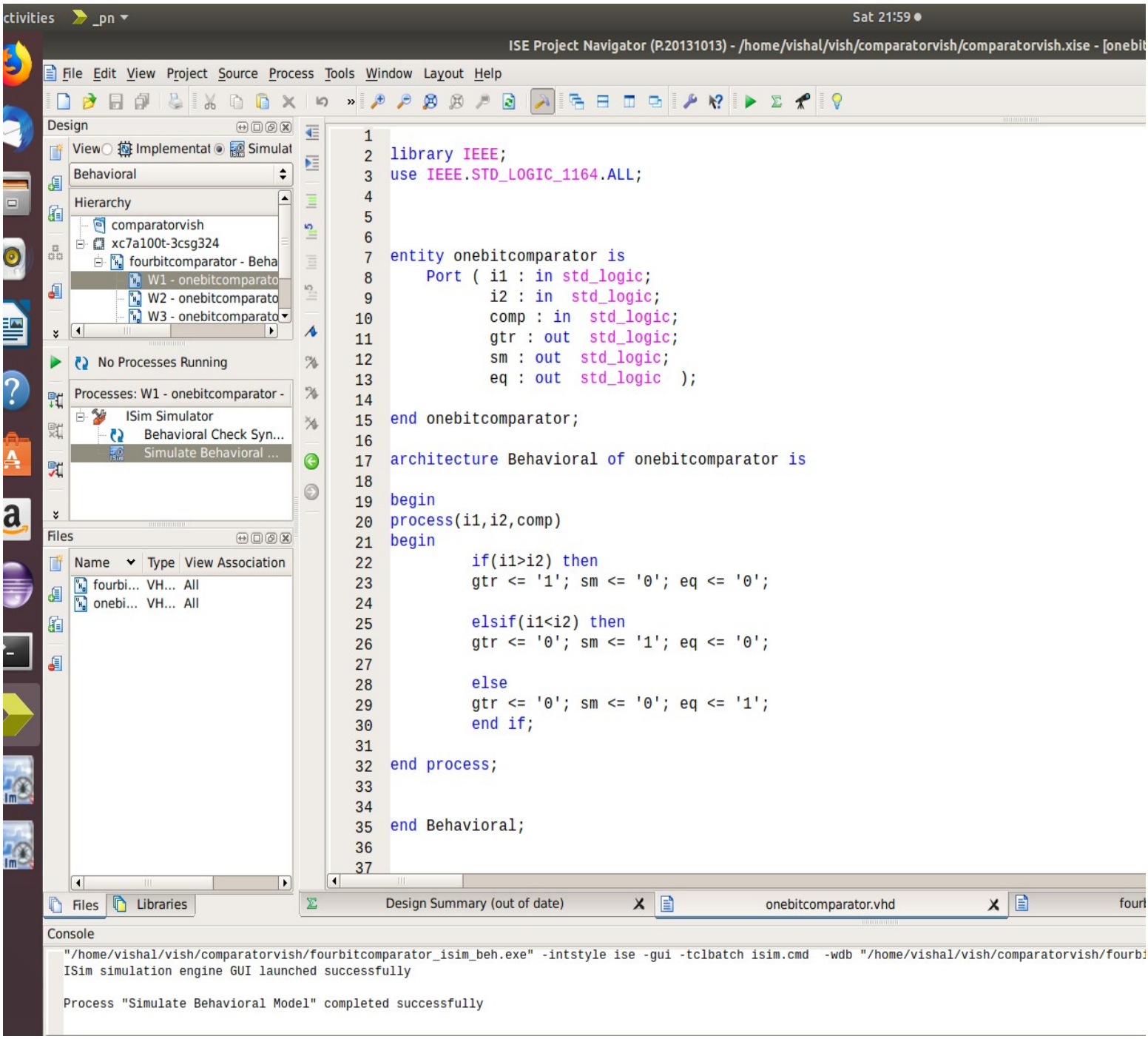
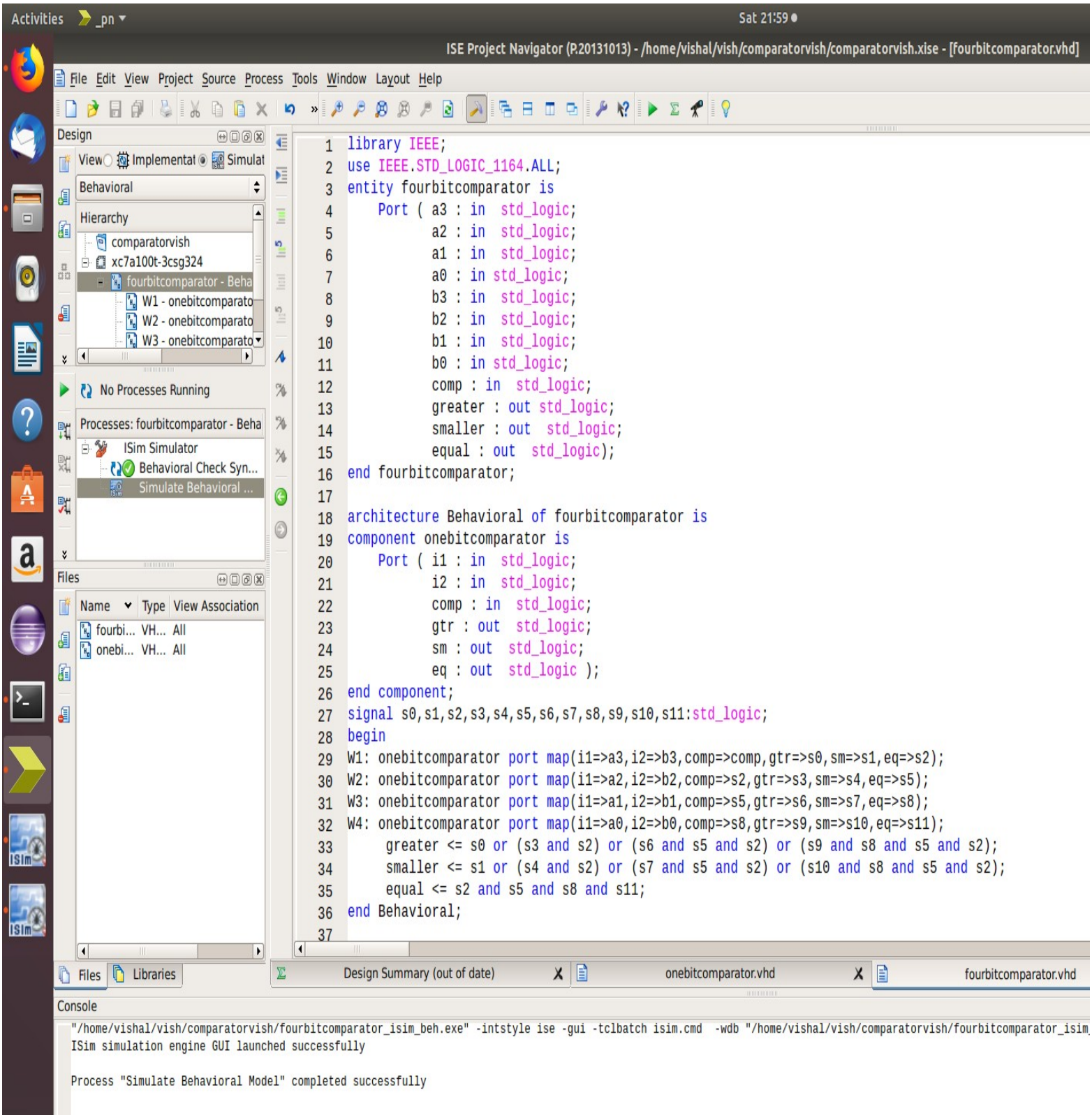
1 BIT COMPARATOR PROGRAM :



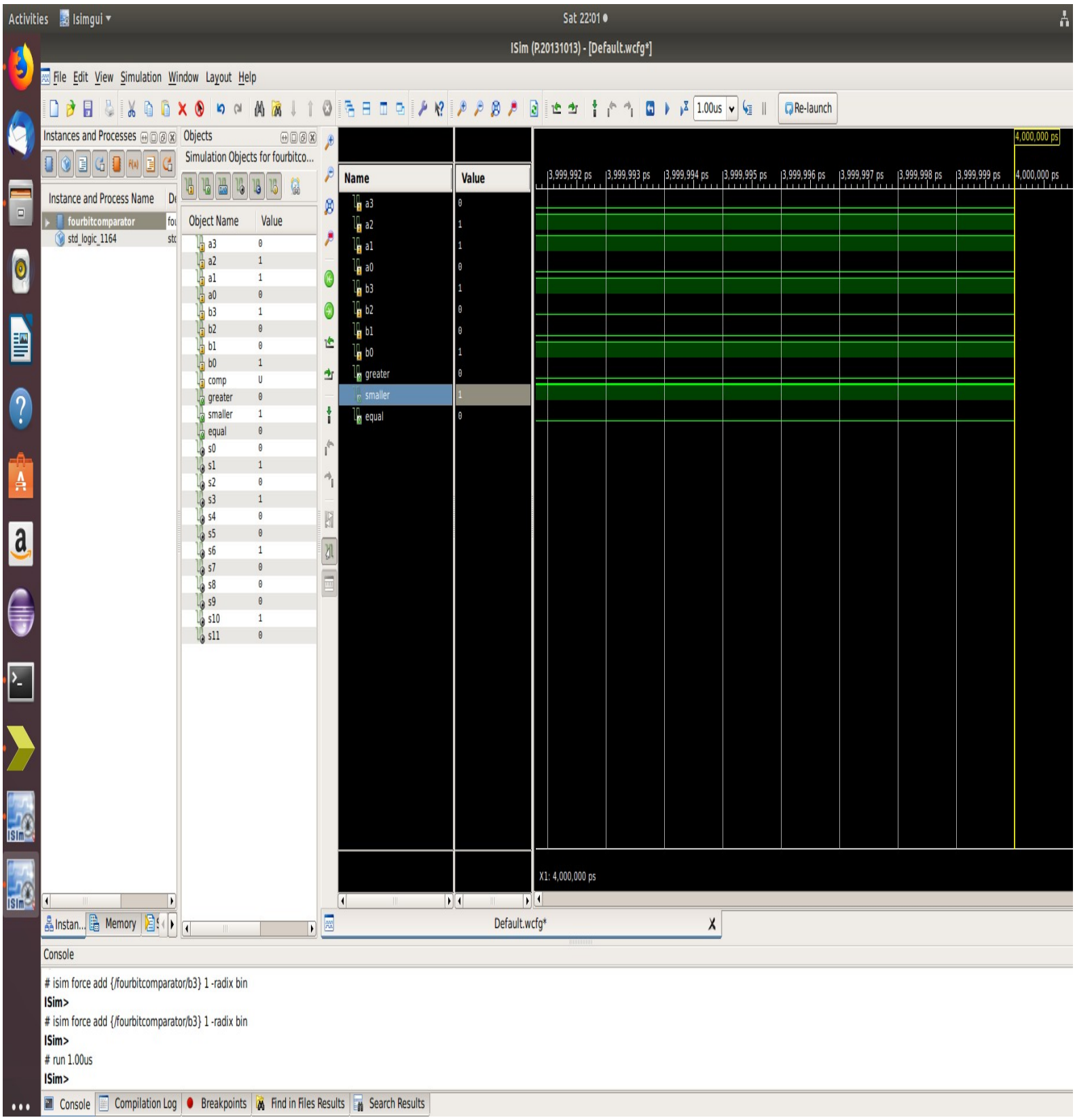

```
1
2  library IEEE;
3  use IEEE.STD_LOGIC_1164.ALL;
4
5
6
7  entity onebitcomparator is
8      Port ( i1 : in std_logic;
9             i2 : in  std_logic;
10            comp : in  std_logic;
11            gtr : out  std_logic;
12            sm : out  std_logic;
13            eq : out  std_logic  );
14
15 end onebitcomparator;
16
17 architecture Behavioral of onebitcomparator is
18
19 begin
20 process(i1,i2,comp)
21 begin
22          if(i1>i2) then
23          gtr <= '1'; sm <= '0'; eq <= '0';
24
25          elsif(i1<i2) then
26          gtr <= '0'; sm <= '1'; eq <= '0';
27
28          else
29          gtr <= '0'; sm <= '0'; eq <= '1';
30          end if;
31
32 end process;
33
34
35 end Behavioral;
36
37
```

4 BIT MAGNITUDE COMPARATOR PROGRAM :

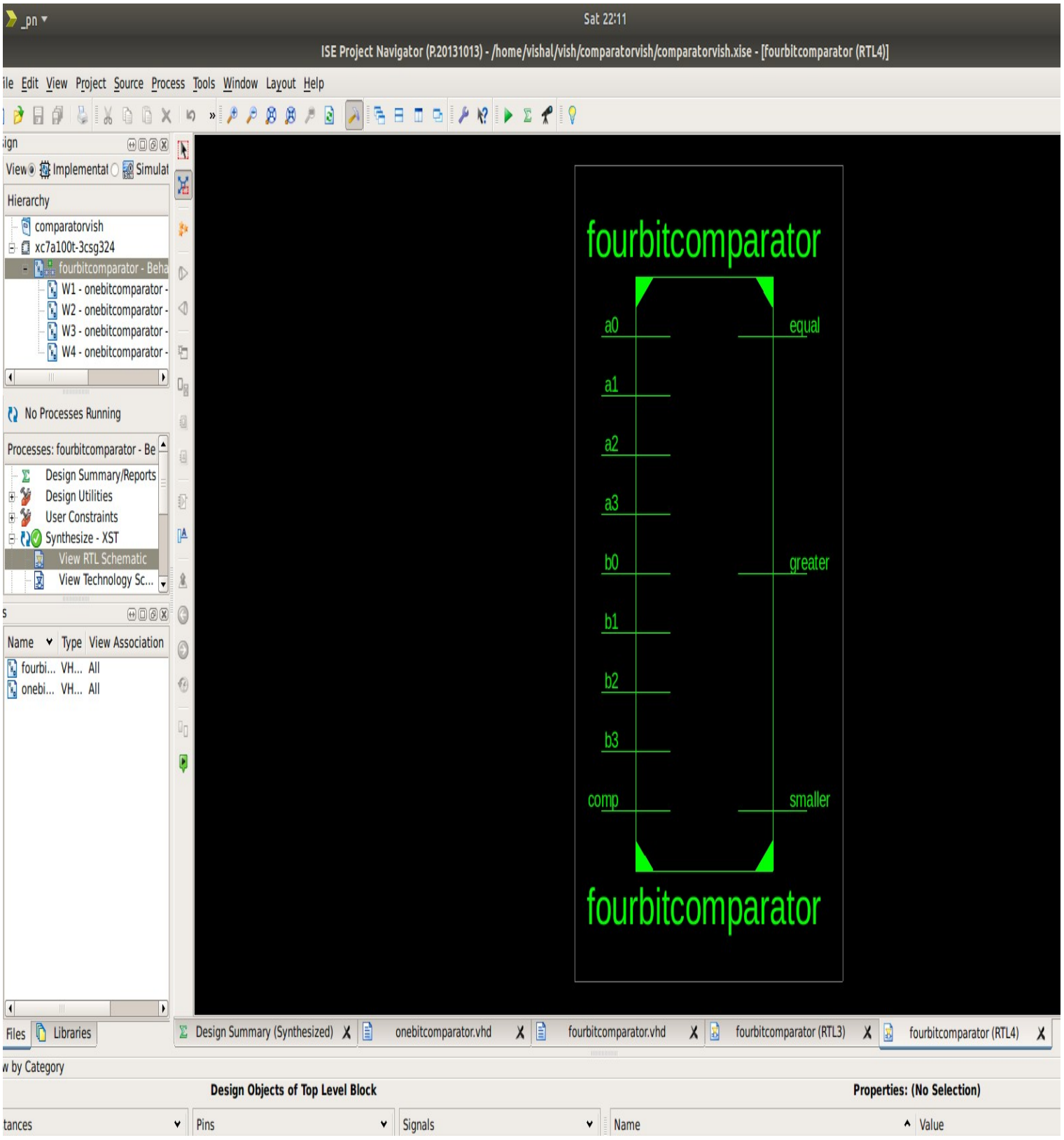



```
1  library IEEE;
2  use IEEE.STD_LOGIC_1164.ALL;
3  entity fourbitcomparator is
4      Port ( a3 : in  std_logic;
5             a2 : in  std_logic;
6             a1 : in  std_logic;
7             a0 : in std_logic;
8             b3 : in  std_logic;
9             b2 : in  std_logic;
10            b1 : in  std_logic;
11            b0 : in std_logic;
12            comp : in  std_logic;
13            greater : out std_logic;
14            smaller : out  std_logic;
15            equal : out  std_logic);
16 end fourbitcomparator;
17
18 architecture Behavioral of fourbitcomparator is
19 component onebitcomparator is
20     Port ( i1 : in  std_logic;
21            i2 : in  std_logic;
22            comp : in  std_logic;
23            gtr : out  std_logic;
24            sm : out  std_logic;
25            eq : out  std_logic );
26 end component;
27 signal s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s11:std_logic;
28 begin
29 W1: onebitcomparator port map(i1=>a3,i2=>b3,comp=>comp,gtr=>s0,sm=>s1,eq=>s2);
30 W2: onebitcomparator port map(i1=>a2,i2=>b2,comp=>s2,gtr=>s3,sm=>s4,eq=>s5);
31 W3: onebitcomparator port map(i1=>a1,i2=>b1,comp=>s5,gtr=>s6,sm=>s7,eq=>s8);
32 W4: onebitcomparator port map(i1=>a0,i2=>b0,comp=>s8,gtr=>s9,sm=>s10,eq=>s11);
33      greater <= s0 or (s3 and s2) or (s6 and s5 and s2) or (s9 and s8 and s5 and s2);
34      smaller <= s1 or (s4 and s2) or (s7 and s5 and s2) or (s10 and s8 and s5 and s2);
35      equal <= s2 and s5 and s8 and s11;
36 end Behavioral;
37
```

OUTPUT :


Activities
Isimgui
Sat 22:01
ISim (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
1.00us
Re-launch
Instances and Processes
Objects
Simulation Objects for fourbitco...
Instance and Process Name
fourbitcomparator
std_logic_1164
Object Name
Value
a3 0
a2 1
a1 1
a0 0
b3 1
b2 0
b1 0
b0 1
comp U
greater 0
smaller 1
equal 0
s0 0
s1 1
s2 0
s3 1
s4 0
s5 0
s6 1
s7 0
s8 0
s9 0
s10 1
s11 0
Name
Value
3,999,992 ps
3,999,993 ps
3,999,994 ps
3,999,995 ps
3,999,996 ps
3,999,997 ps
3,999,998 ps
3,999,999 ps
4,000,000 ps
X1: 4,000,000 ps
Default.wcfg*
Console
isim force add {/fourbitcomparator/b3} 1 -radix bin
ISim>
isim force add {/fourbitcomparator/b3} 1 -radix bin
ISim>
run 1.00us
ISim>
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Memory

SCHEMATICS (4 BIT MAGNITUDE COMPARATOR):



SCHEMATICS(4 ONE BIT COMPARATOR)(STRUCTURAL APPROACH)