

VHDL ASSIGNMENT 2

8 BIT ADDER

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Full adder Program:

The screenshot displays the ISE Project Navigator interface for a project named 'fulladder'. The main window shows the VHDL code for a full adder entity. The code is as follows:

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3
4
5
6
7 entity fulladder is
8     Port ( a : in bit;
9           b : in bit;
10          s : out bit;
11          cin : in bit;
12          cout : out bit);
13 end fulladder;
14
15 architecture Behavioral of fulladder is
16
17 begin
18
19 s <= a xor b xor cin;
20 cout <= ((a and b)) or (cin and (a xor b));
21
22
23 end Behavioral;
24
25
```

The left sidebar shows the project hierarchy with the following components:

- xc7a100t-3csg324
 - eightbitadder - Behavior
 - LS283L - fourbitadder
 - FA1 - fulladder - Behavior
 - FA2 - fulladder - Behavior
 - FA3 - fulladder - Behavior
 - FA4 - fulladder - Behavior

The bottom of the window shows the 'View by Category' section with the following tabs:

- Instances
- Pins
- Signals
- Name

The 'Design Objects of Top Level Block' section is currently empty.

74LS283 IC PROGRAM:

The screenshot displays the ISE Project Navigator interface for a project named "fourbitadder.vhd". The main window shows the VHDL code for a four-bit adder, which is a behavioral implementation of the 74LS283 IC. The code is organized into several sections: a library declaration, an entity declaration, an architecture declaration, a component declaration, and a begin/end block. The code is as follows:

```
1
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4
5 entity fourbitadder is
6     Port ( A,B,C,D,A0,B0,C0,D0 : in bit;
7           E,F,G,H : out bit;
8           PCin : in bit;
9           Cout : out bit);
10 end fourbitadder;
11
12 architecture Behavioral of fourbitadder is
13
14     component fulladder is
15         Port ( a : in bit;
16               b : in bit;
17               s : out bit;
18               cin : in bit;
19               cout : out bit);
20     end component;
21
22     signal c1,c2,c3:bit;
23
24     begin
25
26     FA1: fulladder port map( A, A0,E,'0', c1);
27     FA2: fulladder port map( B, B0,F, c1, c2);
28     FA3: fulladder port map( C, C0,G,c2, c3);
29     FA4: fulladder port map( D, D0,H, c3, Cout);
30
31
32 end Behavioral;
33
34
```

The left sidebar shows the project hierarchy, including the "xc7a100t-3csg324" device, the "eightbitadder - Behavioral" block, and the "LS283L - fourbitadder" block. The "Processes" section shows "No Processes Running". The "Files" section lists the project files: "eight...", "fourbi...", and "fullad...". The bottom status bar indicates "Design Objects of Top Level Block".

8 Bit Adder Program:

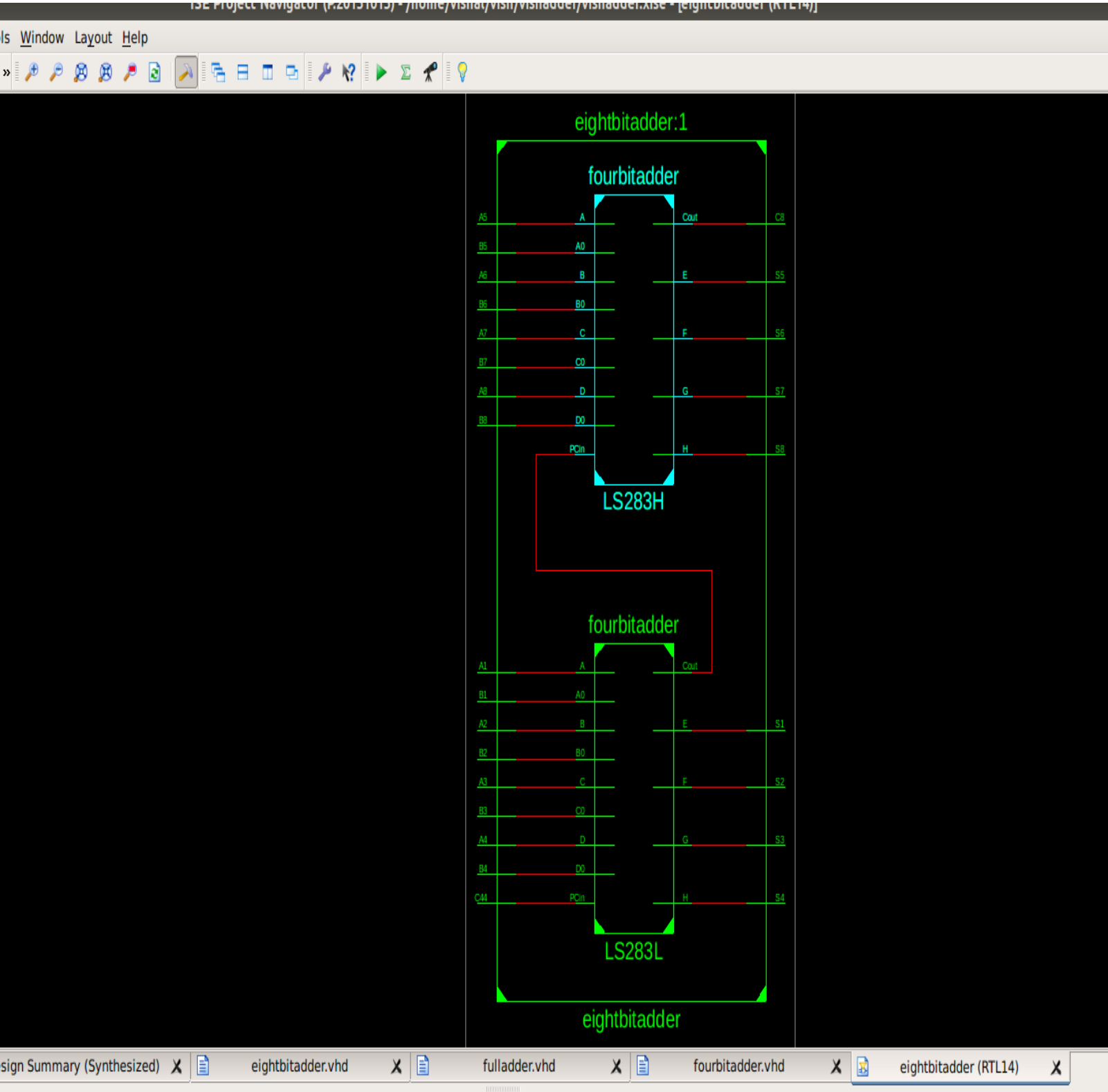
ISE Project Navigator (P.20131013) - /home/vishal/vish/vishadder/vishadder.xise - [eightbitadder.vhd]

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3
4
5
6
7 entity eightbitadder is
8     Port ( A1,A2,A3,A4,B1,B2,B3,B4,A5,A6,A7,A8,B5,B6,B7,B8 : in bit;
9           S1,S2,S3,S4,S5,S6,S7,S8 : out bit;
10          C44 : in bit;
11          C8 : out bit);
12 end eightbitadder;
13
14 architecture Behavioral of eightbitadder is
15
16 component fourbitadder is
17     Port ( A,B,C,D,A0,B0,C0,D0 : in bit;
18           E,F,G,H : out bit;
19           PCin : in bit;
20           Cout : out bit);
21 end component;
22
23
24 signal c4:bit;
25
26 begin
27
28 LS283L: fourbitadder port map(A=>A1,B=>A2,C=>A3,D=>A4,A0=>B1,B0=>B2,C0=>B3,D0=>B4,E=>S1,F=>S2,G=>S3,H=>S4,PCin=>C44,Cout=>c4);
29 LS283H: fourbitadder port map(A=>A5,B=>A6,C=>A7,D=>A8,A0=>B5,B0=>B6,C0=>B7,D0=>B8,E=>S5,F=>S6,G=>S7,H=>S8,PCin=>c4,Cout=>c8);
30
31 end Behavioral;
32
```

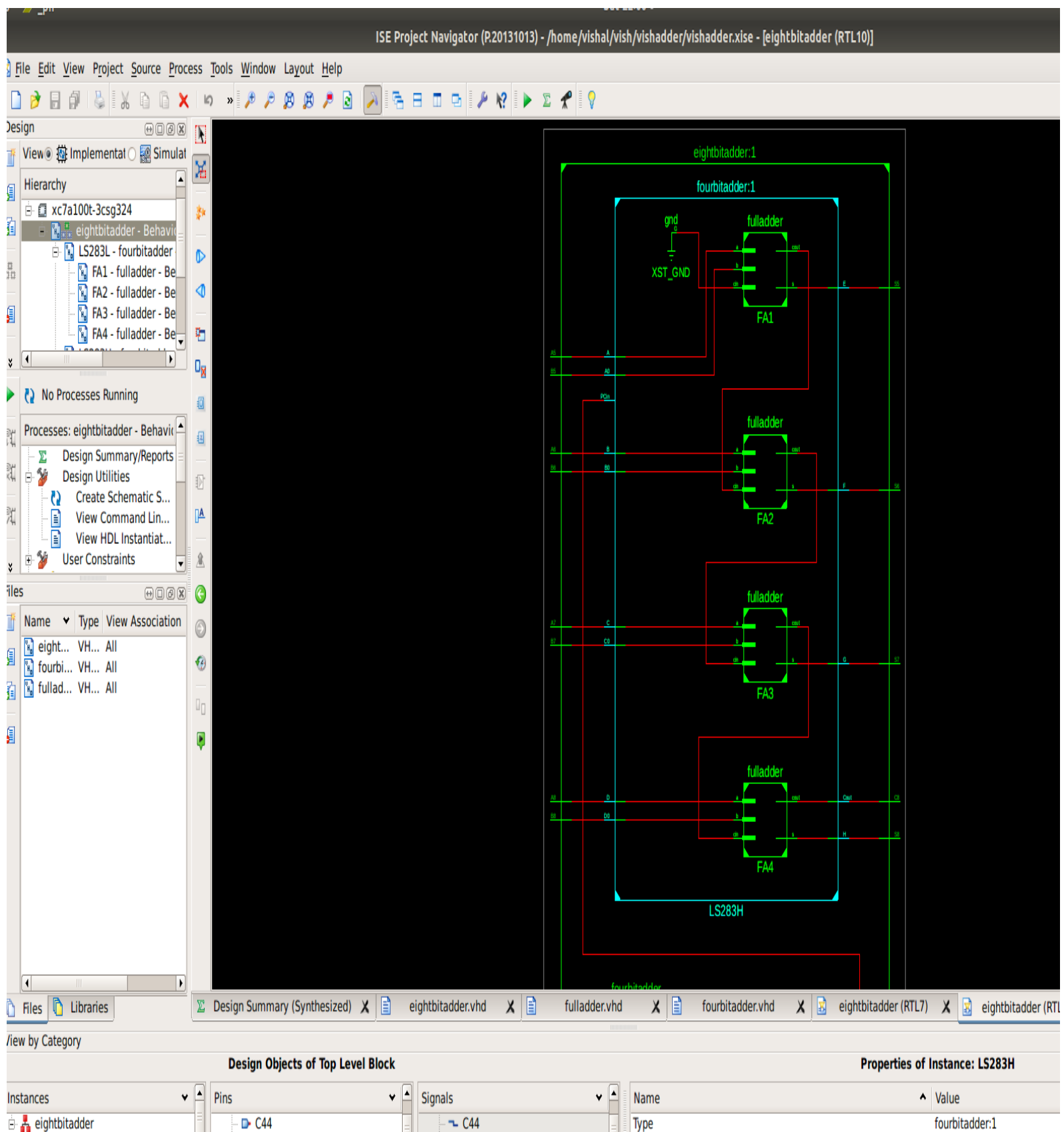
Design Objects of Top Level Block

Design Objects of Top Level Block			Properties: (No Selection)	
Instances	Pins	Signals	Name	Value

SCHEMATICS(8BIT ADDER):



SCHEMATICS(74LS283):



WAVEFORM OUTPUT:

