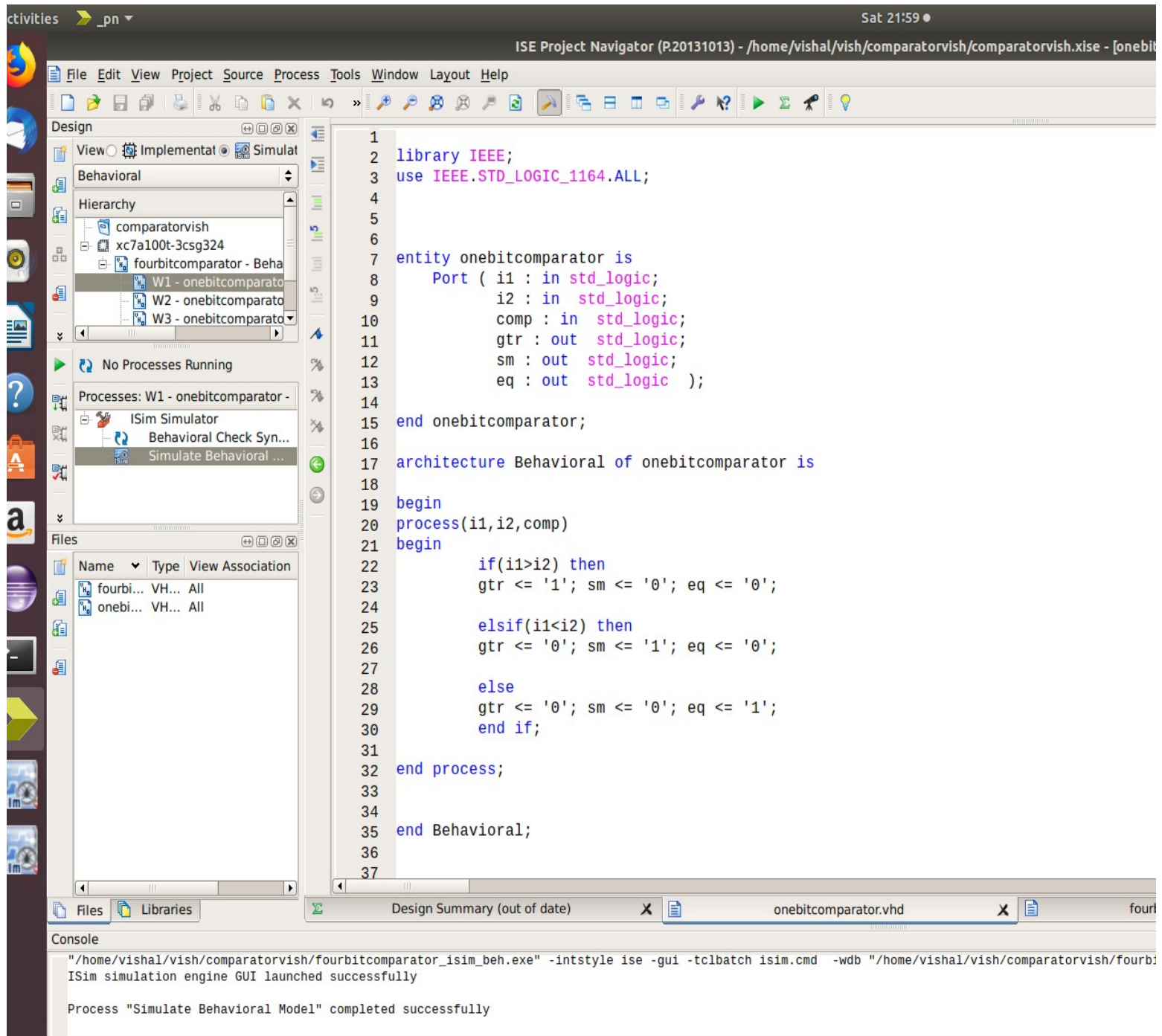


**VHDL ASSIGNMENT 3**  
**4 BIT MAGNITUDE COMPARATOR**  
**NAME : VISHAL HARGOVINDBHAI HASRAJANI**  
**STUDENT ID: C0761544**

**1 BIT COMPARATOR PROGRAM :**



## 4 BIT MAGNITUDE COMPARATOR PROGRAM :

Activities \_pn Sat 21:59 ISE Project Navigator (P.20131013) - /home/vishal/vish/comparatorvish/comparatorvish.xise - [fourbitcomparator.vhd]

File Edit View Project Source Process Tools Window Layout Help

Design View Implement Simulat Behavioral Hierarchy comparatorvish xc7a100t-3csg324 fourbitcomparator - Beha W1 - onebitcomparator W2 - onebitcomparator W3 - onebitcomparator No Processes Running Processes: fourbitcomparator - Beha ISim Simulator Behavioral Check Syn... Simulate Behavioral ... Files Name Type View Association fourbi... VH... All onebi... VH... All

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 entity fourbitcomparator is
4     Port ( a3 : in std_logic;
5           a2 : in std_logic;
6           a1 : in std_logic;
7           a0 : in std_logic;
8           b3 : in std_logic;
9           b2 : in std_logic;
10          b1 : in std_logic;
11          b0 : in std_logic;
12          comp : in std_logic;
13          greater : out std_logic;
14          smaller : out std_logic;
15          equal : out std_logic);
16 end fourbitcomparator;
17
18 architecture Behavioral of fourbitcomparator is
19     component onebitcomparator is
20         Port ( i1 : in std_logic;
21               i2 : in std_logic;
22               comp : in std_logic;
23               gtr : out std_logic;
24               sm : out std_logic;
25               eq : out std_logic );
26     end component;
27     signal s0,s1,s2,s3,s4,s5,s6,s7,s8,s9,s10,s11:std_logic;
28     begin
29     W1: onebitcomparator port map(i1=>a3,i2=>b3,comp=>comp,gtr=>s0,sm=>s1,eq=>s2);
30     W2: onebitcomparator port map(i1=>a2,i2=>b2,comp=>s2,gtr=>s3,sm=>s4,eq=>s5);
31     W3: onebitcomparator port map(i1=>a1,i2=>b1,comp=>s5,gtr=>s6,sm=>s7,eq=>s8);
32     W4: onebitcomparator port map(i1=>a0,i2=>b0,comp=>s8,gtr=>s9,sm=>s10,eq=>s11);
33     greater <= s0 or (s3 and s2) or (s6 and s5 and s2) or (s9 and s8 and s5 and s2);
34     smaller <= s1 or (s4 and s2) or (s7 and s5 and s2) or (s10 and s8 and s5 and s2);
35     equal <= s2 and s5 and s8 and s11;
36 end Behavioral;
37
```

Design Summary (out of date) onebitcomparator.vhd fourbitcomparator.vhd

Console  
"/home/vishal/vish/comparatorvish/fourbitcomparator\_isim\_beh.exe" -intstyle ise -gui -tclbatch isim.cmd -wdb "/home/vishal/vish/comparatorvish/fourbitcomparator\_isim  
ISim simulation engine GUI launched successfully  
Process "Simulate Behavioral Model" completed successfully

The screenshot displays the ISim (Integrated Simulator) interface for a four-bit comparator simulation. The main window is titled "ISim (P20131013) - [Default.wcfg\*]".

**Instances and Processes:** The left panel shows the instance and process names for the simulation. The instance "fourbitcomparator" is selected, and its process "std\_logic\_1164" is visible.

**Simulation Objects:** The middle panel displays the simulation objects for the fourbitcomparator. The objects are listed in a table with their names and values:

Object Name	Value
a3	0
a2	1
a1	1
a0	0
b3	1
b2	0
b1	0
b0	1
comp	U
greater	0
smaller	1
equal	0
s0	0
s1	1
s2	0
s3	1
s4	0
s5	0
s6	1
s7	0
s8	0
s9	0
s10	1
s11	0

**Waveform:** The right panel shows a waveform viewer with a time axis ranging from 0 to 4,000,000 ps. The waveform displays the signals for the four-bit comparator, including the inputs a3, a2, a1, a0, b3, b2, b1, b0, and the outputs greater, smaller, and equal. The signals are shown as digital waveforms.

**Console:** The bottom panel shows the command history in the console:

```
# isim force add {/fourbitcomparator/b3} 1 -radix bin
ISim>
# isim force add {/fourbitcomparator/b3} 1 -radix bin
ISim>
# run 1.00us
ISim>
```



# SCHEMATICS (4 BIT MAGNITUDE COMPARATOR):

Sat 22:11

ISE Project Navigator (P.20131013) - /home/vishal/vish/comparatorvish/comparatorvish.xise - [fourbitcomparator (RTL4)]

File Edit View Project Source Process Tools Window Layout Help

Sign

View Implement Simulat

Hierarchy

- comparatorvish
  - xc7a100t-3csg324
    - fourbitcomparator - Beha
      - W1 - onebitcomparator -
      - W2 - onebitcomparator -
      - W3 - onebitcomparator -
      - W4 - onebitcomparator -

No Processes Running

Processes: fourbitcomparator - Be

- Design Summary/Reports
- Design Utilities
- User Constraints
- Synthesize - XST
- View RTL Schematic
- View Technology Sc...

Names

Name	Type	View Association
fourbi...	VH...	All
onebi...	VH...	All

fourbitcomparator

a0 a1 a2 a3 b0 b1 b2 b3 comp

equal greater smaller

fourbitcomparator

Files Libraries

Design Summary (Synthesized) X onebitcomparator.vhd X fourbitcomparator.vhd X fourbitcomparator (RTL3) X fourbitcomparator (RTL4) X

Design Objects of Top Level Block

Properties: (No Selection)

Instances	Pins	Signals	Name	Value
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# SCHEMATICS( 4 ONE BIT COMPARATOR )(STRUCTURAL APPROACH)

