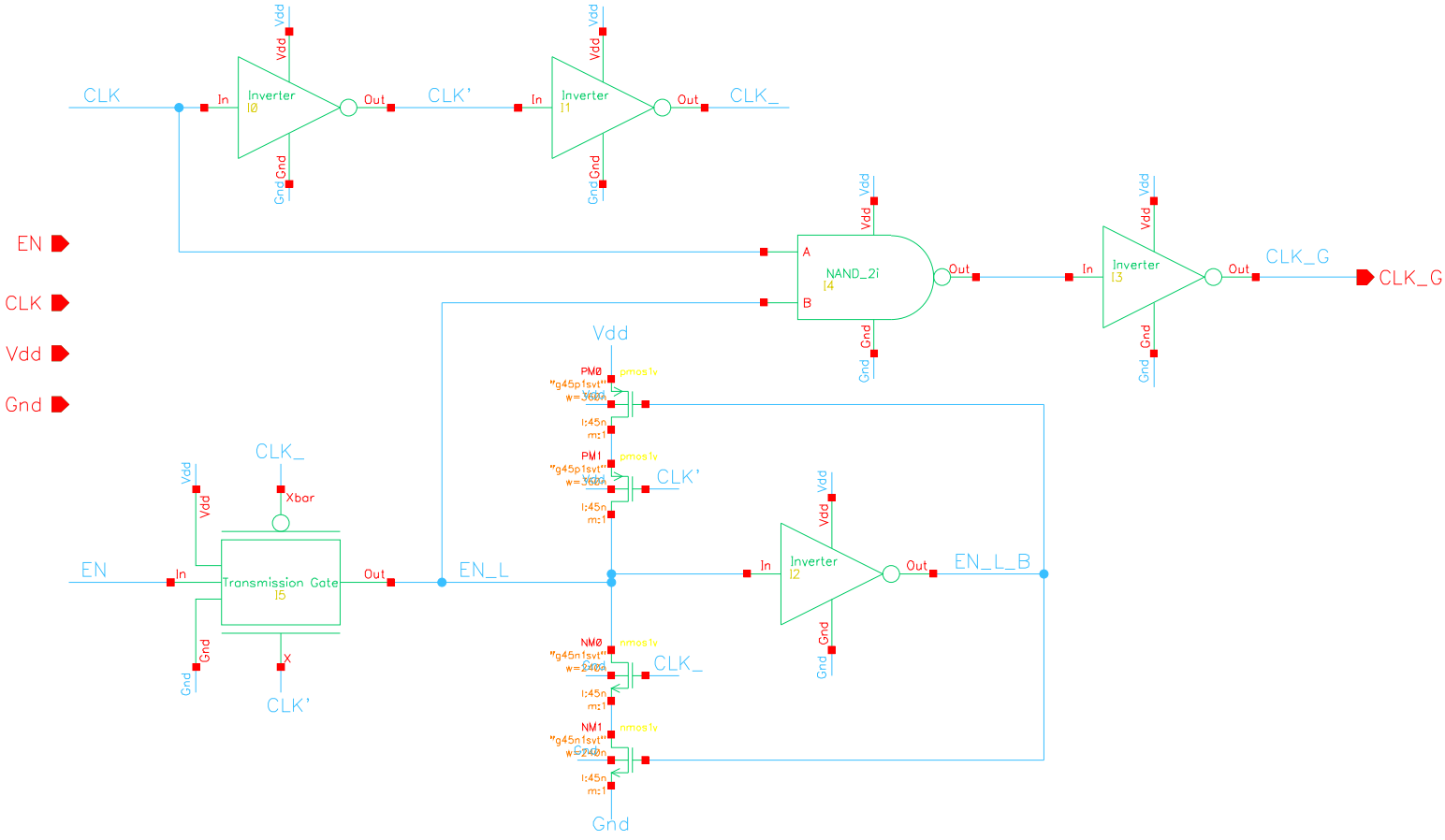
USER: 695v16
DATE: Fri Feb 27 22:38:38 2026
PLOT SIZE: 8.01 x 4.61 Inches
Library: AVD_HW3
Cell: clock_gater_std
View: schematic
Plot Area: ((-3.475 -4.33125) (7.1375 1.775))


EN
CLK
Vdd
Gnd
CLK
Inverter
I0
CLK'
Inverter
I1
CLK_
NAND_2i
I4
CLK_G
Inverter
I3
CLK_G
Vdd
Gnd
CLK_
Xbar
EN
Transmission Gate
I5
EN_L
PM0
PM1
CLK'
NM0
CLK_
NM1
Inverter
I2
EN_L_B
Vdd
Gnd