CLK

Inverter
I0
In Out
Vdd Vdd
Gnd Gnd
Out CLK'

Inverter
I1
In Out
Vdd Vdd
Gnd Gnd
Out CLK_

EN

CLK

Vdd

Gnd

Vdd Vdd
A
NAND_2i
I4
B
Out
Gnd Gnd

Inverter
I3
In Out
Vdd Vdd
Gnd Gnd
CLK_G

CLK_G

Vdd

PM0
"g45p1svt"
w=Ycca
l:45n
m:1
pmos1v
Vdd

PM1
"g45p1svt"
w=Ycca
l:45n
m:1
pmos1v
CLK'

Inverter
I2
In Out
Vdd Vdd
Gnd Gnd
EN_L_B

Vdd
Vdd

CLK_
Xbar

EN In Out

Transmission Gate
I5

Gnd Gnd

X
CLK'

EN_L

NM0
"g45n1svt"
w=240n
l:45n
m:1
nmos1v
CLK_

NM1
"g45n1svt"
w=240n
l:45n
m:1
nmos1v
EN_L_B

Gnd