

## **UTTARANCHAL UNIVERSITY**

(Established vide Uttaranchal University Act, 2012, Uttarakhand Act No. 11 of 2013)

Premnagar-248007, Dehradun, Uttarakhand, INDIA

# **ASSIGNMENT COVER PAGE**

Name of Student:	VISHAL
Batch:	JULY-2023
Program:	BACHELOR OF COMPUTER APPLICATIONS
Subject & Code:	COMPUTER ORGANIZATION AND ARCHITECTURE & OBCA 234
Semester:	3RD SEMESTER
Learner ID:	2313020052

## **NECESSARY INSTRUCTIONS**

- 1. Cover Page must be filled in Capital Letters. All Fields of the Form are compulsory to be filled.
- 2. The assignment should be written / computer typed on A4 size paper and it should be neat and clearly readable.
- 3. The cover page should be stapled at the front of each and every assignment.
- 4. Incomplete Assignments will not be accepted.

# Q 1. Develop an instruction set for a RISC-based CPU tailored to the needs of a specific computational task.

## Designing an Instruction Set for a RISC-Based CPU

When it comes to processor architecture, Reduced Instruction Set Computing (RISC) stands out for its simplicity and efficiency. RISC-based CPUs are built around a minimal set of instructions, each designed to execute rapidly, often in just one clock cycle. This design philosophy makes RISC particularly effective for specialized tasks that demand high performance, such as matrix multiplication—a key operation in machine learning, graphics, and scientific computing. In this essay, I'll outline a custom instruction set for a RISC-based CPU tailored specifically for matrix multiplication, highlighting how it maximizes efficiency while maintaining simplicity and scalability.

## Why Focus on Matrix Multiplication?

Matrix multiplication is a fundamental computation in many fields, but it can be resource-intensive due to the sheer volume of arithmetic and memory operations involved. A poorly designed instruction set can lead to inefficiencies like bottlenecks in memory access and excessive control logic overhead. The goal here is to create an instruction set that simplifies these operations, reduces latency, and enhances parallel processing.

## **Key Components of the Instruction Set**

To design an instruction set optimized for matrix multiplication, we need to include five essential categories of instructions:

#### 1. Arithmetic Instructions

These handle basic operations like addition, subtraction, and multiplication. Since matrix multiplication involves repetitive arithmetic, these instructions are the foundation:

- **ADD R1, R2, R3**: Add the values in registers R2 and R3, storing the result in R1.
- o **MUL R1, R2, R3**: Multiply the values in registers R2 and R3, storing the result in R1.

## 2. Memory Access Instructions

Efficiently transferring data between memory and registers is critical for matrix operations. These instructions ensure smooth memory access:

- **LOAD R1, [R2]**: Load the value from the memory address in R2 into register R1.
- **STORE R1, [R2]**: Store the value in R1 into the memory address specified by R2.

#### 3. Control Flow Instructions

Loops and conditional branches are necessary for navigating through matrix rows and columns. These instructions manage program flow:

- o **BEQ R1, R2, LABEL**: Branch to LABEL if the values in R1 and R2 are equal.
- BNE R1, R2, LABEL: Branch to LABEL if the values in R1 and R2 are not equal.

## 4. Specialized Matrix Instructions

Custom instructions designed specifically for matrix multiplication can significantly reduce the number of general-purpose instructions needed:

- MAT\_LOAD R1, R2: Load a block of matrix data starting from memory address R2 into register R1.
- MAT\_MUL R1, R2, R3: Perform matrix multiplication with matrices in R2 and R3, storing the result in R1.

## 5. Utility Instructions

These help with tasks like setting values or introducing delays for synchronization:

- **SET R1, #VALUE**: Set register R1 to a specific constant.
- **NOP**: Perform no operation, useful in pipelining delays.

## A Step-by-Step Workflow for Matrix Multiplication

Using this instruction set, the process for multiplying matrices can be broken into three key steps:

## **Loading Data**

Use the MAT\_LOAD instruction or a series of LOAD commands to bring matrix data into registers:

```
MAT_LOAD R1, [0x1000]; Load matrix A into R1 MAT_LOAD R2, [0x2000]; Load matrix B into R2
```

## **Performing Multiplication**

Execute matrix multiplication using MAT\_MUL:

```
MAT_MUL R3, R1, R2; Multiply matrices in R1 and R2, store result in R3
```

## Storing the Result

Save the result back to memory using STORE:

```
STORE R3, [0x3000]; Store result matrix in memory
```

For larger matrices, loops and control flow instructions manage iterations over smaller blocks:

```
SET R4, 0 ; Row index
LOOP_ROW:
SET R5, 0 ; Column index
LOOP_COL:
MAT_MUL R3, R1, R2
STORE R3, [0x3000 + R4 * N + R5]
ADD R5, R5, 1
BNE R5, N, LOOP_COL
ADD R4, R4, 1
BNE R4, N, LOOP_ROW
```

## **Evaluating the Instruction Set**

#### 1. Efficiency

The inclusion of specialized instructions like MAT\_MUL and MAT\_LOAD reduces the number of cycles needed for matrix computations, enhancing performance.

## 2. Simplicity

The uniform and straightforward design of the instructions simplifies CPU control logic, making the architecture faster and easier to implement.

#### 3. Flexibility

While optimized for matrix multiplication, this instruction set includes general-purpose instructions, making it suitable for a wide range of applications.

## 4. Scalability

By supporting techniques like pipelining and SIMD, the instruction set can handle larger data sets efficiently as computational demands grow.

## **Conclusion**

A well-designed instruction set tailored for a RISC-based CPU can significantly improve the efficiency of computationally intensive tasks like matrix multiplication. By incorporating specialized instructions alongside general-purpose commands, this set strikes a balance between simplicity and performance. It not only optimizes operations but also ensures scalability and ease of maintenance, making it a robust solution for high-performance computing applications.