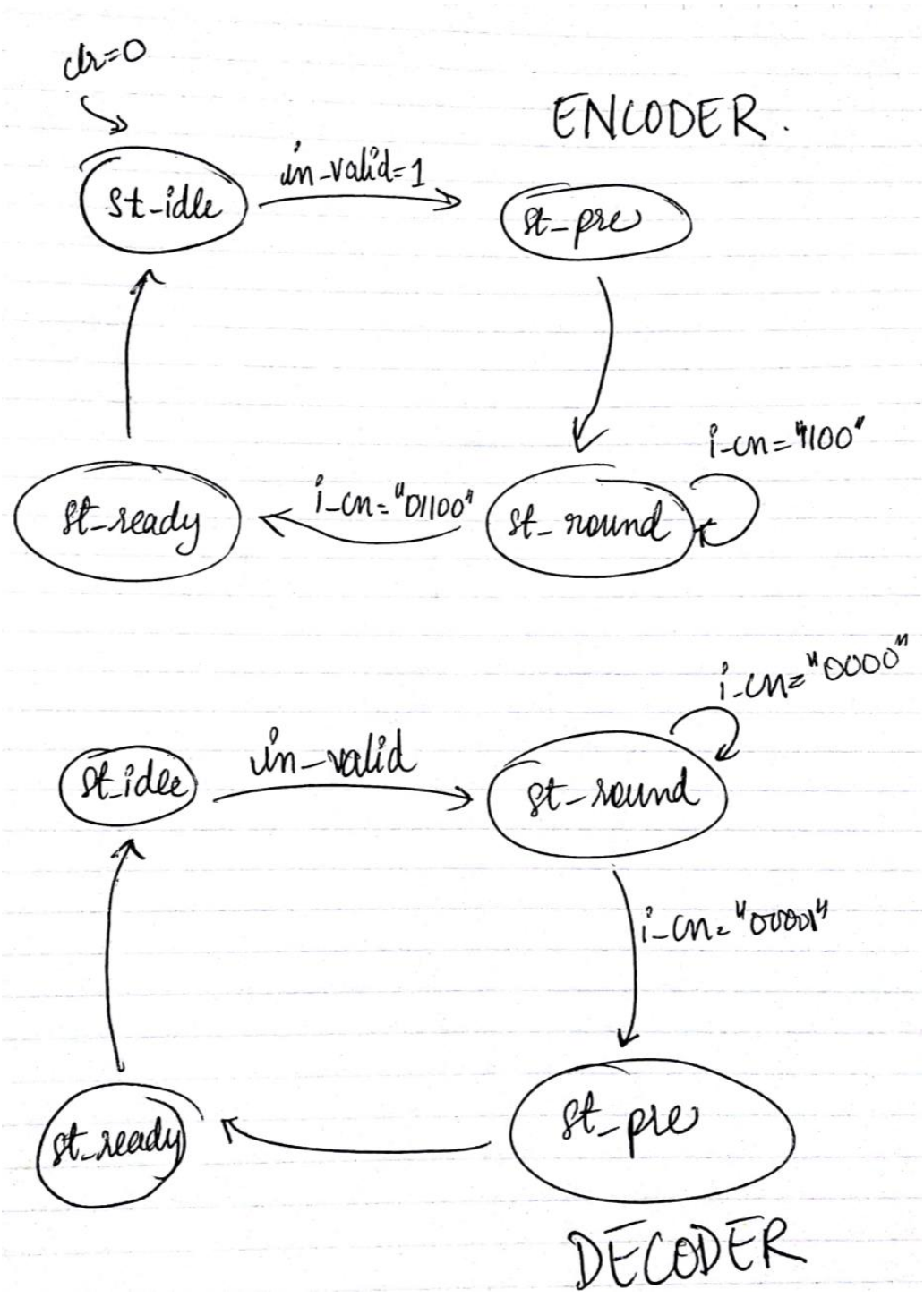
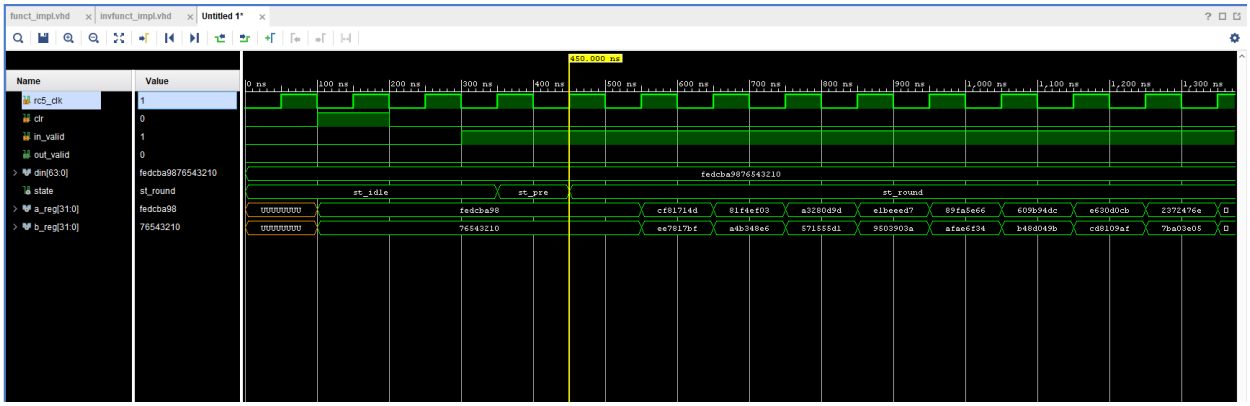
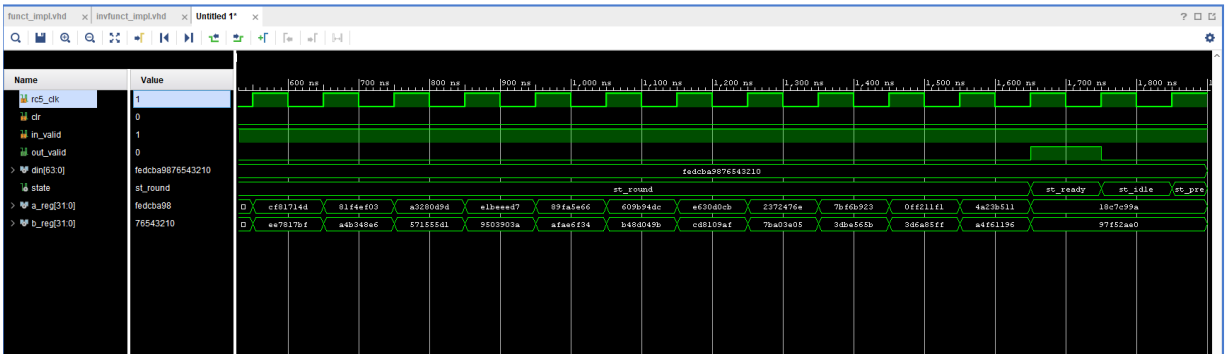
Lab 5 report:

FSM:

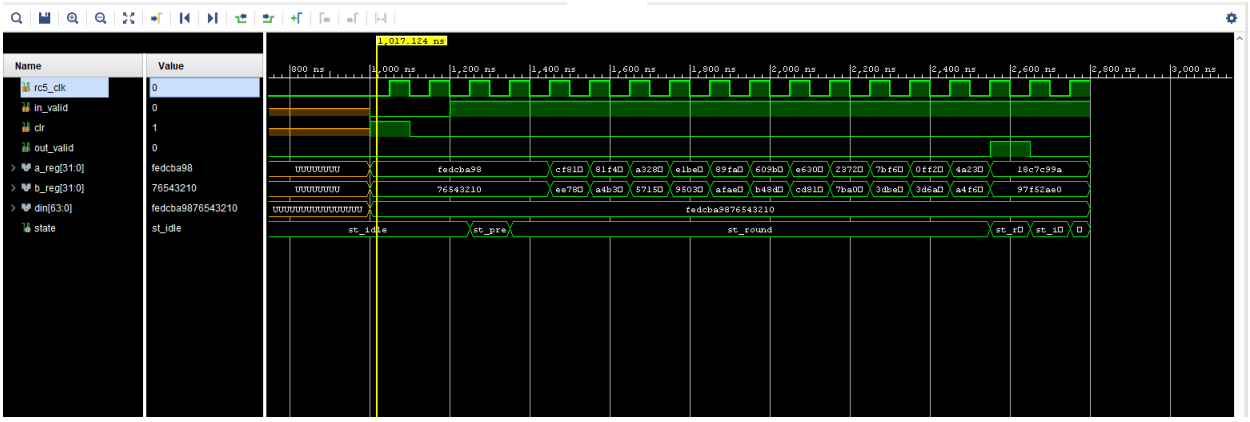


Behavioral Analysis of RC5

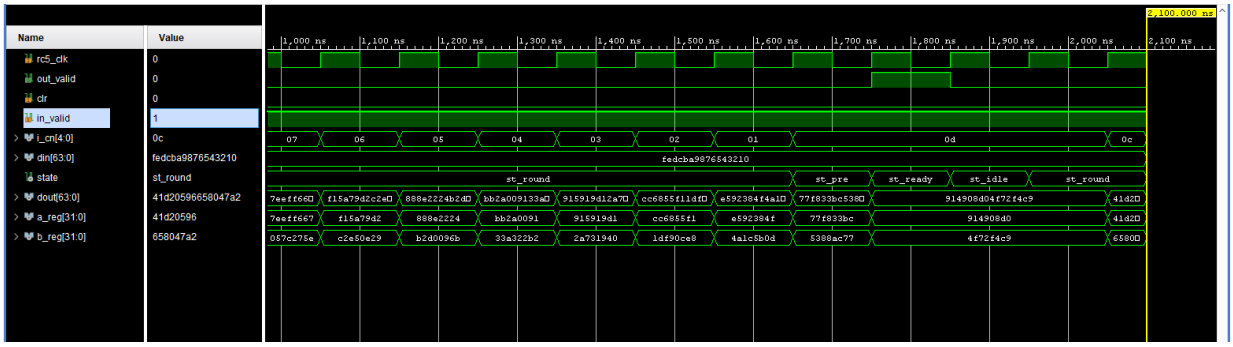




Timing Simulation of RC5



Timing Analysis of RC5
Decoder



Utilisation: (Post – Synthesis)

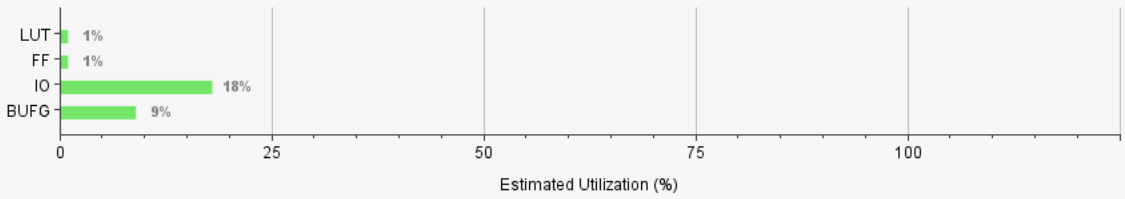
Utilization — **Post-Synthesis** | Post-Implementation

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	757	63400	1.19
FF	224	126800	0.18
IO	37	210	17.62
BUFG	3	32	9.38

Utilization — **Post-Synthesis** | Post-Implementation

Graph | Table



Utilisation (post – implementation)

Utilization — Post-Synthesis | **Post-Implementation**

Graph | **Table**

Resource	Utilization	Available	Utilization %
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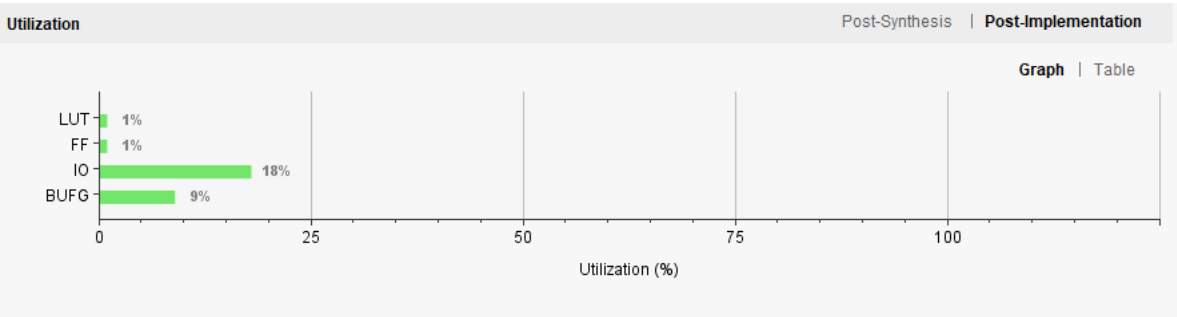

Timing Analysis:

| Timing Details

From Clock: sys_clk_pin

To Clock: sys_clk_pin

Setup : 0 Failing Endpoints, Worst Slack 6.070ns, Total Violation 0.000ns

Hold : 0 Failing Endpoints, Worst Slack 0.263ns, Total Violation 0.000ns

PW : 0 Failing Endpoints, Worst Slack 4.500ns, Total Violation 0.000ns

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Max Delay Paths

Slack (MET) : 6.070ns (required time - arrival time)

Source: i_cnt_reg[19]/C

(rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Destination: i_cnt_reg[10]/R

(rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})

Path Group: sys_clk_pin

Path Type: Setup (Max at Slow Process Corner)

Requirement: 10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)

Data Path Delay: 3.331ns (logic 0.766ns (22.999%) route 2.565ns (77.001%))

Logic Levels: 2 (LUT5=1 LUT6=1)

Clock Path Skew: -0.040ns (DCD - SCD + CPR)

Destination Clock Delay (DCD): 5.011ns = (15.011 - 10.000)

Source Clock Delay (SCD): 5.310ns

Clock Pessimism Removal (CPR): 0.259ns

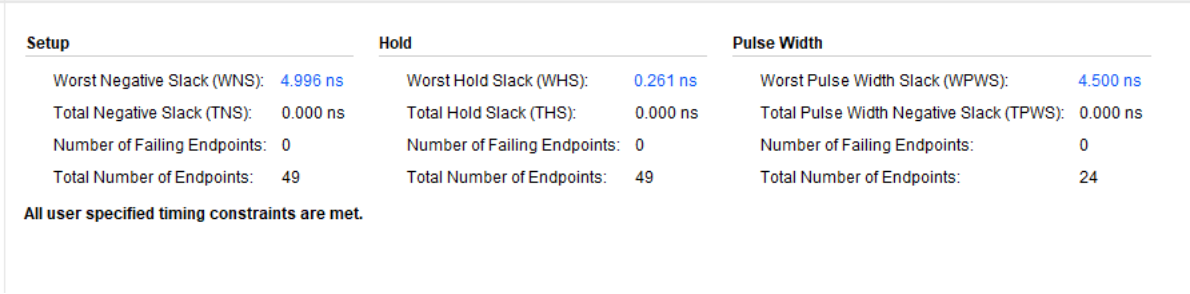
Clock Uncertainty: 0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE

Total System Jitter (TSJ): 0.071ns

Total Input Jitter (TIJ): 0.000ns

Discrete Jitter (DJ): 0.000ns

Phase Error (PE): 0.000ns



Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	4.996 ns	Worst Hold Slack (WHS):	0.261 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	49	Total Number of Endpoints:	49	Total Number of Endpoints:	24

All user specified timing constraints are met.

Critical path delay = 10ns – 4.996ns = 5.004 ns

Maximum speed : = 1/crirical path delay = 1/5.004 ns

Youtube Link: https://www.youtube.com/watch?v=juUdOn35mKs&feature=youtu.be