# Vishal Ramakrishna

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## Education

M.Sc. Information and Communication Engineering
Technical University of Darmstadt
2018 | GPA:2.54/5.0 (80-90 %)

B.E. Electronics and Communication Engineering
Visveswaraya Technological Institute
2014 | GPA:8.92/10 (81.7 %)

Class XII
SBMJC V.V.Puram, Bangalore
2010 | 94 %

## Skills

Programming : Assembly, C, Python, Unix Scripting, C++, Basics of Verilog

Tools : MATLAB, Agilent ADS, CST Microwave Studio, MS-Office, Arduino

Hardware : TCI6638K2K Multicore DSP, LA9358, LA1224 NXP SoC, Arduino

Languages: English, German, Kannada, Hindi

## Work Experience

2018 May - DSP Engineer - CommAgility | Duisburg, Germany — 1.7 Years
- Embedded Software Developer PHY L1 on baseband Digital Signal Processors for small cell 5G NR gNB, LTE/LTE-A/private LTE eNodeB.
- Implemented UL chain symbol level at gNB (3GPP Rel.15) including physical channels such as PUCCH, PUSCH, SRS, on platforms such as TCI6638K2K Multicore DSP + ARM Keystone II SoC, and Vector signal processors NXP.
- Implemented primitive kernel functions in assembly optimized for FIR filters, FFT, Channel estimation, MMSE Equalizer.
- Implemented primitive modules in the host side to read/write shared memory over TCP/IP, schedule tasks, memory management etc.
- Support to generation of Test Vectors, verifying with VSA, and automating the testing using bash/python scripts.
- Simulations in MATLAB for 5G NR Tx/Rx Beamforming, Channel Estimation, Antenna modelling at gNB.

Aug-Feb'18 Master Thesis - TU Darmstadt | Darmstadt, Germany — 10 months
- Channel estimation for Massive MIMO systems based on compressive sensing principles using receive power measurement.
- Simulated an UL Massive MIMO system with Receive Beamforming and perform Channel Estimation using a novel algorithm based on Compressed sensing principles (STELA).

Aug-Feb'17 Student Intern - Intel | Munich, Germany — 6 Months
- System level plan and signal generation in MATLAB for RF receiver test cases for addition of CDMA2000 RAT in Intel Modems (3GPP2).
- DL receiver chain modelling in MATLAB and preparation of reference at UE side.

Apr-Jun'16 Student Intern - Rohde & Schwarz GmBh | Munich — 3 months
- Channel sounding measurement campaigns for channel parameter estimation at mm-wave frequencies.
- Experience to work with R & S signal generators and frequency analyzers.

## Academic Projects

Apr-Aug'15 Search free based direction of arrival estimation algorithms
- Simulated signal processing algorithms MUSIC, ESPRIT, Root-MUSIC, Root-RARE for fully and partly calibrated array of antenna systems.

Oct-Mar'16 BAW based RF duplexer module
- Designed and fabricated a RF duplexer module using Agilent ADS with Power Amplifier and BAW filter at GSM bands.
- S-parameters of the fabricated device were measured to compare with the simulations of the design.

Oct-Mar'16 Design, implementation and synthesis of a MIPS-I processor core
- Implemented architecture was a 4 stage pipeline with a load store 32 bit instruction set and synthesized on a FPGA.

Oct-Mar'16 Optimal luminance control of networked lights
- Programmed an Arduino Yun using Python to automatically control luminance of the networked lights.

Sep-Aug'14 Bachelor Thesis
- Eyes free interaction for mobile reading devices.
- Constructed a mobile prototyping device based on the Arduino Yun capable of capturing an image document, comprehending the text and converting text to speech