

# CONTINUUM '25

## PS - 1

### The Two Stage Op-Amp Design

You are required to design a two-stage Miller-compensated op-amp with a capacitive load. A typical two-stage op-amp looks like:

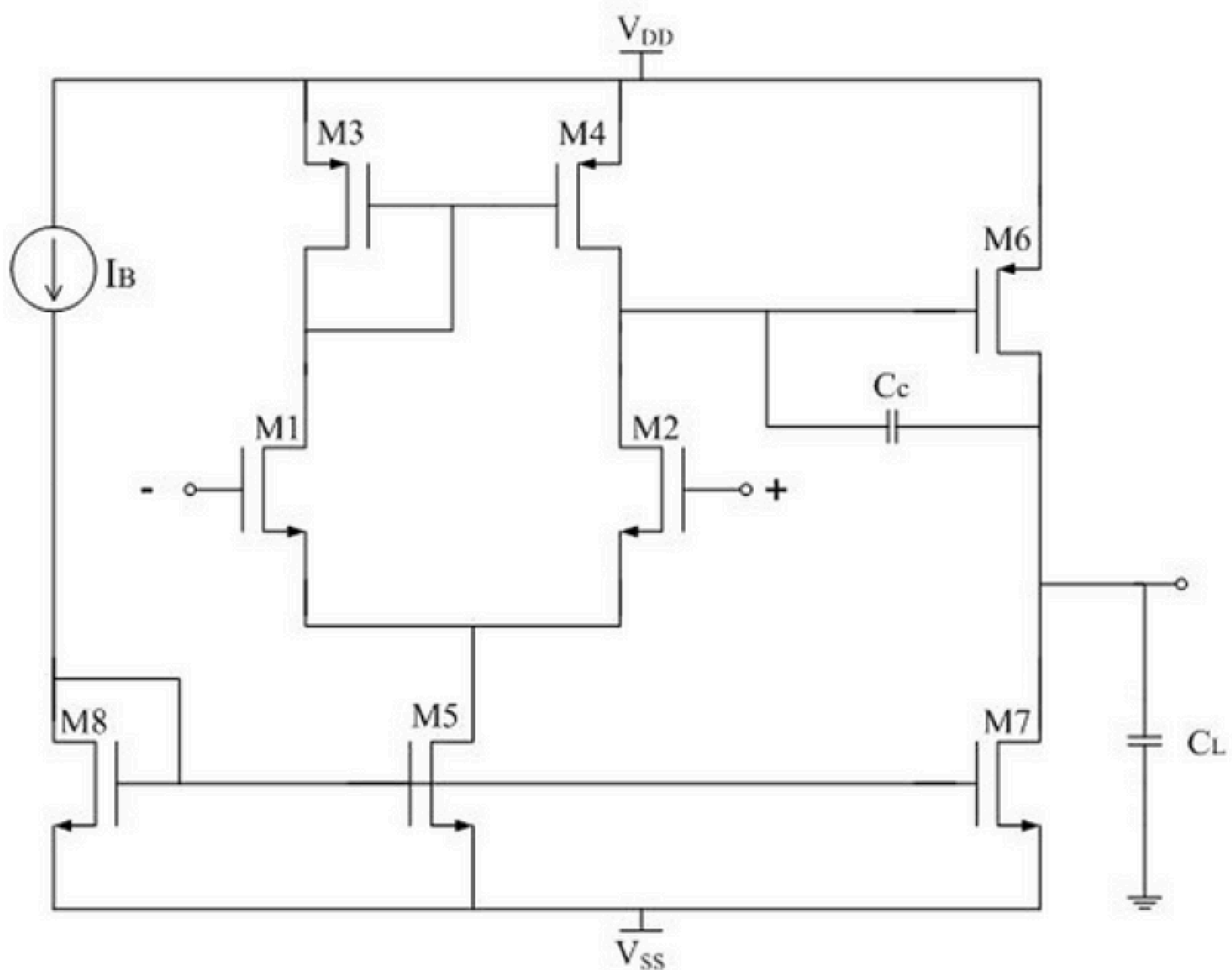


Figure 1: NMOS Two Stage op amp

## Design Specifications

Your op-amp model will be evaluated based on how closely it meets the following specifications:

- Reasonable lengths and widths of NMOS transistors must be used. Report the W and L of each transistor. [ 5 points ]
- DC gain = 90dB [ 5 points ]
- Input Common Mode Range 0.7 V to 1.6 V [ 5 points ]
- Phase margin > 60 degrees for a capacitive load of 5 pF [ 5 points ]
- Gain-bandwidth (GBW) product of 30 MHz [ 5 points ]

Given:

For NMOS,  $V_{th} = 0.7V$ ,  $\lambda = 0.04 V^{-1}$ ,  $\mu_n C_{ox} = 100 \mu A/V^2$

For PMOS,  $V_{th} = -0.7V$ ,  $\lambda = 0.05 V^{-1}$ ,  $\mu_p C_{ox} = 50 \mu A/V^2$