Design & Implementation of High Speed and Low Power PLL Using GPDK 90nm Technology.

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Abstract: With progress in the design of phase locked loop (PLL) circuit, critical parameters like, power dissipation, phase noise, and area, has had to be considered within the analysis. The key aspect of effective PLL design is the lock in time, which presents a major challenge in the PLL usage in high-speed communication systems. As the PLLs are gradually being used for synchronization, clock synthesis, and reducing the jitter in wireless communications, due to increment in the circuit operation rate, there is an immediate need to design PLL circuits with fast locking capacity. In this article, an efficient PLL, employing current starved voltage controlled

oscillator is designed to maintain linear it of its gain, using the Cadence Virtuoso tool, which is then simulated using the Spectre tool. Since the PLLs are extensively implemented over high frequency ranges due to incurring less time to lock frequency, the designed PLL's lock time is set to 300 ns. Further, the designed PLL features a 3.09–3.2 GHz tuning range, a 5.2 GHz central frequency, small phase noise of − 71.51 dB/Hz at 1000 kHz, along with 264 p s jitter. In addition, the proposed PLL dissipates a power of 50.8 μ W, for 1 V supply. Extensive simulation results demonstrate that the proposed sub module architecture of the proposed PLL system performs better compared to the existing designs with respect to power consumption, operating frequency, phase noise, and jitter.

Introduction: Key factors for current and future communication systems include power, cost, and wide frequency range. PLLs, critical in system-on-chip designs, synchronize output frequency and phase with input using a phase frequency detector (PFD). They generate clock signals (multiples of a reference clock) and are widely used in communication systems, clock synchronization, frequency synthesis, and data recovery. However, traditional PLL designs face challenges like high power consumption, complexity, and large chip area. A study [2] demonstrated a high-speed, low-power PLL operating at 3.5 GHz with 508 ns lock time, using 180 nm technology and 1.8 V supply.

Keywords:

· PFD

· Charge pump

· Current starved VCO

· Phase locked loop

CMOS PLL Block Diagram:

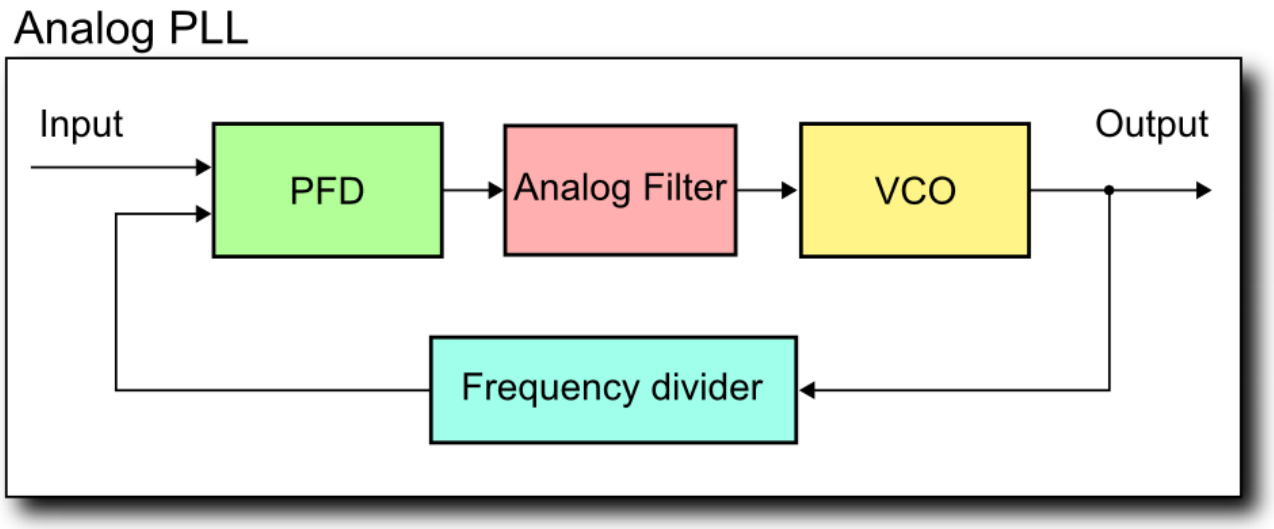

Fig1: Block diagram of Analog phase Locked Loop (PLL)

A Phase-Locked Loop (PLL) is a vital electronic circuit widely used in communication systems, signal processing, and integrated circuits for synchronizing an output signal's phase and frequency with a reference signal. It operates as a feedback control system and comprises key components such as a Phase Frequency Detector (PFD), charge pump, low-pass filter (LPF), and voltage-controlled oscillator (VCO). The PFD compares the phase of the reference signal with the output, generating an error signal that the charge pump converts into control voltages. The LPF smoothens these voltages to remove noise before they adjust the VCO, which generates the output signal. PLLs are employed in frequency synthesis, clock recovery, jitter reduction, and channel selection in communication and signal processing applications. Despite their advantages, such as accurate frequency matching and stable performance, PLLs face challenges like high power consumption, large chip area, and design complexity, especially at high frequencies. Modern advancements in PLL technology focus on reducing power dissipation, supporting ultra-wideband (UWB) frequencies (3.1–10.6 GHz), and leveraging advanced fabrication technologies like 90 nm and 180 nm CMOS to enhance performance and miniaturization. These developments have solidified PLLs as indispensable components in modern electronic and communication systems.

Phase frequency Detector(PFD):

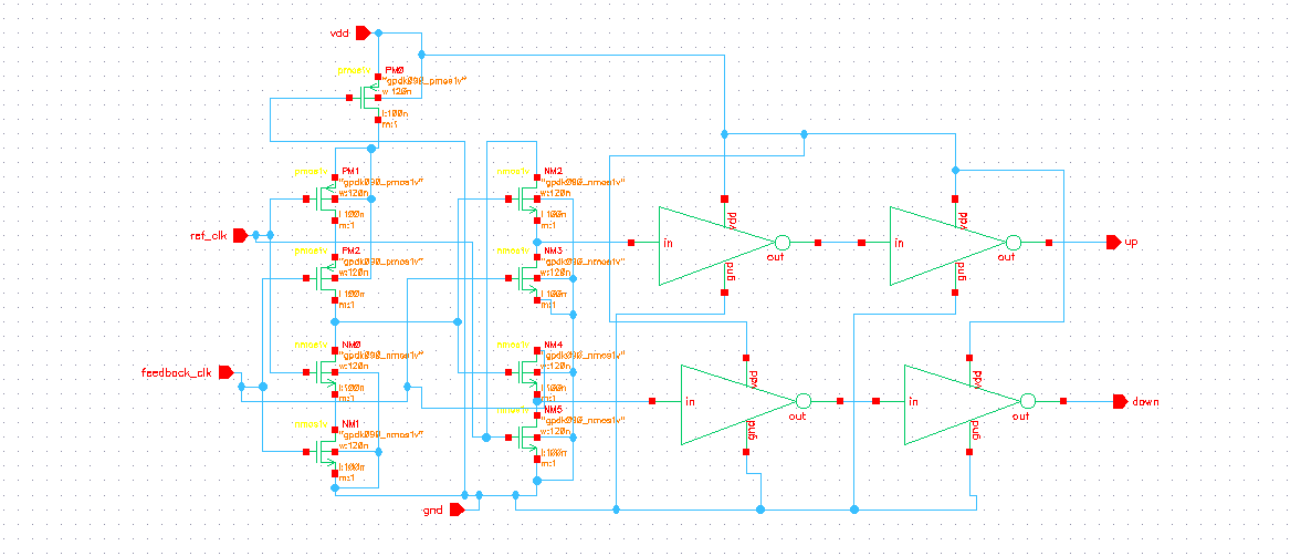

Fig2: PFD (Phase frequency Detector)

1. Power dissipation of the proposed PFD is reduced as compared to the existing studies by removing the reset path.

2. Speed of the proposed PFD is also improved by reducing the clock skew using true single phase clock (TSPC) and widening the acquisition range.

3. VCOs oscillation frequency is improved by increasing the number of stages compromising the circuit's complexity.

4. PLL's overall phase noise and jitter is improved considerably by using TSPC logic.

It must be noted that, in the current work, the dead-zone free dual-edge triggered D flip-flop is assumed for the PFD architecture. It is also assumed that the design of CP consumes a power of 79.069 m W [4]. In addition, the CS-VCO is designed at an operating frequency of 10 MHz with control voltage of 1 V, which provides an output oscillation frequency of 1.119 GHz and a total power of 18.91 µW lastly, it must be noted that the power consumption will be higher as the output frequency increases. The structure of remaining article is as mentioned below: Section "Proposed

PLL Design" details with related sub blocks. Section "Simulation Results" presents and discusses the simulation results of each sub-block, and compares the proposed design with recent existing studies. Finally, Section "Conclusion" concludes the study.

Charge pump schematic:

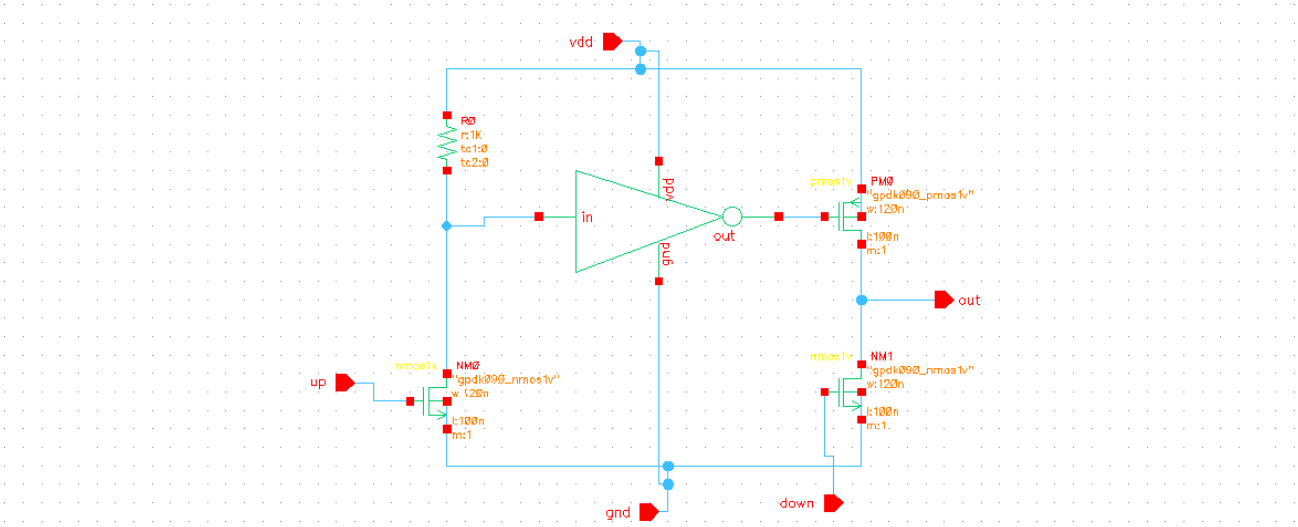

Fig3: Charge pump schematic

The schematic for a CP with a loop filter is depicted in Fig. 3. The CP changes the difference in phase (error signal) to the current signal, when it serves as a bipolar switched current source in the PLL. Hence, CP generates source, sink current pulses in proportion to difference in frequency, and phase difference amid the feedback and reference signal. The loop filter is driven by the current pulses, which produces varied control voltage and, consequently, varies the PLL output frequency. The CP acts as current sourcing or sinking device in harmony to the voltage applied. Tristate CPs, often considered as single-ended CPs, is mostly used owing to their small power necessities, flexibility, and reduced chip size, with pads, and peripheral components. A CP circuit transforms the logic state of PFD to analog signal, which is then used by the VCO to modify the frequency. It is positioned between the VCO and the PFD block and connected to the loop filter. In Fig. 3, two PFD outputs i.e., UP and DOWN, are applied to the CP, which then produces one output to be sent to the loop filter. Charging occurs when the CP's current flows across it, and enters the loop filter,

which follows when the DOWN signal would be LOW and HIGH for UP signal. On the other hand, discharge occurs when CP current leaves the loop filter, if the DOWN signal reaches high and the UP signal becomes LOW. In general, output of the CP is independent of the strength of the UP and DOWN input signals.

Schematic of CS-VCO:

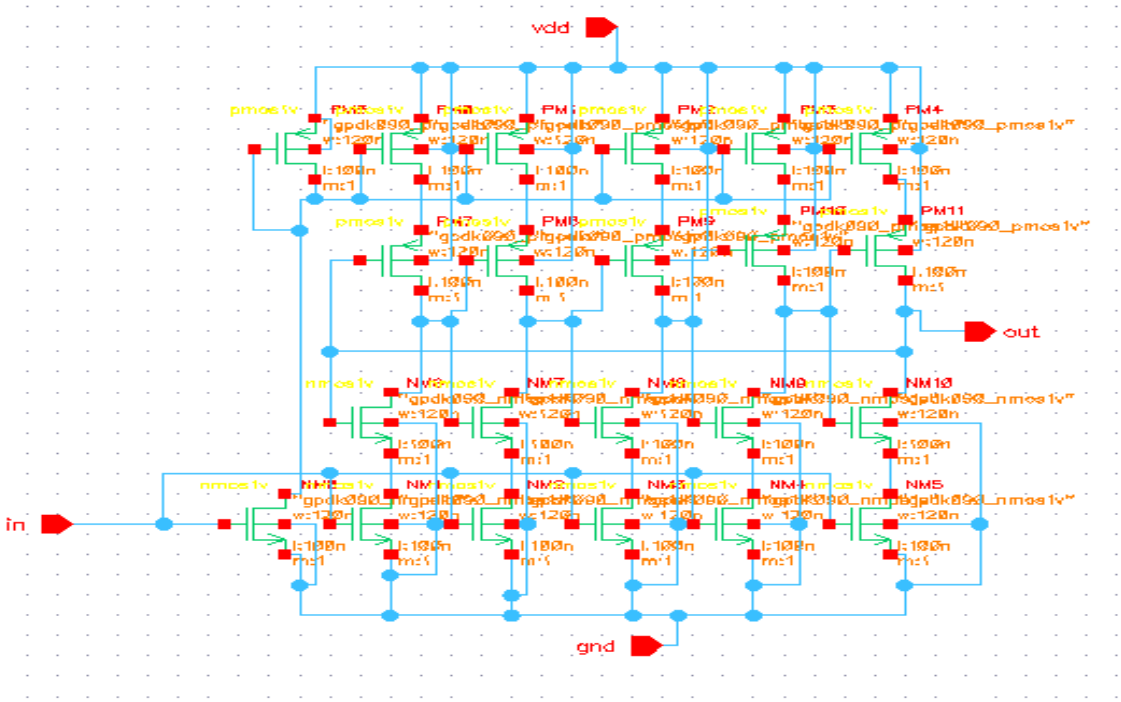

Fig. 4 Schematic of CS-VCO

The VCO is an essential block as its performance controls multiple performance parameters of the PLL system. An input voltage produces the oscillating frequency. In VCO, the number of stages implemented can alter its output frequency. Further, VCO's oscillation frequency can be improved by increasing number of stages, in turn improve the phase noise as it is filtered at every stage. In fact, with greater number of stages 'N', circuit complexity increases which increases the power dissipation. The VCO's input signal can alter the oscillation frequency of VCO.

Fig.4 shows the schematic diagram of a CS based VCO, which performs the role of a ring oscillator, and is frequently used due to its wide frequency range and low power [15]. The top and bottom current

sources (i.e., PM20 and NM11) reduce the amount of current available to the inverter, causing it to be current starved. The transistors in the center (i.e., PM8 and NM16) create an inverter. Further, PM25 and NM18 drain currents are identical, which are con trolled through the control voltage V ctrl. The current is reflected from the PM25 transistor to all pull up PMOS transistors. Drawback of the CS-VCO is that it consumes large amount of power, which necessitates the deployment of alternate circuit viz., the stacked sleep circuit that significantly reduces the power.

Schematic of freq. divider:

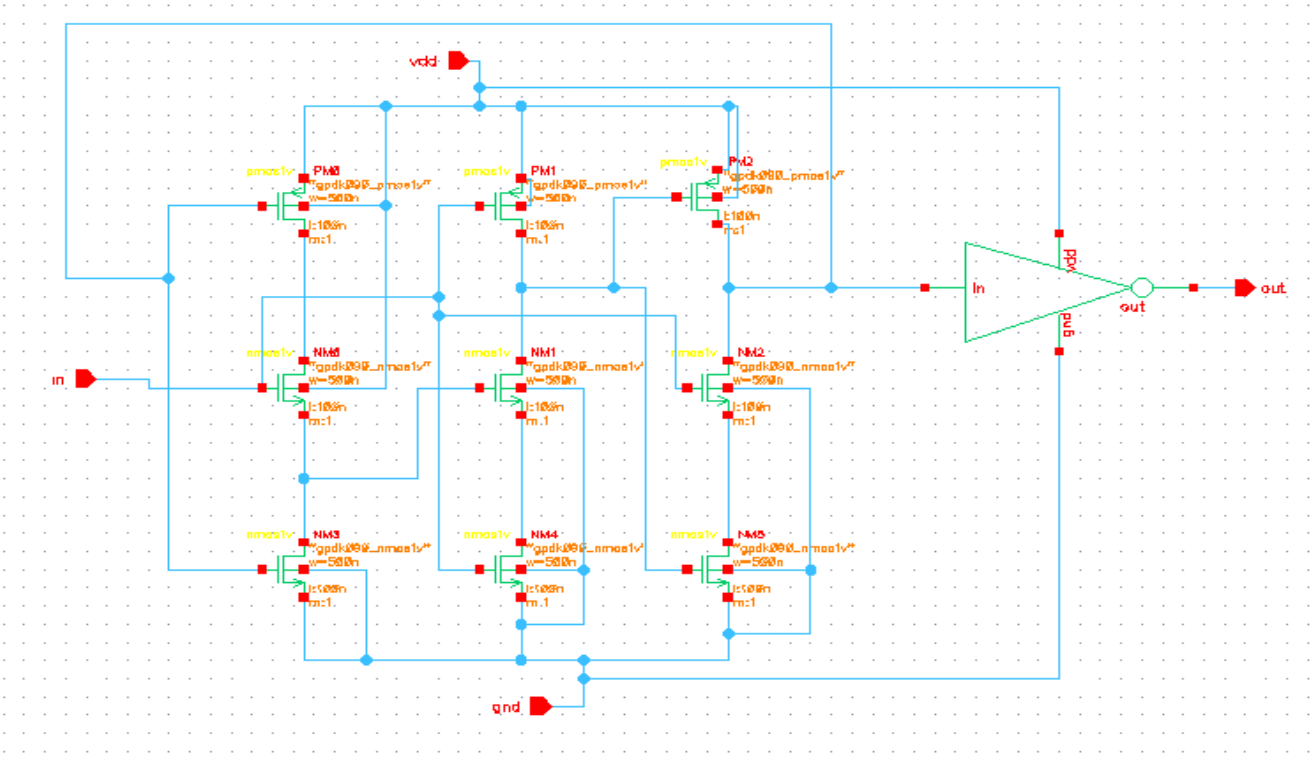

Fig5: Schematic of freq. divider

The output of VCO is provided as input to the frequency divider, where the frequency is divided by two, in turn, its output will act as input to PFD. Then the reference signal is compared with this feedback signal, when both signals have same phase and same frequency, PLL arrives to lock mode and the output frequency will be double of the input frequency [16]. The signal generated by a VCO circuit, its frequency changes with the input voltage. An error signal is produced by the PFD when it compares phases of the two

signals. By producing a signal with half frequency as that of the number of pulses counted, a counter circuit generates and counts the number of pulses in a signal. Two D flip-flops are used to create a counter circuit, as shown in Fig. 5. When clock signal changes, a D flip-flop circuit switches its output while keeping one bit of data.

Power Analysis:

Power analysis for a Phase-Locked Loop (PLL) involves evaluating the power consumption of its key components, such as the Phase Detector (PD), Voltage-Controlled Oscillator (VCO), Charge Pump (CP), Frequency Divider, and Loop Filter. Here's how you can structure and interpret your analysis using Cadence software:

Phase Detector

- Simulate to measure the dynamic and static power of the PD.
- Factors to analyze.
    - Switching activity (frequency and duty cycle of the input signals).
    - Technology node (affects leakage current).

Charge Pump

- Monitor the current drawn during the UP/DOWN pulses.
- Calculate P=VDD ·I avg P = V_{DD} \cdot I_{avg}P=VDD·I avg to estimate dynamic power.
- Analyze the mismatch effects if present, which could cause extra power dissipation.

Voltage-Controlled Oscillator (VCO)

- Measure power consumption during oscillation at the desired frequency.
- Include supply voltage and tuning voltage variations in your analysis.

Frequency Divider:

- Estimate power based on the division ratio and switching frequency.
- Higher division ratios typically lead to more toggling and, thus, increased dynamic power.

Corner Analysis:

Corner Analysis	PWR
AVG (NN)	7.754E-3
AVG (SS)	7.746E-3
AVG (FS)	7.746E-3
AVG (SF)	7.783E-3
AVG (FF)	7.763E-3

Table: Corner Analysis of PLL.

POWER ANALYSIS OUTPUT:

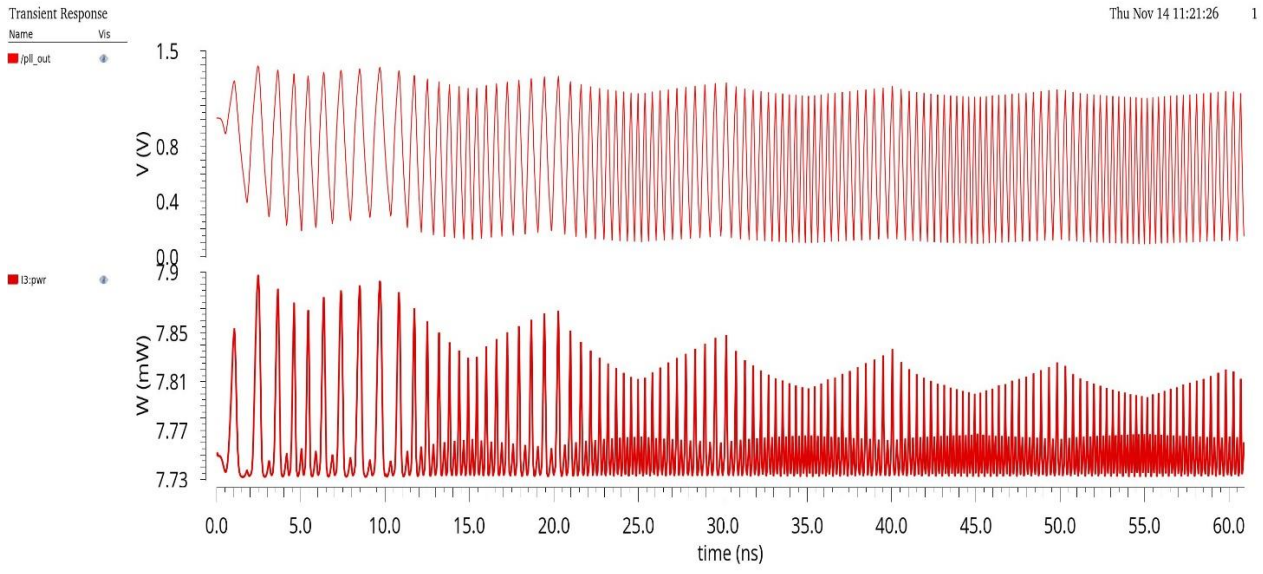

Fig6: Power analysis

Schematic of phase locked loop (PLL):

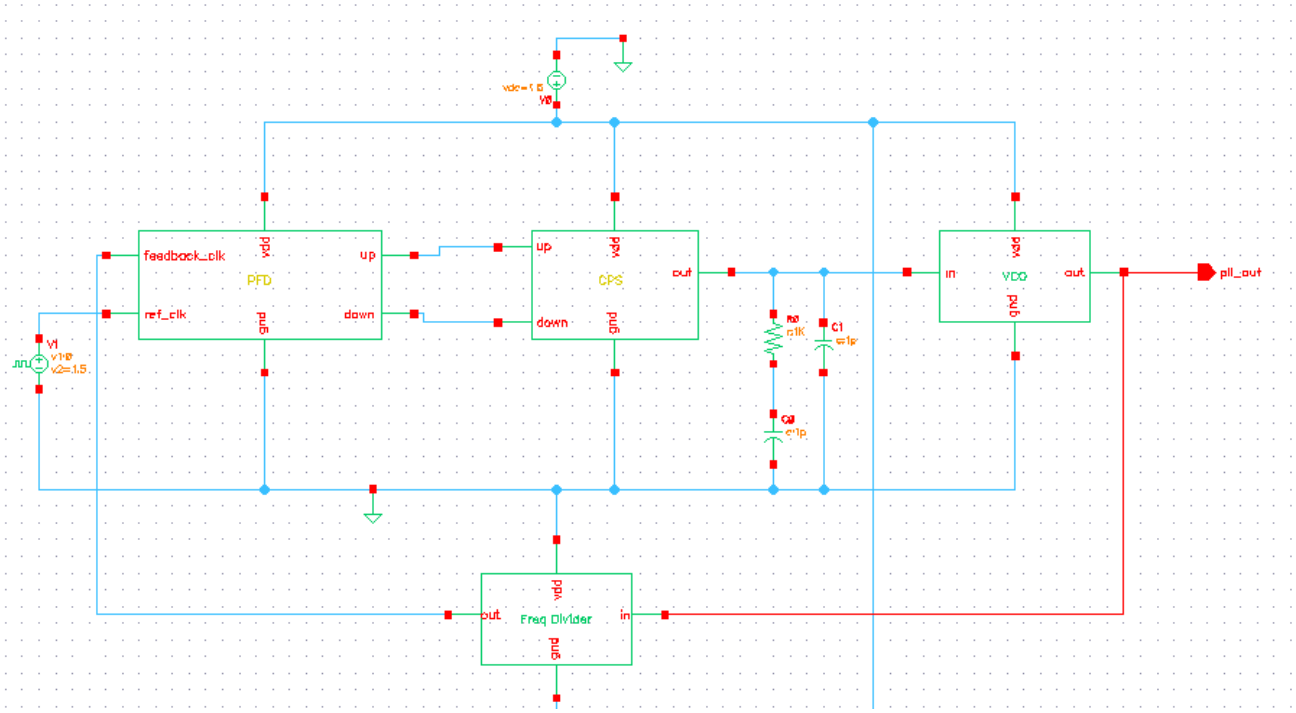

Fig7: Final PLL Block

Final output of PLL:

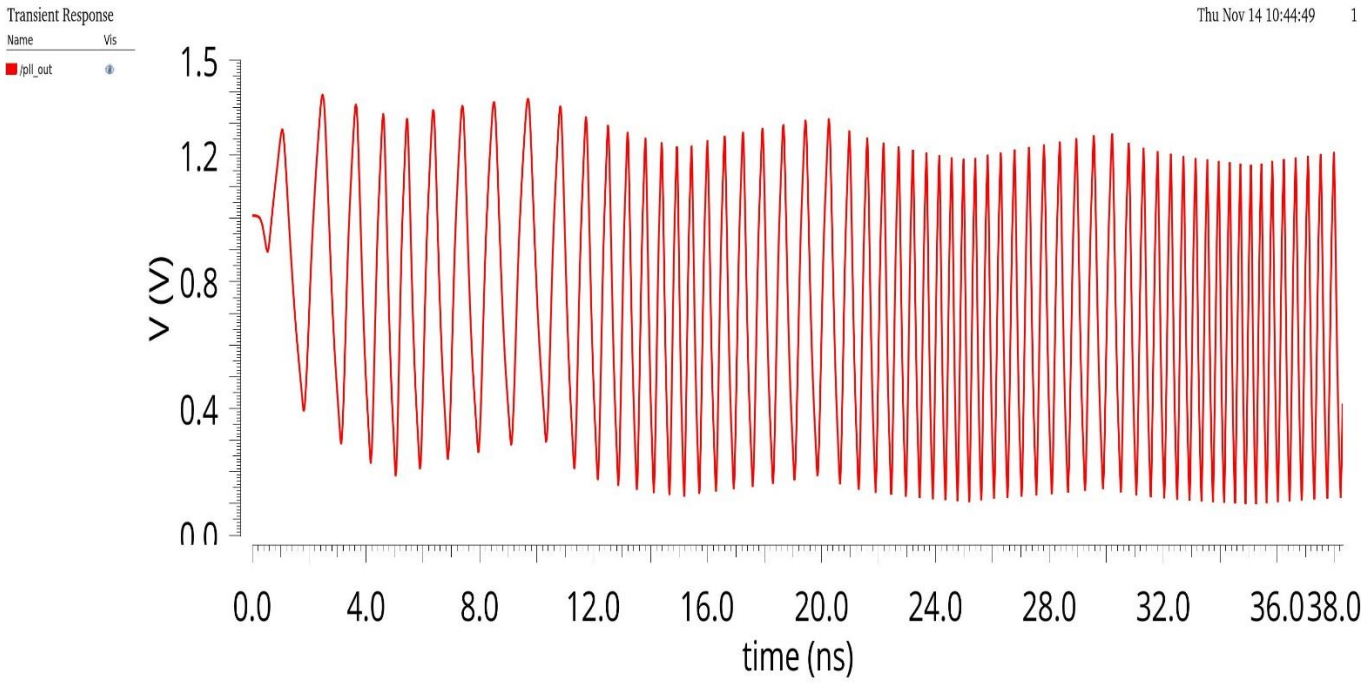

Fig8: PLL OUTPUT

Conclusion:

In this report, a PLL system is proposed with sub modules, which are designed, using the Cadence Virtuoso tool and Spectre simulator in 90 nm GPDK technologies. The proposed design performance is analyzed with existing designs considering multiple key parameters. The power dissipation achieved for the proposed PFD is found to be 70.96 n W, and power consumption for the traditional CP of 2nd order passive filter and CS-VCO are observed as 68.5 μ W and 37.62 m W, respectively. Further, all the sub blocks are integrated to form a high speed and low power PLL, which results in high frequency generation. The work in this paper improves the performance of each blocks of PLL, and demonstrates a power dissipation of approximately 50.80 m W in the frequency range of 3.09–3.20 GHz. The results make it evident that the proposed design significantly improves the power dissipation, phase noise and output frequency. As a future scope for research, it is required to improve the phase noise and reduce the PLL's lock-in-time, area and power dissipation.

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