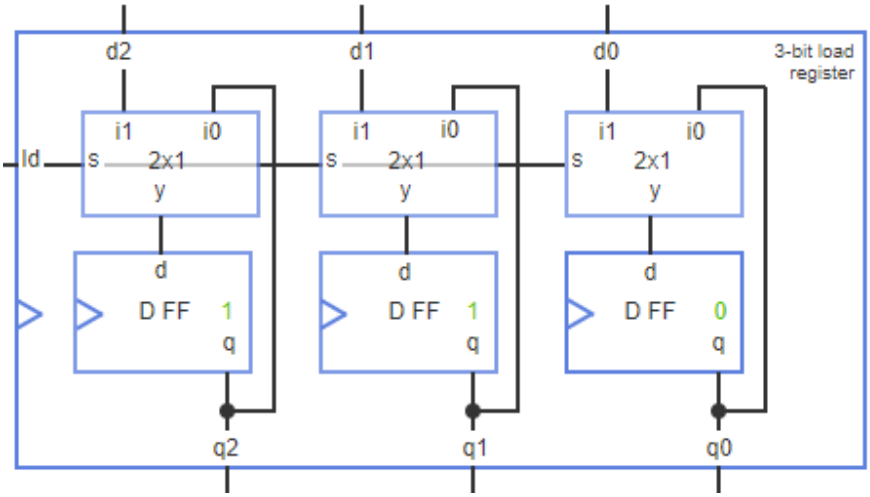
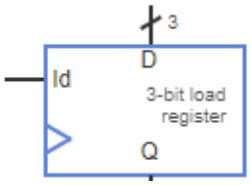
Problem 1) Develop an 8-bit load register similar to the register shown in the diagram below (except yours will be 8-bits wide instead of 3):




Function table

| ld | Register function |
|---|---|
| 0 | Maintain |
| 1 | Load |

Block symbol




Use SW[7:0] for the data input, SW[9] for the Load signal, and Key 1 for the clock signal.

Problem 2) Extend the register in problem 1 to include the functions in the following table:

| SW[9:8] | Register Function |
|---|---|
| 00 | Maintain (No change in Q) |
| 01 | Load (Q = D) |
| 10 | Synchronous Clear (Q = 0) |
| 11 | Complement (Q = NOT Q) |