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(57) Abstract :
This patent presents LSAC (Low-Power Adder Tree for Digital Computing-in-Memory), a novel approach designed to enhance energy-efficient computation in memory (CIM) architectures. As digital CIM architectures replace analog implementations for improved accuracy, the power and area overhead of digital adder trees remain a significant challenge. This invention introduces a low-power adder tree design that integrates sparsity techniques and approximate circuit co-design. By leveraging multiple sparsity modes and fine-grain pruning algorithms, the proposed solution effectively reduces power consumption by 30.0% and area by 19.3% while maintaining high accuracy in neural network applications. The LSAC method utilizes customized approximate full adders (AFAs) and a two-level Wallace tree structure to minimize computation errors while optimizing performance. This invention significantly improves the efficiency of digital CIM architectures, making it a breakthrough for power-constrained edge computing devices.

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