Assignment

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4 'B'

Q1 List the assembler directives of ARM controller with details of each of them.

Ans The ARM assembly language has assembler directives to reserve storage space, assign numerical values to address labels and constant symbols, define where program and data blocks are to be placed in memory, and specify the end of the source program text.

Some of the assembler directives are:-

(i) AREA → which uses the argument CODE or DATA, indicates the beginning of a block of memory that contains either program instructions or data.

(ii) ENTRY → specifies that program execution is to begin at the instruction that follows it.

(iii) DCD → Used to label and initialize the data operands.

(iv) EQU → Declare symbolic names for constants.

(v) RN → To use symbolic names for registers, relating to their usage.

Q2 List the various modes of controller operation and how the bank registers are used during mode switches.

Ans There are 7 different modes of controller operation:-

(i) User Mode:-
- → Application programs run in User Mode
- → The normal 16 processor registers are in use.

(ii) Five Exception Modes:-

→ Fast interrupt (FIQ) mode is entered when an external device raises a fast interrupt request to obtain urgent service. The FIQ interrupt is intended for one device or a small number of devices that require rapid response.

→ Ordinary interrupt (IRQ) mode is entered when an external device raises a normal interrupt request. All other I/O devices use the IRQ interrupt line to request service.

→ Supervisor (SVC) mode is entered on powerup or reset or when a user program executes a Software Interrupt instruction (SWI) to call for an operating system routine to be executed. This is the highest priority exception. It places the processor into a known initial state so that operating system software can begin or restart operation properly. Any program executing when this exception occurs is abandoned.

→ Memory access violation (abort) mode is entered when an attempt by the current program to fetch an instruction or data operand causes a memory access violation. Processor implementations may include a memory management unit that restricts programs to valid areas of the address space for their instructions and data. If the processor issues an address for an instruction fetch or data operand access outside these areas, an exception occurs and the Abort mode is entered.

→ Unimplemented instruction mode is entered when the current program attempts to execute an unimplemented instruction. If the processor tries to execute an instruction that is not implemented in hardware, an exception is raised and the Undefined mode is entered.

(iii) System Mode :-

→ The System mode is a priviledged mode that uses the same registers as those used in the User mode.

→ It can only be entered from another exception mode. Its purpose is to facilitate linkage to subroutines during exception handling without overwriting the link register R14_mode.

→ When in System mode, subroutine Call instructions use the normal link register R14. After returning from all subroutine calls, the original exception mode is reentered, regaining acess to the link register R14_mode.

Banked register perform the following functions to switch mode operation:-

(i) The contents of the Program Counter (R15) are loaded into the bank Link Register (R14_mode) of the exception mode.

(ii) The contents of the Status Register (CPSR) are loaded into the banked Saved Status register (SPSR) mode.

(iii) The mode bits of CPSR are changed to represent the approximate exception mode, and the interrupt-disable bits I and F are set appropriately.

(iv) The Program Counter (R15) is loaded with the dedicated vector address for the exception, and the instruction at that address is fetched and executed to begin the exception-service routine.