EECT/CE 6325 VLSI Design

Fall 2022

PROJECT #4: Cell Library
Due: Wed. Oct. 26 (11:30 am)

Project Introduction

For this project you will be creating your standard library of cells (without D-Flip Flop), which will be used for your final project.

Project Goals

1) Layout and verify the following cells:
   - INV
   - NAND2
   - NOR2
   - XOR2
   - MUX2:1
   - AOI21
   - OAI22
   - AOAI211
2) All your cells should be placed side by side, next to each other, and have no DRC errors. All pins must be aligned horizontally with uniform spacing.
3) Do not use the library.lib provided for Project 2, instead generate a .lib file for the given set of cells using *PrimeLib*. For generating a library follow the instructions given in *PrimeLib by Synopsys* document uploaded on eLearning in Project 4 folder.
4) The height of the pMOS diffusion (RX drw layer) must accommodate 6 contacts and the height of the nMOS diffusion (RX drw layer) must accommodate 4 contacts.
5) Generate abstract views of your cells, use instructions given in *Abstract View Generation* document uploaded on eLearning in Project 4 folder)

Project Rules & Requirements

1) All the cells should have the same height with VDD & GND rails aligned horizontally.
2) The length of the channel (L) must be 70 nm
3) The input slew rate is 60 ps (0.1*Vdd to 0.9*Vdd and vice versa)
4) Assume a 70 fF load capacitance when simulating.

What to Turn In (points are deducted for anything missing)

1) A cover page containing all the following information.
   - Name, NetID and project title
2) Each cell layout with **rulers** showing the dimensions of the cell. Part of grade depends on the clarity of your ***report***.
   - Show the distance between your pins
   - Show the length of the channel
   - Show the height & width of entire cell.
3) Also turn in the following for each cell in your library:
   - Simulation data that shows each transistor works in each cell
4) Please also hand in a layout showing all your cells lined up in a row with the boundary layers touching to demonstrate that they can be placed next to each other with no problems (yes, that means run DRC).
   - Show distance between pins to verify that they have a uniform pitch.
5) Upload the project report on eLearning.
6) Upload the zipped folder containing all layouts and schematics on eLearning

Grading Breakdown

Correct functionality of all cells	50%
Correct pin spacing and cell sizing	20%
Report	30%