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EEDG6302: Microprocessor and Embedded Systems

Wednesday Lab Report

Part_5 Task:

- Understanding hierarchical designs in HDLs
- Creating testbench to validate the whole design
- Creating a bit file and upload it to an FPGA
- Interfacing FPGA evaluation board with inputs and outputs

Week 5 Summary:

The goal of this week's task is to verify the entire MCU modules created so far.

We have written Verilog module for stitching whole MCU according to pipeline stages. As given in the MCU module Top view, it has 4 stages of pipeline namely, Instruction fetch, Instruction Decode, Execute, Write Back. I wrote testbench for the MCU to verify its functionality by checking the signal values for each module. This helps me to debug the bottom-up hierarchical design.

Also, we interconnected the modules for the given driver inputs with minsys module provided in the handout. Looking forward to interface with FPGA board and observe the output.

Problems Encountered During Design:

- We had to check with other modules for the exact input and output dependent names are similar.
- Writing the modules in non-blocking to avoid synthesize error in future.