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EEDG6302: Microprocessor and Embedded Systems

Wednesday Lab Report

Part 3 Task: Designing and simulating synthesizable ID (Instruction Decoder) and Constant Unit of the MCU

Week 3 Summary:

The goal of this week's task is to verify the Verilog module synthesizable ALU (Arithmetic Logic Unit), Register File and required Multiplexors individually.

We have written Verilog module for instruction decoder for MCU. As described in project description, Instruction decoder takes 17-bit instruction as input and generates control signal for MCU to function properly. Verilog module decodes the 5-bit opcode from instructions. We are using switch case to execute corresponding opcode. We have implemented the given opcodes. To test this module, we have hardcoded few instructions like No operation, Add, logical left shift in a test bench to verify the corresponding control signal in simulation. In simulation, we get the desired results.

We have written Verilog module for Constant Unit for MCU. As described in project description, , we need to "extend" 6 bits to 8 bits. The duty of the Constant Unit in your MCU is to perform this extension. To test this module, we have passed hard coded inputs in a test bench to verify the sign extended output signal in simulation, where we get the desired results.

Problems Encountered During Design:

- We had to check with other modules for the exact input and output dependent names are similar.

1. What is sign extension mean? Explain briefly in 1 to 2 lines.

   Sign extension is utilized to increase its bit-length by duplicating the most significant bit and filling the remaining bits in-order to maintain the sign of a binary number.

2. Imagine that you want to add another instruction named "ADN". This specific instruction gets two inputs. It inverts one of them and add it with the other input. Into which category of instructions does "AND" fall?

   If we assume that "AND" is referring to the logical AND operation, it can be classified as a logical instruction. Logical instructions, such as AND, OR, NOT, and XOR, perform logical operations on their inputs. However, the new instruction "ADN" performs a combination of an arithmetic operation (addition) and a logical operation (inversion) on its inputs. This kind of instruction does not fit into any typical category of instructions and may be considered a custom or hybrid instruction specific to a particular application or processor.

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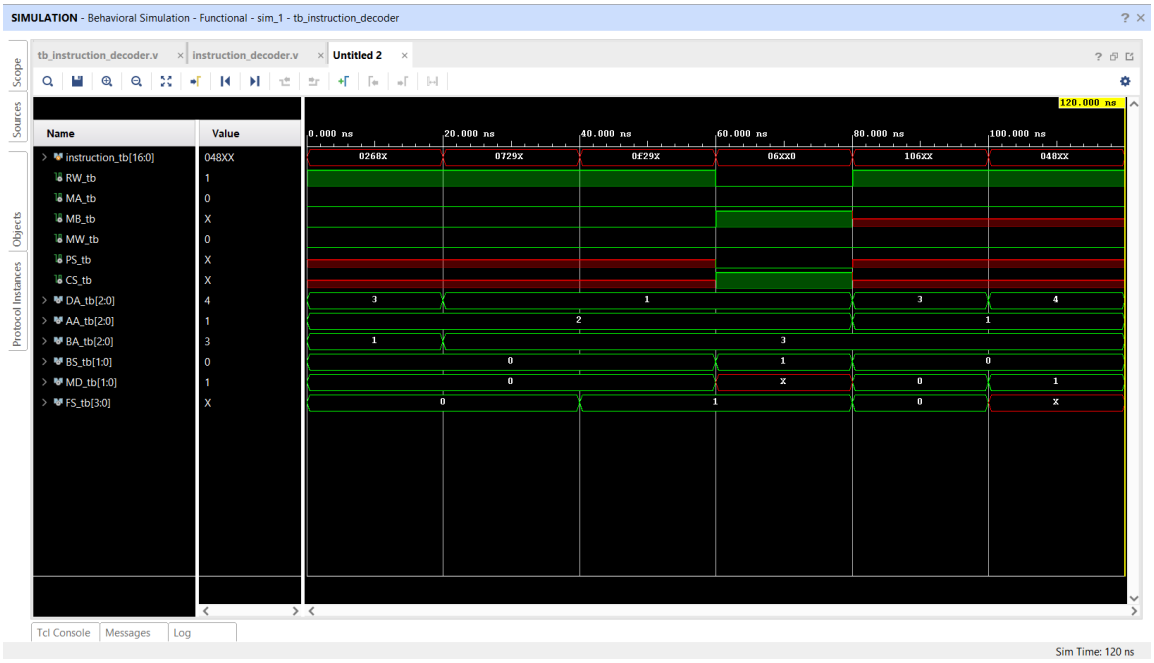
3. If we want to have this instruction in our MCU, specify related control signals in the following table.

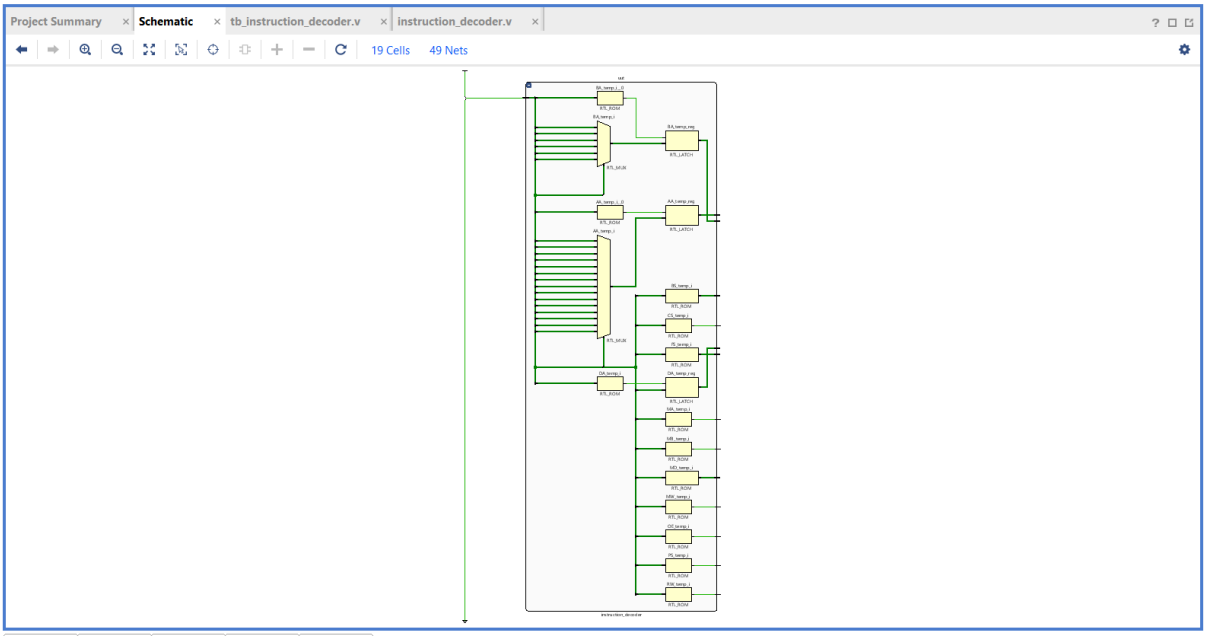
RW	MD	BS	PS	MW	FS	MB	MA	CS	OE
1	00	00	X	0	Arb.	0	0	X	0

INSTRUCTION DECODER:

Simulation:



Schematic:



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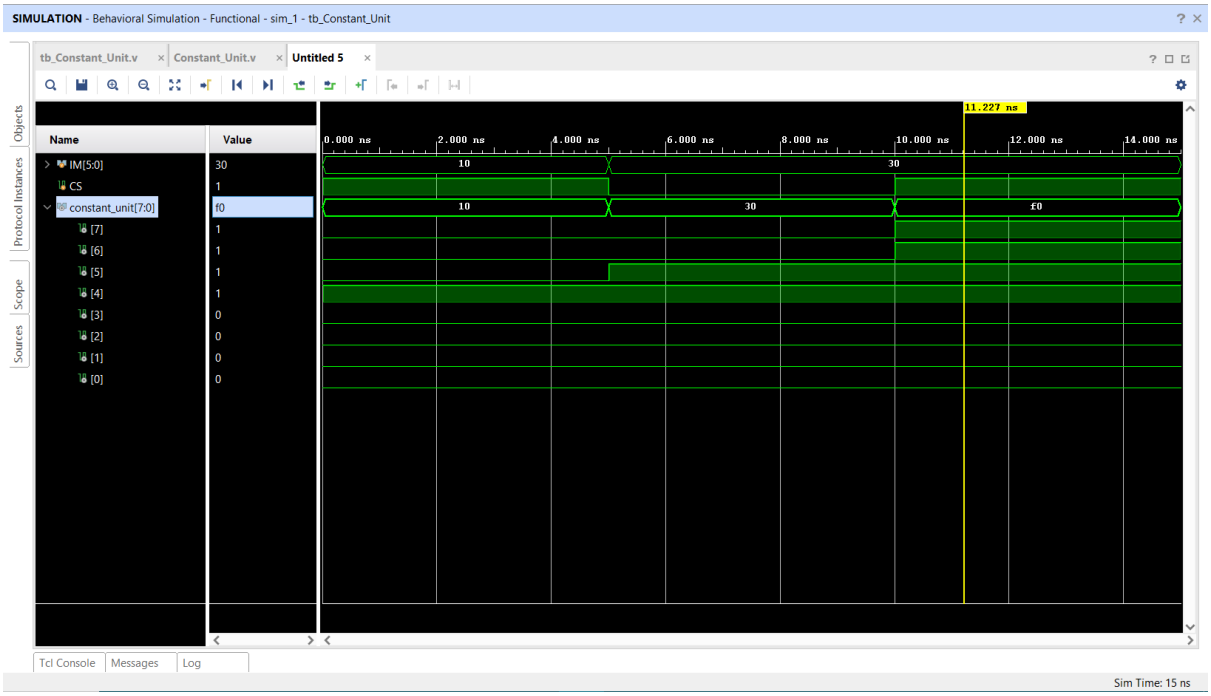
CONSTANT UNIT:

Simulation:



Schematic: