SEIA2202	DIGITAL SYSTEMS LAB	L	T	P	Credits	Total Marks
		0	0	4	2	100

COURSE OBJECTIVES

- To understand the functioning of logic gates and design of combinational circuits using logic gates.
- To understand the working of Flip flops and its applications in Shift Register and Counters.

SUGGESTED LIST OF EXPERIMENTS

1. Verification of the Basic gates.
2. Verification of Boolean function using logic gates.
3. To Construct and verify the full and half adder using logic gates.
4. To Verify 2x4 Decoder and 4x2 Encoder functionally.
5. Code Converter.
   (a.) BCD to GRAY
   (b.) GRAY to BINARY
6. Comparator.
7. Design and study of Multiplexer and Demultiplexer.
8. To construct and study the working of RS flip-flop, D flip-flop, T flip-flop, JK flip-flop.
9. To verify various shift register.
   (a) SISO
   (b) SIPO
   (c) PISO
   (d) PIPO
10. Design a counter using suitable flip-flop.
    (a) MOD Counter
    (b) Ripple Counter
    (c) Up- Down Counter

COURSE OUTCOMES

On completion of the course, student will be able to

CO1 - Understand the functioning of logic gates.
CO2 - Understand the functioning of flip flops.
CO3 - Implement Boolean functions using logic gates.
CO4 - Analyze and design combinational circuits.
CO5 - Implement Shift Registers using flip flops.
CO6 - Design counters using flip flops.

EXP NO.1. VERIFY THE BASIC GATES / BOOLEAN FUNCTION USING LOGIC GATES

Expt. No. 1 a STUDY OF BASIC DIGITAL ICS

AIM:

To verify the truth table of basic digital ICs of AND, OR, NOT, NAND, NOR, EX-OR gates**.**

APPARATUS REQUIRED:

S.No	Name of the Apparatus	IC number	Quantity
1.	Digital IC trainer kit		1
2.	AND gate	IC 7408	1
3.	OR gate	IC 7432	1
4.	NOT gate	IC 7404	1
5.	NAND gate	IC 7400	1
6.	NOR gate	IC 7402	1
7.	EX-OR gate	IC 7486	1
8.	Connecting wires	As required	

THEORY:

a. AND gate:

An AND gate is the physical realization of logical multiplication operation. It is an electronic circuit which generates an output signal of '1' only if all the input signals are '1'.

b. OR gate:

An OR gate is the physical realization of the logical addition operation. It is an electronic circuit which generates an output signal of '1' if any of the input signal is '1'.

c. NOT gate:

A NOT gate is the physical realization of the complementation operation. It is an electronic circuit which generates an output signal which is the reverse of the input signal. A NOT gate is also known as an inverter because it inverts the input.

d. NAND gate:

A NAND gate is a complemented AND gate. The output of the NAND gate will be '0' if all the input signals are '1' and will be '1' if any one of the input signal is '0'.

e. NOR gate:

A NOR gate is a complemented OR gate. The output of the OR gate will be '1' if all the inputs are '0' and will be '0' if any one of the input signal is '1'.

f. EX-OR gate:

An Ex-OR gate performs the following Boolean function,

$$A \oplus B = (A . B') + (A' . B)$$

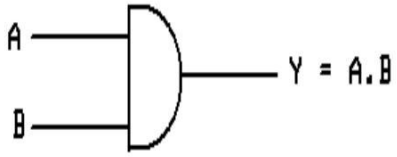
It is similar to OR gate but excludes the combination of both A and B being equal to one. The exclusive OR is a function that give an output signal '0' when the two input signals are equal either '0' or '1'.

PROCEDURE:

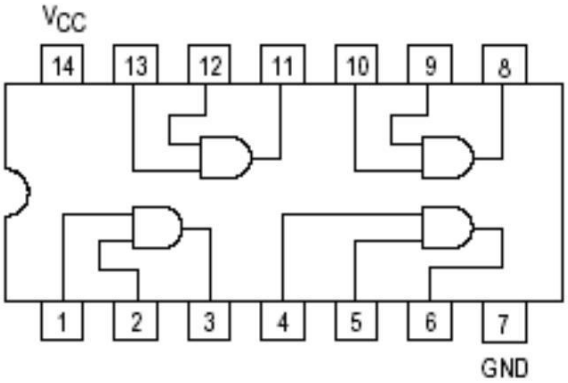
1. Connections are given as per the circuit diagram
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for all gates.

AND GATE

LOGIC DIAGRAM: `



PIN DIAGRAM OF IC 7408 :

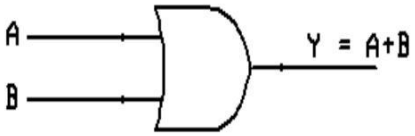


TRUTH TABLE:

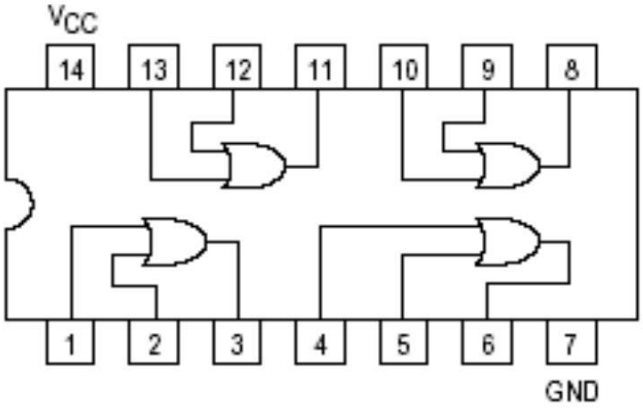
S.No	INPUT		OUTPUT
	A	B	Y = A . B
1.	0	0	0
2.	0	1	0
3.	1	0	0
4.	1	1	1

OR GATE

LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7432 :

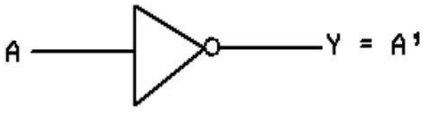


TRUTH TABLE:

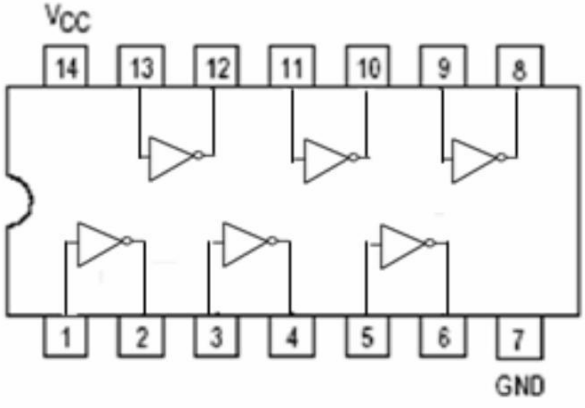
S.No	INPUT		OUTPUT
	A	B	Y = A + B
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	1

NOT GATE

LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7404 :

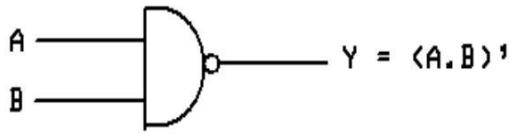


TRUTH TABLE:

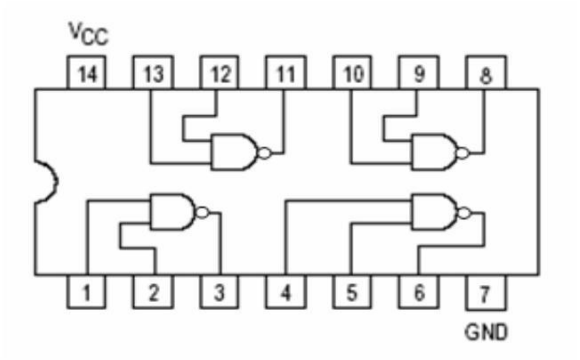
S.No	INPUT	OUTPUT
	A	Y = A’
1.	0	1
2.	1	0

NAND GATE

LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7400 :

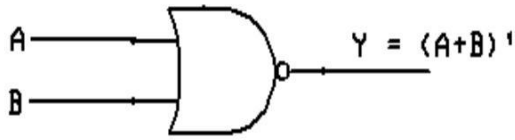


TRUTH TABLE:

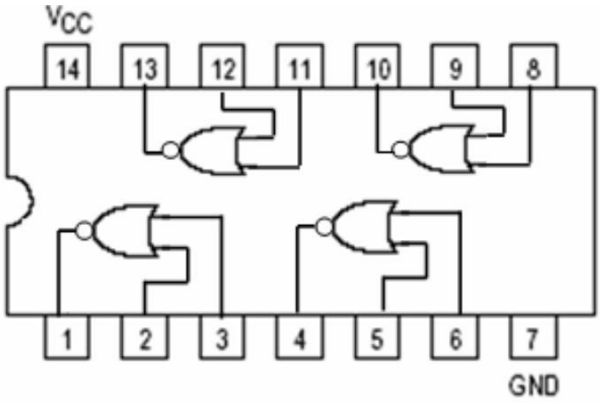
S.No	INPUT		OUTPUT
	A	B	Y = (A. B)’
1.	0	0	1
2.	0	1	1
3.	1	0	1
4.	1	1	0

NOR GATE

LOGIC DIAGRAM:



PIN DIAGRAM OF IC 7402 :

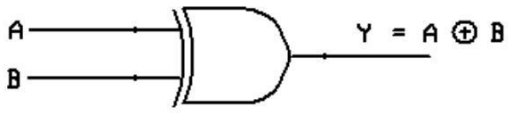


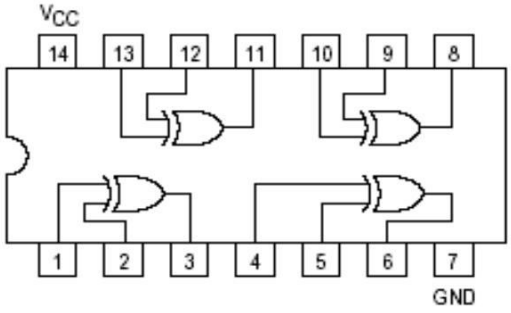
TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = (A + B)'
1.	0	0	1
2.	0	1	0
3.	1	0	0
4.	1	1	0

EX-OR GATE

LOGIC DIAGRAM **PIN DIAGRAM OF IC 7486:**





TRUTH TABLE:

S.No	INPUT		OUTPUT
	A	B	Y = A⊕B
1.	0	0	0
2.	0	1	1
3.	1	0	1
4.	1	1	0

RESULT:

The truth table of all the basic digital ICs were verified.

Expt. No.1b **IMPLEMENTATION OF BOOLEAN FUNCTIONS**

AIM:

To design the logic circuit and verify the truth table of the given Boolean expression,

F (A, B, C, D) = Σ (0, 1, 2, 5, 8, 9, 10)

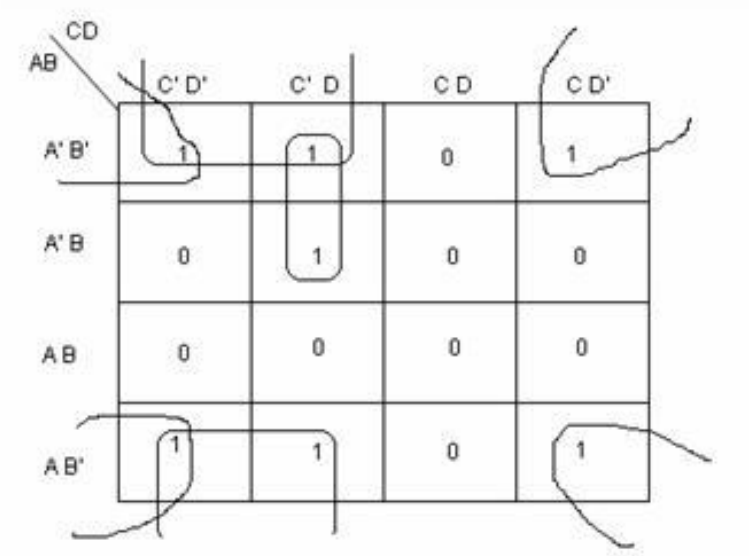
APPARATUS REQUIRED:

S.No	Name of the Apparatus	IC number	Quantity
1.	Digital IC trainer kit		1
2.	AND gate	IC 7408	
3.	OR gate	IC 7432	
4.	NOT gate	IC 7404	
5.	NAND gate	IC 7400	
6.	NOR gate	IC 7402	
7.	EX-OR gate	IC 7486	
8.	Connecting wires		As required

DESIGN:

Given , F (A,B,C,D) = Σ (0,1,2,5,8,9,10)

The output function F has four input variables hence a four variable Karnaugh Map is used to obtain a simplified expression for the output as shown,



From the K-Map,

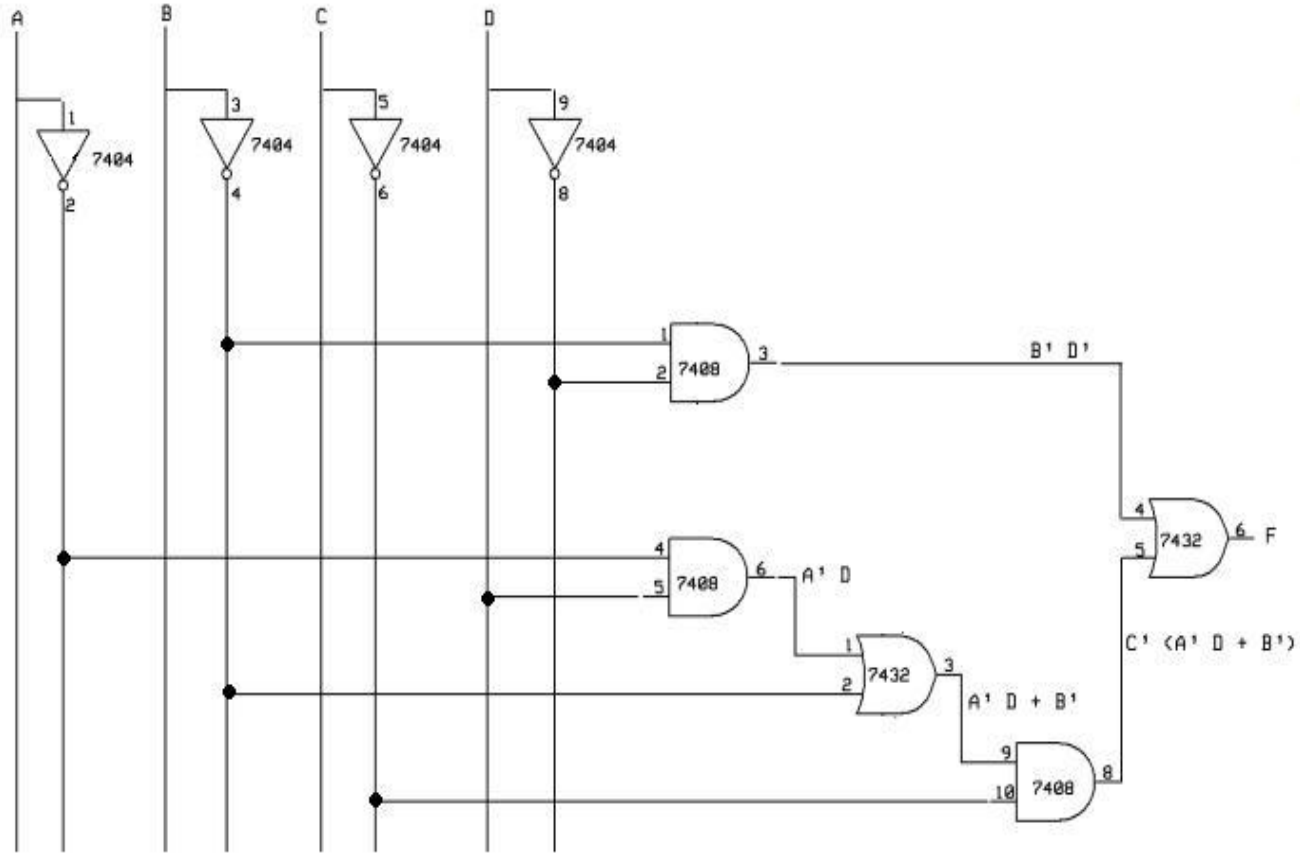
F = B’ C’ + D’ B’ + A’ C’ D

Since we are using only two input logic gates the above expression can be re-written as,

F = C’ (B’ + A’ D) + D’ B’

Now the logic circuit for the above equation can be drawn.

CIRCUIT DIAGRAM:



TRUTH TABLE:

S.No	INPUT				OUTPUT
	A	B	C	D	F=D'B'+C'(B'+A'D)
1.	0	0	0	0	1
2.	0	0	0	1	1
3.	0	0	1	0	1
4.	0	0	1	1	0
5.	0	1	0	0	0
6.	0	1	0	1	1
7.	0	1	1	0	0
8.	0	1	1	1	0
9.	1	0	0	0	1
10.	1	0	0	1	1
11.	1	0	1	0	1
12.	1	0	1	1	0
13.	1	1	0	0	0
14.	1	1	0	1	0
15.	1	1	1	0	0
16.	1	1	1	1	0

PROCEDURE:

1. Connections are given as per the circuit diagram
2. For all the ICs 7^{th} pin is grounded and 14^{th} pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the given Boolean expression.

RESULT:

The truth table of the given Boolean expression was verified.

EXPT. NO. 2 TO CONSTRUCT AND VERIFY THE FULL AND HALF ADDER USING LOGIC GATES.

AIM:

To design and verify the truth table of the Half Adder & Full Adder circuits.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	IC number	Quantity
1.	Digital IC trainer kit		1
2.	AND gate	IC 7408	
3.	OR gate	IC 7432	
4.	NOT gate	IC 7404	
5.	EX-OR gate	IC 7486	
6.	Connecting wires	As required	

THEORY:

The most basic arithmetic operation is the addition of two binary digits. There are four possible elementary operations, namely,

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10_2$$

The first three operations produce a sum of whose length is one digit, but when the last operation is performed the sum is two digits. The higher significant bit of this result is called a carry and lower significant bit is called the sum.

HALF ADDER:

A combinational circuit which performs the addition of two bits is called half adder. The input variables designate the augend and the addend bit, whereas the output variables produce the sum and carry bits.

FULL ADDER:

A combinational circuit which performs the arithmetic sum of three input bits is called full adder. The three input bits include two significant bits and a previous carry bit. A full adder circuit can be implemented with two half adders and one OR gate.

HALF ADDER

TRUTH TABLE:

S.No	INPUT		OUTPUT	
	A	B	S	C
1.	0	0	0	0
2.	0	1	1	0
3.	1	0	1	0
4.	1	1	0	1

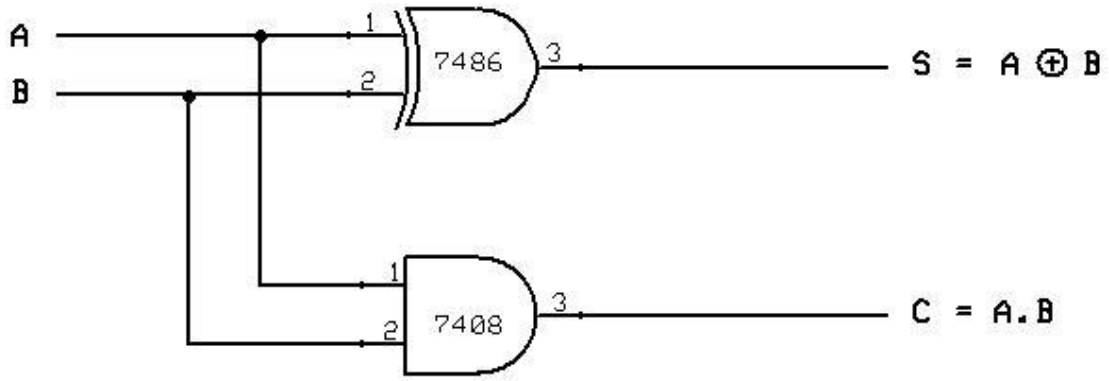
DESIGN:

From the truth table the expression for sum and carry bits of the output can be obtained as,

Sum, S = A ⊕ B

Carry, C = A . B

CIRCUIT DIAGRAM:



FULL ADDER

TRUTH TABLE:

S.No	INPUT			OUTPUT	
	A	B	C	SUM	CARRY
1.	0	0	0	0	0
2.	0	0	1	1	0
3.	0	1	0	1	0
4.	0	1	1	0	1
5.	1	0	0	1	0
6.	1	0	1	0	1
7.	1	1	0	0	1
8.	1	1	1	1	1

DESIGN:

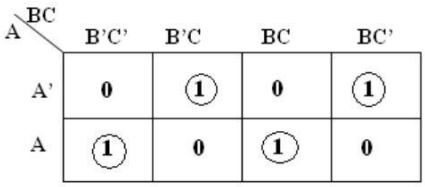
From the truth table the expression for sum and carry bits of the output can be obtained as,

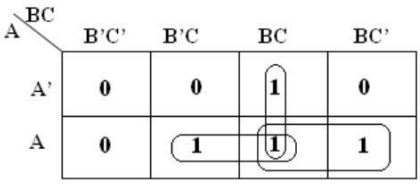
SUM = A'B'C + A'BC' + AB'C' + ABC

CARRY = A'BC + AB'C + ABC' +ABC

Using Karnaugh maps the reduced expression for the output bits can be obtained as,

SUM **CARRY**

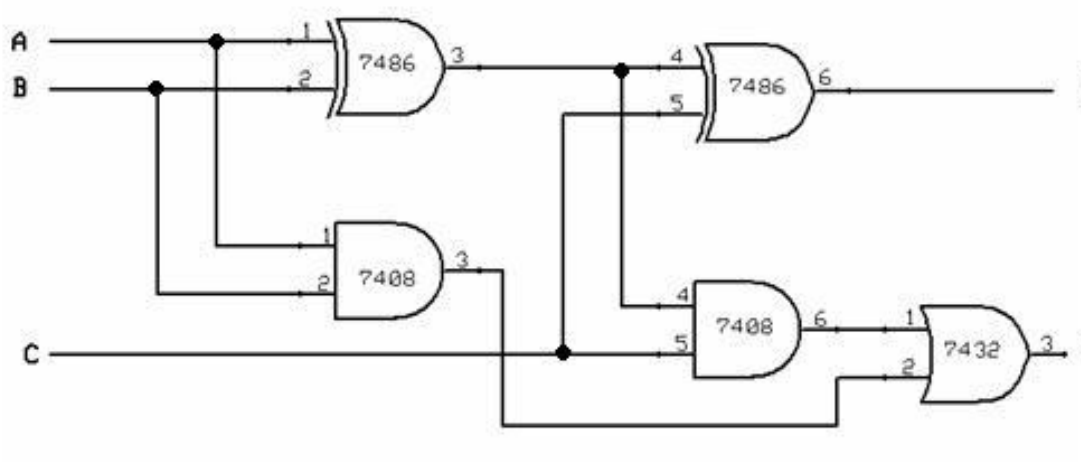




SUM = A'B'C + A'BC' + AB'C' + ABC = A $\oplus$ B $\oplus$ C

CARRY = AB + AC + BC

CIRCUIT DIAGRAM:



PROCEDURE:

1. Connections are given as per the circuit diagrams.
2. For all the ICs 7th pin is grounded and 14th pin is given +5 V supply.
3. Apply the inputs and verify the truth table for the half adder and full adder circuits.

RESULT:

The design of the half adder and full adder circuits was done and their truth tables were verified.

Expt No 3 To Verify 2x4 Decoder and 4x2 Encoder functionally.

Aim:

To design and implement encoder and decoder using logic gates.

Apparatus Required:

SI. No.	COMPONENT	SPECIFICATION	QTY
1.	NOT GATE	IC 7404	1
2.	OR GATE	IC 7432	1
3.	AND Gate	IC 7408	1
4.	DIGITAL IC TRAINER KIT	-	1
5.	PATCH CORD	-	-

Theory:

Encoder:

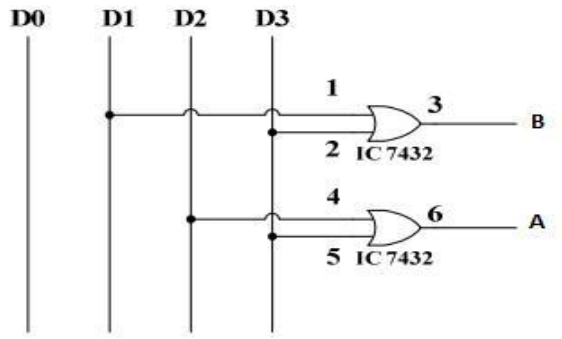
An encoder is a combinational logic circuit that has 2^n input lines and n output lines. As an example consider an four input and two output encoder. It is assumed that only one input has '1' at any given time. From truth table, it is obvious that the output is '1' for A when the input is 2 and 3; B is '1' when the input is 1 and 2.

De-Coder:

A decoder is a combinational circuit that converts n-bit binary input lines into 2^n output lines such that output line will be activated for only one of possible combination of inputs. The outputs are selected based on two select inputs. The inputs AB are decoded into four digits output each representing one of minterms of two input variables.

4 X 2 Encoder

Logic Diagram:



Truth Table:

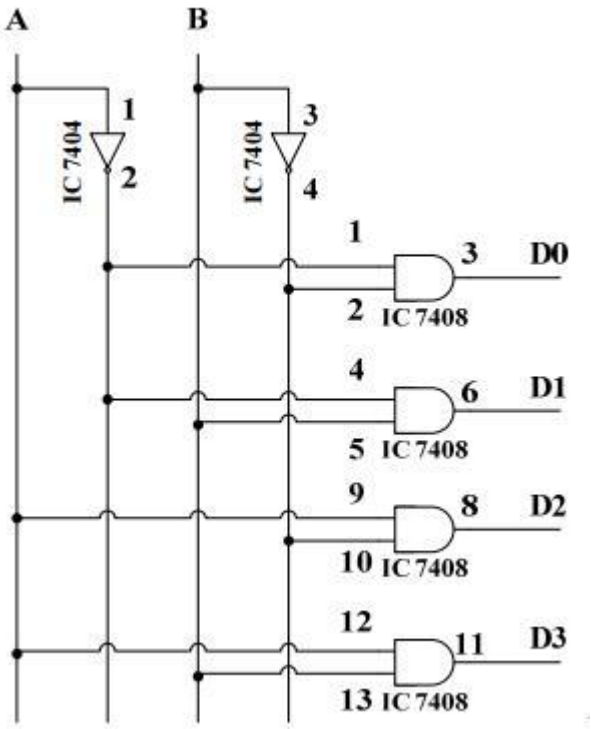
Input				Output	
D0	**D1**	**D2**	**D3**	**A**	**B**
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

A = D2 + D3

B = D1 + D3

Logic Diagram:

2x4 De-Coder:



Truth Table:

Input		Output			
A	**B**	**D0**	**D1**	**D2**	**D3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

D0 =

A’B’ D1

= A’B

D2 =

AB’ D3

= AB

Procedure:

1. Make the connections as per the circuit diagram.
2. Switch on VCC and apply various combinations of input according to truth table.
3. For all input combinations verify the outputs with the truth table.

Result:

Thus the Encoder and De-Coder were designed and implemented using logic gates with their truth table verified.

Expt. No. 4

To construct and study the working of RS flip-flop, D flip-flop, T flip-flop, JK flip-flop

AIM:

To verify the characteristic table of RS, D, JK, and T Flip flops.

APPARATUS REQUIRED:

S.No	Name of the Apparatus	Range	Quantity
1.	Digital IC trainer kit		1
2.	NOR gate	IC 7402	
3.	NOT gate	IC 7404	
4.	AND gate (three input)	IC 7410	
5.	NAND gate	IC 7400	
6.	Connecting wires		As required

THEORY:

A Flip Flop is a sequential device that samples its input signals and changes its output states only at times determined by clocking signal. Flip Flops may vary in the number of inputs they possess and the manner in which the inputs affect the binary states.

RS FLIP FLOP:

The clocked RS flip flop consists of NAND gates and the output changes its state with respect to the input on application of clock pulse. When the clock pulse is high the S and R inputs reach the second level NAND gates in their complementary form. The Flip Flop is reset when the R input high and S input is low. The Flip Flop is set when the S input is high and R input is low. When both the inputs are high the output is in an indeterminate state.

D FLIP FLOP:

To eliminate the undesirable condition of indeterminate state in the SR Flip Flop when both inputs are high at the same time, in the D Flip Flop the inputs are never made equal at the same time. This is obtained by making the two inputs complement of each other.

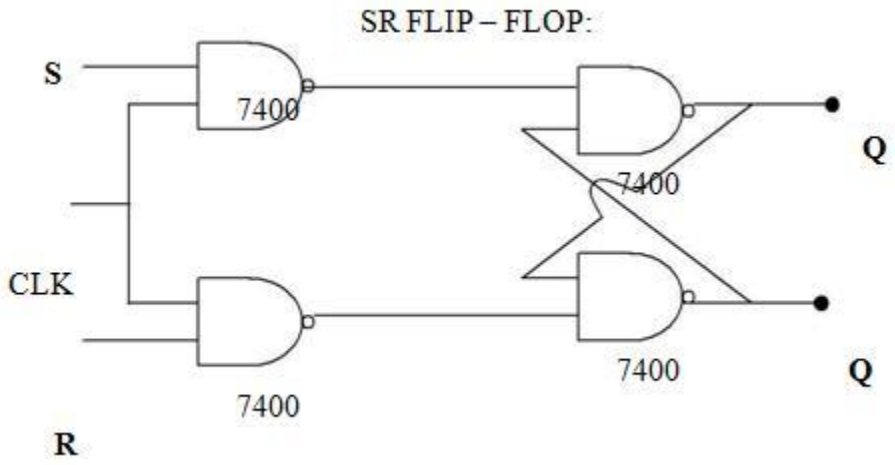
JK FLIP FLOP:

The indeterminate state in the SR Flip-Flop is defined in the JK Flip Flop. JK inputs behave like S and R inputs to set and reset the Flip Flop. The output Q is NAND with K input and the clock pulse, similarly the output Q' is NAND with J input and the Clock pulse. When the clock pulse is zero both the AND gates are disabled and the Q and Q' output retain their previous values. When the clock pulse is high, the J and K inputs reach the NOR gates. When both the inputs are high the output toggles continuously. This is called Race around condition and this must be avoided.

T FLIP FLOP:

This is a modification of JK Flip Flop, obtained by connecting both inputs J and K inputs together. T Flip Flop is also called Toggle Flip Flop.

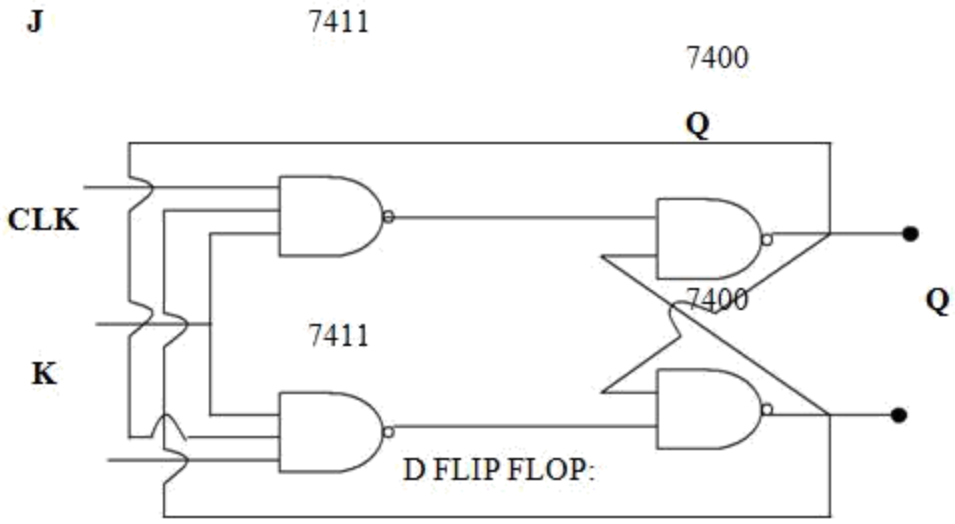
Circuit Diagram:



Truth Table RS Flip -Flop

Clock Pulse	Input		Present State (Q)	Next State(Q+1)
	S	R		
1	0	0	0	0
2	0	0	1	1
3	0	1	0	0
4	0	1	1	0
5	1	0	0	1
6	1	0	1	1
7	1	1	0	X
8	1	1	1	X

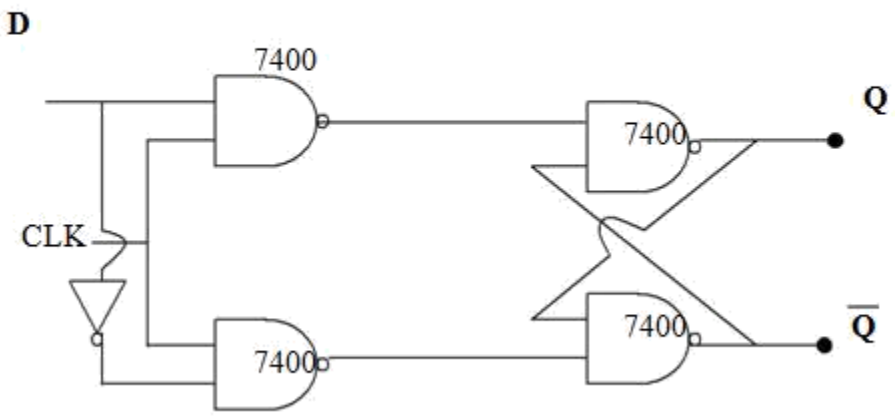
JK FLIP – FLOP:



JK Flip -Flop

Clock Pulse	Input		Present State (Q)	Next State(Q+1)
	J	K		
1	0	0	0	0
2	0	0	1	1
3	0	1	0	0
4	0	1	1	0
5	1	0	0	1
6	1	0	1	1
7	1	1	0	1
8	1	1	1	0

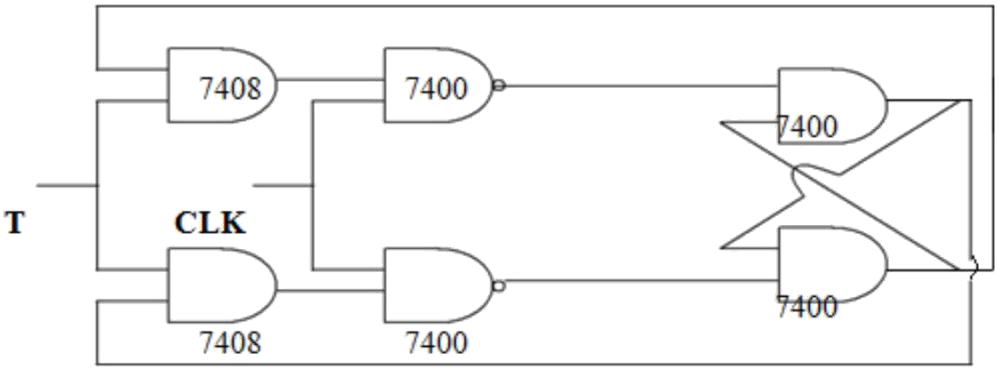
D FLIP FLOP:



D Flip -Flop

Clock Pulse	Input D	Present State (Q)	Next State(Q+1)
1	0	0	0
2	0	1	0
3	1	0	1
4	1	1	1

T FLIP FLOP:



T Flip -Flop

Clock Pulse	Input T	Present State (Q)	Next State(Q+1)
1	0	0	0
2	0	1	1
3	1	0	1
4	1	1	0

Result: Thus the characteristic table of RS, D, JK, and T Flip flops are verified.