Design and perform Analysis of Full Adder Using FinFET Technique

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Abstract :

In recent years, modern VLSI area-efficient devices are most used due to most of the devices becoming portable. The FinFET technique is often employed in designing low-power, area-efficient, and high-speed devices. The one-bit full adder circuit using CMOS-based logic and domino-based logic on Cadence Virtuoso 6. 1. 7 has been designed based on 180nm technology with the supply voltage of 3V. This work evaluates the performance of CMOS and Domino logic based on the full adder circuit in terms of delay and power consumption. It was found that Domino logic-based one-bit full adder circuit occupied lesser area and delay as a comparison to one-bit full adder circuit based on CMOS logic. The FinFET technology is a present trend in the low power circuits designing as it comprises less delay and power consumption than CMOS or domino-based logic and has been designed based on 18nm Finfet technology. The output response was verified by comparing the obtained waveform along with its truth table. Cadence output simulation matches will the Full Adder with theoretical expectations.

Keywords :

CMOS, Domino, FinFET, Full adder, Cadence Virtuoso, Performance Parameters.

Introduction :

In the rapidly expanding VLSI industry, transistor density is increasing at an alarming rate. According to Moore's law, transistor density will double every eighteen months. The device's area, delay, and power consumption will all grow as the number of transistors increases. As a result, a solution is necessary to lower the space while increasing the device's performance. For the past few decades, CMOS technology has been utilised to develop chips in the semiconductor industry, but as the number of transistors increases, so does the area of the device and the delay. As a result, it is necessary to convert to a technology that utilises less area and has a shorter delay. As a result, the Domino logic is utilised to create the one-bit full adder, and the various performance parameters such as area, delay, and power consumption in both technologies are compared.

A.CMOS Logic- CMOS stands for "Complement Metal Oxide Semiconductor." As seen in Fig.1, CMOS logic employs pMOS and nMOS transistors, which function as pull-up and pull-down transistors, respectively. When the input is low, the P-MOS turns on and charges the output node to Vdd; when the input is high, the n-MOS turns on and the charge stored at the output node forms a conducting channel between the output node and ground. When compared to previous logic designs, CMOS logic design has several advantages. In this case, both transistors are connected in a complementary manner, which means that if one transistor is turned on, the other is turned off, and vice versa. The key advantages of CMOS logic are its large noise margin, low power dissipation, and rail-to-rail output. There are some drawbacks to CMOS logic, such as the need for a large area and the slow speed of operation. As a result, for a circuit with a large number of transistors, the area required is very large, and the speed of operation becomes slow. That's why there is a need to move on to another technology that requires a smaller number of transistors and provides a high speed of operation.

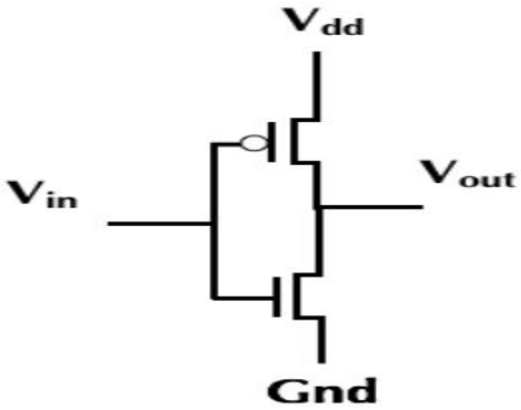

Fig. 1. CMOS logic inverter.

B. Domino logic- The Domino logic family is used in a wide range of applications that need a low transistor count and fast speed of operation, such as microprocessors, dynamic memory, digital signal processors, and so on. Domino logic is an advancement in CMOS-based dynamic logic approaches that employ either p-MOS or n-MOS for the pull-down or pull up the network. The Domino logic methodology for constructing complete adders uses less transistors than typical CMOS logic and produces a high-performance device.

The Domino logic is an improvement over dynamic logic, however, it has a disadvantage when one gate is cascaded to the next. In the domino effect. To overcome the disadvantage of dynamic logic, a static inverter is utilised between the two stages. Domino logic has several advantages, including a smaller size than traditional CMOS logic, lower parasitic capacitance, which allows for faster operation and eliminates glitches because each gate makes just one transition.

Domino logic has two stages of action, the first of which is pre-charging and the second of which is evaluation. As illustrated in Fig. 2, when the clock 'CLK' is equal to zero or low, the pMOS turns on and charges the output node to Vdd. When the clock reaches high, the p-MOS is turned off, and the evaluation phase begins. In this phase, the output is determined by the configuration of the input. If the inputs have a direct conducting link to the ground, the output node may discharge; otherwise, it will remain high. As a result, the output of the circuit is obtained, which was only supposed to be designed during the assessment step. Because we employed an inverter in this logic style for cascading the following stage, it will offer minimal output during the pre-charge phase.

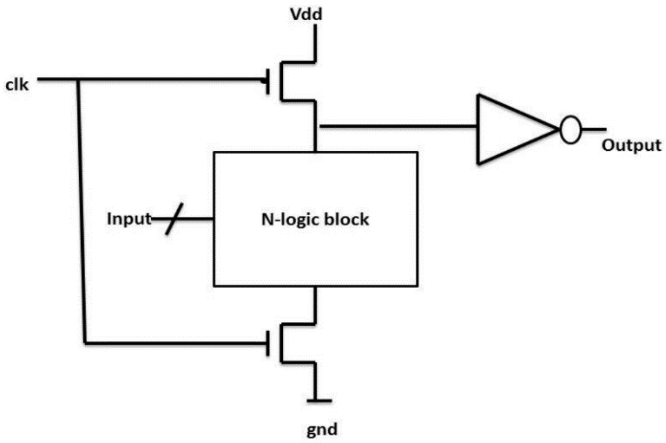

Fig. 2. Domino logic.

C. FinFET Technique- A fin field-effect transistor (FinFET) is a multigate device, a MOSFET (metal-oxide-semiconductor field-effect transistor) built on a substrate with the gate put on two, three, or four sides of the

channel or wrapped around the channel, forming a double or even multi-gate structure. Because the source/drain area generates fins on the silicon surface, these devices have been given the generic moniker "FinFETs." FinFET devices feature far faster switching times and higher current density than planar CMOS devices. FinFETs are a form of the non-planar transistor, also known as "3D" transistors. It serves the development of modern nano-electronic semiconductor devices. To maximise drive strength and performance, it is typical for a single FinFET transistor to comprise numerous fins positioned side by side and all covered by the same gate.

The advantages of FinFET is the Better control over the channel, Suppressed short-channel effects, Lower static leakage current Faster switching speed Higher drain current, Lower switching voltage, Low power consumption and where the disadvantages are for building the FinFET it involves many additional steps, so the fabrication cost is high and controlling the Fin depth is difficult.

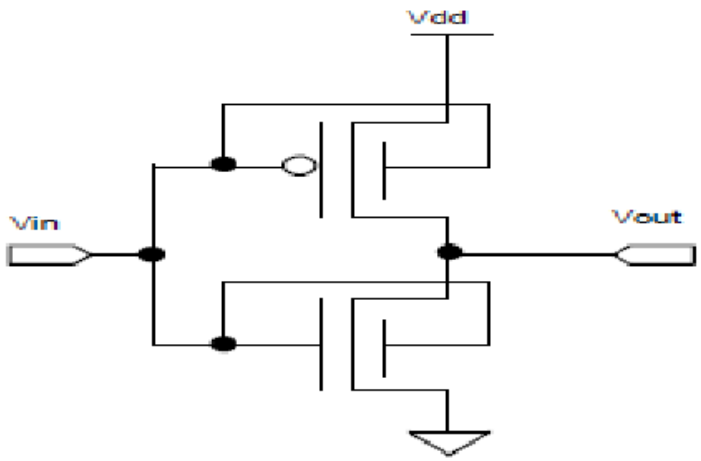

Fig.3. FinFET Inverter

Literature Survey :

Power consumption may be a major constraint in a variety of electronic systems, ranging from mobile telecommunications to portable and desktop computing systems. Power is also a deal-breaker for several emerging applications such as near intelligence and detector networks. As a result, new design processes and techniques for regulating and controlling power dissipation are required. A combinational circuit is made up of logic gates whose outputs are decided only by the current combination of inputs, with no respect for previous inputs. The logic gates accept input signals and generate output signals. This method converts binary data from the given input data to the desired output data. As a result, binary signals are used to represent both input and output data, i.e., they have two possible values, one indicating logic-0 and the other logic-1 [1].

Leakage loss is a key challenge in nanoscale CMOS technology. The problem of growing leakage in the current VLSI design is the topic of this dissertation. We investigated numerous domino strategies for low power VLSI design in this dissertation. This raised threshold voltage, on the other hand, enhances noise immunity. The entire simulation and comparison are based on HSPICE and 65nm CMOS technology. Furthermore, the proposed domino circuit techniques can be employed in carbon nanotube technology to improve performance in real-world systems [2]. Domino logic is widely employed because it has a smaller delay at the expense of reduced noise immunity when compared to static CMOS logic. Domino logic has a speed advantage because of its more compact circuit layout (the pull-up network is substantially simpler than in CMOS logic). When considering wide fan-in gates, the speed advantage becomes even more evident [3].

For enhanced power savings and dependable operation in an increasingly noisy on-chip environment, low swing domino logic circuits with weakly driven keepers and completely driven keepers have been proposed. The suggested low swing domino logic circuits have the potential to drastically reduce active power usage while maintaining noise immunity. When compared to SDK (standard domino logic circuit with a keeper), LSDFDK (Low

Swing Domino Logic Circuit with Fully Driven Keepers) consumes up to 9.4 percent less active power and tolerates up to 2.6 percent more noise. The active power is reduced further by weakening the keeper, which also reduces the evaluation latency due to lower contention current. LSDWDK (Low Swing Domino Logic Circuit with Weakly Driven Keeper) has been proven to lower active power consumption by up to 12.4% when compared to SDK while decreasing evaluation delay by up to 8.6% when compared to LSDFDK [4].

Programmable Logic Controller (PLC) based process control automation projects are multiphase tasks requiring months of planning, specification documentation, design, implementation, debugging, and final commissioning. Debugging real-time process control implementation is a three-phase process; logic simulation debugging, field static checkout, and in-plant final testing and tuning. This paper briefly discusses the fundamental techniques used in the first two stages of implemented ladder logic debugging [5]. The basic operations of communication are multiplication and division. The multiplier typically uses a larger area and ower, as well as having very high latency. All of the above-mentioned multiplier properties are dependent on the methodologies used for multiplication. It is vital to implement an appropriate multiplier that decreases both latency and power usage. So the performance of the various multipliers and scopes was analysed to build a low-power high-speed multiplier based on the Baugh Wooley algorithm [6].

Existing Method :

Two design techniques, CMOS-based logic style, and domino-based logic will be employed for the analysis of a full-adder circuit and their comparison results will be reported. An adder is a digital circuit that is used to conduct numerical addition. Adders are used in arithmetic and logic units in calculators and computers. This combinational circuit accepts three one-bit inputs labeled A, B, and C. It has two outputs, the sum, and the carry, as illustrated in Fig. 4.

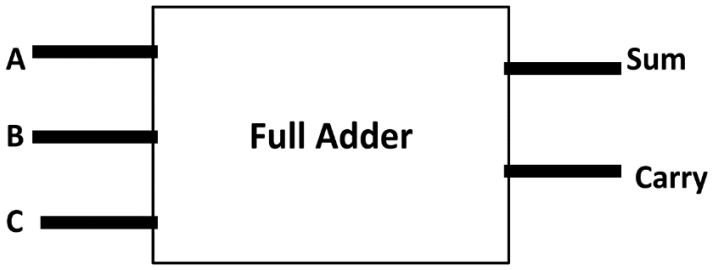

Fig. 4. Block diagram of one-bit full adder.

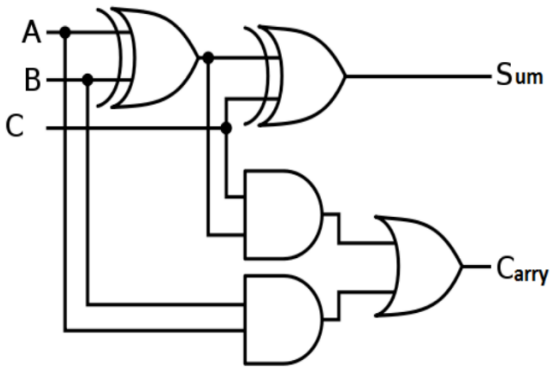

Fig.5. Logic diagram of one-bit full adder.

The gate-level logical diagram of a one-bit full adder has been shown in Fig.5 which uses the two X-OR gates for the sum, two AND gates, and one OR gate for carry. The output of the two AND gates is used as an input of the

OR gate and the output of the OR gate is providing the carry of a one-bit full adder. Table I shows the truth table for the full adder designed using CMOS-based logic.

TABLE I. FULL ADDER TRUTH TABLE

Inputs			Outputs	
A	**B**	**C**	**Sum**	**Carry**
Low	*Low*	*Low*	*Low*	*Low*
Low	*Low*	*High*	*High*	*Low*
Low	*High*	*Low*	*High*	*Low*
Low	*High*	*High*	*Low*	*High*
High	*Low*	*Low*	*High*	*Low*
High	*Low*	*High*	*Low*	*High*
High	*High*	*Low*	*Low*	*High*
High	*High*	*High*	*High*	*High*

A. Designing of one-bit full adder based on CMOS logic- The one-bit full adder schematic using CMOS logic is shown in Fig. 6. This circuit uses the 14 p-MOS transistors which are used for charging the output capacitance and 14 n-MOS transistors for discharging the output node according to the value of inputs. As a result, a total of 28 transistors are employed in the construction of a one-bit complete adder that employs CMOS logic. The design of a one-bit full adder is extremely challenging and sophisticated due to the enormous number of transistors involved. As seen in Fig.6., a high number of wires are utilised to link the transistors, introducing a large delay into the circuit.

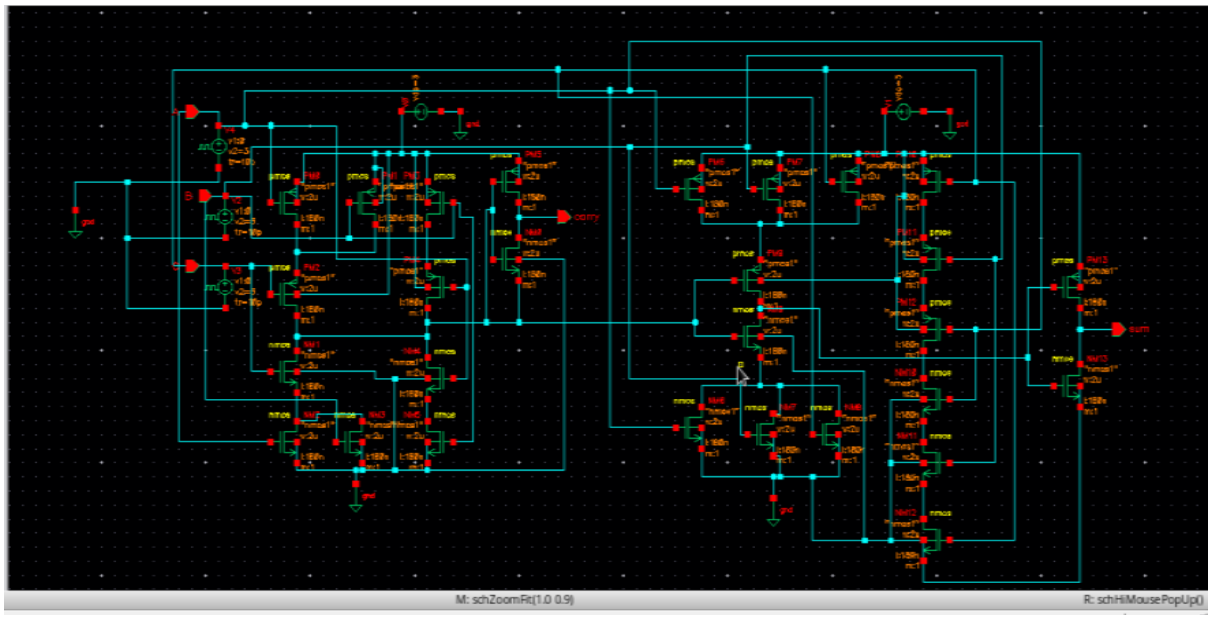

Fig. 6. Schematic structure of one-bit full adder which uses the CMOS logic.

B. Design of one-bit full adder using Domino logic- The one-bit full adder schematic using Domino logic is shown in Fig. 7. For designing the one-bit full adder by using domino logic we use the p-MOS transistors for the pre-charge phase and inverter, rest we used the n-MOS transistors for the evaluation phase. In this logic style, we have

used 4 p-MOS transistors and 16 n-MOS transistors. So a total of 20 transistors are being used in designing the adder circuit by using Domino logic.

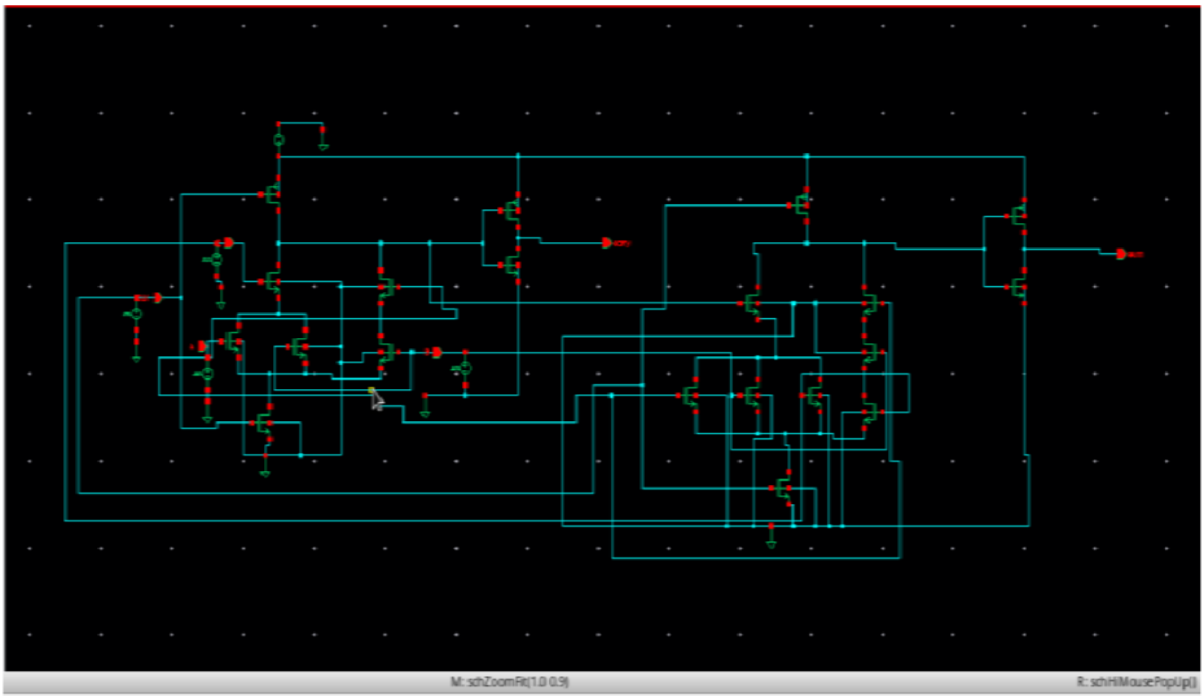

Fig. 7. Schematic design of one-bit full adder which uses the Domino logic.

Problem Identification :

Domino logic is very sensitive to noise, circuit, and layout topologies. Therefore its use introduces many design risks and increases the effort needed to verify its functionality and performance, whereas CMOS has less control over the channel, limited speed, frequency, noisy, very high power consumption at higher frequencies and CMOS is an outdated technology. The size of existing technology is 180nm as it is very large which creates a problem for decreasing the size of the electronic devices as the technology enhancement. The operational voltage is 3V which is high for designing the low power consumption to operate at low voltage.

Proposed Method :

The proposed design Technique is the FinFET Technique which is an advanced technology of CMOS logic, will be employed for the analysis of a full-adder circuit and results will be compared with the CMOS logic and Domino logic. An adder is a digital circuit that is used to conduct numerical addition. Adders are used in arithmetic and logic units in calculators and computers. This combinational circuit accepts three one-bit inputs labeled A, B, and C. It has two outputs, the sum and the carry for designing of Full Adder.
Designing of one-bit full adder based on FinFET Technique- The one-bit full adder schematic using FinFET logic is shown in Fig. 8 this circuit on Cadence Virtuoso 6. 1. 7 has been designed based on 18nm technology with the supply voltage of 1V. As the Cadence Virtuoso in-built library of p1hvt – PMOS transistor, n1hvt – NMOS transistor and their specifications are Multiplier: 1, Number of fingers :1, Fin pitch: 48nM, draw gate length:18nm. The design of a one-bit full adder is extremely challenging and sophisticated due to the enormous number of transistors involved. As seen in Fig. 9, a high number of wires are utilised to link the transistors, introducing a large delay into the circuit.

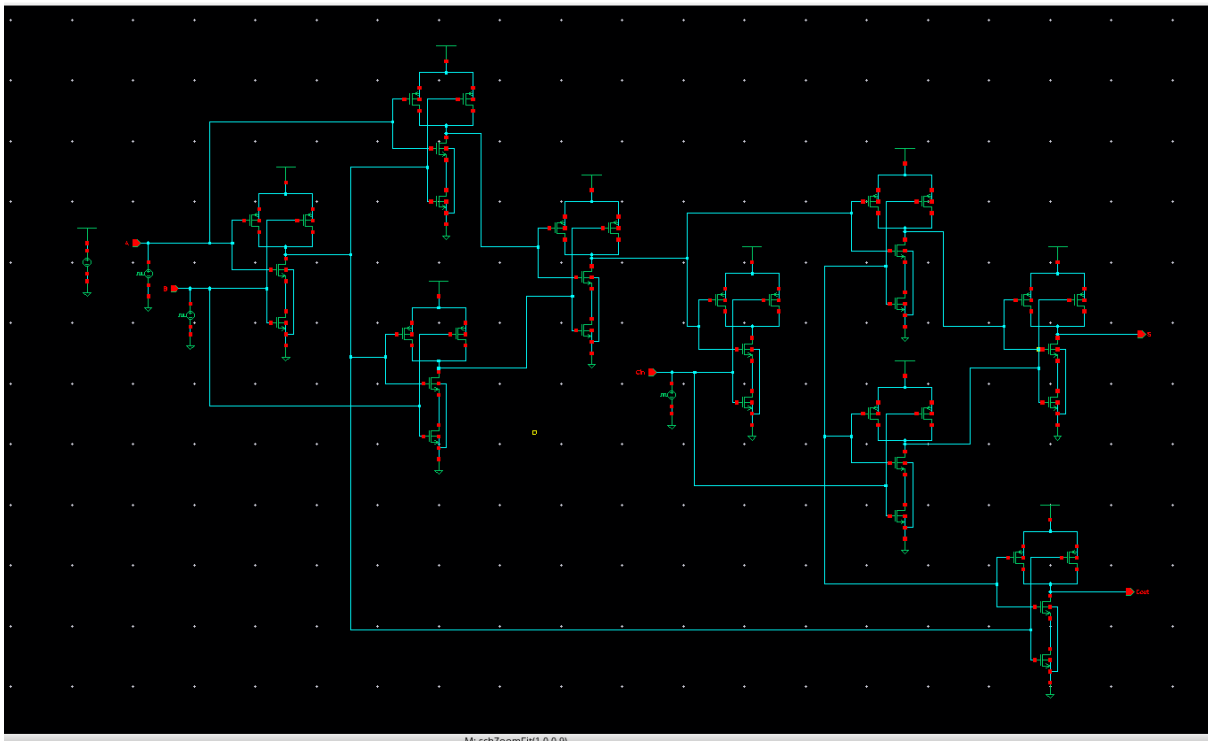

Fig.8. Schematic design of one-bit full adder which uses the FinFET Technique.

Flow chart :

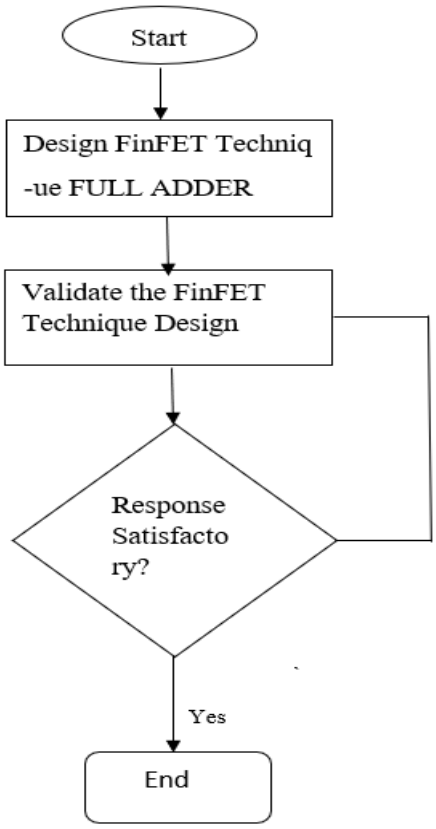

Fig.9. General Flow chart with Cadence Software

The above flow chart Fig.9. illustrate the design of the process of the system. The schematic circuit was designed in Cadence software using PMOS and NMOS available in the library. The circuit is validated using Netlist and Run available in Cadence. If the case is satisfactory output with theoretical values then saved otherwise repeated till the accurate and desired output response is obtained.

Results and Discussions :

The analysis of a one-bit full adder circuit is done using Cadence Virtuoso 6.1.7, 18nm technology. We have given the supply voltage 'VDC', 1V, and the inputs are provided by using 'pulse' with the following parameters.

TABLE II. PARAMETERS AND VALUES OF 'VPULSE'

PARAMETERS	A	B	Cin
Voltage 1 (in V)	0	0	0
Voltage 2 (in V)	1	1	1
Period (in ns)	40	20	10
Delay Time (in ps)	1	1	1
Rise Time (in ps)	1	1	1
Fall Time (in ps)	1	1	1
Pulse Width (in ns)	20	10	5

A. Analysis of one-bit full adder using CMOS logic

Full adder using CMOS logic is analysed by the schematic circuit shown in Fig. 6 and the results were verified through the truth table of the full adder. The transient analysis result of the full adder circuit that verifies the truth table is shown in Fig 10. Fig. 10 clearly shows that the truth table of the full adder circuit gate has been verified. The output 'SUM' is high when we have an odd number of high states in the input and it is low otherwise. In a similar manner output 'CARRY' is high when we have two or more input states high. After getting the accurate result we calculated the delay of the circuit.

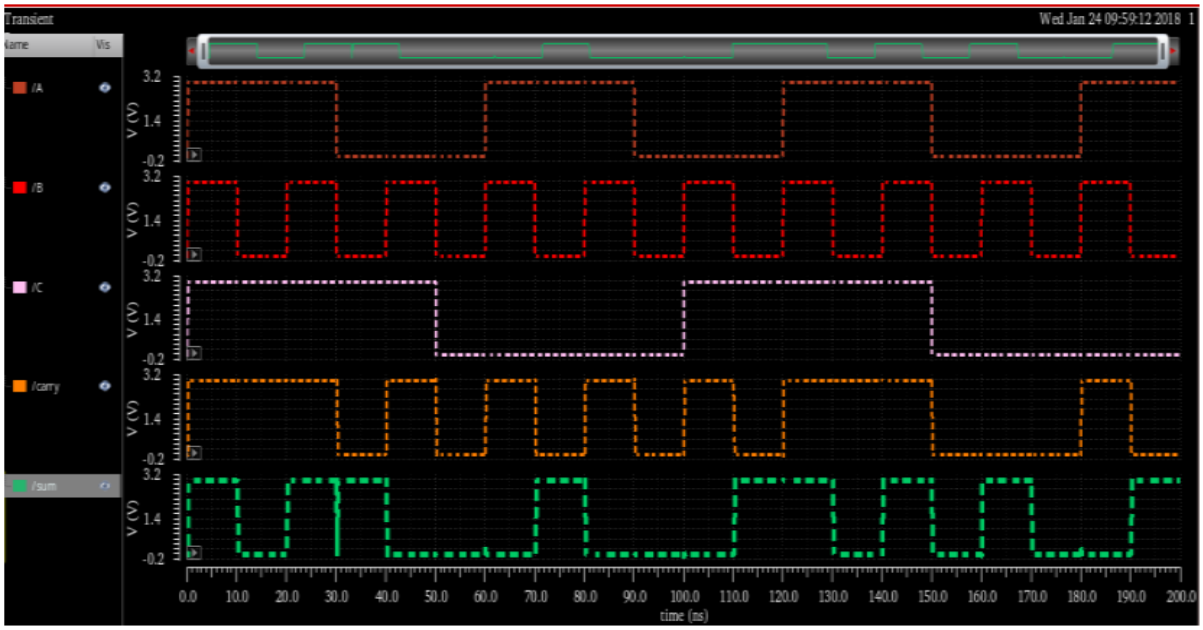

Fig. 10. Simulated result of one-bit full adder based on CMOS logic.

B. Analysis of one-bit full adder using Domino logic

We analysed the schematic of the one-bit full adder circuit Fig.7. using Domino logic. Thereafter we verified the result for this logic with the truth table of the full adder circuit as shown in Fig.11. When CLK is low p-MOS will be on and it will charge the output node to Vdd, so we get the high output in this stage but we use an inverter for getting the output of the adder so it will show both sums and carry low when the CLK signal is low. The timing of the pre-charge and evaluation phase will depend on the period of the CLK given during the simulation. Domino logic uses less number of transistors and also produces less delay as compared to the CMOS logic style.

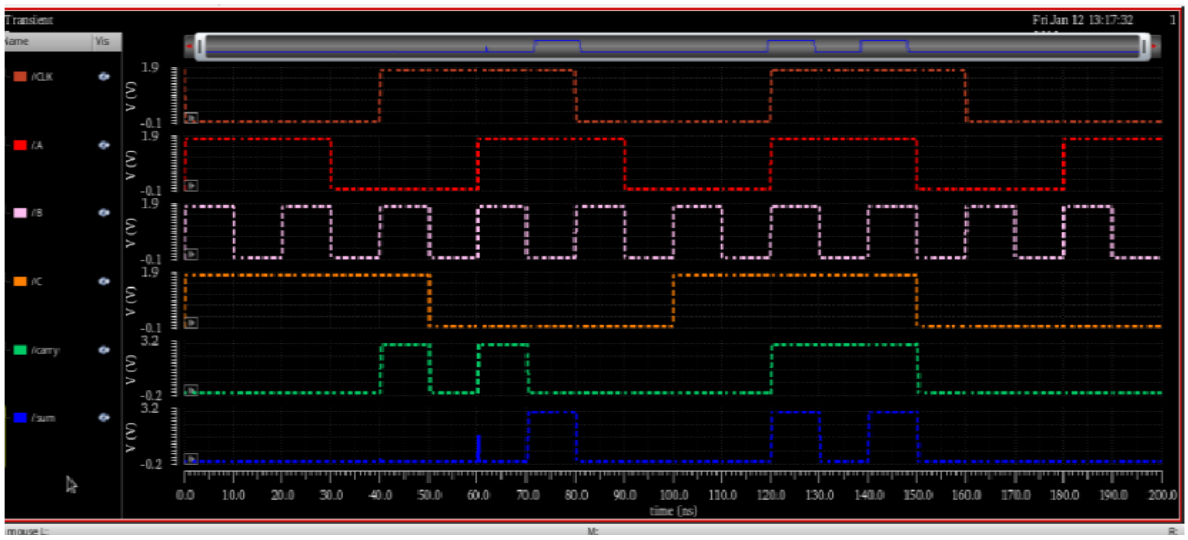

Fig. 11. Simulated result of one-bit full adder using Domino logic

C. Analysis of one-bit full adder using FINFET Logic :

Full adder using FinFET Technique is analysed by the schematic circuit shown in Fig. 8 and the results were verified through truth table of full adder. The result of the full adder circuit that verifies the truth table is shown in Fig 12. Fig. 12 clearly shows that the truth table of the full adder circuit gate has been verified. By launching Analog Design environment L Editor, choosing the AC and DC analyses we can determine the **Total Power Dissipation = 127 .077 nW.** By using Calculator in the output waveforms we calculated Average Delay Table III, by mentioning the Threshold Value - 0.5 for FinFET(0.6 – CMOS) and periodicity 1.

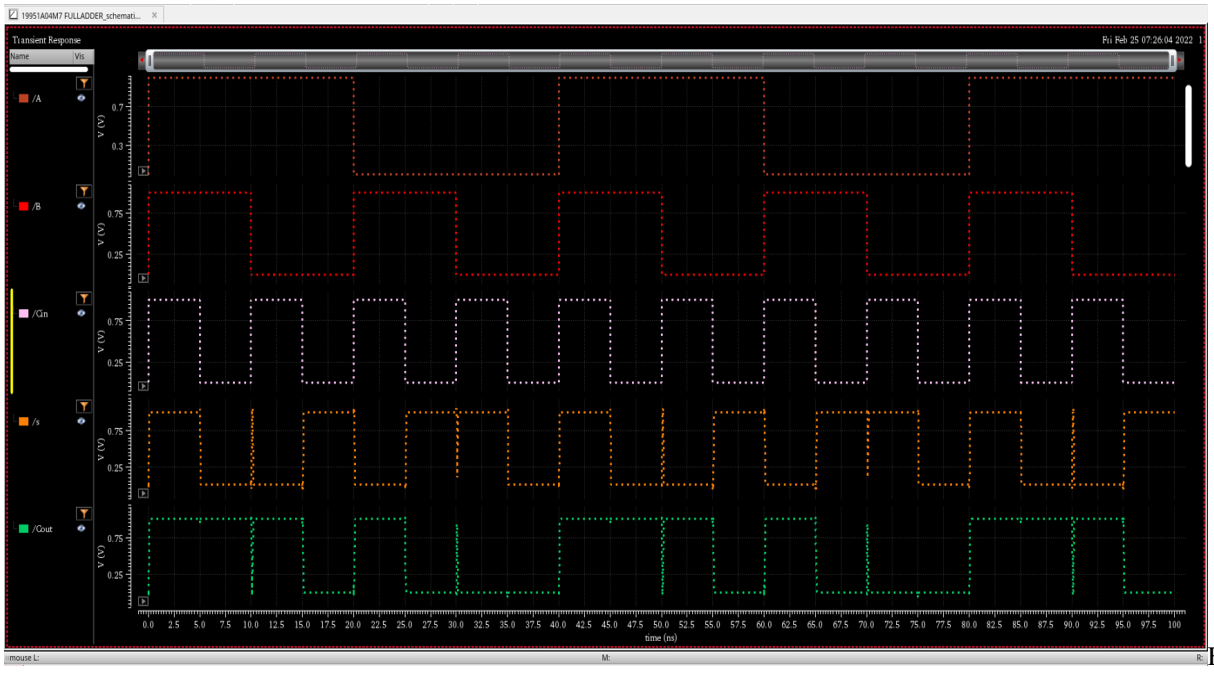

Fig. 12. Simulated result of one-bit full adder using FinFET Technique

Table III. Comparison of various performance parameters

	Existing Method		Proposed Method
Name of Parameters	CMOS Logic	DOMINO Logic	FinFET
Technology	180nm	180nm	18nm
Input Voltage	3V	3V	1V
Average Delay	19.94e-9s	10.07e-9s	36.14e-12s

Conclusion and Future Scope :

The designing of a full adder circuit using the FinFET Technique has been done. We used Cadence Virtuoso 6.1.7 software, 18nm technology for analyzing the full adder circuit, and made the comparison between the FinFET technique, CMOS logic, and Domino Logic. It was found that FinFET gives us very accurate results with minimum delay as compared to the CMOS, Domino design logic. There are almost slight glitches in the FinFET Technique analysis. By using FinFet operate at the low voltage at 1V and Total Power Dissipation is 127 .077 nW is calculated. The circuit design is Universal and may readily apply to real-world engineering applications. Future work will focus on Prototype development and applications of the present work.

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