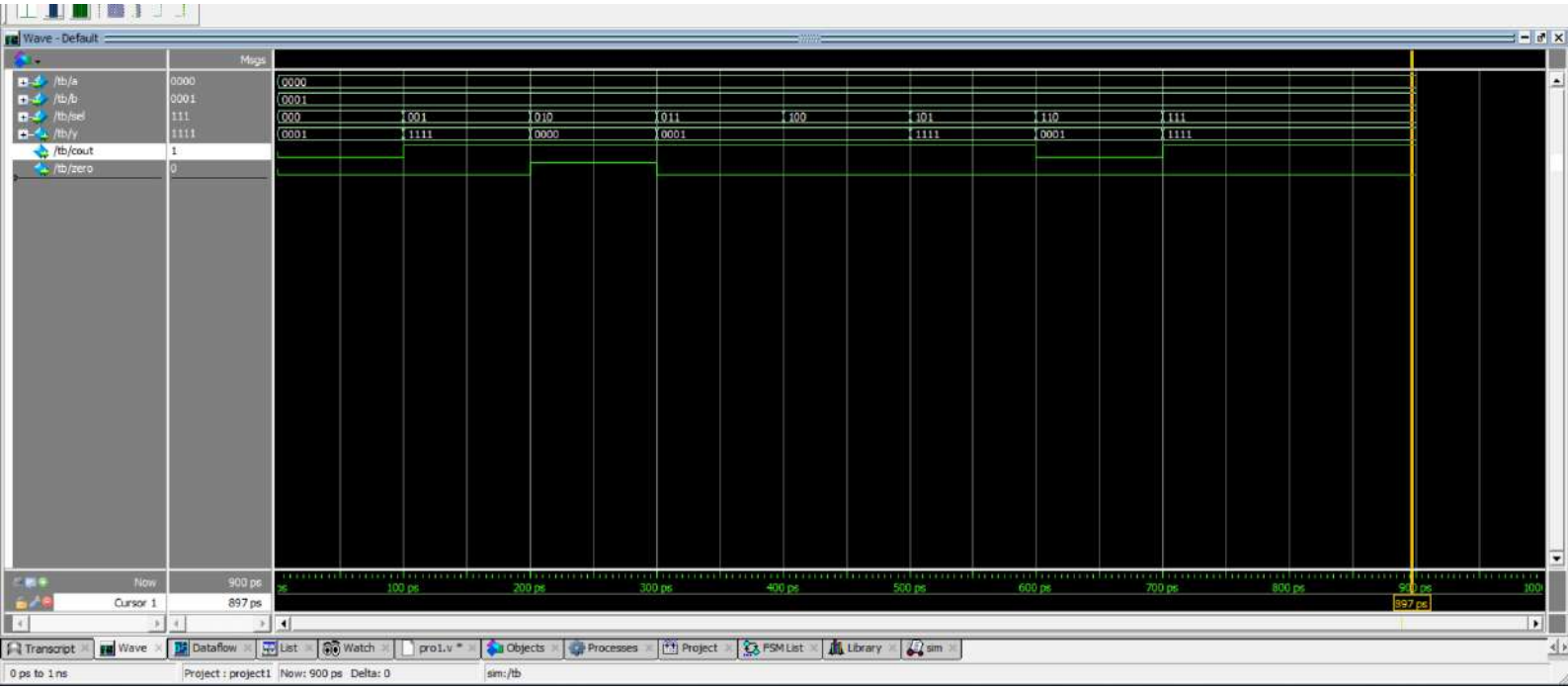
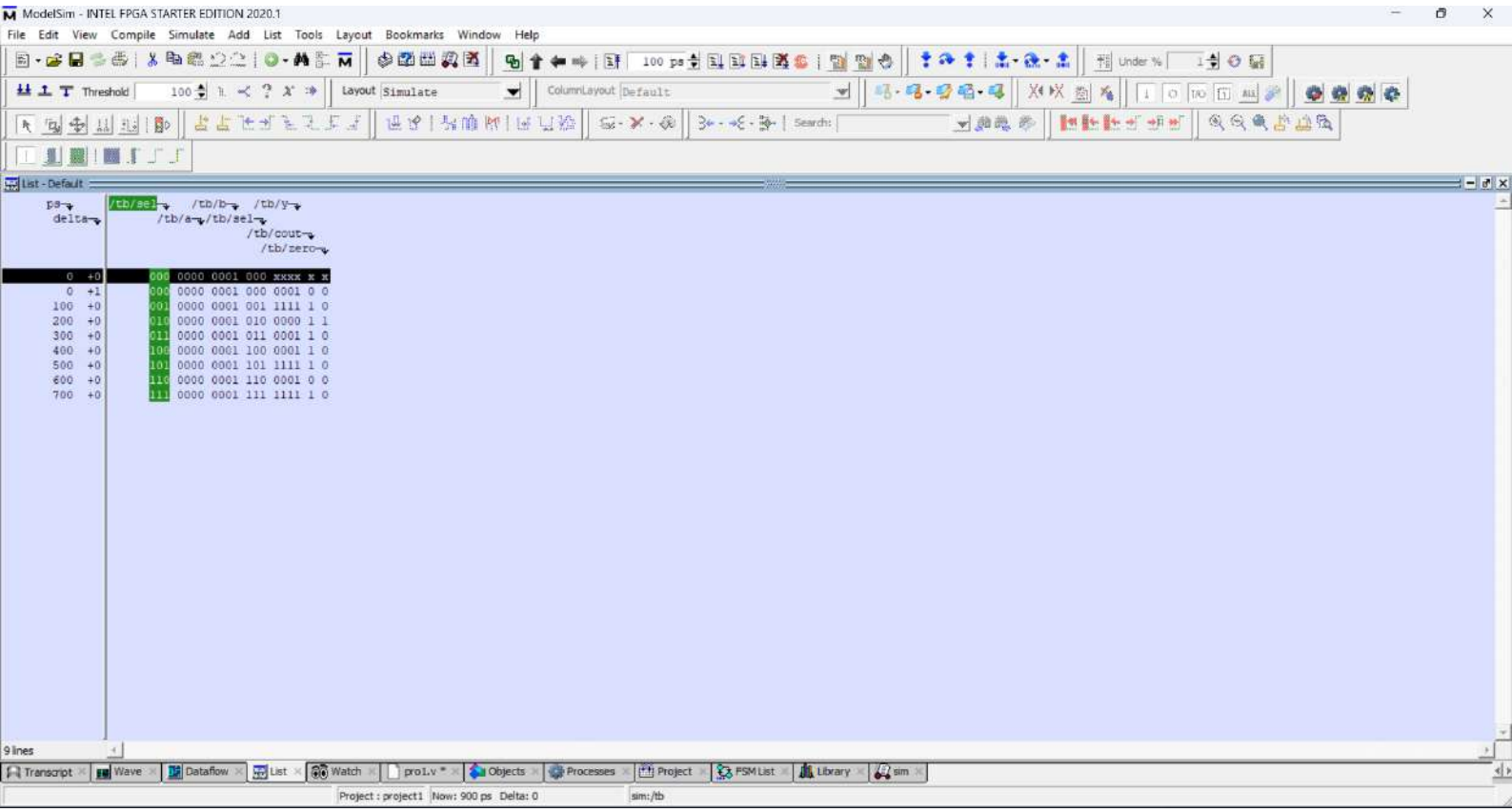
C:/intelFPGA_lite/pro1.v (/tb) - Default *

Ln#

```
1  module tb(a,b,sel,y,cout,zero);
2  input [3:0] a,b;
3  input [2:0] sel;
4  output reg [3:0] y;
5  output reg cout;
6  output reg zero;
7  always @(*)begin
8  case(sel)
9      3'b000: {cout, y} = a + b;
10     3'b001: {cout, y} = a - b;
11     3'b010: y = a & b;
12     3'b011: y = a | b;
13     3'b100: y = a ^ b;
14     3'b101: y = ~a;
15     3'b110: {cout, y} = a + 1;
16     3'b111: {cout, y} = a - 1;
17     default: y = 4'b0000;
18 endcase
19 zero = (y == 4'b0000) ? 1'b1 : 1'b0;
20 end
21 endmodule
22
```


Wave - Default
Msgs
/tb/a
/tb/b
/tb/sel
/tb/y
/tb/cout
/tb/zero
0000
0001
111
1111
1
0
000
001
010
011
100
101
110
111
0001
1111
0000
0001
1111
0001
1111
Now
900 ps
Cursor 1
897 ps
100 ps
200 ps
300 ps
400 ps
500 ps
600 ps
700 ps
800 ps
900 ps
897 ps
Transcript
Wave
Dataflow
List
Watch
pro1.v *
Objects
Processes
Project
FSM List
Library
sim
0 ps to 1 ns
Project : project1
Now: 900 ps Delta: 0
sim:/tb


ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add List Tools Layout Bookmarks Window Help
List - Default
ps
delta
/tb/sel
/tb/b
/tb/y
/tb/a
/tb/sel
/tb/cout
/tb/zero
0 +0 000 0000 0001 000 xxxx x x
0 +1 000 0000 0001 000 0001 0 0
100 +0 001 0000 0001 001 1111 1 0
200 +0 010 0000 0001 010 0000 1 1
300 +0 011 0000 0001 011 0001 1 0
400 +0 100 0000 0001 100 0001 1 0
500 +0 101 0000 0001 101 1111 1 0
600 +0 110 0000 0001 110 0001 0 0
700 +0 111 0000 0001 111 1111 1 0
9 lines
Transcript
Wave
Dataflow
List
Watch
pro1.v *
Objects
Processes
Project
FSM List
Library
sim
Project : project1
Now: 900 ps Delta: 0
sim:/tb