VISHAL SAHU

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EDUCATION

Stony Brook University(SUNY), United States **Aug 2015-Dec 2016(expected)**
Masters in Computer Science (GPA:3.67/4.0)

National Institute of Technology, Tiruchirappalli, India **Jul 2007-May 2011**
B.Tech, Electronics and Communication Engineering (GPA:8.76/10.0)

- Degree Honors: First Class with Distinction

RELEVANT COURSEWORK

Systems: Operating Systems • Analysis of Algorithms • Artificial Intelligence • Big Data systems
Architecture: Advanced Microprocessors • Computer Architecture (x86 and ARM) • Embedded systems design.

TEHCNICAL SKILLS

Languages: C/C++ (proficiency), Python, Bash, Assembly, Verilog, LaTeX
Operating System: Linux (kernel & user space programming), Windows, FreeBSD
Tools & platforms: Git, MATLAB, Virtualization(familiar), OpenNebula, OpenGL

ACADEMIC PROJECTS

Anti-malware stackable file system(amfs), Stony Brook University **Sep 2015-Nov 2015**
Guide: ***Prof. Erez Zadok***, Files Systems Lab, dept. of Computer Science

- Implemented a stackable file system that efficiently quarantines files containing malware during kernel level file operations. Developed virus pattern database and mechanism to update it with minimal overhead of re-scanning.[*webpage*]

Asynchronous utility module for Linux, Stony Brook University **Oct 2015-Dec 2015**

- Developed asynchronous job queuing mechanism based on producer- consumer design paradigm. This makes user process non-blocking. Implemented locking mechanisms to avoid races and deadlocks. [*webpage*]
- Implemented fair scheduling policy for starvation prevention and netlink socket based callback mechanism for kernel-to-user space communication.

Optimization of Speech Recognition System, NIT Trichy **May 2010-Jul 2010**

- ***Problem***: Processing delay in real time speech recognition system results in bad user experience.
- We optimized the running time of the speech-recognition system implemented in C++ using linear assembly. Linear assembly uses directives which lets assembly optimizer optimize the code by using efficient architecture specific functional units and registers.
- The optimized system was ported and tested on TMS320C6713 DSP Starter Kit. We observed an average 20% reduction in processing time without impacting the detection accuracy.

INDUSTRIAL EXPERIENCE

Samsung Research Institute, Bangalore, India **Jun 2013-Jul 2015**
Lead Engineer

- Developed scaler for Pinch-to-Zoom feature. It performs real time scaling on input pixel data using bi-cubic interpolation and guided filtering. The architecture handles streaming data using minimal amount of line buffers. **Domain**: Multimedia IP
- Implemented SPIHT compression algorithm based on bit-plane tree of wavelet coefficients. Achieved upto 30% lossless compression factor. **Domain**: Image processing.
- Optimized the run time of low power Imaging pipeline from 220ms to 90ms by utilizing multi-core processing on GPU. This is significant improvement because modern cameras suffer lag most. **Platform**: OpenGL on Qualcomm Adreno GPU.

Atmel R&D India Pvt. Ltd., Chennai, India **Jun 2011-May 2013**
Associate IC Design Engineer

- Member of architecture group defining I/O & memory map of ATTiny microcontroller. My role was to support in memory management specifically in efficient caching. I also developed interrupt handler for MaxTouch device driver. **Base operating system**: Linux.
- Designed asynchronous FIFO memory using Gray coded pointers for data synchronization.

HONORS AND AWARDS

Employee of the Month Award at Samsung India for significant contribution in Image compression algorithm development and implementation. My contributions are commercialized in Samsung Galaxy *Note4*.