Please check that this question paper contains ___9___ questions and ____2__ printed pages within first ten

MORNING

[Total No. of Questions: 09] 04 DEC 2023 [Total No. of Pages: 02]

Uni. Roll No. .....

Program: B.Tech. (Batch 2018 onward)
Semester: 3rd
Name of Subject: Digital Electronics
Subject Code: ESCS-101
Paper ID: 16012
Scientific calculator is not allowed.

Time Allowed: 03 Hours **Max. Marks: 60**

NOTE:

1) Parts A and B are compulsory
2) Part-C has Two Questions Q8 and Q9. Both are compulsory, but with internal choice
3) Any missing data may be assumed appropriately

Part – A **[Marks: 02 each]**

Q1.

a) Why do we need shift registers?

b) Identify the fastest logic family along with suitable justification.

c) Demonstrate the concept of FPGA.

d) What is Race around condition? How it can be eliminated?

e) Interpret $(4096)_{10}$ into its equivalent Gray code and Excess 3 code.

f) Evaluate (11001)2÷(101)2 using the long division method.

Part – B **[Marks: 04 each]**

Q2. Demonstrate the block diagram and working of Programmable Logic Array.

Q3. List various types of Digital to Analog converters. Explain R-2R Ladder D/A converter in detail.

Q4. Explain the functional block diagram and working of S-R Flip Flop.

Q5. Minimize the Boolean expression *(A+B) (A'+C) (B+C)* and draw the circuit diagram using NAND gates only.

Q6. Design a Johnson or Twisted Ring counter to explain its working states.

Q7. Write the expression for Boolean function F(A,B,C)= Σm(1,4,5,6,7) in a standard product of sum (POS) form.

Part – C

[Marks: 12 each]

Q8. Explain a 3-bit Binary to Gray and 3-bit Gray to binary converter along with their block diagram, truth table and circuit diagram.

OR

Solve the following using K-maps:

a) $Y = \Sigma m(3,5,6,11,12) + \Sigma d(1,7,13,15)$

b) $f(A,B,C,D) = \Sigma m(0,1,3,4,5,6,7,8,9) + \Phi(10,11,12,13,14,15)$

Q9. Implement the following function using Type 0, Type 1 and Type 2 of MUX designing. f (A,B,C,D) = Σm(0, 1, 3, 4, 6, 8, 12, 14, 15). Comment on changes occur, if would be designed using Type 3.

OR

Explain the following differences:

(a) A/D converter and D/A converter.

(b) Moore and Mealy Machines.

(c) Synchronous and Asynchronous counters.

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Please check that this question paper contains 09 questions and 02 printed pages within first ten minutes.

MORNING

[Total No. of Questions: 09]
Uni. Roll No. .....

27 FEB 2024

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Part – A

[Marks: 02 each]

Q1. (a) Solve $(614.15)_7$ into $(X)_{10}$

(b) List any two applications of multiplexer.

(c) Interpret the concept of Duality principle with an example.

(d) What is Race around condition? How it can be avoided?

(e) Find the value of X in $(1101.101)_2 = (X)_{10}$

(f) Compare performance of ECL and TTL.

Part – B

[Marks: 04 each]

Q2. Explain the working and truth table of master slave J-K flip flop in detail.

Q3. Compare and contrast Synchronous counter and Asynchronous counter?

Q4. Translate **C'D+ABC'+A'B'D+ABD'** into standard POS form.

Q5. Design a two bit magnitude comparator to compare equality and inequality.

Q6. Minimize the given expression using K-Maps. $\mathbf{f = \pi M (1, 3, 6, 7, 8, 9, 12, 13, 17, 19, 22, 23, 24, 25, 30, 31).}$

Q7. Explain block diagram of decoder to explain its functions.

MORNING

Part – C 27 FEB 2024 **[Marks: 12 each]**

Q8. Construct a 4-bit Binary to Gray Code Converter with proper truth table, K-Maps and Circuit Diagram Implementation.

OR

Implement 4:1 MUX using 2:1 MUX.

Q9. Design a 3-bit Twisted Ring or Johnson counter using J-K flip flops to count the sequence of states with the help of truth table and timing diagram.

OR

Explain the following in detail:

(a) Programmable Logic Array (PLA),

(b) Programmable Array Logic (PAL),

(c) Field Programmable Gate Arrays (FPGA).

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