

UNIT TEST : 2

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Q: I(A)

I. Give one solution of how to overcome with external fragmentation?

→ Compaction is one of the solution of how to overcome with external fragmentation.

2. What is page fault?

→ If there is a reference to a page, first reference to the page will trap to operating system that is called page fault.

3. Define address binding?

→ If given logical address is mapped by the MMU (memory management unit) to physical address.

4. What do you mean by hit ratio?

→ The percentage of that page number of us interest is found in the TLB is called the hit ratio.

Q: I(B)

I. State two disadvantage of best fit memory allocation policy.

→ Best fit policy scans all available holes and chooses the one with a size closest to the requirement.

→ It is slower and may even tend to fill up memory with tiny useless holes.

II. Difference between internal and external fragmentation.

- ⇒ (i) basic reason behind the occurrences of Internal and external fragmentation is that internal fragmentation occurs when memory is partitioned into fixed-sized blocks whereas external fragmentation occurs when memory is partitioned into variable size blocks.
- (ii) When the memory block allocated to the process comes out to be slightly larger than requested memory then the free space left in the allocated memory block causes internal fragmentation.

(iii) define : ~~Definition of internally fragmented memory~~

(i) TLB Hit :

The translation look side buffer is a memory cache that is used to reduce the time taken to access a user memory location.

(ii) TLB miss :

If the page number is not in the TLB known as TLB miss

(iv) What do you mean by page and frame in the context of paging? Why page size is always power of 2.

⇒ "divide physical memory into fixed-sized blocks called frames"

"divide logical memory into blocks of same size called pages."

⇒ Splitting an address between bits results in a page size that is power of 2 because each bit position represents a power of 2

Q: 2

(A) Explain the three different stages for binding of instructions and data to memory with necessary diagram.



Address binding of instructions and data to memory address can happen at three different stage.

(i) Compile time

(ii) Load time

(iii) Execution time.

(i) Compile time:

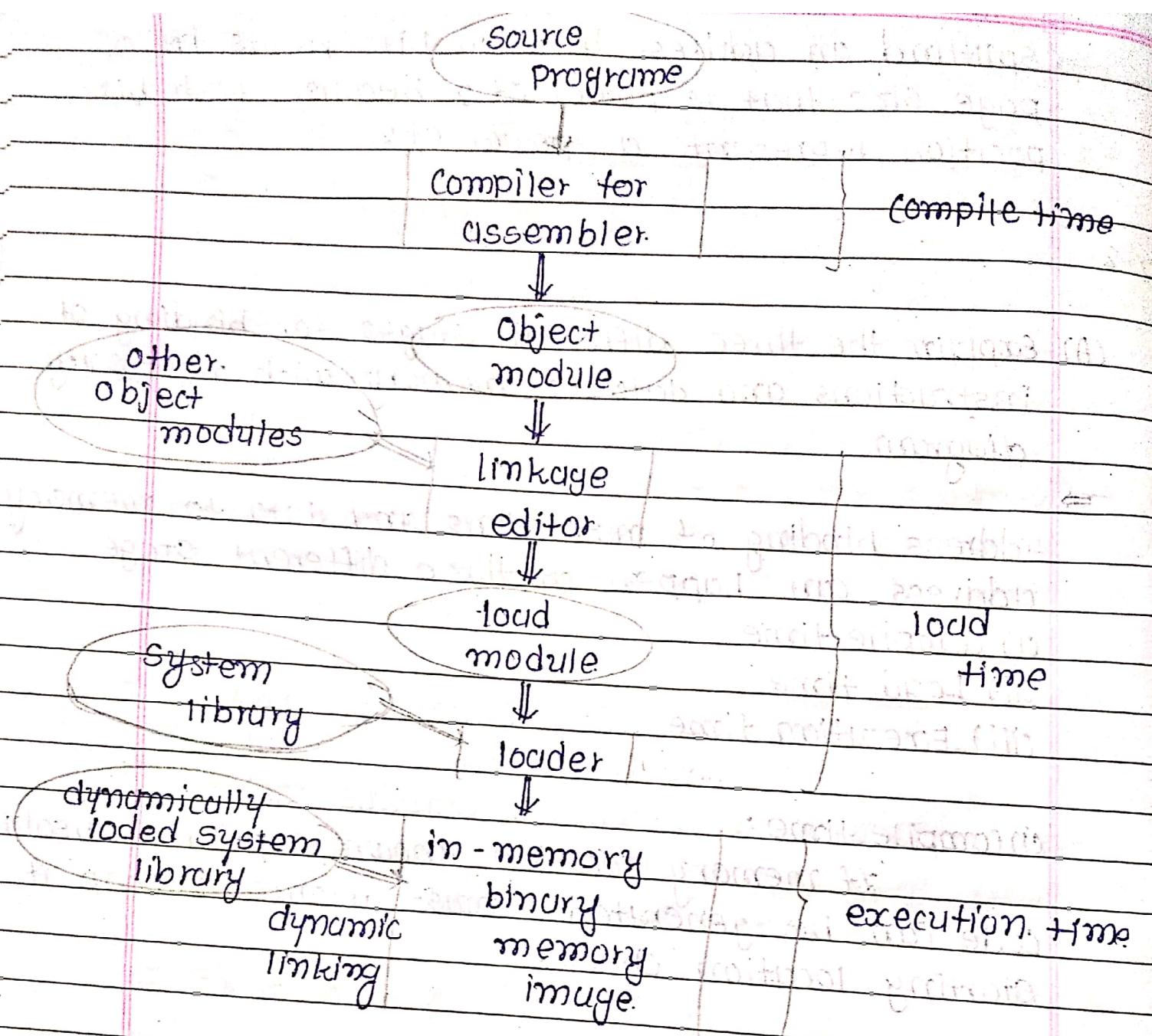
If memory location known a priori, absolute code can be generated; must recompile code if starting location changes.

(ii) Load time:

Must generate relocatable code if memory location is not known at compile time

(iii) Execution time:

Binding delayed until run time if the process can be moved during its execution from one memory segment to another. need hardware support for address maps



OR

- (A) Explain buddy system of memory partitioning with proper diagram.
- The buddy system of partitioning relies on the fact that space allocations can be conveniently handled in size of power of 2.

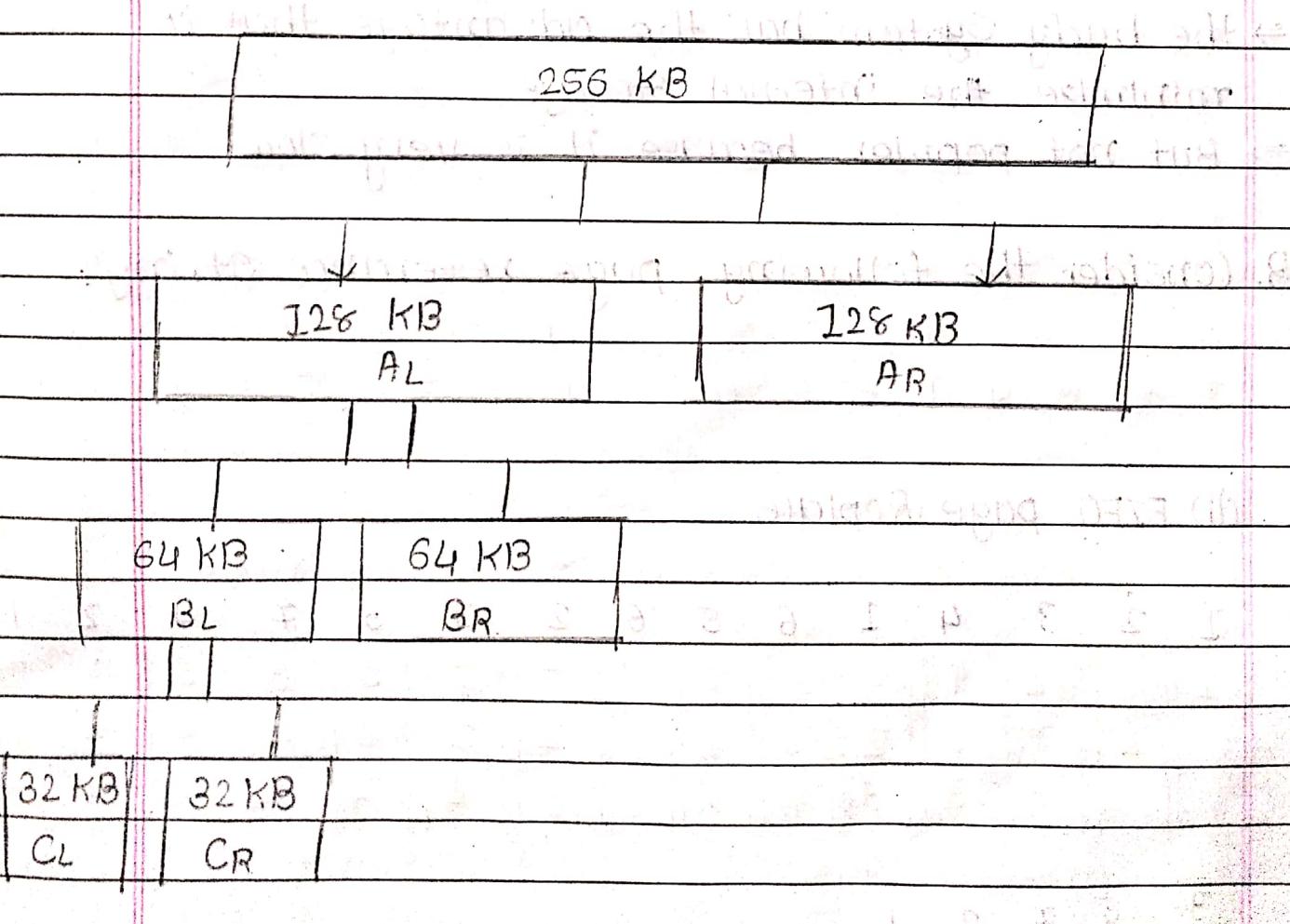
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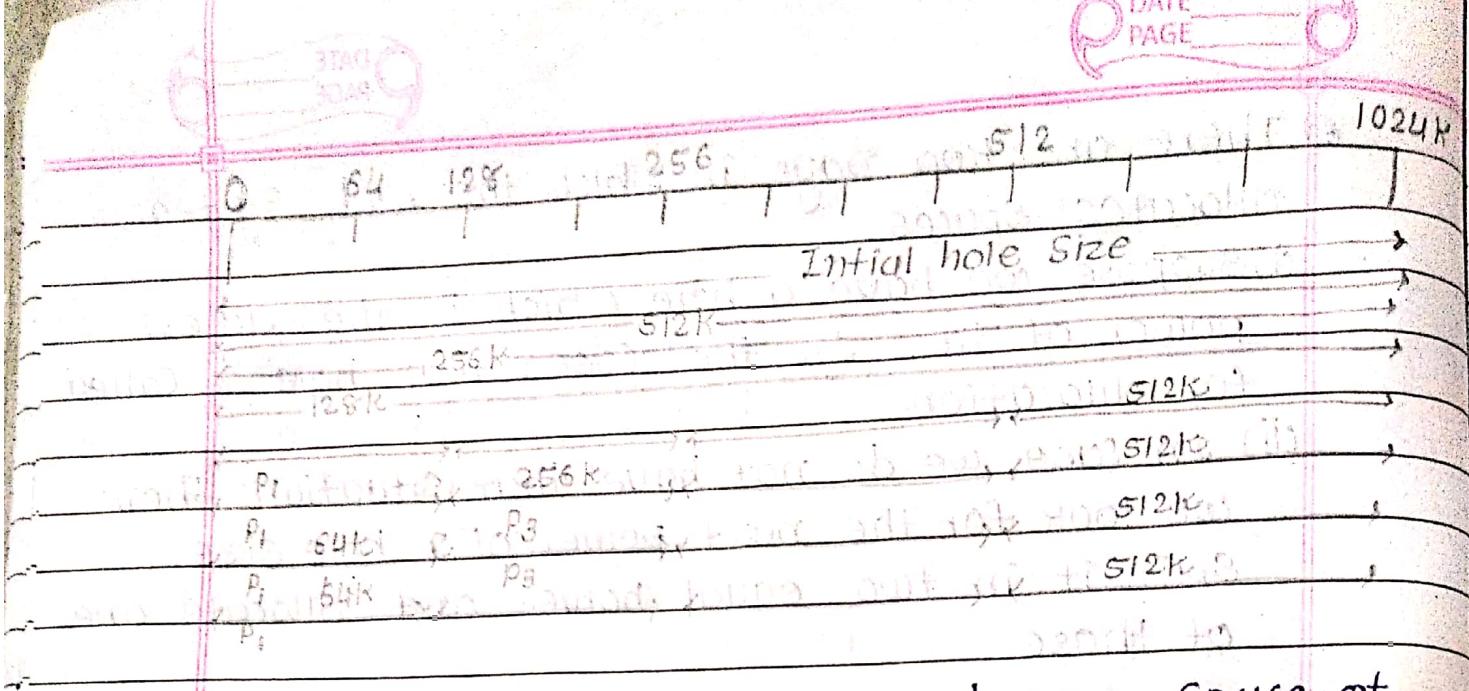
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Q There are two ways in which the buddy system allocates spaces.

- i) Suppose we have a hole which is the closest power of two. In that case, that hole is called for allocation.
- ii) In case we do not have that situation then we look for the next power of 2 hole size. Split it in two equal halves and allocate one of these.

Because we always split the holes in two equal the two are "buddies". Hence, the name buddy system.





we assume that initially we have a space of 1024K. we also assume that processes arrive and are allocated following in a time sequence as shown in figure.

- the buddy system has the advantage that it minimize the internal storage.
- But not popular because it is very slow.

B. Consider the following page reference string:

1, 2, 3, 0, 1, 6, 5, 6, 2, 1, 3, 7, 4, 2, 1, 3, 5, 7, 0, 1,

(ii) FIFO page Replace.

1	2	3	4	1	6	5	6	2	1	3	7	4	2	1
1	1	1	4	4	4	5	-	5	5	3	3	3	2	2
2	2	2	1	1	1	-	-	2	2	2	2	2	2	2
3	3	3	6	6	-	-	-	6	1	2	2	4	4	4
3	5	7	2	1	-	-	-	-	-	-	-	-	-	-
2	5	5	5	1	-	-	-	-	-	-	-	-	-	-
1	1	7	7	7	-	-	-	-	-	-	-	-	-	-
3	3	3	2	2	-	-	-	-	-	-	-	-	-	-

Page fault = 19

(iii) optimal page Replacement

1	2	3	4	1	6	5	6	2	1	3	7	4	2	3
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
3	4			6	5	6			3	7	4			

3	5	7	2	1
1	1	1		
2	2	2		

Page fault = 13

B. Consider the initial physical memory mapping having follows contiguous allocation

1. Operating System

P1 < 10 > KB

Free < 20 > KB

P2 < 40 > KB

Free < 30 > KB

P3 < 15 > KB

Free < 35 > KB

Suppose process P4 < 18 > KB :

P1 < 10 > KB

Free < 20 > KB

P2 < 40 > KB

Free < 30 > KB

P3 < 15 > KB

P4 < 18 > KB

Free < 17 > KB

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Suppose process P5 & U0> KB has descriptor

P1 <10> KB

P2 <40> KB

P3 <15> KB

P4 <18> KB

P5 <20> KB

Free <7> KB

Element 3 P1

Q3

c. Define paging : Explain paging hardware with TLB

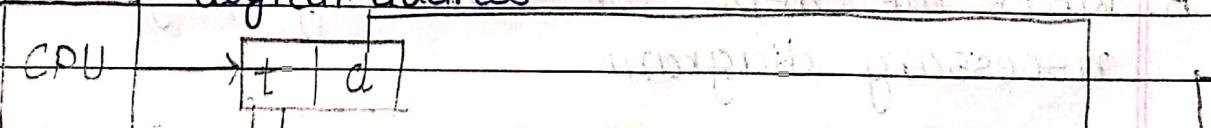


Paging : It is a technique used with LRU

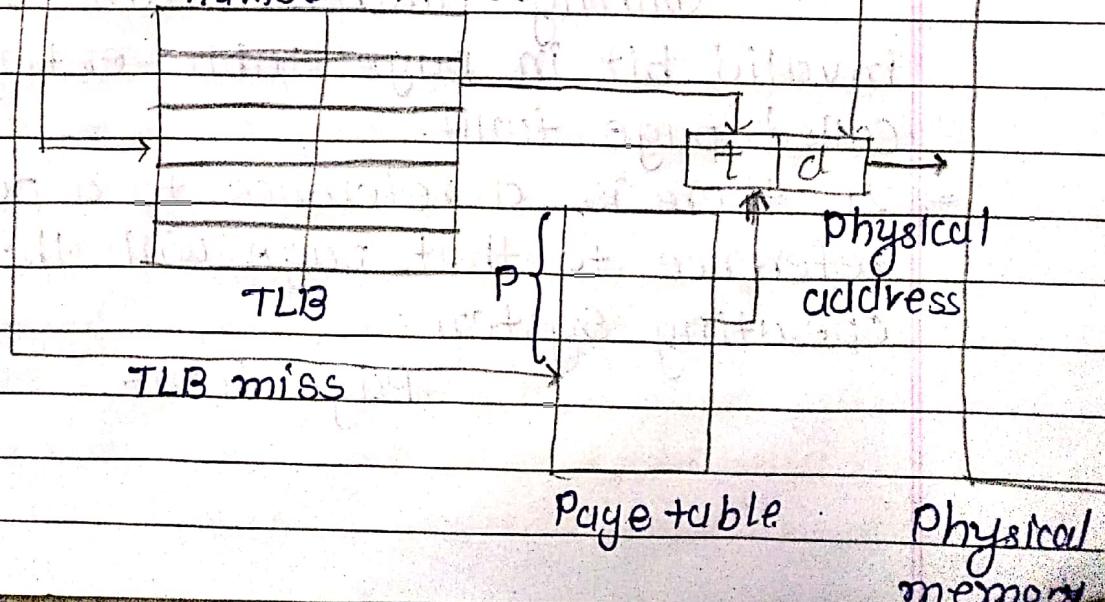
Logical address space of a process can be noncontiguous ; process is allocated physical memory whenever the latter is available.

- "divide physical memory fixed-sized blocks called frames"
- "divide logical memory into blocks of same size called pages"
- take track of all free frames
- To run a program of size n pages, need to find n free frames and load programs.
- Set up a page table to translate logical to physical address.

Logical address



page frame
number number



hit ratio:

"the percentage of times that page number of interest is found in the TLB is called the hit ratio."

"If the page number is not in the TLB.

(known as a TLB miss)

the hardware implementation of page table can be done by using dedicated register. But the usage of register for the page table is satisfactory only if page table is small. If page table contains large number of entries then we can use TLB, a special small, fast look up hardware cache.

- TLB associate high speed memory.
- each entry in TLB contains of two parts tag and a value

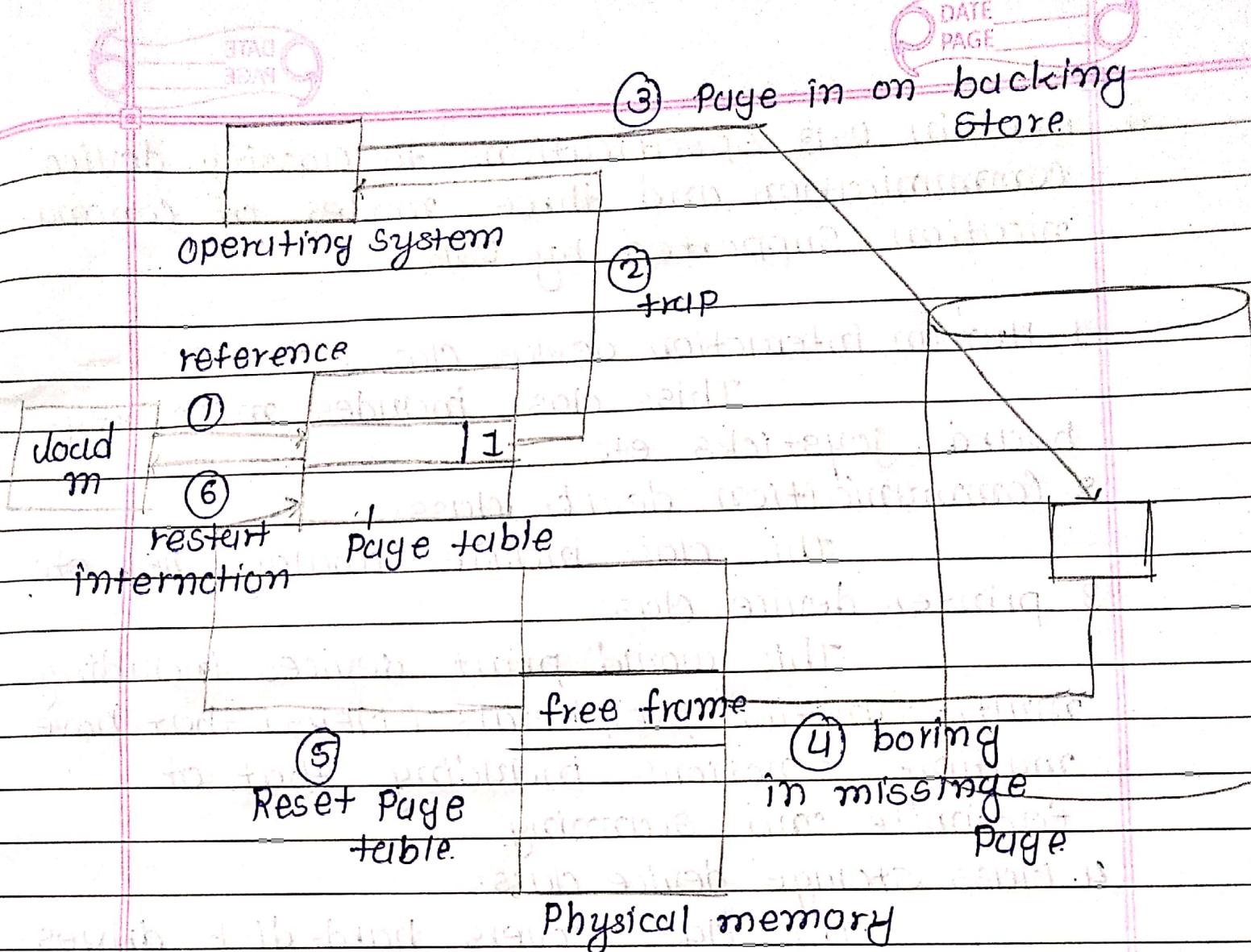
B. Write the steps for handling page fault with necessary diagram

Page fault:

"During address translation, if valid bit in page table entry is (0) it's called page fault."

→ If there is a reference to a page first reference to that page will trap to operating system:

Page fault



* operating system looks at another table to device:

Invalid reference \Rightarrow abort (page not in memory, just not in memory.)

- Get empty frame
- Swap page into frame
- Reset tables
- Set valid bit = V
- Restart the instruction that caused the page fault

A. Explain USB specifications to classify device communication and three modes of communication supported by USB.

1. Human interaction device class:

This class includes mice, keyboard, joystick etc.

2. Communication device class:

This class includes analog, DSL etc.

3. printer device class:

This would print devices including multi-function peripherals (MFPs) that have multiple functions including that of facsimile and scanning.

4. Mass storage device class:

This class covers hard-disk drives,

CD-ROMs, DVDs

* USB supports the following mode of communication:

(i) Interrupt:

for devices like keyboard, mice, joysticks

(ii) Bulk transfer:

Usually medium speed devices like pointers, one main characteristic of this transfer is in "error correction mode."

(iii) Isochronous:

Usually for media like audio and video. These transfer are carried out without any error correction support. Mostly, the communication is for real-time or near-real-time communication.