3-Bit Resistor String DAC

Advanced Integrated Circuit Design Lab (SoSe 2014)

Integrated Electronic System Lab

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1. Lab Task

The aim of this lab is to design a 3-Bit Resistor String Digital-to-Analog Converter.

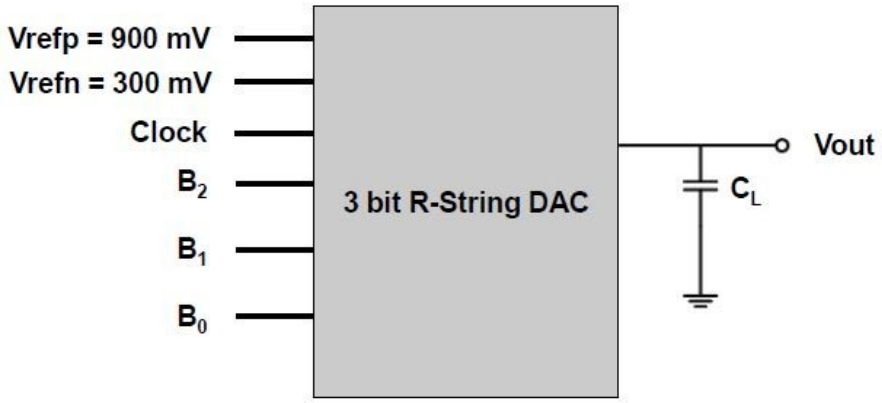
Digital-to-Analog Converter :

A device that converts discrete digital binary code into a continuous varying analog signal. DAC is implemented as integrated circuits. DACs are commonly used in music players to convert digital data streams into analog audio signals. And also used in televisions and mobile phones to convert digital video data into analog video signals. The suitability of a DAC for a particular application is determined by tradeoff among six main parameters: physical size, power consumption,resolution, speed, accuracy, cost.

3-bit Resistor String DAC is formed of a series of resistors, which are connected to an OPAMP buffer through an analog multiplexer. Based on the digital inputs, the switch multiplexer selects the corresponding voltage from the resistor string(which acts as voltage divider within the referenced voltage range) and gives it to the Opamp buffer, which simply buffers the signal to drive a high capacity load.

Based on the inputs and design specifications, schematics and layout for different blocks of DAC mentioned above are designed in **Cadence Custom IC Design Tools** (Virtuoso Front to Back Design Environment) using 0.13um mixed mode and RF CMOS process (**umc130mmrf)** technology library. Schematic simulation and Post-Layout simulations are tabulated and the designed DAC's static performance parameters such as Integral Non Linearity (INL), Differential Non Linearity (DNL), Gain Error, Offset Error with Power and Area of design are measured using Cadence.

The block diagram of DAC with inputs and outputs is as shown below :



3-Bit Resistor String DAC Signal Inputs :

1. Reference Voltages, Vrefp = 900mV and Vrefn = 300mV.
2. Clock Signal : Voltage = 1.2 V, Rise time = Fall time = 300 ps, Pulse Width = 49.7 ns, Period = 100 ns.
3. B2 (Binary) : Voltage = 1.2 V, Rise time = Fall time = 300 ps, Pulse Width = 399.7 ns, Period = 800 ns.
4. B1 (Binary) : Voltage = 1.2 V, Rise time = Fall time = 300 ps, Pulse Width = 199.7 ns, Period = 400 ns.
5. B0 (Binary) : Voltage = 1.2 V, Rise time = Fall time = 300 ps, Pulse Width = 99.7 ns, Period = 200 ns.

3-Bit Resistor String DAC Characteristics :

1. Ideal Output Voltages for input [B2 B1 B0] are :
   (000) = 337.5mV, (001) = 412.5mV, (010) = 487.5mV, (011) = 562.5mV,
   (100) = 637.5mV, (101) = 712.5mV, (110) = 787.5mV, (111) = 862.5mV.

2. The DAC has LSB value of 75mV.

   $1\,LSB = (Vrefp - Vrefn)/2^n$ Where no of bits = n = 3

3. The errors for the resistor string DAC should be less than 0.5 LSB for both INL and DNL errors.

2. Design Flow

The DAC architecture realized in this task is a String (Resistor Ladder) DAC. Basically it has 4 network components. They are :

1. OPAMP Buffer :

It is two stage CMOS OPAMP which is used to buffer incoming signals from resistor string so that high capacity loads are to be driven. It has a negative feedback.

Fundamentally, the first stage is differential input stage and the second stage is common source amplifier gain stage. Further, a biasing circuit is designed to provide the input differential stage with biased reference current.

2. Control Signal Logic (3 to 6 Decoder) :

It takes the input binary codes coming from an external source and buffers them to generate the original signal and its complement before driving the analog switch multiplexer.

This block is of 3-bit Parallel In Parallel Out type designed with 3 Positive edge triggered D-Flip Flops having a synchronous Clock signal.

These Edge triggered D-Flip Flops are built with a 2 stage combination of Transmission Gates and Inverters. Each of these D-Flip Flop buffer out 1 bit of 3 bit input[B2 B1 B0] along with its complement.

Control Logic is complete digital block used to synchronize(at positive edge of clock) the switching of all switches in multiplexer array using high fan out buffers and reduce glitching noise.

3. Analog Switch Multiplexer (8:1 Mux) :

It is made up of analog switches. Depending on the control signals (as Select signal of Mux), the corresponding voltage from the resistor string is passed on the OPAMP buffer.

It makes use of simplest analog CMOS switch (Transmission Gate) with low on-resistance and high off-resistance.

The 1st input stage is made up of 8 CMOS switches controlled by B0 and ~B0 select signals which inturn drive the intermediate stage consisting of 4 CMOS switches controlled by B1 and ~B1 select signals. The output from this stage collectively drive the last stage with 2 CMOS switches controlled by B2 and ~B2 select signals from control signal logic.

4. Resistor Ladder :

It is R-2R ladder network. It is voltage divider network with the supplied reference voltage range. To carry out mismatch analysis, we take into consideration 3 types of layout.

a. Linear Layout
b. Folded Layout
c. Inter digitized Layout.

This ladder plays a significant role in determination of analog voltage which inturn influences the power dissipation, speed, area and static performance of our DAC. A optimum choice of layout is made based upon these parameters.

3. Schematic-based Design and Simulation:

A. Two-Stage CMOS OPAMP Buffer

Specifications :

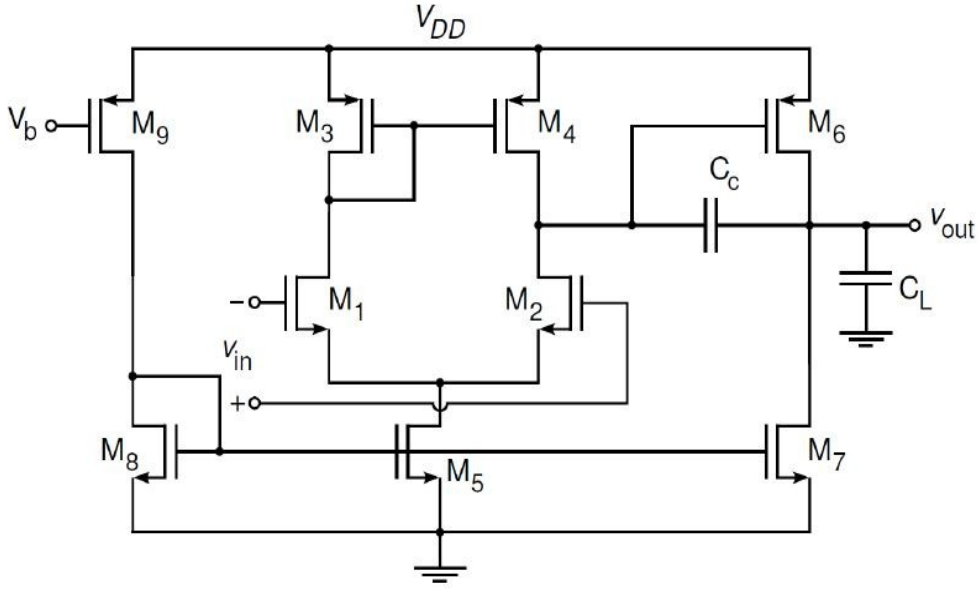
Parameter	Required Specification
DC Gain ($A_v(0)$)	> 50 dB
Gain Bandwidth (GB)	$\geq$20 MHz
Phase Margin (PM)	$\geq 50^\circ$
Slew Rate (SR)	$\geq$15 V/μs
Positive Input Common-Mode Range ($V_{in}(max)$)	900 mV
Negative Input Common-Mode Range ($V_{in}(min)$)	300 mV
Output Voltage Swing	0.2 V – 1 V
Power Dissipation (P_{diss})	$\leq$ 3 mW
Load Capacitance (C_L)	$\geq$ 1 pF
Positive Supply Voltage (V_{DD})	1.2 V
Negative Supply Voltage (gnd)	0 V

Transistor Parameters: UMC 130 Technology

Parameter	NMOS	PMOS	Units
V_{T0} = threshold voltage ($V_{BS} = 0$)	2.165e-1	-2.508e-1	V
$K' = \mu_0 \cdot C_{ox}$ = transcond. parameter in saturation	523.53	145.81	μA/V^2
μ_0 = surface mobility of the channel	415.5	120.5	cm^2/(V·s)
t_{ox} = gate oxide thickness	2.73e-9	2.86e-9	m
C_{ox} = gate oxide capacitance per unit area	1.26e-6	1.21e-6	F/cm^2
N_{SUB} = substrate doping concentration	6e16	6e16	cm^{-3}
γ = bulk threshold parameter	0.112	0.117	V$^{1/2}$
$2\lvert\Phi_F\rvert$ = surface potential at strong inversion (27°C)	0.788	0.788	V
λ = channel length modulation parameter	0.781	1.078	V^{-1}

Constant	Value	Units
V_{G0} = silicon band gap (27°C)	1.205	V
k = Boltzmann's constant	1.381e-23	J/K
n_i = intrinsic carrier concentration (27°C)	1.45e10	cm^{-3}
ε_0 = permittivity of free space	8.854e-14	F/cm
ε_{Si} = permittivity of silicon	11.7·ε_0	F/cm
ε_{ox} = permittivity of SiO_2	3.9·ε_0	F/cm

I. Operation :



Differential Input Gain Stage : Transistors M1, M2, M3, M4 and M5 constitute the first stage of the op amp. The gate of M1 is the non-inverting input and of M2 is the inverting input. A differential input signal is applied across the two input terminals will be amplified according to the gain of the differential stage. Transistors M3 and M4 form high strength current mirrors. The current mirror topology performs the differential to single- ended conversion of the input signal. The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. Finally, the differential current from M1 and M2 multiplied by the output resistance of the input stage gives the single-ended output voltage, which is the part of the input to the next stage. The bias current of the input differential pair is provided by M5.

Common Source Second Gain Stage : The second stage is a current sink load inverter. The motive of the second gain stage is to provide additional gain consisting of transistors M6 and M7. This stage receives the output from the drain of M2 and amplifies it through M6 by common source configuration. This stage is equipped with an active device, M7, which serve as the load resistance for M6. The gain of this stage is the trans-conductance of M6 times the equivalent load resistance seen at the output of M6 and M7. M6 is the driver while M7 acts as load. The bias current of the second stage is provided by M7. This stage provides voltage gain and high output resistance.

Biasing Circuit : A simple resistor divider circuit is used to apply bias voltage to gate of M9. Transistor M8 and M9 form high strength current mirror. Transistors M8 and a reference current from M9 form a simple current mirror biasing network that provides a voltage between the gate and source of M5 and M7. Transistors M5 and M7 sink a current based on their gate to source voltage which is controlled by the bias network.

Compensation Circuit : The OPAMP consists of an Operational Trans-conductance Amplifier (OTA) followed by an output buffer. The OTA is compensated with a miller capacitor connected between the input and output of the buffer. The motive of the compensation circuit is to decrease the gain at high frequencies and to maintain stability when negative feedback is applied to the op amp. It also improves the unity gain frequency (the bandwidth) and phase margin of the OPAMP.

II. Design Procedure (Hand Calculations) :

1. Choose the device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

$$L_1 = L_2 = 480\text{nm}$$
$$L_3 = L_4 = 480\text{nm}$$
$$L_5 = L_8 = 360\text{nm}$$
$$L_6 = L_7 = L_9 = 120\text{nm}$$
$$W_9 = 160\text{nm};$$

2. From the desired phase margin, choose the minimum value for *Cc*, i.e. for a 60° phase margin we use the following relationship. This assumes that $z \geq 10GB$.

$$C_c > (2.2/10)C_L$$

Here we choose,

$$C_L = 1.25 \text{ pF}$$

$$C_C = 2.5 * 0.22 * C_L$$

$$Cc = 0.6875 \text{ pF}$$

3. Determine the minimum value for the "tail current" ($I5$) from the largest of the two values.

$$I_5 = SR.\ C_c$$

Here, we choose Slew Rate = SR= 15V/μs

Hence , $I_5 = 10.3125$ uA

$$I_3 = I_4 = I_5/2 = 5.15625 \text{ uA}$$

4. Design for $S3$ from the maximum input voltage specification.

$$S_3 = (W/L)_3 = I_5 / (K'_3)[VDD - Vin(max) - |VT_{03}|(max) + VT_1(min)]^2 \geq 1$$

$$S_3 = S_4 = 2.38$$

$$W_3 = S_3 L_3 = 1.14 \text{ um}$$

$$W_4 = S_4 L_4 = 1.14 \text{ um}$$

5. Verify that the pole of M3 due to $Cgs3$ and $Cgs4$ (= 0.67W3L3Cox) will not be dominant by assuming it to be greater than 10 GB.

i.e $(g_{m3}/2C_{gs3}) > 10GB$.

Therefore, $g_{m3} = g_{m4} = \sqrt{-2K'_p S_3 I_3}$

$$g_{m3} = g_{m4} = 59.87285\text{e-}06$$

$$p3 = (-g_{m3}/2C_{gs3}) = (\sqrt{-2K'_p S_3 I_3} / 2(0.667) W_3 L_3 C_{ox})$$

$$p3 = 1.0747\text{E+}07 \text{ M Hz}$$

6. Design for $S1$ ($S2$) to achieve the desired GB.

Lets take, $GB = 175$ MHz

$$g_{m1} = GB\ .\ Cc$$

$$g_{m2} = g_{m1} = 7.5595\text{e-}04$$

Therefore, $S_2 = g_{m2}^2 / K'_2 I_5$

$$S_1 = S_2 = 105.85$$

$W_1 = S_1 L_1 = 50.81$ um

$W_2 = S_2 L_2 = 50.81$ um

7. Design for *S*5 from the minimum input voltage. First calculate *VDS*5(sat) then find *S*5.

$V_{DS5}(sat) = Vin(min) - VSS - I_5\beta_1 - V_{T1}(max) > 100$mV

$V_{DS5}(sat) = 26.5581$ mA

$S_5 = 2I_5 / K'_5[V_{DS5}(sat)]^2$

$S_5 = 55.85$

$W_5 = S_5 L_5 = 20.11$ um

8. Find *g*m6 and *S*6 by the relationship relating to phase margin, load, and compensation capacitors, and the balance condition.

$g_{m6} = 2.2g_{m2}(C_L/C_C)$

$g_{m6} = 3.0238$e-03

$S_6 = S_3(g_{m6}/g_{m3})$

$S_6 = 120.40$

$W_6 = S_6 L_6 = 14.45$ um

9. Calculate *I*6 :

$I_6 = (S_6/S_4)I_3 = (S_6/S_4)(I_5/2)$

$I_6 = 260.41$ mA

10. Design *S*7 to achieve the desired current ratios between *I*5 and *I*6.

$S_7 = (I_6 / I_5)S_5$

$S_7 = 1410.41$

$W_7 = S_7 L_7 = 169.25$ um

11. Calculate $V_{out}(max)$ and $V_{out}(min)$ and check with specifications.

$V_{out}(min) = V_{ds7}(sat)$

$V_{ds7}(sat) = \sqrt{((2I_6) / (K'_7 S_7))}$

$V_{out}(min) = 0.02655$ V

$V_{ds6}(sat) = \sqrt{((2I_6)/(K'_6 S_6))}$

$$V_{ds6}(sat) = 0.1722 \text{ V}$$

$$V_{out}(max) = VDD - V_{ds6}(sat)$$

$$V_{out}(max) = 1.0278 \text{ V}$$

12. Calculate gain and power dissipation and check with the specifications.

$$P_{DISS} = (VDD - VSS)(I_5 + I_6)$$

$$P_{DISS} = 0.325 \text{ mW}$$

$$A_V = 20\log_{10}((2 g_{m1} g_{m6})/(I_5(\lambda_N + \lambda_P))(I_6(\lambda_N + \lambda_P)))$$

$$A_V = 53.85 \text{ dB}$$

13. Determine S_8 and Reference current I_{REF}

$$S_8 = S_5 = 55.85$$
$$W_8 = S_8 L_8 = 20.11 \text{ um}$$
$$I_{REF} = S_8 I_5 / S_5$$
$$I_{REF} = 10.3125 \text{ uA}$$

14. Determine S_9

$$S_9 = W_9 / L_9$$
$$S_9 = 1.33$$

15. Iterate the above steps, till all the specifications are approximately met.

16. Biasing Circuit :

A simple resistive divider circuit is used for providing the biasing voltage for S_9

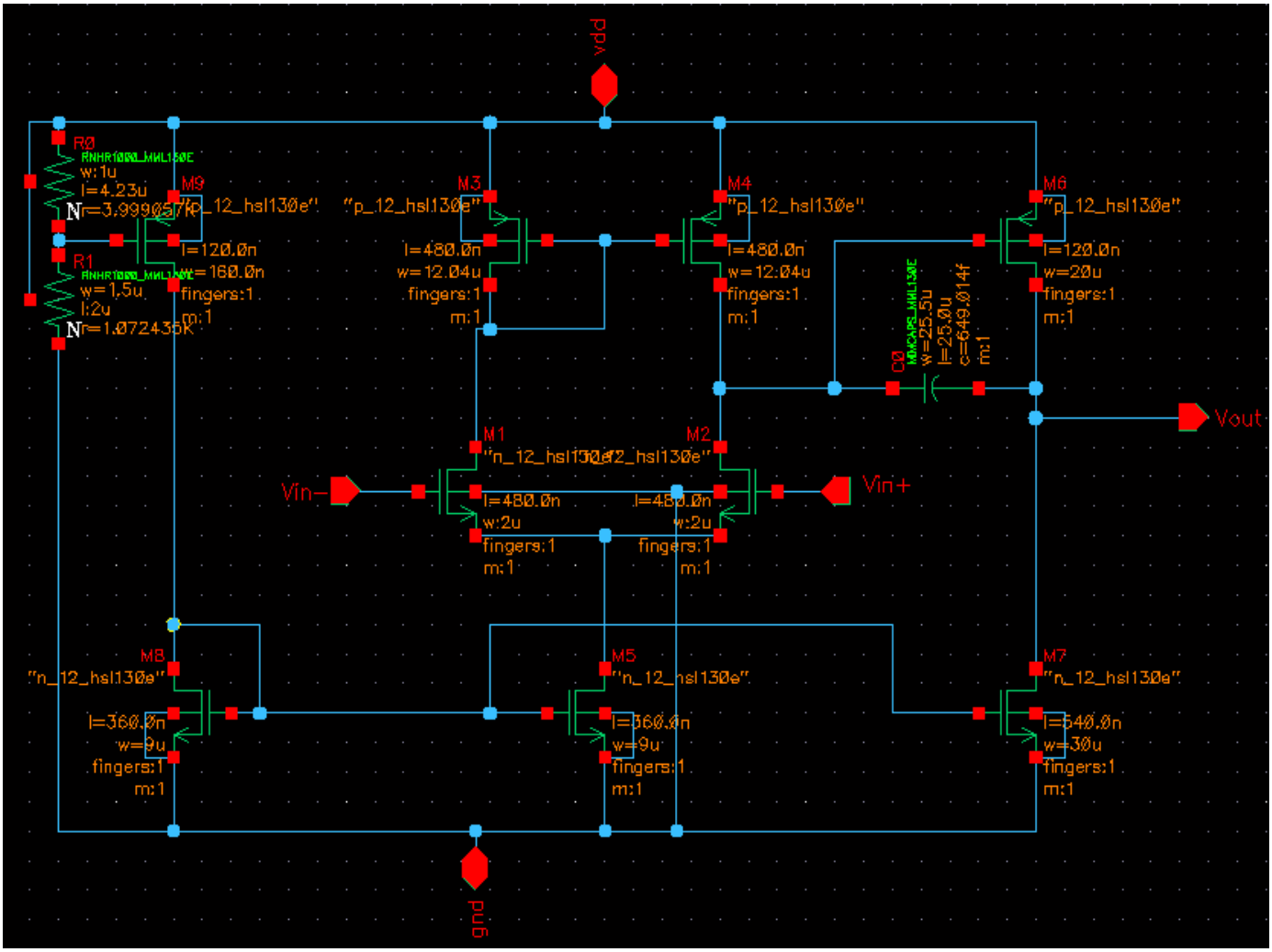
$$V_{\text{out}} = \frac{R_2}{R_1 + R_2} \cdot V_{\text{in}}$$

Initially lets assume R1= 1 KΩ and R2= 2 KΩ .

The results of Hand Calculations are tabulated as shown below :

Transistor	Hand calculations		
	W/L	W (um)	L (nm)
S1,S2	105.85	50.81	480
S3,S4	2.38	1.14	480
S5,S8	55.85	20.11	360
S6	120.4	14.45	120
S7	1410.4	169.25	120
S9	1.33	0.16	120

III. Schematic-based Design



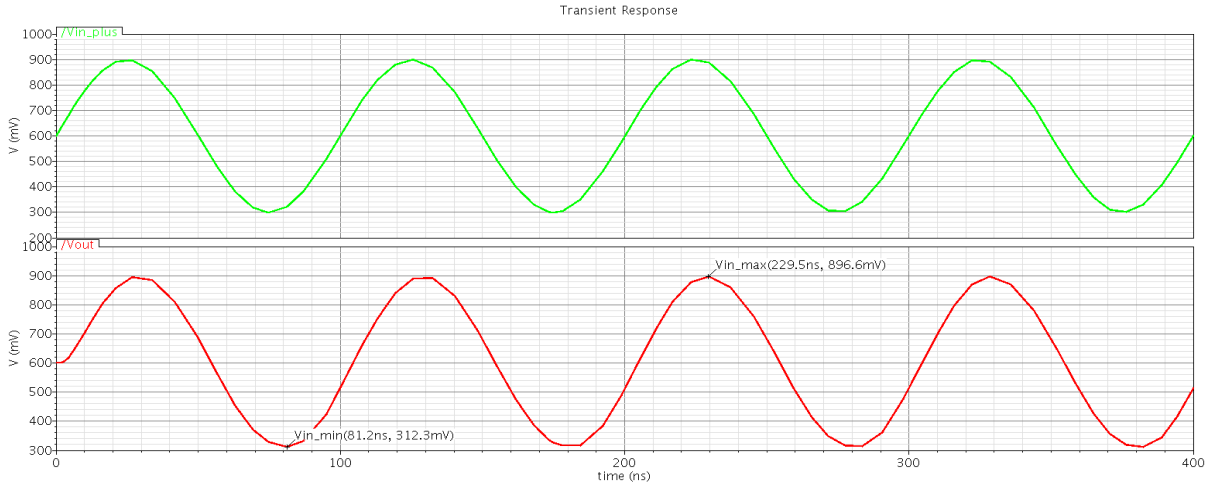
IV. Schematic Simulation

Tweaking the transistor ratios based on relations described below and simulating the resulting Op-amp, we met the given Op-amp specifications.

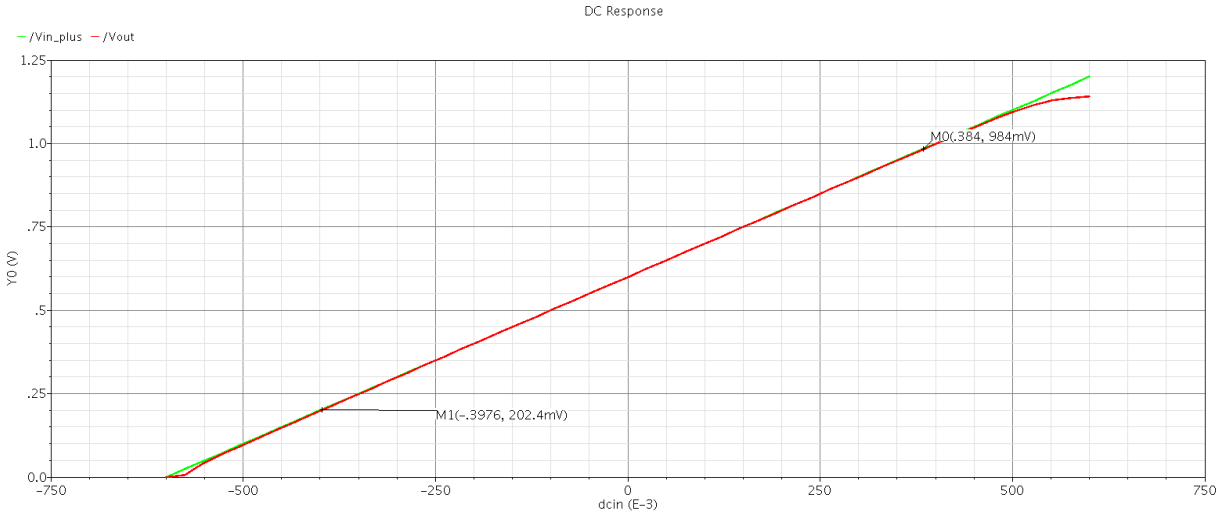
	Drain Currents		S1,2		S3,4		S6	S7		Cc
	I5	I7	W/L	L	W/L	L	W/L	W	L	
Increase A_v	⇩	⇩	⇧	⇧		⇧	⇧		⇧	
Increase GBW	⇧		⇧							⇩
Increase RHP zero		⇧					⇧			⇩
Increase SR	⇧									⇩
Increase C_L										⇩

a. Input Common-Mode Range (ICMR)

From the resulting waveforms : ICMR Vin(min) = 312.3mV , ICMR Vin(max) = 896.6 mV

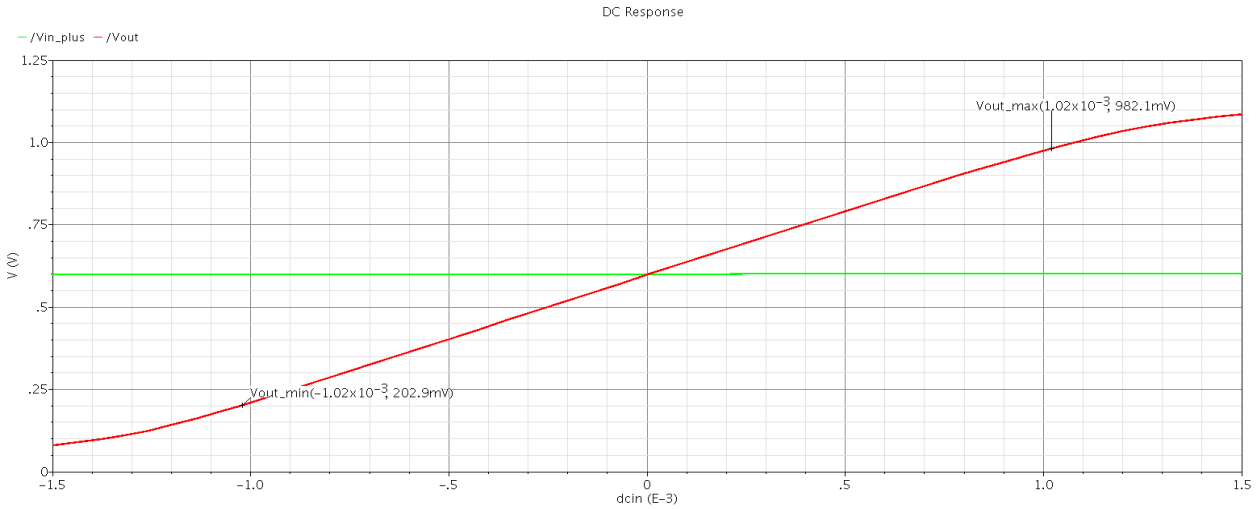


We also observe that the output is following the input closely, in the waveform below



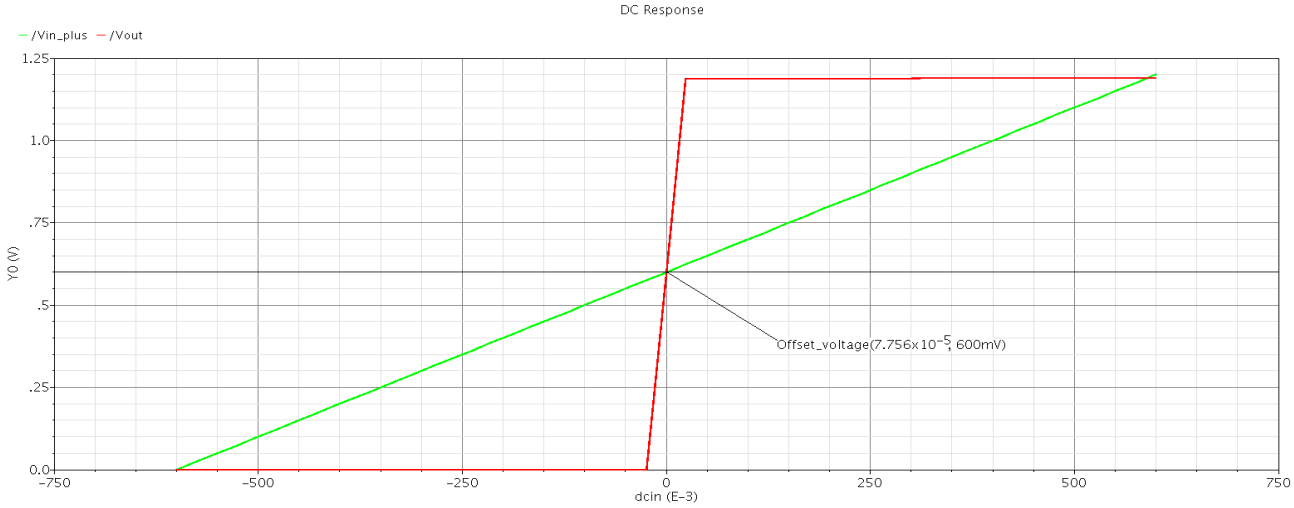
b. Output Range and Power Dissipation

Output Voltage swing = 0.212 V – 0.980 V
Power Dissipation = 0.393 mW



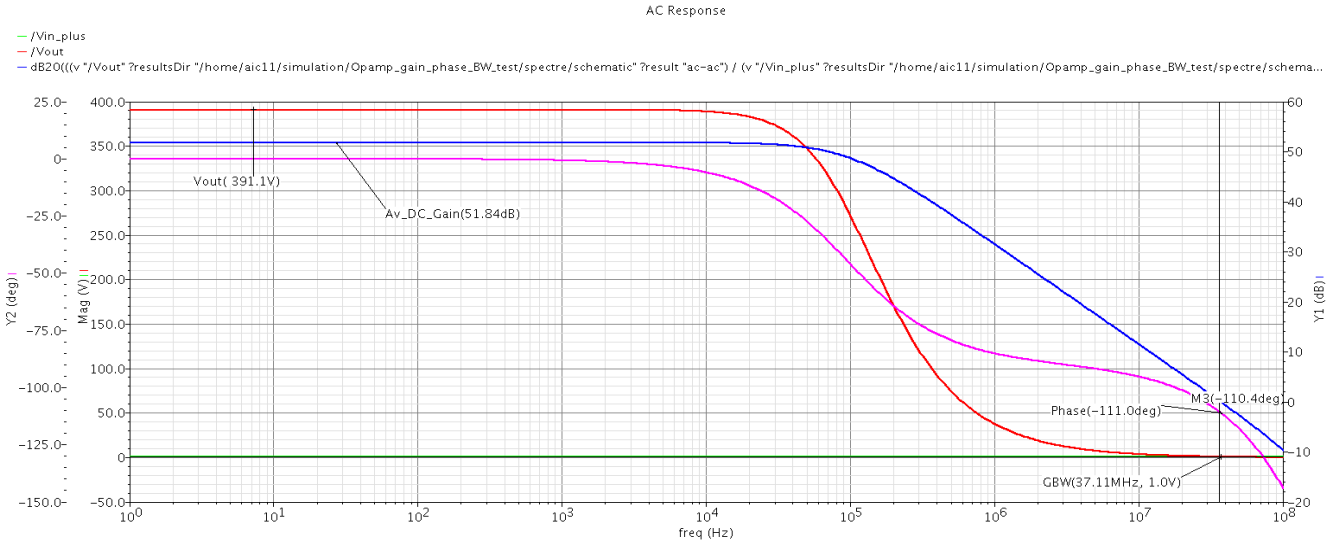
c. Offset Check

Offset voltage = 77.56 uV can be deduced from the resulting wave form.



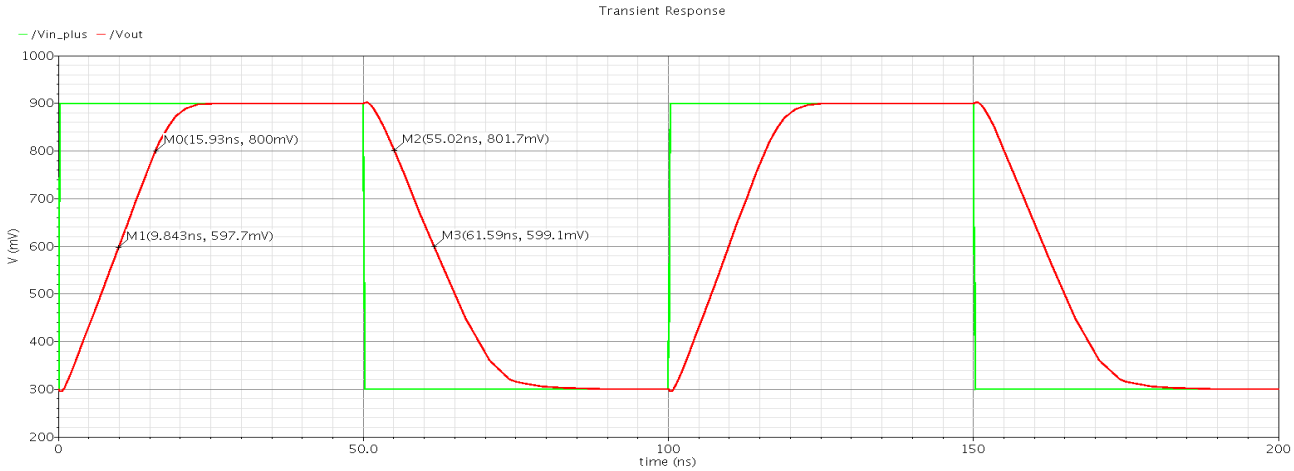
d. DC Gain, Gain Bandwidth and Phase Margin

DC Gain (Av) = 51.84 dB, Gain Band Width (GBW) = 37.11 MHz
Phase Margin = 69.6°



e. Slew Rate

Positive-Slope Slew Rate, Slew Rate (+ve) = 33.23 V/us
Negative-Slope Slew Rate, Slew Rate (-ve) = - 30.8 V/us



OPAMP transistor parameters table: R1= 1 KΩ and R2= 4 KΩ

Transistor	Hand calculations			Schematic without mismatch		
	W/L	W(um)	L(nm)	W/L	W(um)	L(nm)
S1,S2	105.85	50.81	480	4.17	2	480
S3,S4	2.38	1.14	480	25.08	12.04	480
S5,S8	55.85	20.11	360	25	9	360
S6	120.4	14.45	120	166.67	20	120
S7	1410.4	169.25	120	55.55	30	540
S9	1.33	0.16	120	1.33	0.16	120

Opamp DC Operating Points :

Transistors	Drain Current "Id" (uA)	Drain-Source Voltage "Vds" (mV)	Saturated Drain-Source Voltage "Vds_sat" (mV)
M1, M2	11.482	631.102	112.305
M3,M4	-11.482	-346.584	-104.032
M5	22.964	222.315	76.172
M6	-86.461	-601.814	-106.216
M7	87.461	598.186	89.666
M8	23.785	304.478	76.174
M9	23.785	-895.522	-485.319

OPAMP design specifications table: Cc = 0.65 pF, Offset Voltage = 77.56 uV

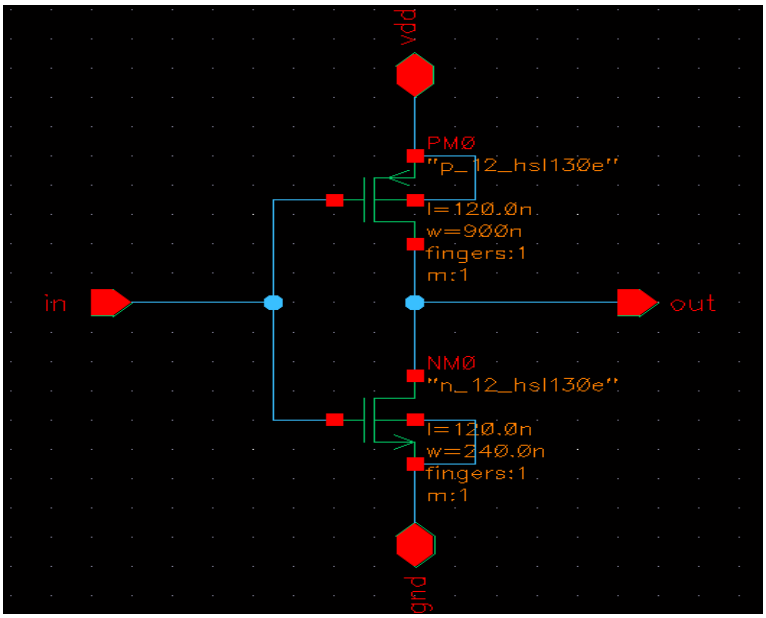
Parameters	Required Specifications	Schematic Without Mismatch
DC Gain	>50 dB	51.84 dB
Gain Bandwidth	≥20 MHz	37.11 MHz
Phase Margin	≥ 50°	69.6°
Slew Rate	≥15 V/us	33.23 V/us
Slew Rate	≥-15 V/us	-30.8 V/us
Positive ICMR Vin(max)	900 mV	896.6 mV
Negative ICMR Vin(min)	300 mV	312.3 mV
Output Voltage Swing	0.2 - 1 V	0.203 – 0.982 V
Power Dissipation	≤ 3 mW	0.394 mW
Load Capacitance	≥1 pF	1.25 pF
Positive Supply Voltage	1.2	1.2
Negative Supply Voltage	0	0

B. Inverter

I. Operation and Schematic Design

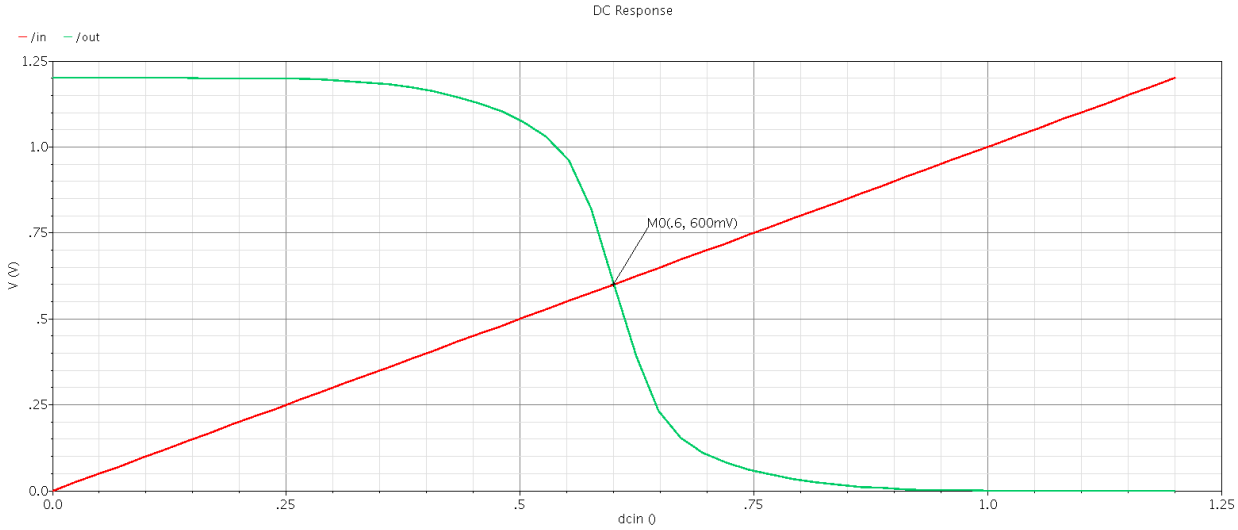
In the schematic of the CMOS inverter circuit. It can be seen that the gates of PMOS (P_12_HSL130E) and NMOS (N_12_HSL130E) are at the same bias "in" which means that they are always in a complementary state. When "in" is high, the voltage between gate and substrate of the nMOS transistor is also approx. vdd and the transistor is in on-state. The gate-substrate bias at the pMOS on the other side is nearly zero and the transistor is turned off. The output voltage "out" is pulled to ground, which is the low state. When the input voltage is in a high-state, the complementary

situation occurs and the pMOSFET is turned on while the nMOSFET is turned off. The output voltage is therefore pulled to vdd which is the high-state. After simulations, **PMOS : W = 900 nm, L= 120 nm. NMOS : W = 240 nm, L = 120 nm**.



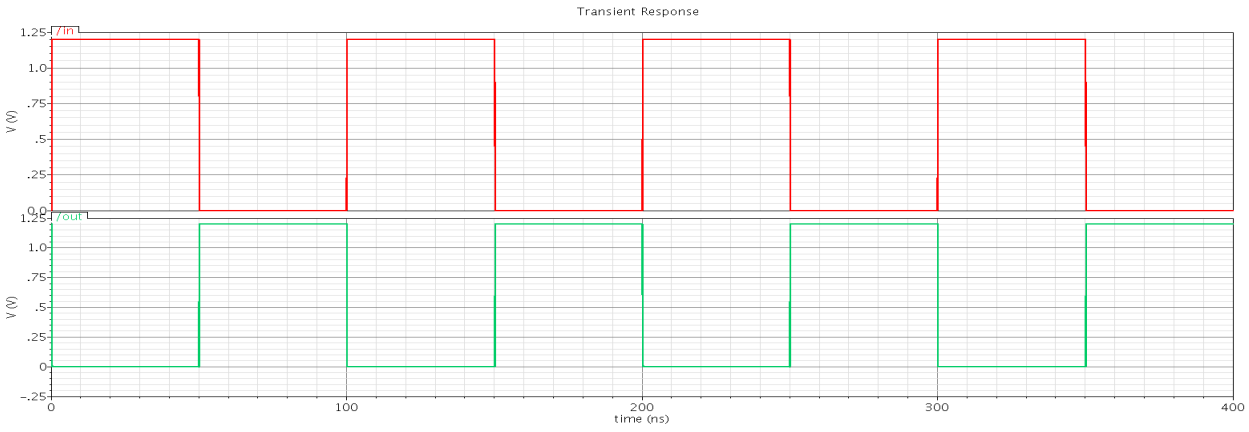
II. Simulation

a. DC analysis



The simulation results show that the designed Inverter is symmetric in nature. For Vin = 600 mV, Vout is 600 mV.

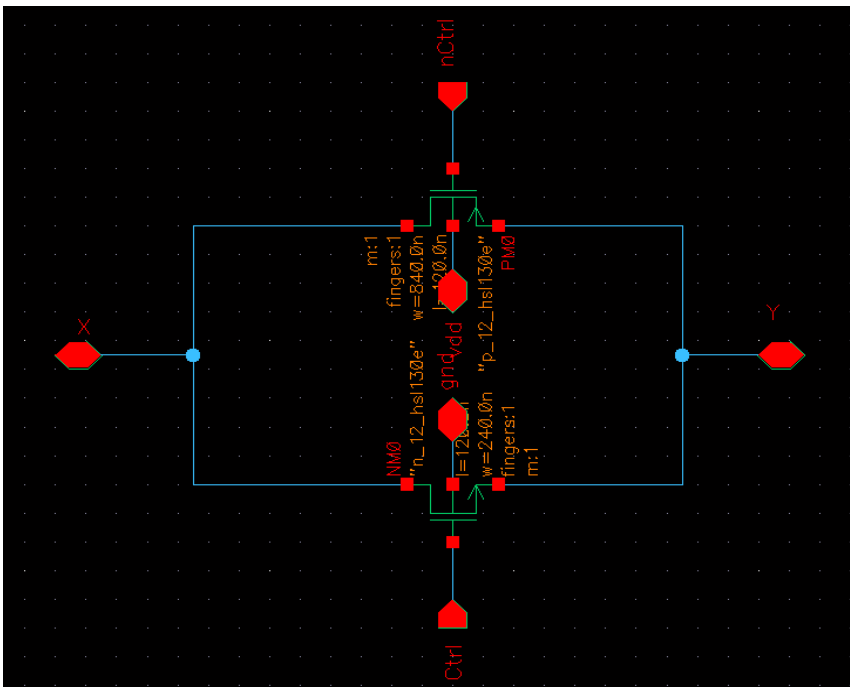
b. Transient Analysis



C. Transmission Gate

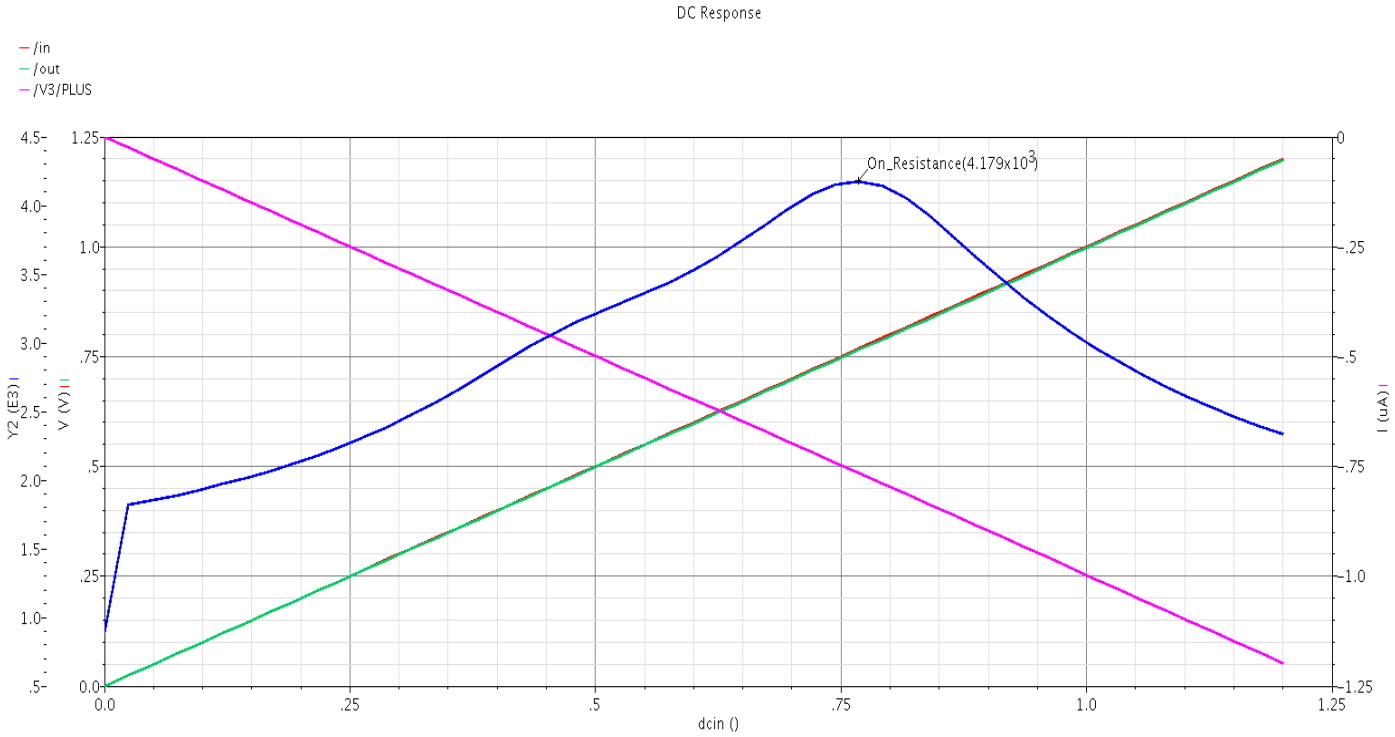
I. Operation and Schematic Design

A Transmission Gate (TG) is a complementary CMOS switch. PMOS (P_12_HSL130E) and NMOS (N_12_HSL130E) are in parallel and are controlled by complementary signals "Ctrl" and "nCtrl". Both transistors are ON or OFF simultaneously. The NMOS switch passes a good "0" but a poor "1". The PMOS switch passes a good "1" but a poor "0". Combining them we get a good 0 and a good 1 passed in both directions. When the “Ctrl” is high, input signal can flow through the transmission gate. When the “Ctrl” is low, the input signal cannot pass through; the transmission gate acts as an open circuit. After simulations, **PMOS : W = 840 nm, L= 120 nm. NMOS : W = 240 nm, L = 120 nm**.

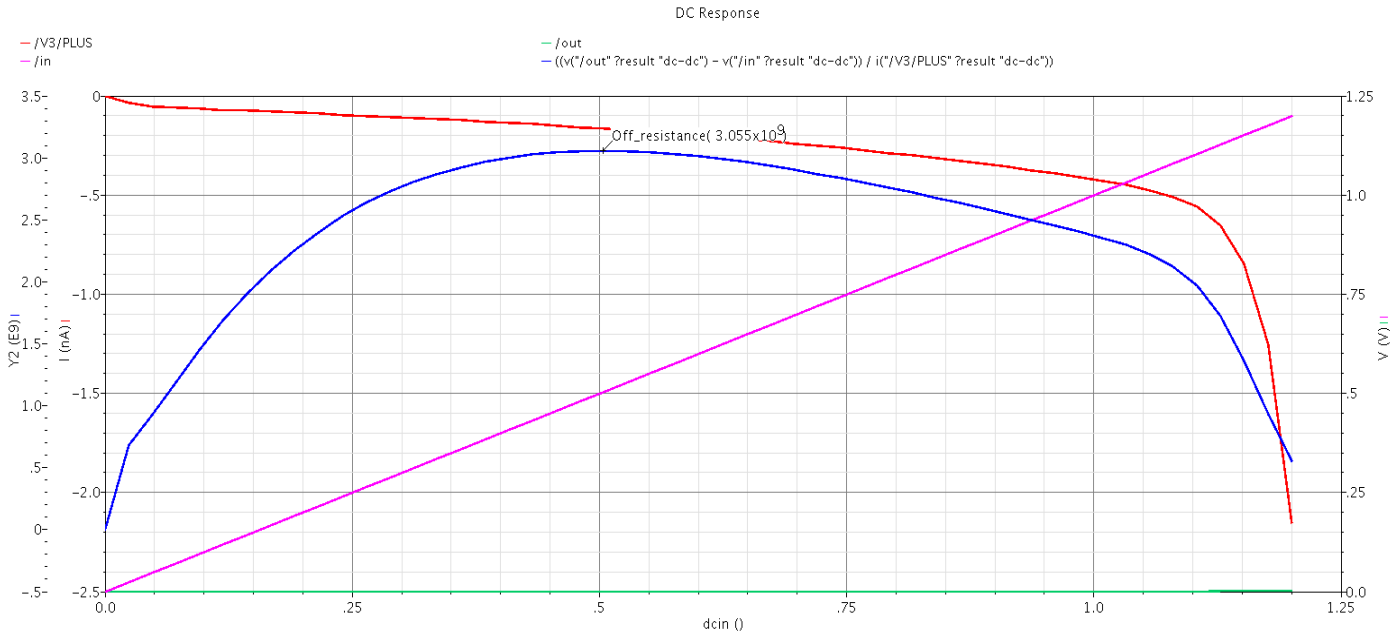


II. Simulation

a. On-off resistance

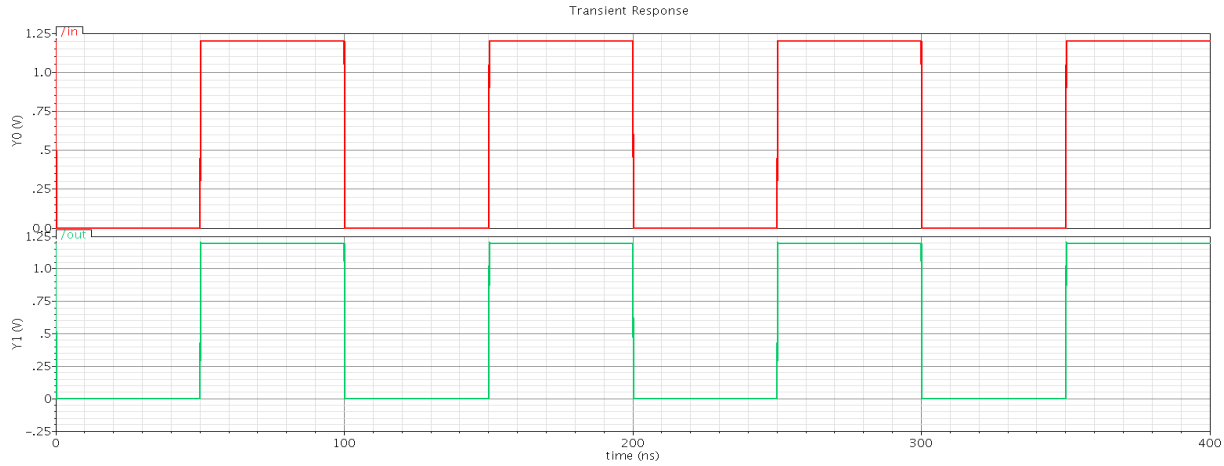


From the waveform editor, the ON-Resistance = 4.179 KΩ



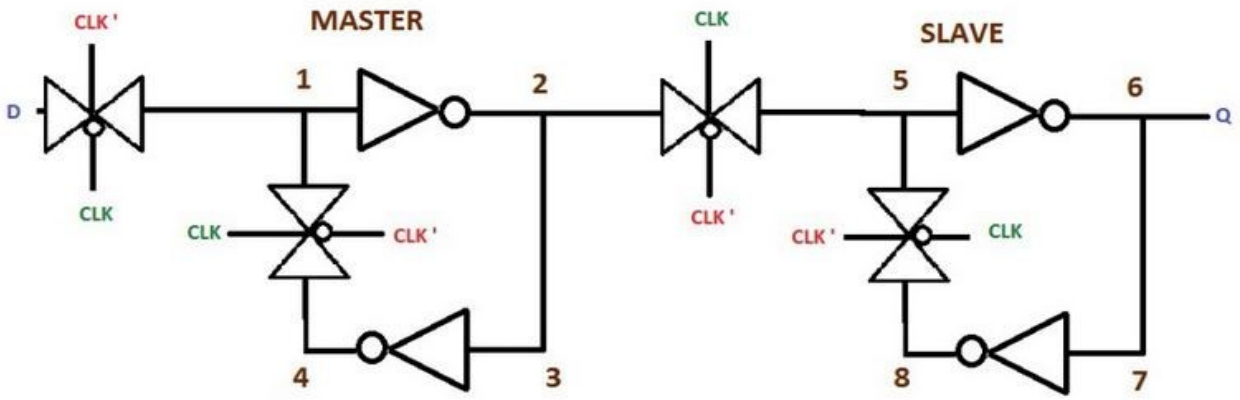
From Waveform editor, the OFF-Resistance = 3.055 GΩ

b. Transient analysis



D. D-Flip Flop

I. Operation



The edge-triggered flip flop is designed from two D-type level-triggered latches. Each Latch have 2 transmission gates and 2 inverters. Both latches are enabled with complementary clock signal: The second slave latch is controlled by the clock signal, while the master latch is enabled by the complemented clock.

The master latch is transparent while the clock signal is low, and the current value of the D input is propagated to the input of the slave latch. Now, the input transmission-gate of the slave latch is non-conducting. Therefore, the flip flop stores its current value.

On the rising edge of the input clock, the input transmission-gate of the master latch becomes non-conducting, while the feedback transmission-gate of the master latch becomes conducting. That is, the master latch stores its current value - the value it had immediately before the rising-edge of the clock signal. At the same time, the slave latch becomes transparent (its input transmission-gate is now conducting) and therefore outputs the value stored in the master latch. The new output value arrives at the Q output about three transistor delays (slave input t-gate, two inverter stages) after the rising edge of the clock signal.

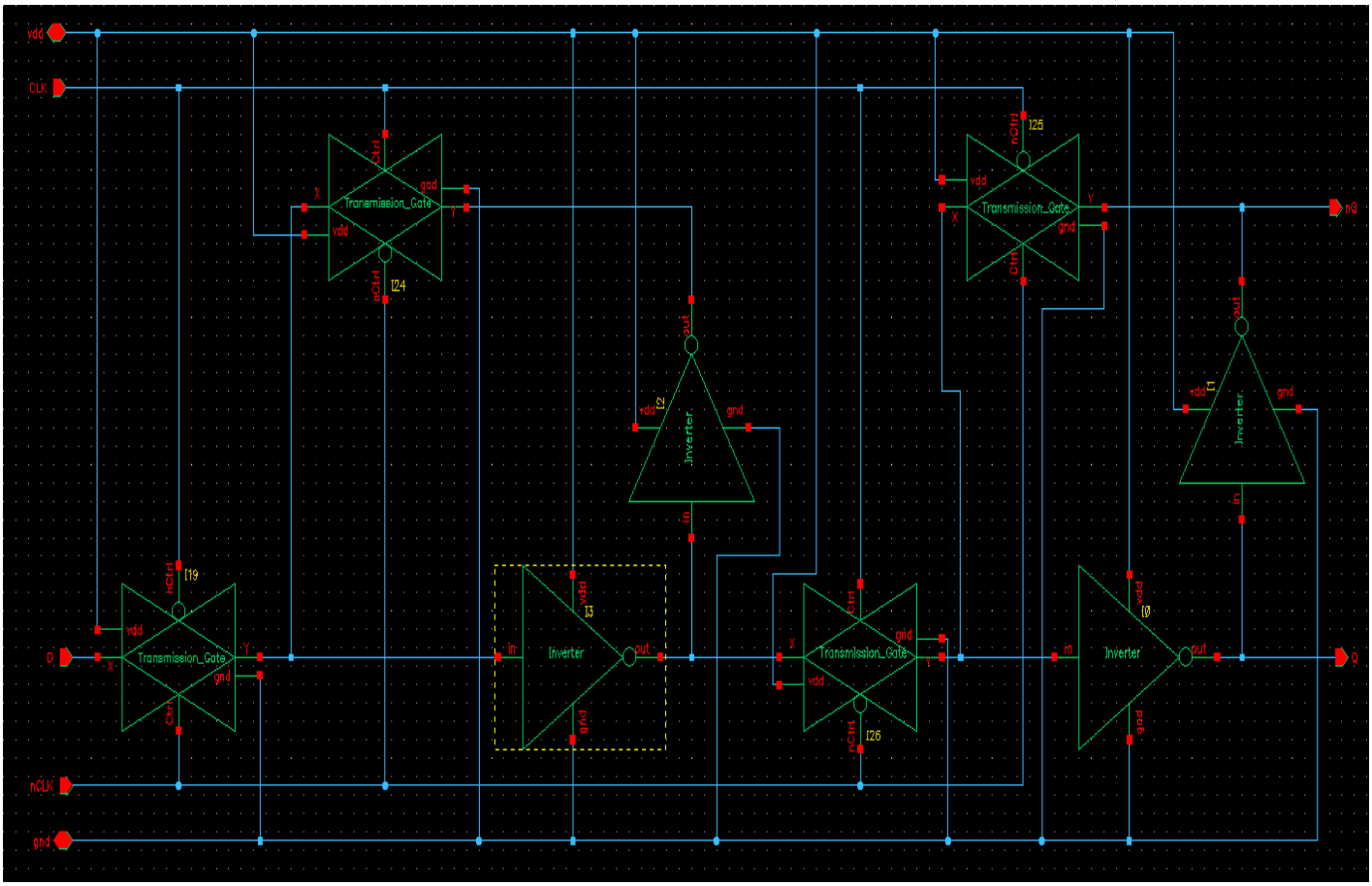
When the clock signal turns low again, the input transmission-gate of the slave latch becomes non-conducting, while the feedback transmission-gate becomes conducting i.e the slave latch keeps storing its current value, the value loaded during the preceding rising-edge of the clock signal into the master latch. Simultaneously, the master latch becomes transparent again and the D input value is propagated through the master latch onto the (now non-conducting) input transmission-gate of the slave latch.

Step 1 : Initially D =0. CLK = low. Path D-1-2-3-4 , now 4 = low.

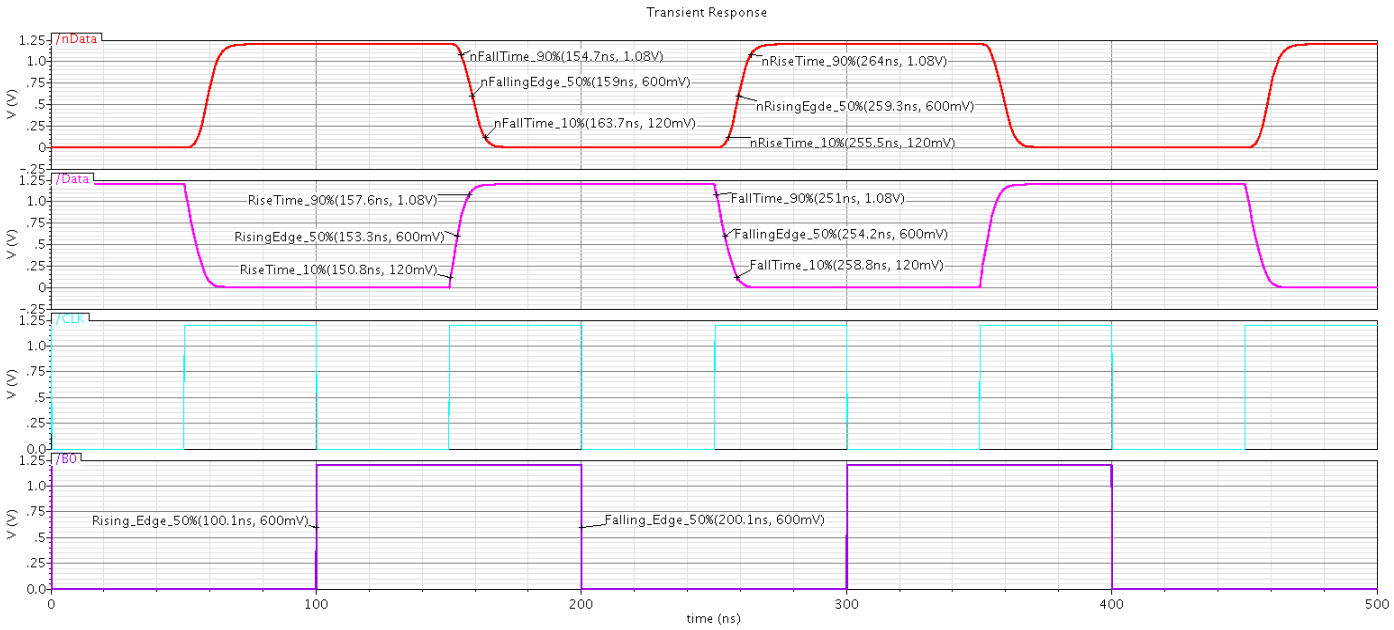
Step 2 : CLK = high, Slave latches to logic 1, i.e Q = 1. Path 1-2-3-4-1 and 2-5-6-7-8

Step 3 : CLK = low , Slave latches to D. Any change to D, is reflected in 4 and latches to Q in next positive edge of clock.

II. Schematic Design



II. Simulation (Transient analysis)



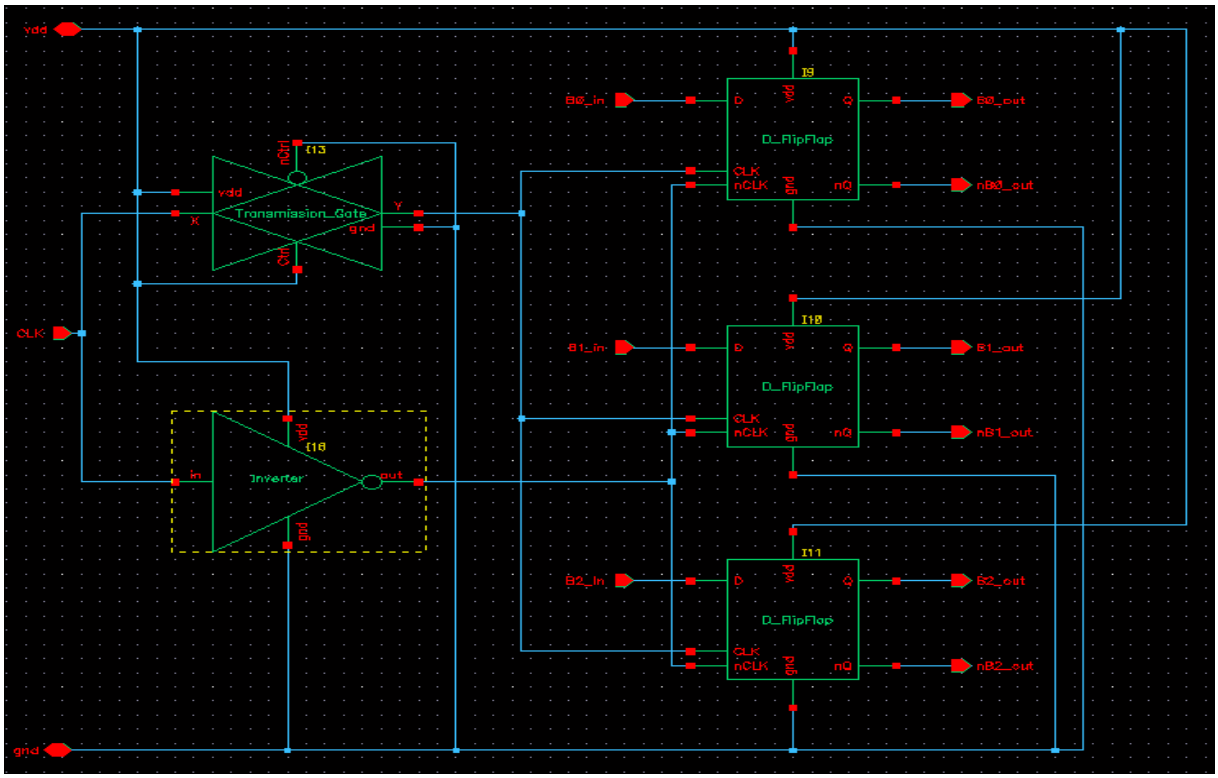
Data : Rise time = 6.8 ns , Fall time = 7.8 ns
Propagation Delay (Input Rising Edge to Output Rising Edge) = 53.2 ns
Propagation Delay (Input Falling Edge to Output Falling Edge) = 54.1 ns

nData: Rise time = 8.5 ns , Fall time = 9 ns
Propagation Delay (Input Rising Edge to Output Rising Edge) = 58.9 ns
Propagation Delay (Input Falling Edge to Output Falling Edge) = 59.2 ns

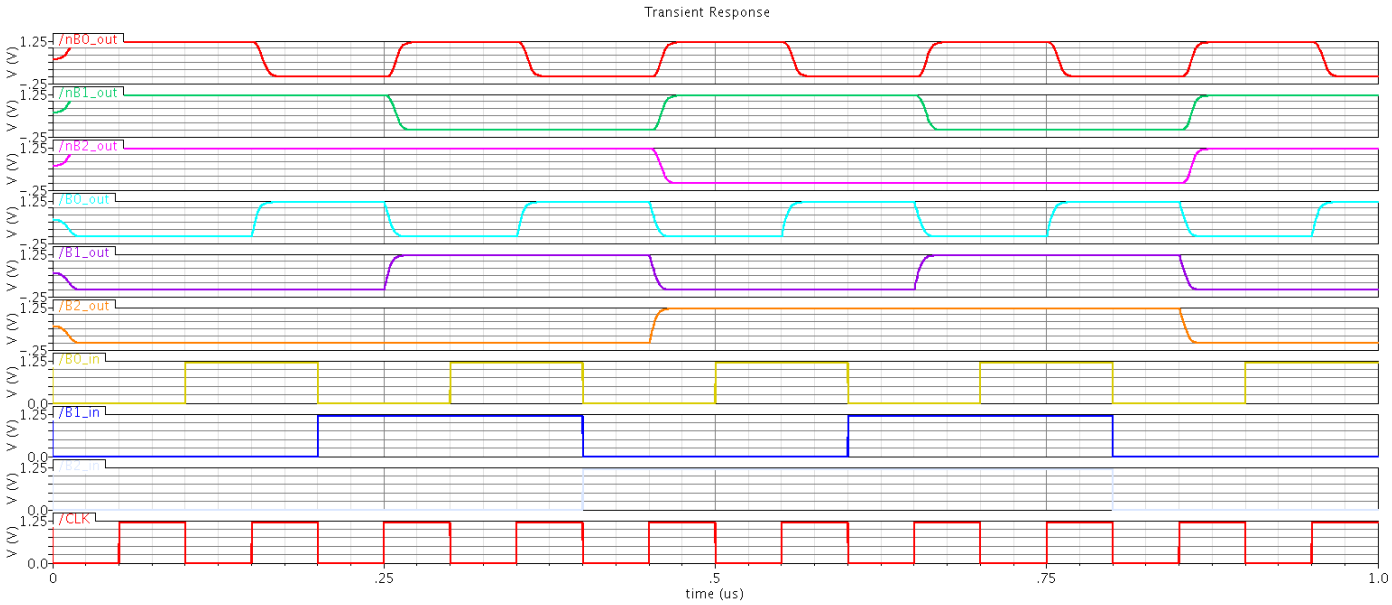
E. Control Signals Logic

I. Operation and Schematic Design

Control Logic block is realized as 3 to 6 Decoder, which takes 3 Input bits and buffers out those signals along with their complement signals. It has 3 D-Flip Flop in Parallel In Parallel Out fashion. A Transmission Gate is added to Clock Signal to compensate the delay caused by Inverter component.



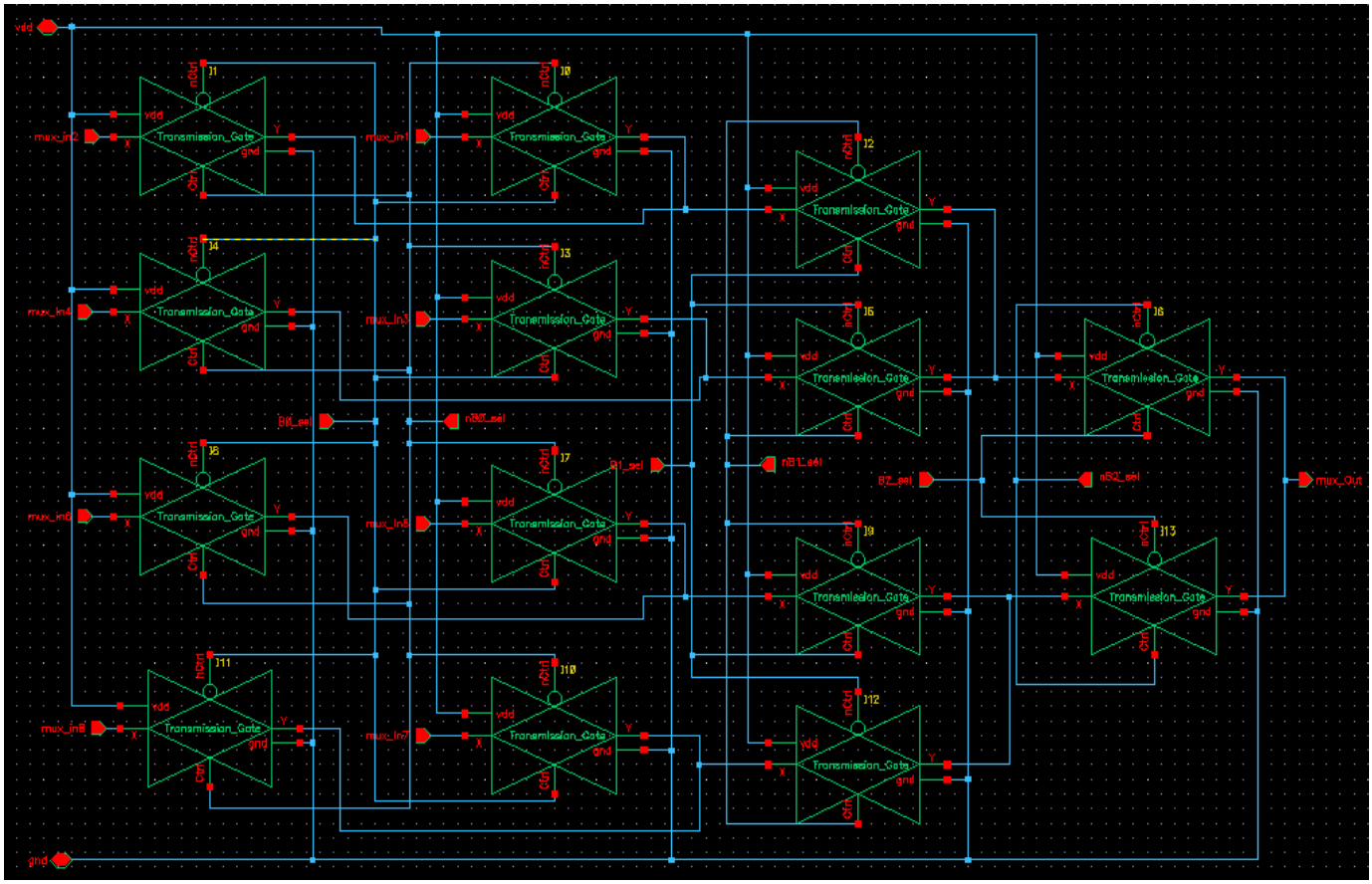
II. Simulation (Transient analysis)



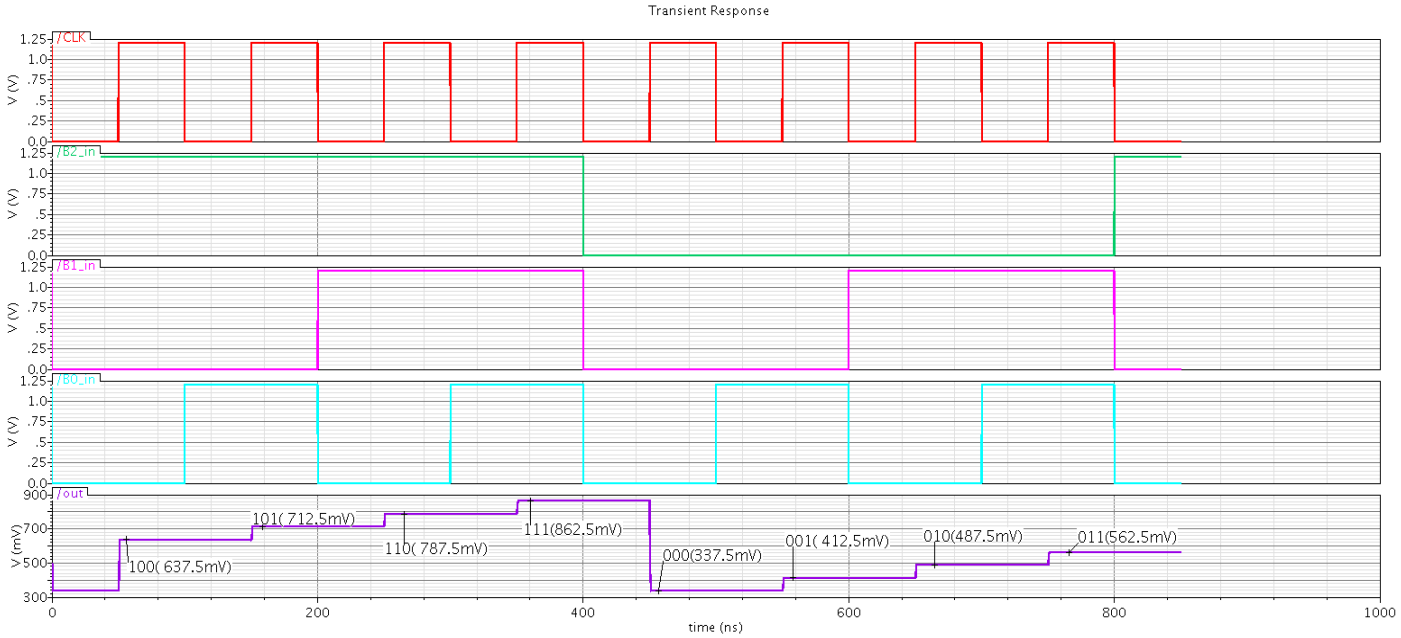
F. Analog Switch Multiplexer

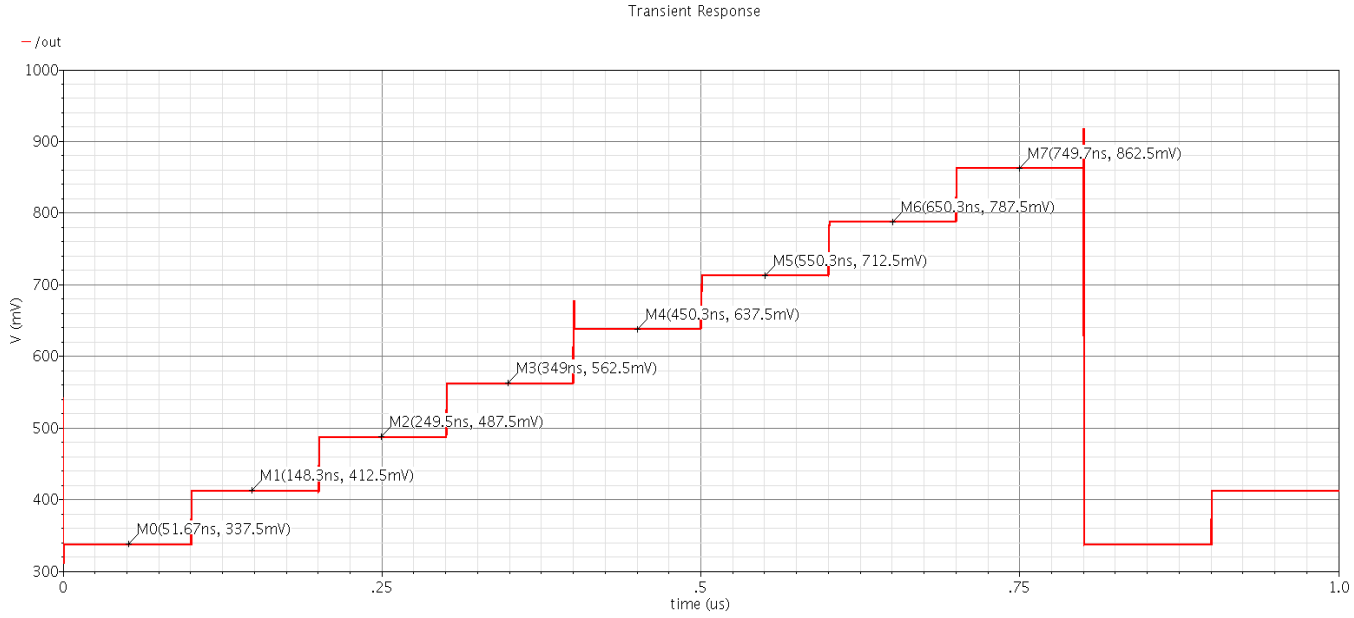
I. Schematic Design

Analog switch multiplexer here is a 8 : 1 MUX, to which corresponding voltage from Resistor String is applied as inputs and control signals from Control Logic Signal is applied a select signals. It is designed using 14 Transmission Gates, where 2 Transmissions gates together acts as 2 : 1 MUX. It has 1st Stage made up of 8 2:1 MUX's controlled by B0 and ~B0. The intermediate stage comprise of 4 2 : 1 MUX's controlled by B1 and ~B2. The last stage designed using 2 2 : 1 MUX's, which outputs a multiplexed signal.



II. Simulation (Transient analysis)





From the waveform editor, the voltage levels for different [B2 B1 B0] combinations are tabulated as :

(000) = 337.5mV, (001) = 412.5mV, (010) = 487.5mV, (011) = 562.5mV,

(100) = 637.5mV, (101) = 712.5mV, (110) = 787.5mV, (111) = 862.5mV.

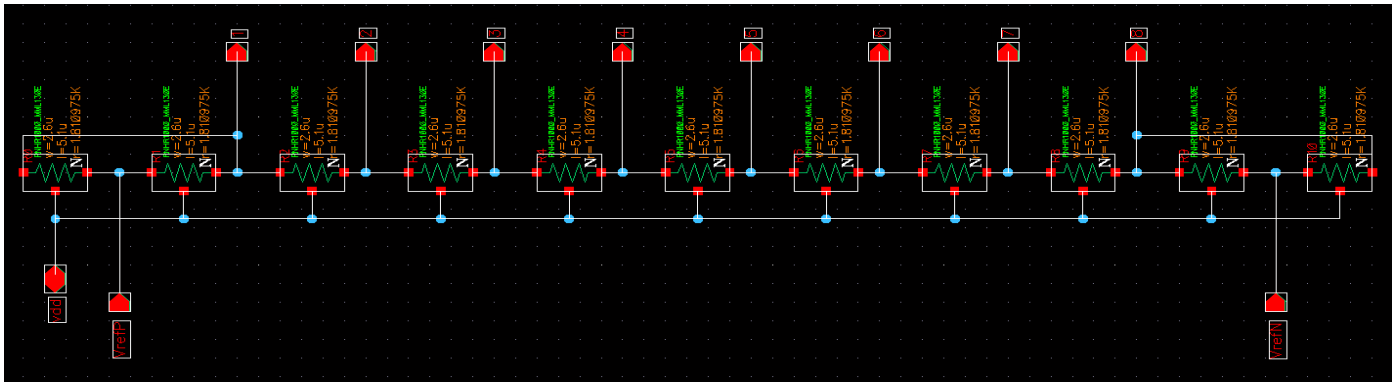
G. Resistor String Ladder

The design approach follows , determination of suitable R value for the DAC, based on which Width and Length of **RNHR1000_MML130E** resistor is decided. The "W" and "L" values determine the mismatch factor for the Resistor String. To carry out Mismatch Analysis, three different string layouts are designed and used for DAC simulation.

I. Linear Layout

R= 1.8109 KΩ
W= 2.6 um , L= 5.1 um
Mismatch Factor = 0.018

Schematic Design :



a. Without Mismatch

R1 = 1.8109 K, R2 = 1.8109 K, R3 = 1.8109 K, R4 = 1.8109 K, R5 = 1.8109 K, R6 = 1.8109 K,
R7 = 1.8109 K, R8 = 1.8109 K, R9 = 1.8109 K, R10 = 1.8109 K, R11 = 1.8109 K

b. Maximum Mismatch

R1 = 2.0972K, R2 = 2.0602K, R3 = 2.0979K, R4 = 2.0608K, R5 = 2.0986K, R6 = 2.0615K,
R7 = 2.0993K, R8 = 2.0622K, R9 = 2.0999K, R10 = 2.0628K, R11 = 2.1006K

c. Minimum Mismatch

R1 = 1.5574K, R2 = 1.5854K, R3 = 1.5569K, R4 = 1.5849K, R5 = 1.5564K, R6 = 1.5844K,
R7 = 1.5559K, R8 = 1.5839K, R9 = 1.5554K, R10 = 1.5833K, R11 = 1.5548K

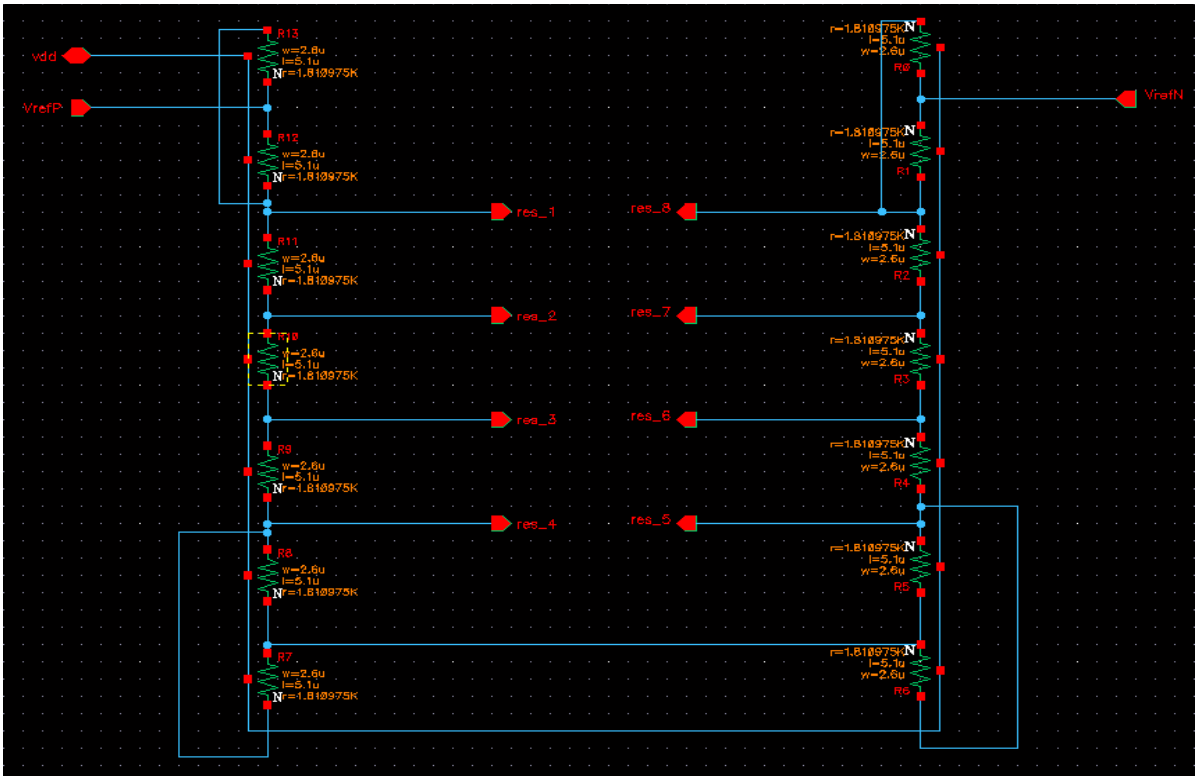
II. Folded Layout

R= 1.8109 KΩ

W= 2.6 um , L= 5.1 um

Mismatch Factor = 0.018

Schematic Design:



a. Without Mismatch

R1 = 1.8109 K, R2 = 1.8109 K, R3 = 1.8109 K, R4 = 1.8109 K, R5 = 1.8109 K, R6a = 1.8109 K, R6b = 1.8109 K, R6c = 1.8109 K, R6d = 1.8109 K,R7 = 1.8109 K, R8 = 1.8109 K, R9 = 1.8109 K, R10 = 1.8109 K, R11 = 1.8109 K

b. Maximum Mismatch

R1 = 2.1550K , R2 = 2.1162K , R3 = 2.1543K , R4 = 2.1155K , R5 = 2.1536K , R6a = 2.1148K , R6b = 2.1529K , R11 = 2.1550K , R10 = 2.1162K , R9 = 2.1543K , R8 = 2.1155K , R7 = 2.1536K , R6d = 2.1148K , R6c = 2.1529 K

c. Minimum Mismatch

R1 = 1.5559K , R2 = 1.5844K , R3 = 1.5564K , R4 = 1.5849K , R5 = 1.5569K , R6a = 1.5854K, R6b = 1.5574K , R11 = 1.5559K , R10 = 1.5844K , R9 = 1.5564K , R8 = 1.5849K , R7 = 1.5569K , R6d = 1.5854K , R6c = 1.5574 K

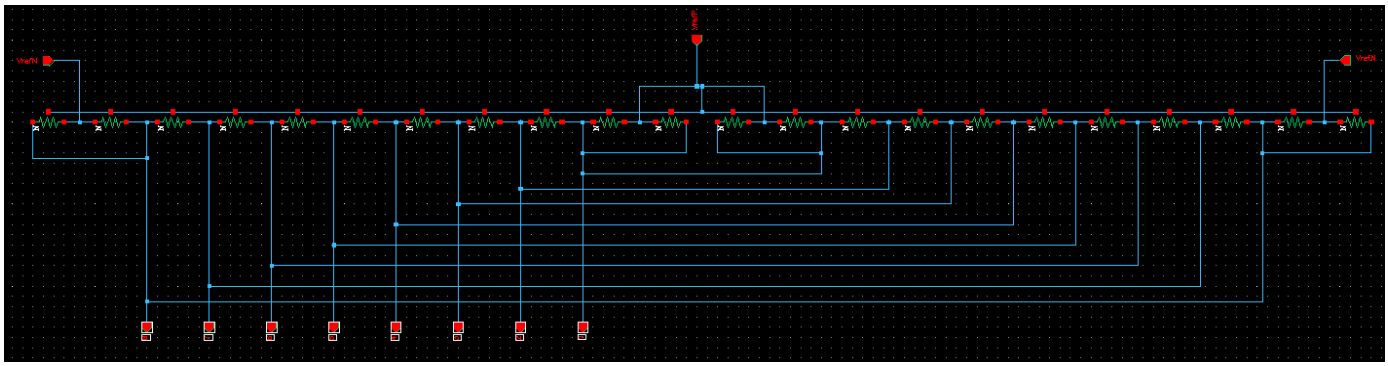
III. Inter-digitized Layout

R= 3.6219 KΩ

W= 1.32 um , L= 5.05 um

Mismatch Factor = 0.025

Schematic Design:



a. Without Mismatch

R1a =3.6219K, R2a =3.6219K, R3a =3.6219K, R4a =3.6219K, R5a =3.6219K, R6a =3.6219K, R7a =3.6219K, R8a =3.6219K, R9a =3.6219K, R10a =3.6219K, R11a =3.6219K, R11b =3.6219K, R10b =3.6219K, R9b =3.6219K, R8b =3.6219K, R7b =3.6219K, R6b =3.6219K, R5b =3.6219K, R4b =3.6219K, R3b =3.6219K, R2b =3.6219K, R1b =3.6219K

b. Maximum Mismatch

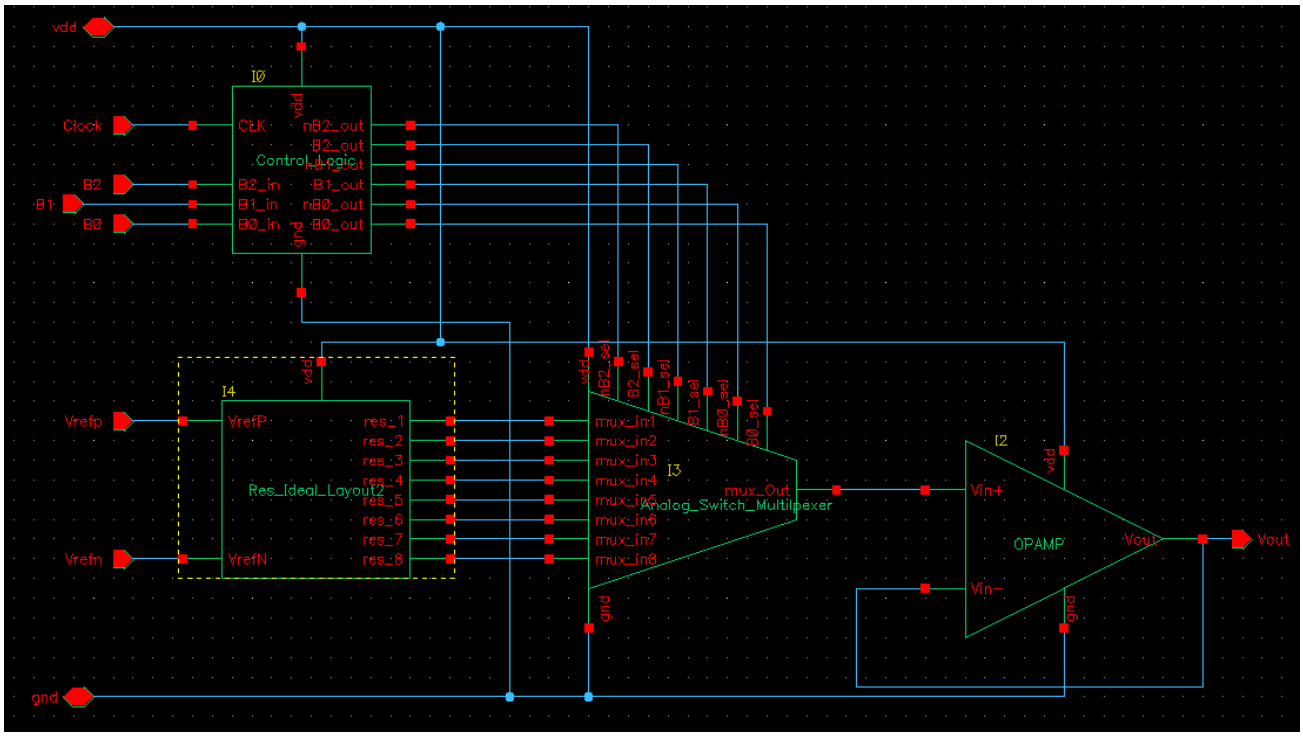
R1a =4.31006K, R2a =4.20231K, R3a =4.30737K, R4a =4.19968K, R5a =4.30467K, R6a =4.19705K, R7a =4.30198K, R8a =4.19443K, R9a =4.29929K, R10a =4.19181K, R11a =4.29661K, R11b =4.18919K, R10b =4.29392K, R9b =4.18657K, R8b =4.29124K, R7b =4.18396K, R6b =4.28856K, R5b =4.18134K, R4b =4.28587K, R3b =4.17873K, R2b =4.28319K, R1b =4.17611K

c. Minimum Mismatch

R1a =3.11483K, R2a =3.19270K, R3a =3.11289K, R4a =3.19071K, R5a =3.11094K, R6a =3.18871K, R7a =3.10899K, R8a =3.18672K, R9a =3.10705K, R10a =3.18473K, R11a =3.10511K, R11a =3.18274K, R10a =3.10317K, R9a =3.18075K, R8a =3.10123K, R7a =3.17876K, R6a =3.09929K, R5a =3.17677K, R4a =3.09735K, R3a =3.17479K, R2a =3.09542K, R1a =3.17280K

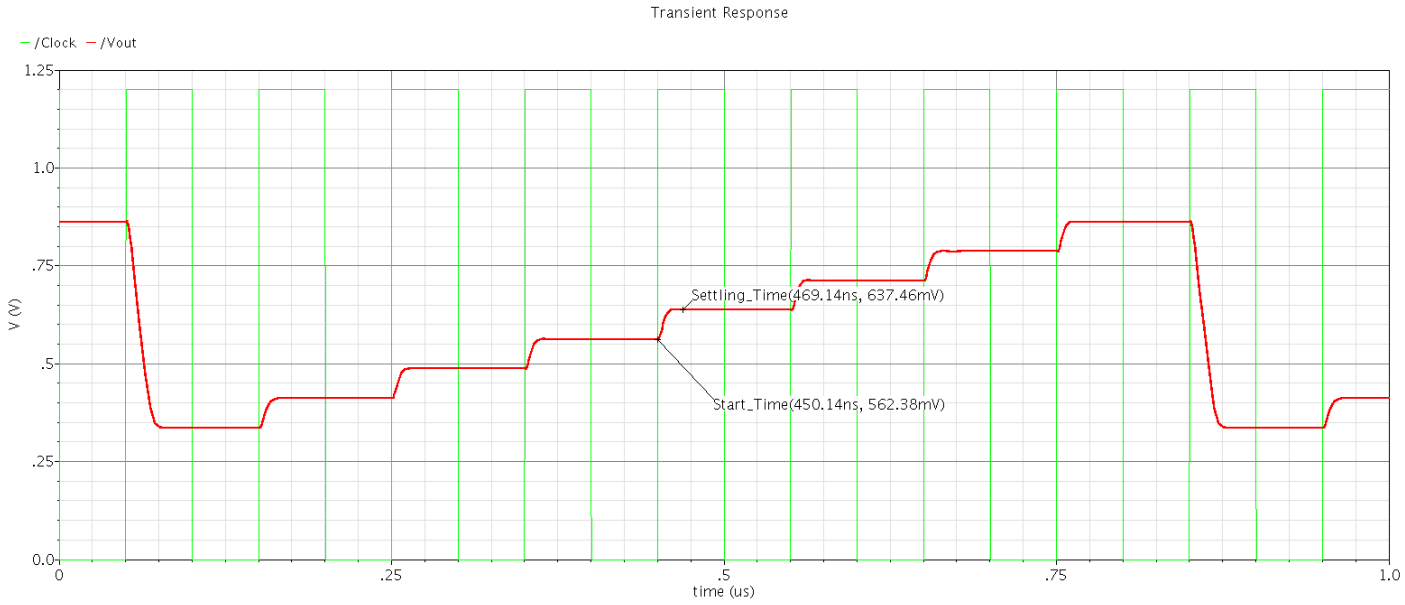
H. 3-Bit Resistor String DAC

I. Schematic Design



II. Simulation (Transient analysis)

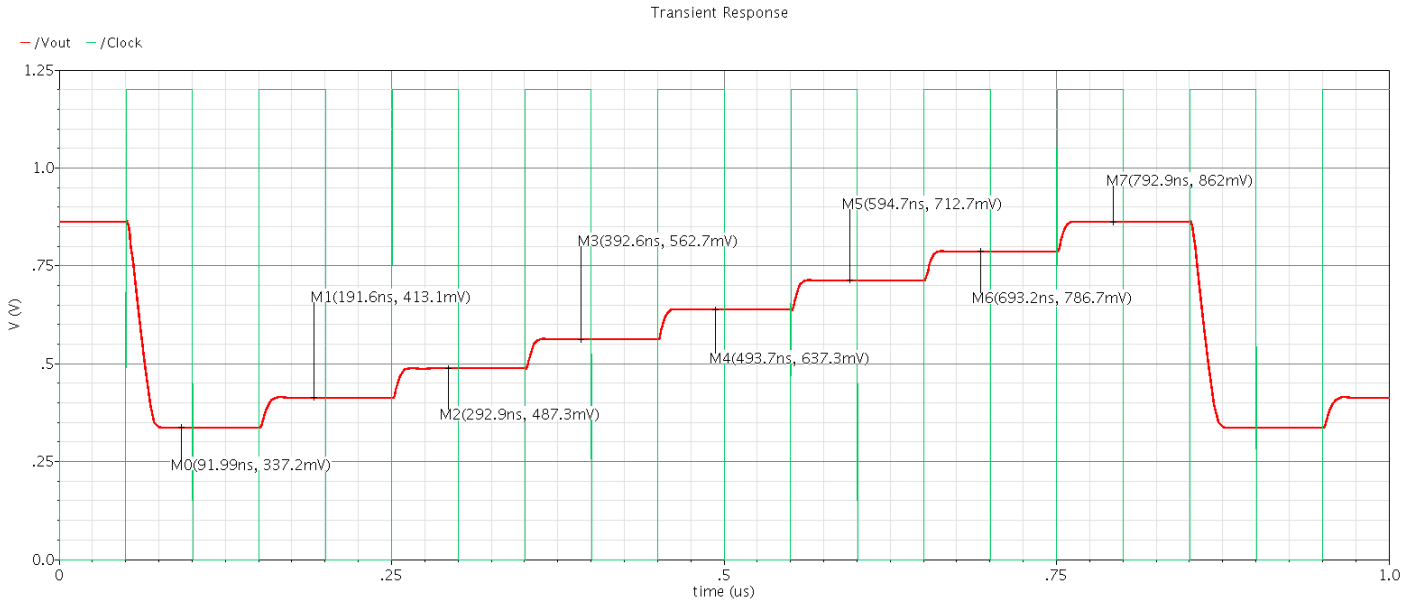
a. Without Mismatch



(000) = 337.232 mV, (001) = 412.662 mV, (010) = 487.684 mV, (011) = 562.566 mV,

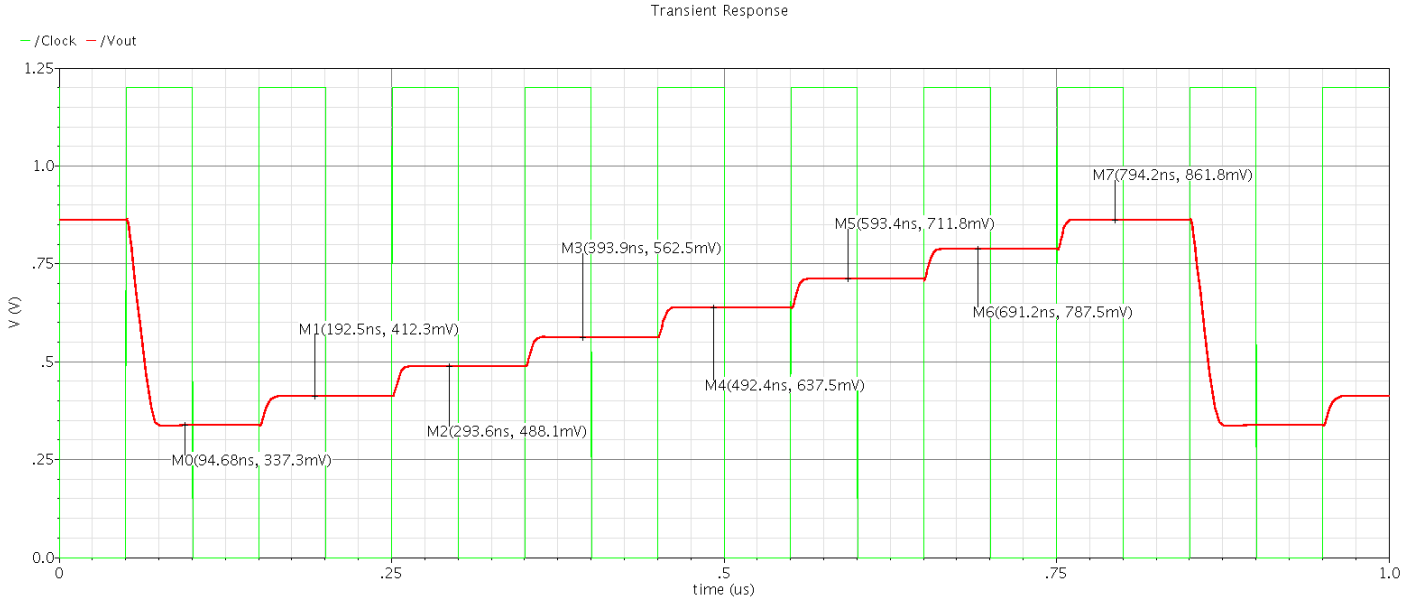
(100) = 637.421 mV, (101) = 712.26 mV, (110) = 787.083 mV, (111) = 861.883 mV.

b. Maximum Mismatch(Res_Max)



(000) = 337.163 mV, (001) = 413.106 mV, (010) = 487.289 mV, (011) = 562.673 mV,
(100) = 637.314 mV, (101) = 712.655 mV, (110) = 786.642 mV, (111) = 861.951 mV.

c. Minimum Mismatch(Res_Min)



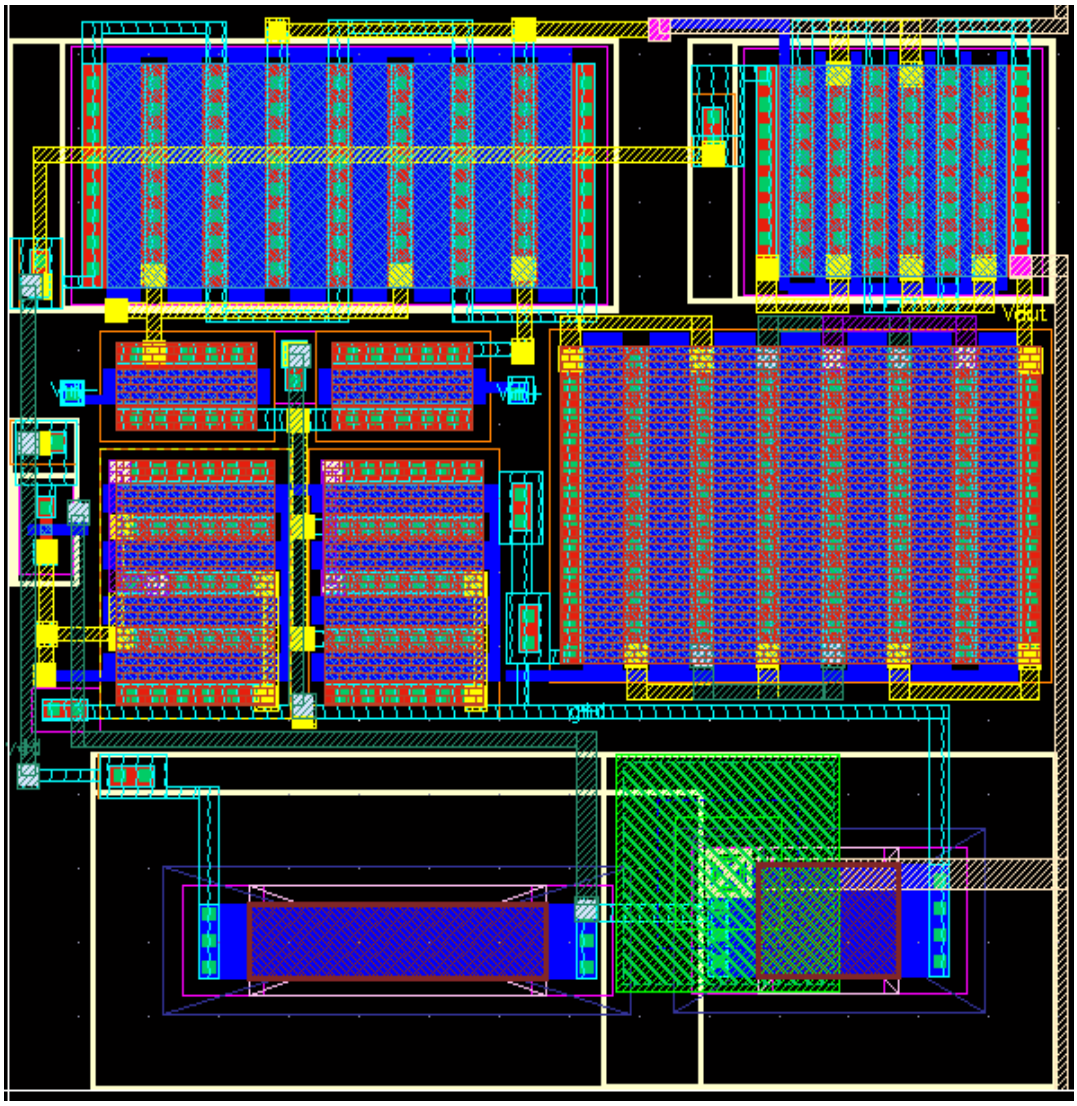
(000) = 337.337 mV, (001) = 412.27 mV, (010) = 488.144 mV, (011) = 562.5mV,

(100) = 637.487 mV, (101) = 711.8 mV, (110) = 787.474 mV, (111) = 861.779 mV.

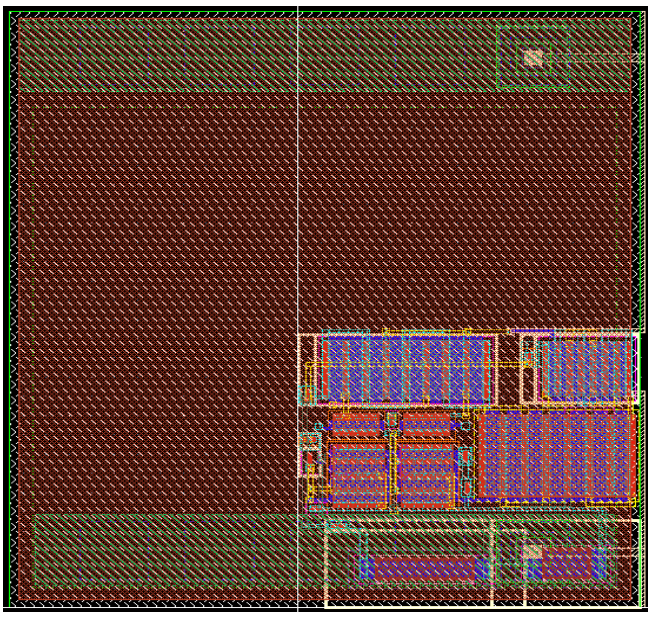
4. Layout-based Design and Post-Layout Simulation

A. Two Stage CMOS Opamp Buffer

I. Layout Design without MIMCAP



II. Layout Design with MIMCAP



III. Post Layout Simulation

a. ICMR

The resulting wave form is similar to the schematic-based waveform.

ICMR Vin(min) = 311.9mV , ICMR Vin(max) = 895.7 mV

b. Output Voltage Swing and Power Dissipation

The resulting wave form is similar to the schematic-based waveform.

Output Voltage swing = 0.212 V – 0.980 V

Power Dissipation = 0.393 mW

c. DC Gain, Gain Bandwidth and Phase Margin

The resulting wave form is similar to the schematic-based waveform.

DC Gain , Av = 51.99 dB

Gain Band Width, GBW = 36.34 MHz

Phase Margin = 69.4°

d. Slew Rate

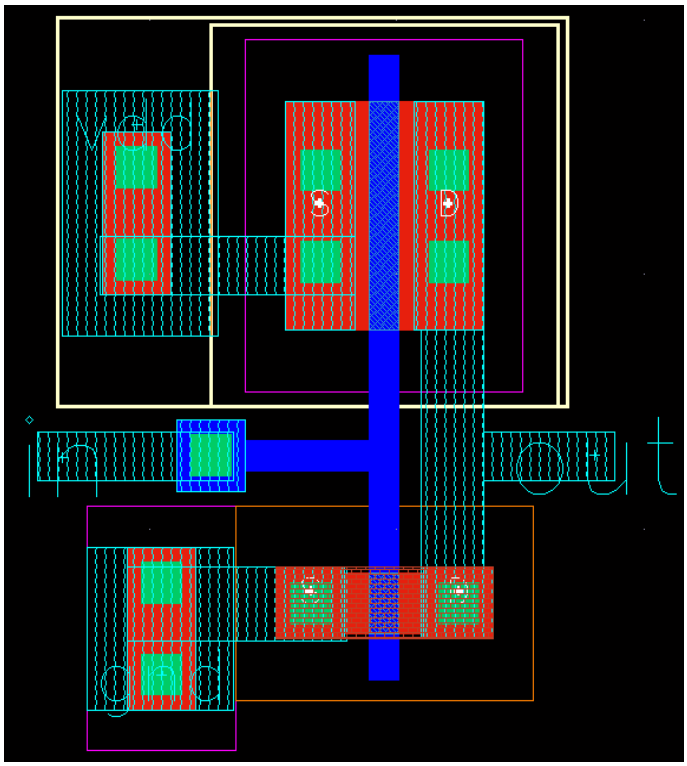
The resulting wave form is similar to the schematic-based waveform.

Positive-Slope Slew Rate, Slew Rate (+ve) = 32.62 V/us

Negative-Slope Slew Rate, Slew Rate (-ve) = - 30 V/us

B. Inverter

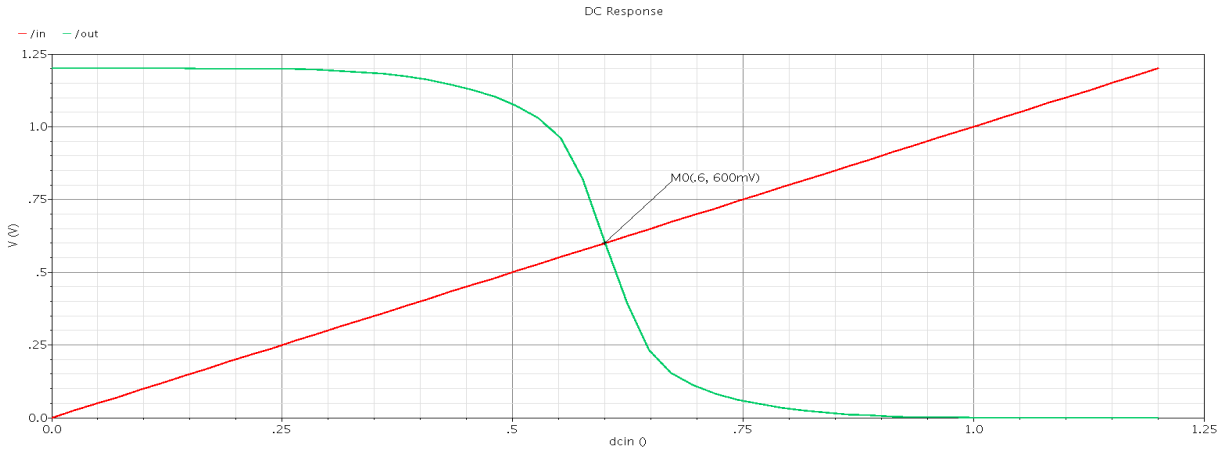
I. Layout Design



II. Post-Layout Simulation

a. DC analysis

The simulation results show that the designed Inverter is symmetric in nature. For Vin = 600 mV, Vout is 600 mV.

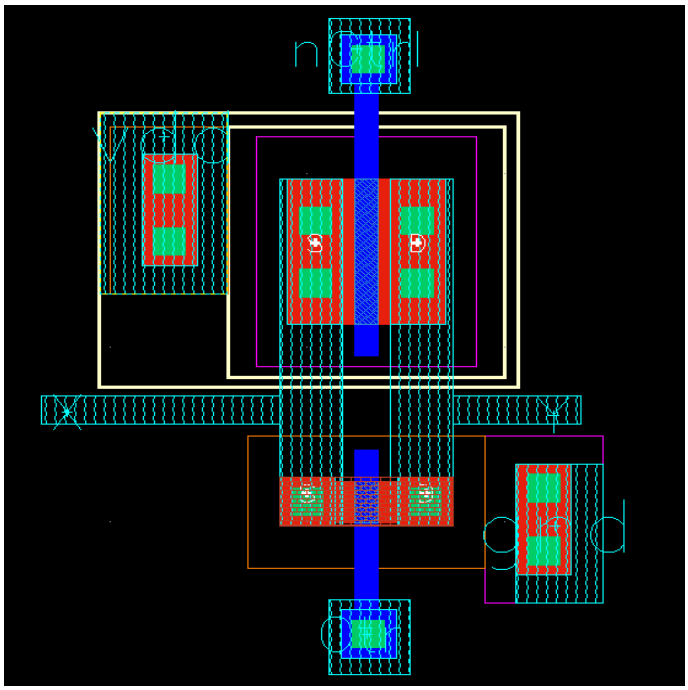


b. Transient Analysis

The resulting wave form is similar to the schematic-based waveform.

C. Transmission Gate

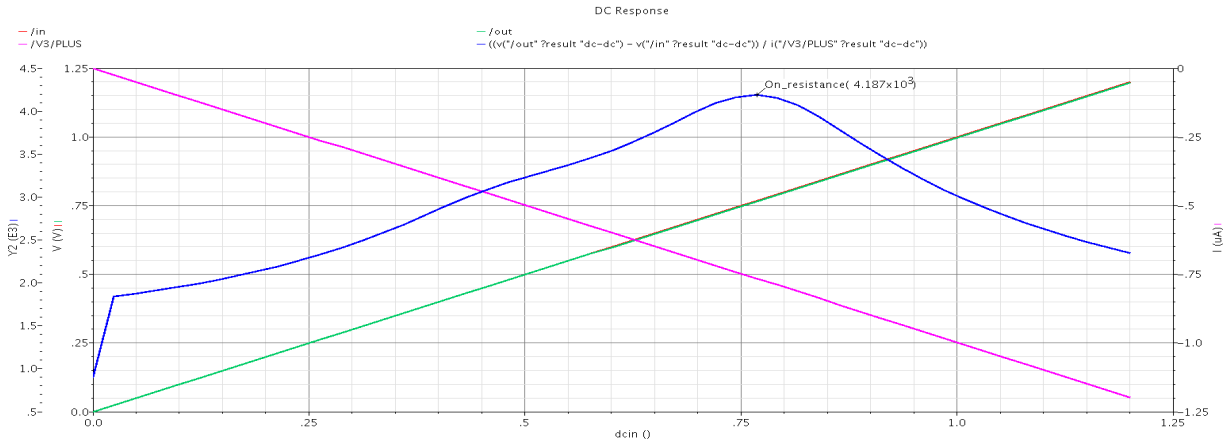
I. Layout Design

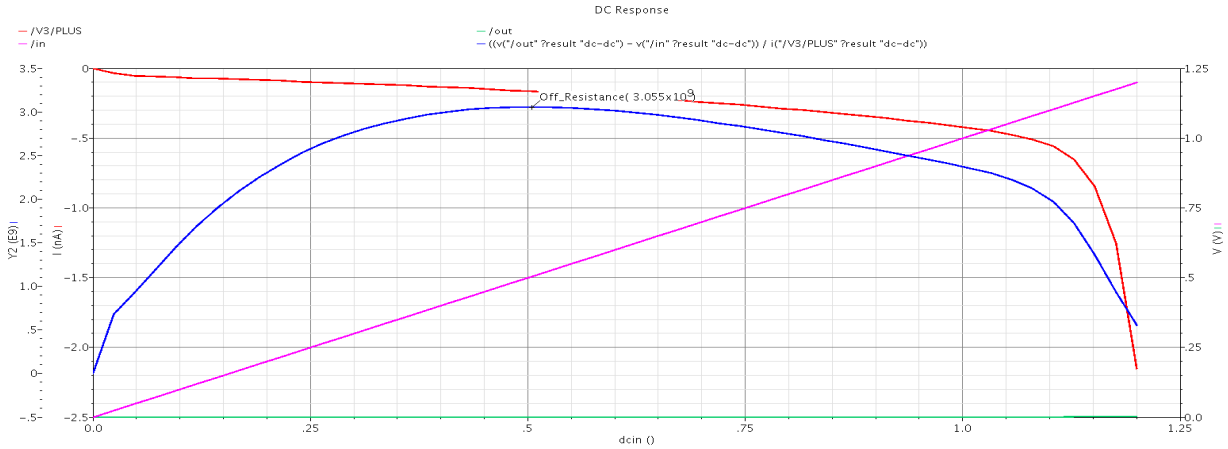


II. Post-Layout Simulation

a. On-off resistance

Ron = 4.178 KΩ , Roff = 3.055 GΩ



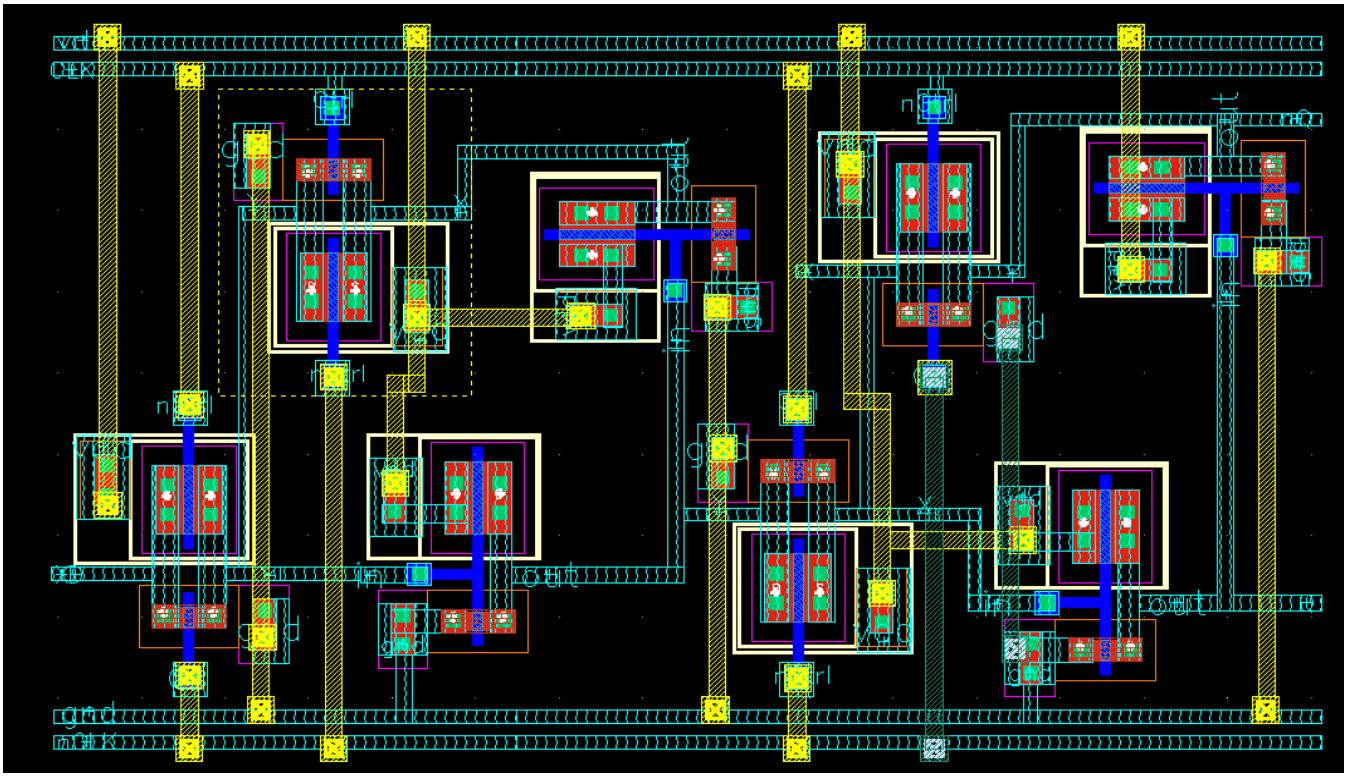


b. Transient analysis

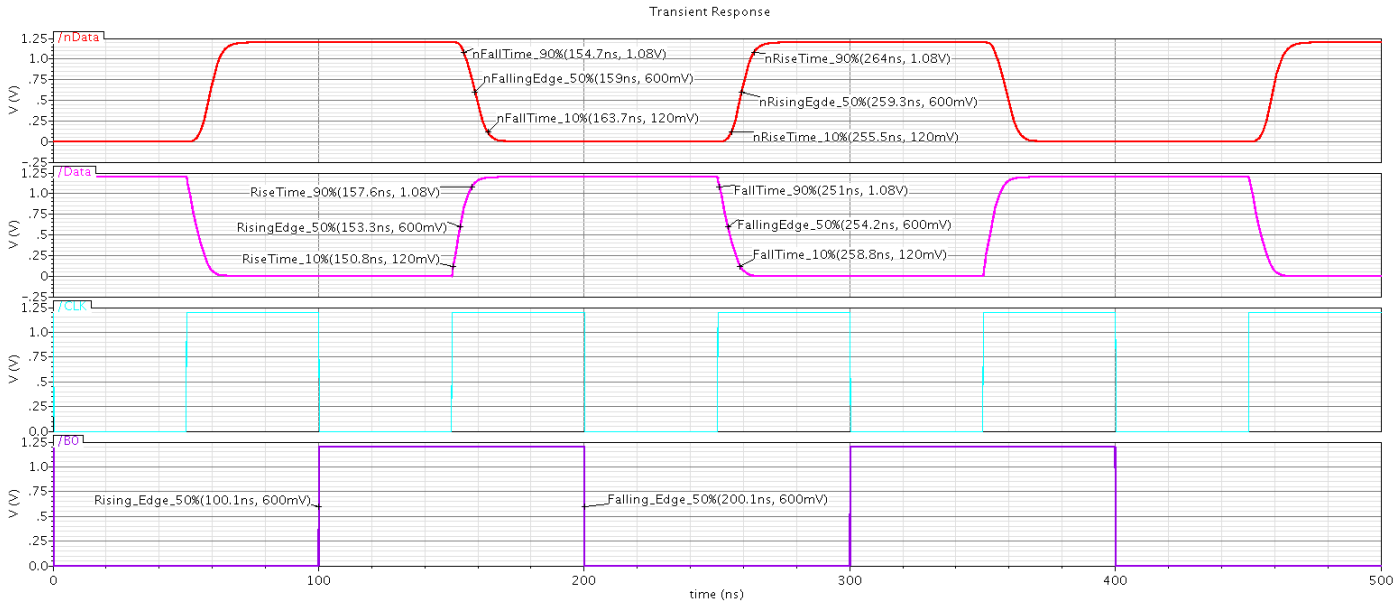
The resulting wave form is similar to the schematic-based waveform.

D. D-Flip Flop

I. Layout Design

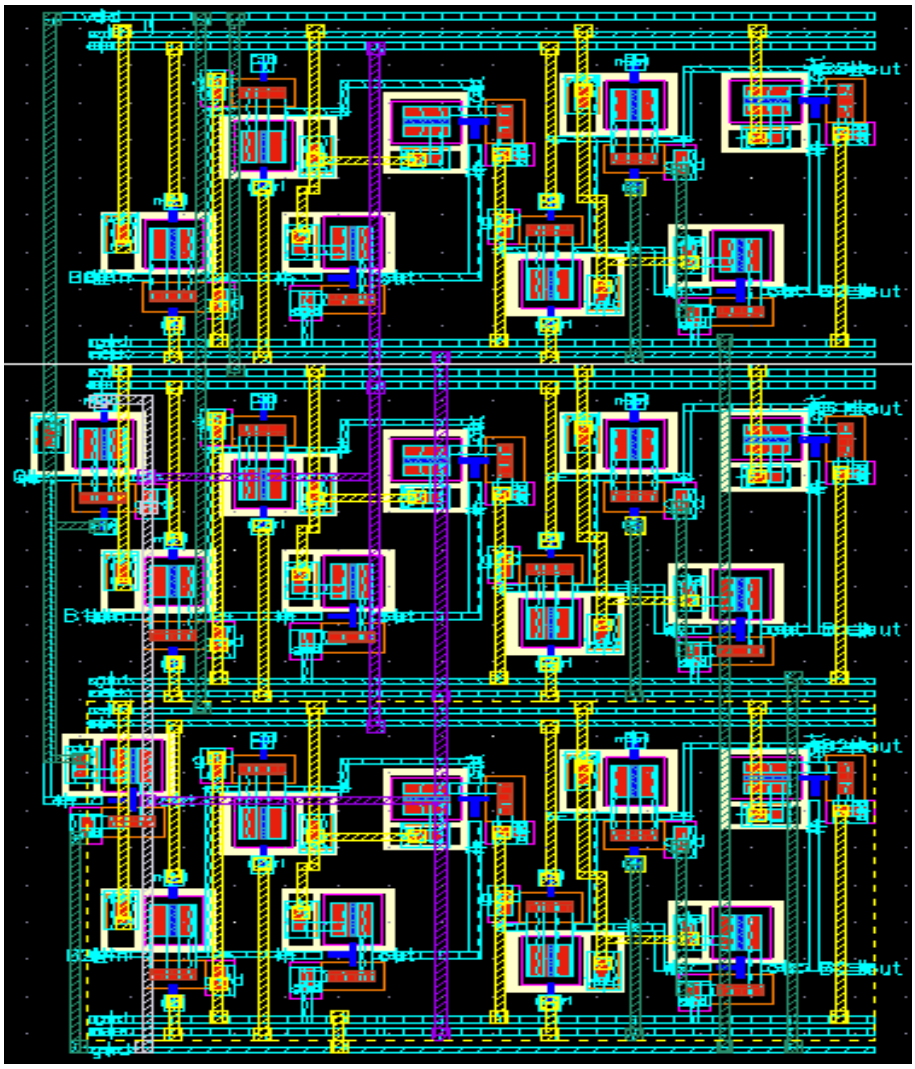


II. Post-Layout Simulation (Transient analysis)



E. Control Signals Logic

I. Layout Design

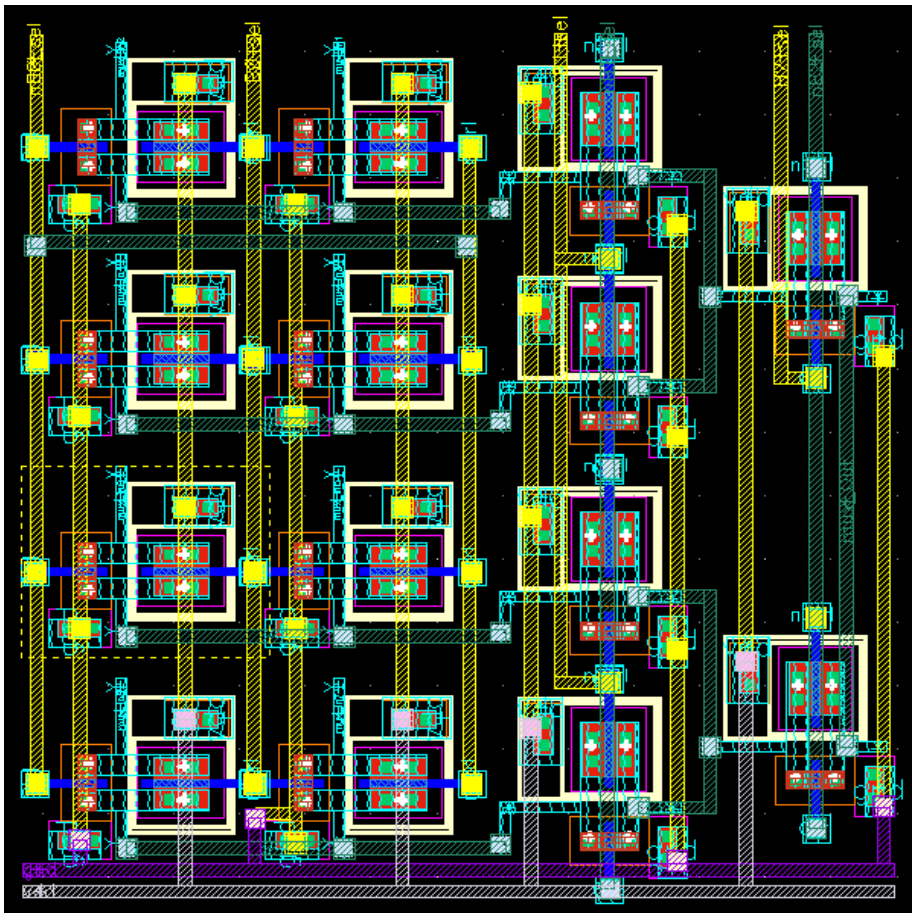


II. Post-Layout Simulation (Transient analysis)

The resulting wave form is similar to the schematic-based waveform.

F. Analog Switch Multiplexer

I. Layout Design



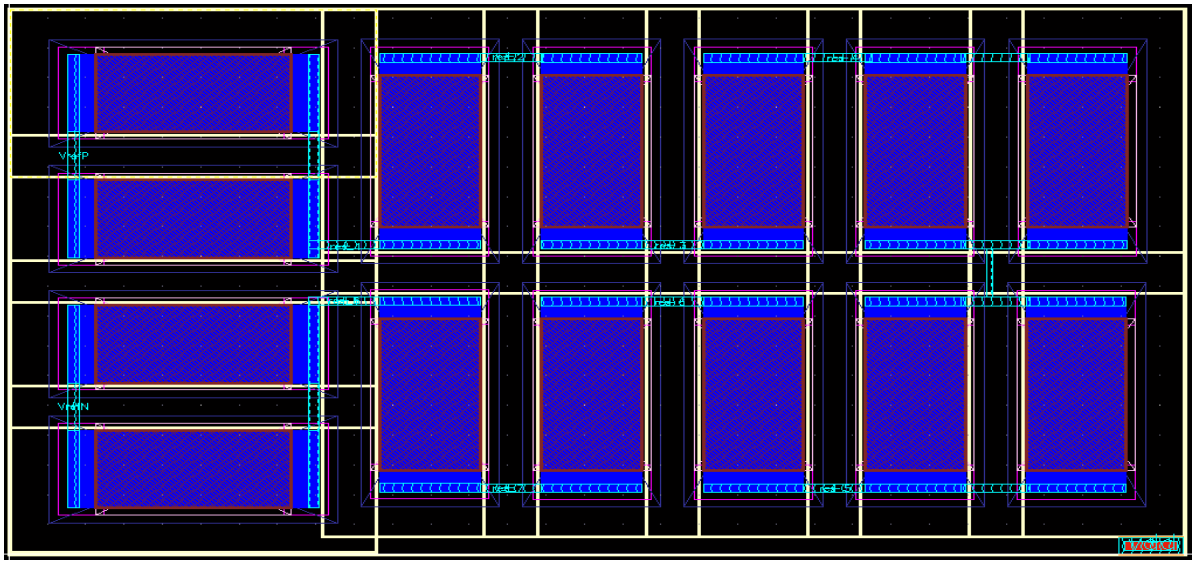
II. Post-Layout Simulation (Transient analysis)

The resulting wave form is similar to the schematic-based waveform.

G. Resistor String Ladder

Folded Layout is chosen for Layout-based design, since it is optimum choice for trade-off between INL, DNL errors , low area and low power.

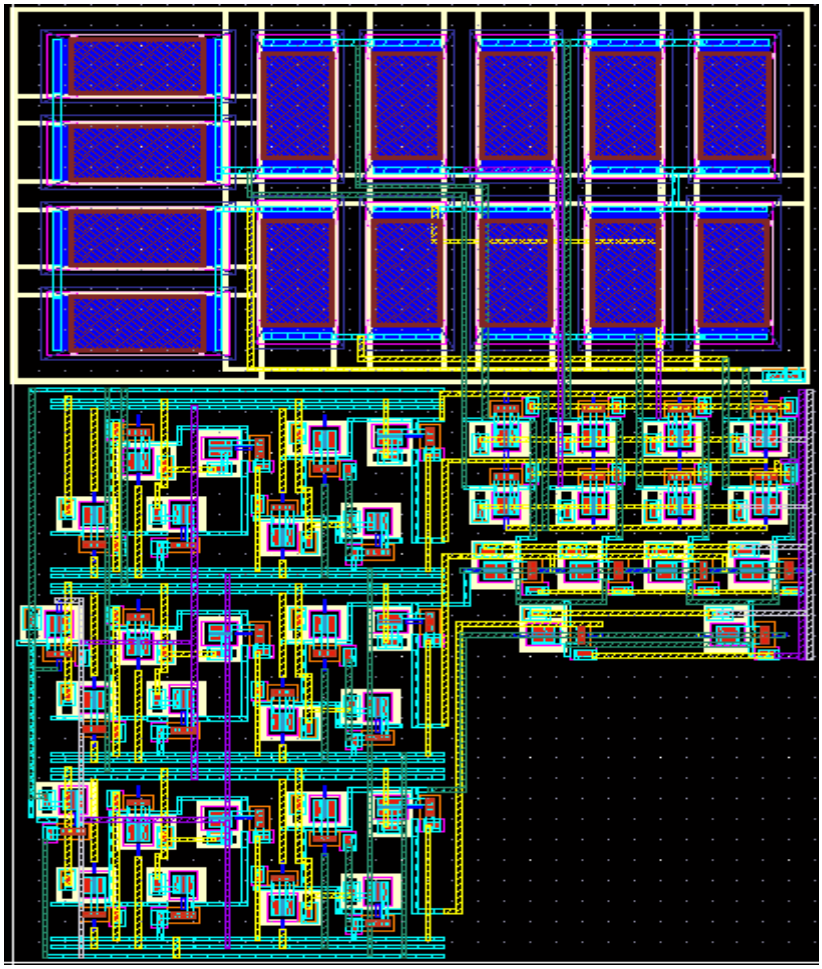
I. Folded Layout Design



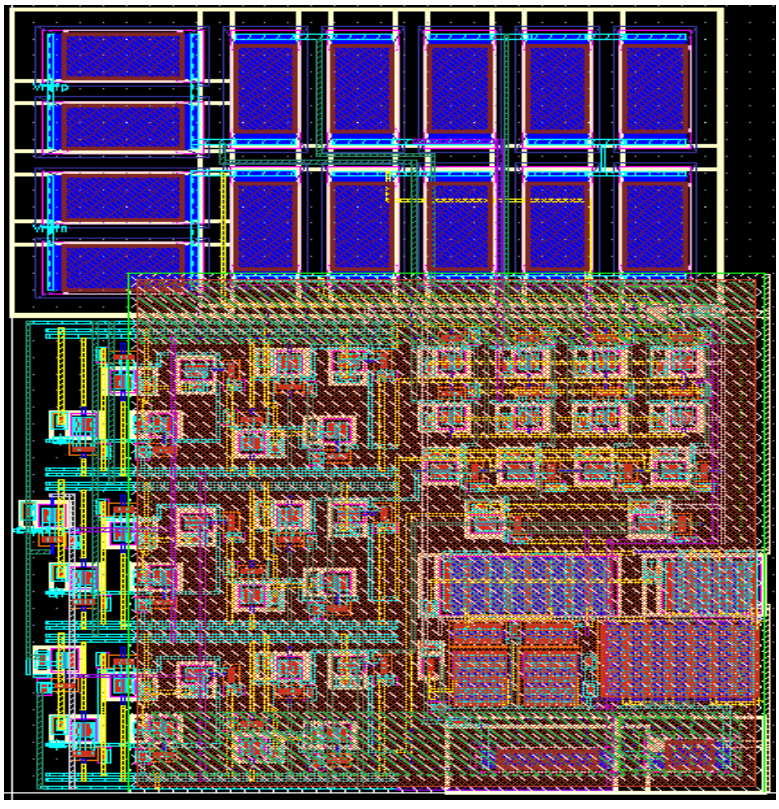
H. 3 Bit Resistor String DAC

I. Layout Design

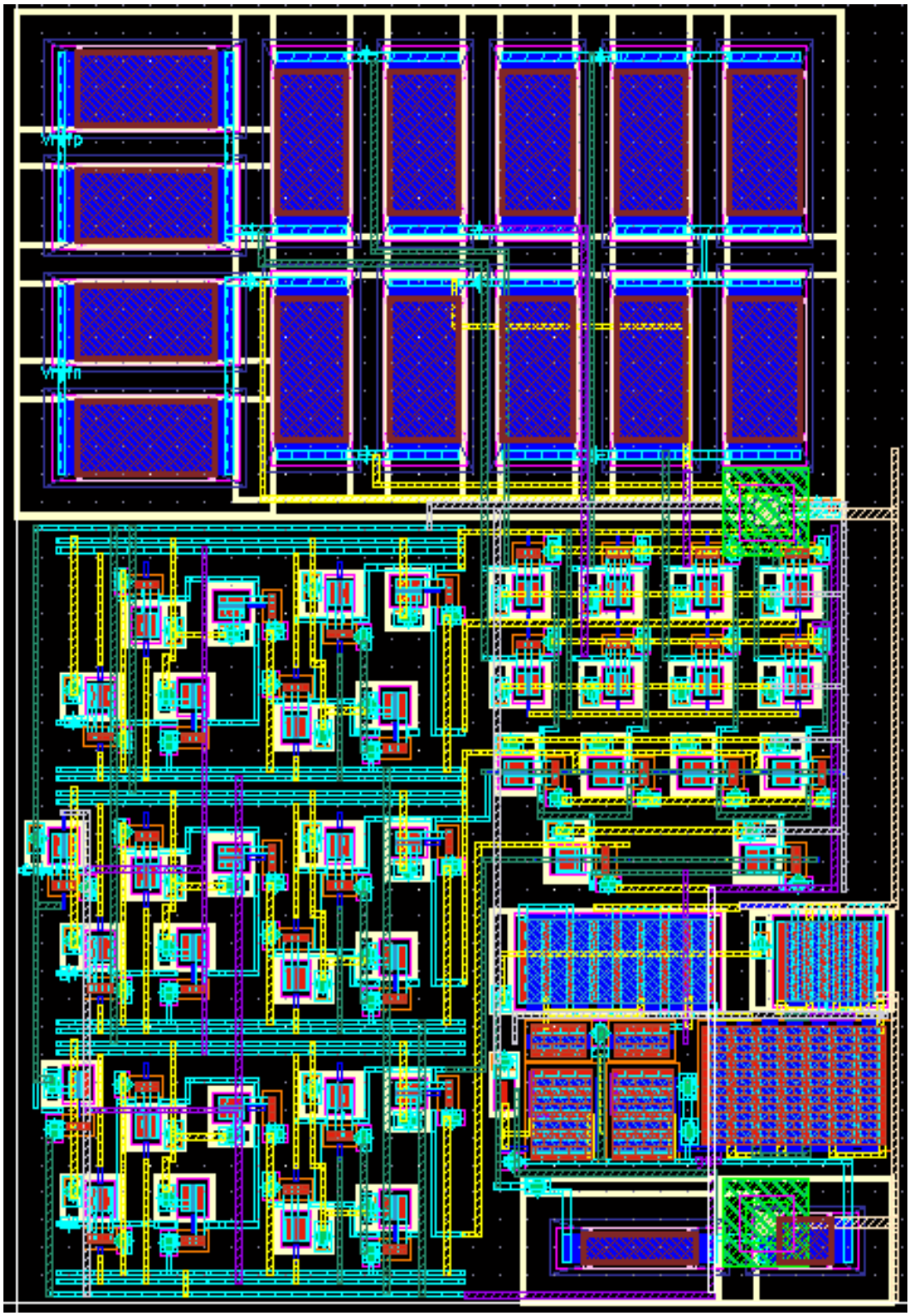
a. Control Logic, Switch Multiplexer and Resistor String



b. DAC with MIMCAPS_MML130E



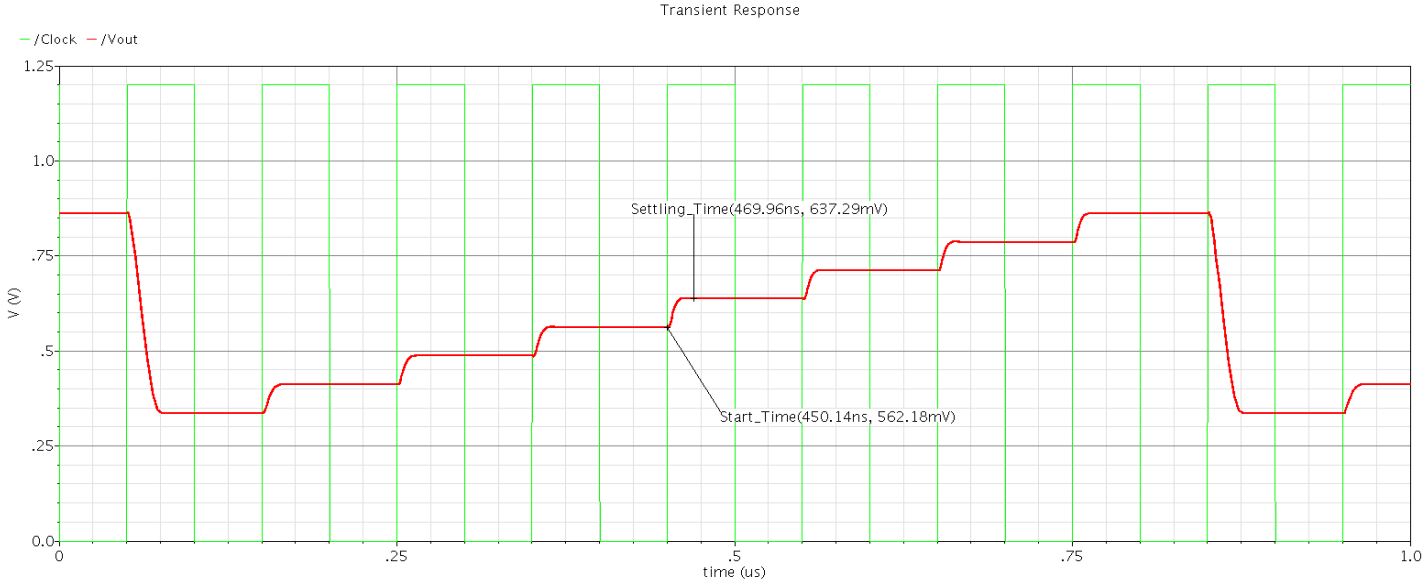
c. DAC without MIMCAPS_MML130E



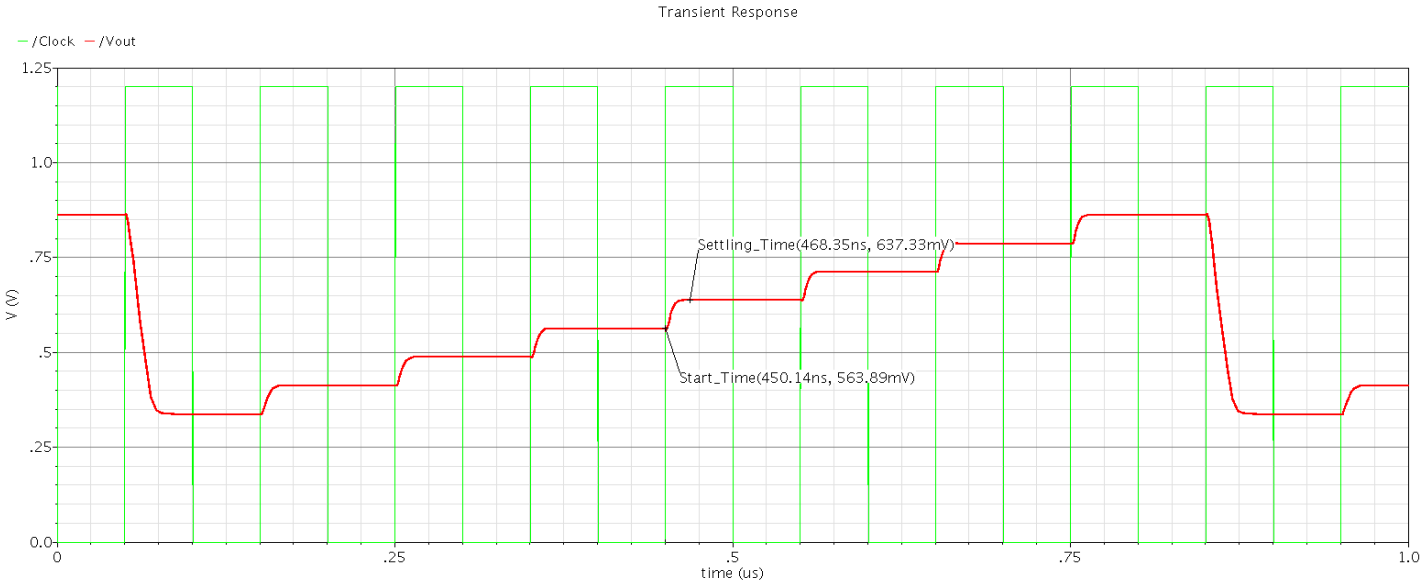
Total Area = 32.80 um x 46.90 um

II. Simulation (Transient analysis)

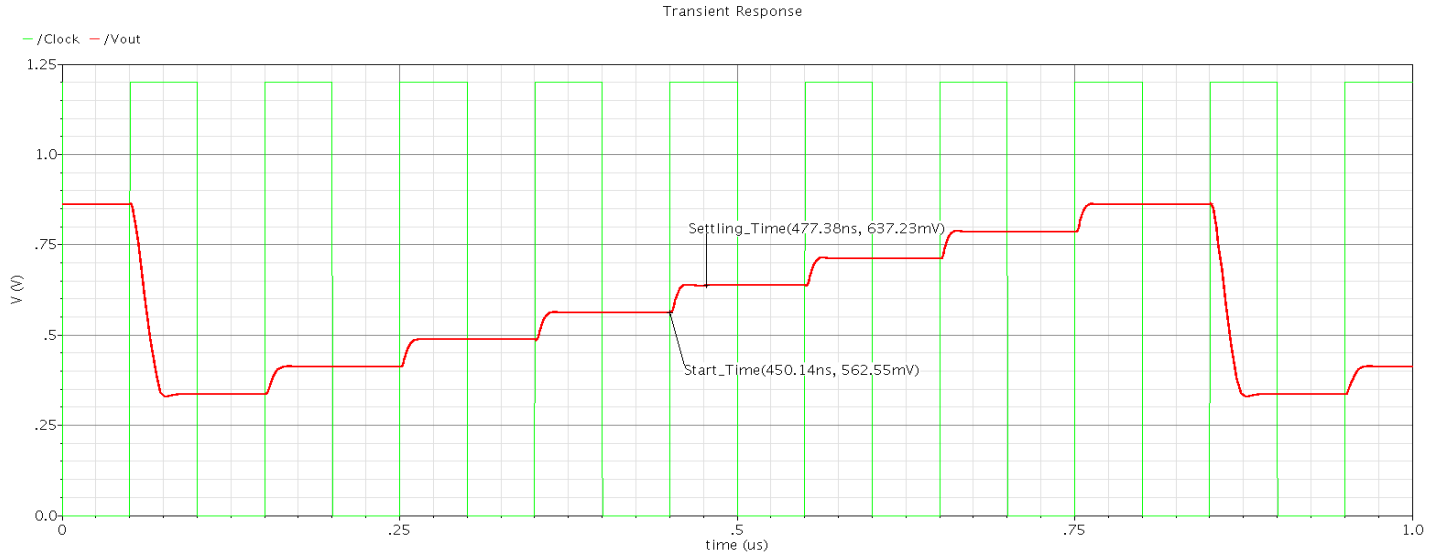
a. With Cload = 1.25 pF



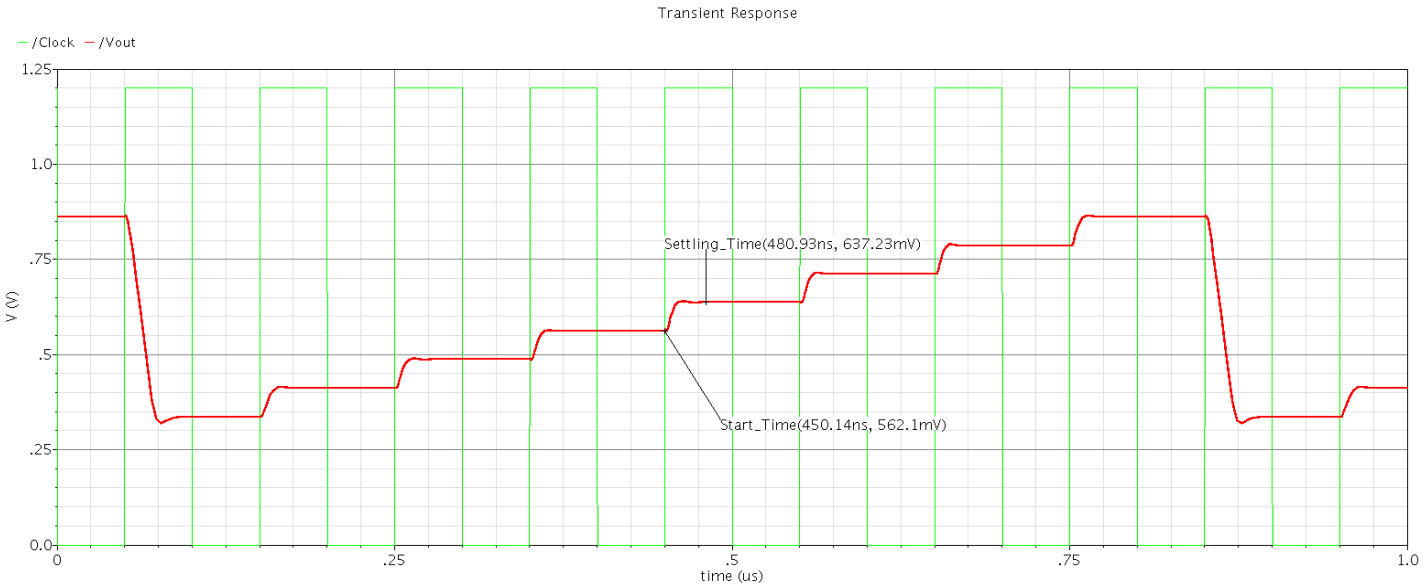
b. With Cload = 1 pF



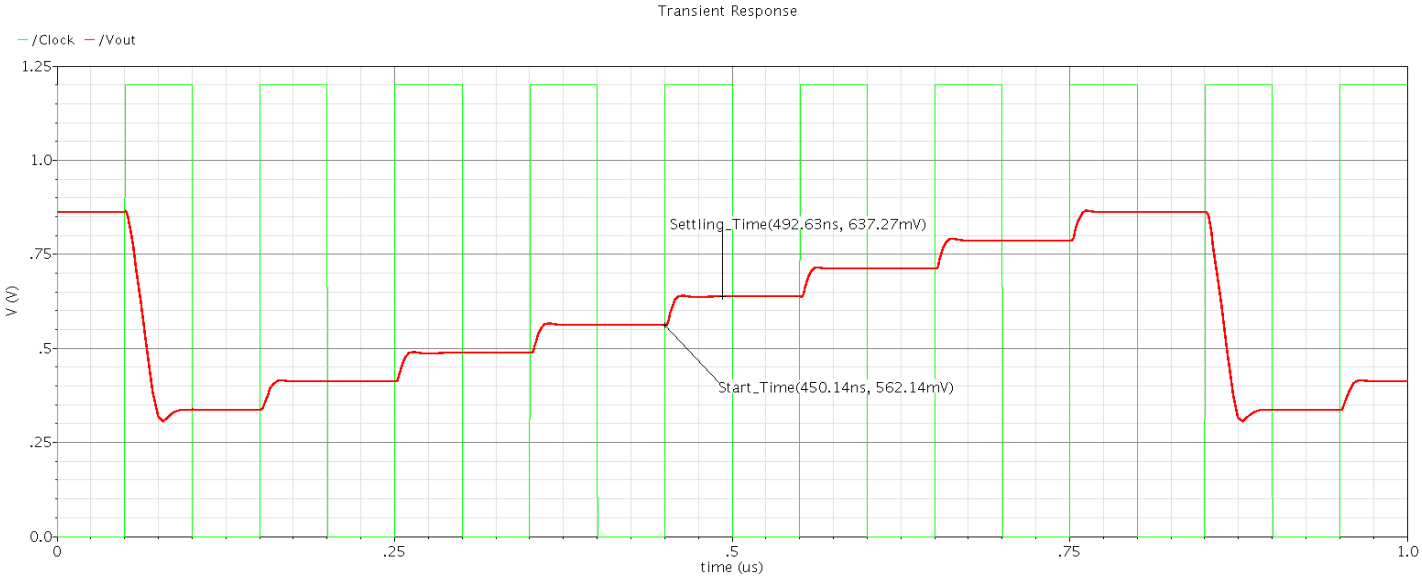
c. With Cload = 1.5 pF



d. With Cload = 1.75 pF



e . With Cload = 2 pF



The settling time for different Cload is calculated when Vout reaches its final value. A **5% error band** or tolerance band is considered for the final value. The DAC is designed for Cload = 1.25 pF, for which the Step-response is **maximally flat** with very **less ringing** effect. The step voltages are :

(000) = 337.079 mV, (001) = 412.48 mV, (010) = 487.468 mV, (011) = 562.369 mV,

(100) = 637.256 mV, (101) = 712.075 mV, (110) = 786.878 mV, (111) = 861.655 mV.

Table of Settling time of DAC for different capacitance load :

Parameters	Cload = 1 pF	Cload = 1.25 pF	Cload = 1.5 pF	Cload = 1.75 pF	Cload = 2 pF
Settling Time (ns)	18.21	19.82	27.24	30.79	42.49
Step-response	Maximally Flat, No Overshoot	Maximally Flat, No overshoot	Light Overshoot + Ringing	Medium Overshoot + Ringing	High Overshoot + Ringing

5. Conclusion

Design Parameters of Components

OPAMP transistor parameters table: R1= 1 KΩ and R2= 4 KΩ

Transistor	Hand calculations			Schematic without mismatch		
	W/L	W(um)	L(nm)	W/L	W(um)	L(nm)
S1,S2	105.85	50.81	480	4.17	2	480
S3,S4	2.38	1.14	480	25.08	12.04	480
S5,S8	55.85	20.11	360	25	9	360
S6	120.4	14.45	120	166.67	20	120
S7	1410.4	169.25	120	55.55	30	540
S9	1.33	0.16	120	1.33	0.16	120

OPAMP design specifications table: Cc= 0.65 pF, Voltage Offset = 77.56 uV

Parameters	Required Specifications	Schematic Without Mismatch	Parasitic Extracted
DC Gain	>50 dB	51.84 dB	51.99 dB
Gain Bandwidth	≥20 MHz	37.11 MHz	36.34 MHz
Phase Margin	≥ 50°	69.6°	69.4°
Slew Rate (+ve)	≥15 V/us	33.23 V/us	32.62 V/us
Slew Rate (-ve)	≥-15 V/us	-30.8 V/us	-30 V/us
Positive ICMR Vin(max)	900 mV	896.6 mV	895.7 mV
Negative ICMR Vin(min)	300 mV	312.3 mV	311.9 mV
Output Voltage Swing	0.2 - 1 V	0.203 – 0.982 V	0.212 – 0.980 V
Power Dissipation	≤ 3 mW	0.394 mW	0.393 mW
Load Capacitance	≥1 pF	1.25 pF	1.25 pF
Positive Supply Voltage	1.2	1.2	1.2
Negative Supply Voltage	0	0	0

Analog Switch(Transmission Gate) :

ON Resistance = Ron = 4.178 KΩ

OFF Resistance = Roff = 3.055 GΩ

Control Logic :

Data : Rise time = 6.8 ns , Fall time = 7.8 ns
Propagation Delay (Input Rising Edge to Output Rising Edge) = 53.2 ns
Propagation Delay (Input Falling Edge to Output Falling Edge) = 54.1 ns

nData: Rise time = 8.5 ns , Fall time = 9 ns
Propagation Delay (Input Rising Edge to Output Rising Edge) = 58.9 ns
Propagation Delay (Input Falling Edge to Output Falling Edge) = 59.2 ns

3-bit Resistor String DAC :

Settling Time = 19.82 ns (with Cload = 1.25 pF)

Static Performance of 3-bit Resistor String DAC

	Without Mismatch		Mismatch Res_Max Case 1a		Mismatch Res_Min 1b		Mismatch Res_Max 2a		Mismatch Res_Min 2b		Mismatch Res_Max 3a		Mismatch Res_Min 3b		Parasitic Extracted	
	LSB	uV	LSB	uV	LSB	uV	LSB	uV	LSB	uV	LSB	uV	LSB	uV	LSB	uV
Power uW	364.610		364.146		363.998		364.088		364.024		363.914		363.998		361.574	
OSE	-0.00027	-20.25	-0.00029	-21.75	-0.00020	-15.00	-0.00034	-25.50	-0.00016	-12.00	-0.00190	-142.50	-0.00027	-20.25	-0.00042	-31.50
GE	-0.00035	-26.25	-0.00026	-19.50	-0.00043	-32.25	-0.00021	-15.75	-0.00056	-42.00	0.00118	88.50	-0.00035	-26.25	-0.00042	-31.50
DNL Errors																
B000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B001	0.00967	725.25	0.01761	1,320.75	0.00224	168.00	0.01608	1,206.00	0.00371	278.25	0.01327	995.25	0.00967	725.25	0.01075	806.25
B010	0.00101	75.75	-0.00882	-661.50	0.01156	867.00	-0.01026	-769.50	0.01250	937.50	0.00409	306.75	0.00102	76.50	0.00082	61.50
B011	-0.00086	-64.50	0.00716	537.00	-0.00853	-639.75	0.00576	432.00	-0.00776	-582.00	0.00218	163.50	-0.00080	-60.00	-0.00034	-25.50
B100	-0.00122	-91.50	-0.01137	-852.75	0.00883	662.25	-0.00415	-311.25	0.00066	49.50	0.00187	140.25	-0.00128	-96.00	-0.00053	-39.75
B101	-0.00143	-107.25	0.00611	458.25	-0.00938	-703.50	0.00519	389.25	-0.00833	-624.75	0.00162	121.50	-0.00146	-109.50	-0.00144	-108.00
B110	-0.00165	-123.75	-0.01212	-909.00	0.00822	616.50	-0.01288	-966.00	0.00983	737.25	0.00135	101.25	-0.00166	-124.50	-0.00165	-123.75
B111	-0.00195	-146.25	0.00527	395.25	-0.01022	-766.50	0.00476	357.00	-0.00844	-633.00	0.00103	77.25	-0.00190	-142.50	-0.00200	-150.00

INL Errors																
B000	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
B001	0.00967	725.25	0.01761	1,320.75	0.00224	168.00	0.01608	1,206.00	0.00371	278.25	0.01327	995.25	0.00967	725.25	0.01075	806.25
B010	0.01068	801.00	0.00878	658.50	0.01380	1,035.00	0.00582	436.50	0.01621	1,215.75	0.01736	1,302.00	0.01069	801.75	0.01157	867.75
B011	0.00983	737.25	0.01594	1,195.50	0.00527	395.25	0.01158	868.50	0.00845	633.75	0.01954	1,465.50	0.00989	741.75	0.01123	842.25
B100	0.00861	645.75	0.00457	342.75	0.01410	1,057.50	0.00743	557.25	0.00911	683.25	0.02141	1,605.75	0.00860	645.00	0.01070	802.50
B101	0.00717	537.75	0.01068	801.00	0.00472	354.00	0.01261	945.75	0.00078	58.50	0.02303	1,727.25	0.00715	536.25	0.00926	694.50
B110	0.00553	414.75	-0.00144	-108.00	0.01293	969.75	-0.00026	-19.50	0.01061	795.75	0.02438	1,828.50	0.00549	411.75	0.00761	570.75
B111	0.00358	268.50	0.00383	287.25	0.00271	203.25	0.00450	337.50	0.00218	163.50	0.02541	1,905.75	0.00359	269.25	0.00562	421.50

Layout Area of OPAMP = 15.2 um x 14.5 um
Layout Area of Control Logic Signal = 17.25 um x 18.25 um
Layout Area of Analog Switch Multiplexer = 13.3 um x 13.7 um
Layout Area of Folded Resistor Ladder = 30.7 um x 18.4
Total Layout Area of 3-bit Resistor String DAC = 32.80 um x 46.90 um

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