adic_DAC3R 3Bit_RString_DAC_test schematic : Jul 29 20:46:27 2014 43

User: aic11   Date: Jul 29, 2014   7:47:38 PM GMT+01:00

Jul 29, 2014   Transient Response

/Clock   /Vout

M7(840.9ns, 861.9mV)

M4(537.9ns, 637.9mV)

M2(339.9ns, 488mV)

M6(739.9ns, 787.7mV)

M0(139.9ns, 337.3mV)

M5(639.5ns, 712.1mV)

M3(434.9ns, 562.3mV)

M1(235.5ns, 412.2mV)

V (V)

time (us)