Vishwanathan Iyer

System Integration Validation Engineer | Intel Corporation
M-Tech | Indian Institute of Technology, Bombay

SKILLS

System Engineering

• Silicon Validation • Software Integration
• Hardware Bring-up • Debugging [5]
• Silicon Graphics • Pre-Silicon Simulation [1] [6]
• Test Automation [3] • Mentoring

Specs and Technologies

• eDP 1.5 • HDMI 2.1 • DP 2.1
• Intel DPST • H265 • AV1
• DirectX • Vulkan
• OpenCL • WebGPU
• Windows Internals

Tools and Languages

• Python [3] •C • Windbg • VS code
• Git • Windows ETW [5]
• Requirements and Bug tracking

EDUCATION

I.I.T. BOMBAY
M-Tech Electronic Systems
CPI: 9.21/10
June 2017 | Mumbai, India

V.E.S.I.T.
B.E. Electronics
CPI: 75.50%
June 2013 | Mumbai, India

CERTIFICATIONS

• Oracle Cloud Infrastructure 2024 Generative AI Certified Professional
• AI Everywhere – AI: Idea to Production
• Advanced Generative AI
• 6.00.1x, Introduction to Computer Science and Programming Using Python
• C Programming for Embedded Applications.

HOBBIES

• Chess • Football • Rubik's cube.
• Volunteer at Intel Involved Events and fun events.

LINKS

Linked In:// **vishwanathan-iyer/**
Email: vsiyer91@gmail.com
Mobile: +91-8169961518

EXPERIENCE

Over a decade of driving innovation and excellence in electronic systems

INTEL CORPORATION | System Integration Validation Engineer
July 2017 - Present | Bengaluru, India

- **Eight years** in silicon, platform software and systems validation, shipping **high-volume**, and **high-quality** products.
- **Problem Solving** and **bringing to life** next-generation [8] hardware platforms.
- System **debugger** on technical challenges at the boundary between hardware and software on simulation [7] and hardware platforms.
- Deployed multimedia **automation** [3] solution across 7 client SKUs, ≈ 100 systems $\approx 18,000$ test runs and found ≈ 1000 unique defects.

I.I.T. BOMBAY | Sr. Project Technical Assistant
July 2013 – July 2017 | Mumbai, India

- **Four years** hands-on in Embedded Systems Design, Development, and Robotics.
- Worked in **Embedded and Real-time Systems Lab** in the **Department of Computer Science and Engineering**.
- Assisted in designing **lab experiments** on the Tiva Launchpad for Embedded Systems course.

AWARDS

Received **40 recognition** from multiple stakeholders, including executives and directors.

2022	SIV Superstar	Cost savings and optimizations.
2021	SIV Change Agent	oneMAP idea to production.
2021	SIV Superstar	Multimedia Automation deployment.
2020	WSS DRA	Distributed, Multi-site Power-on.
2020	SIV Special Award	Windows 10x validation strategy for dual screens.
2020	WSS recognition	Stability debug and Engineering Excellence.

PUBLICATIONS

[1] D. Ambarish and V. Iyer. Usb audio offload end to end on pre-silicon platform (lakefield). *SWPC*, 2018.

[2] R. Angadimani, V. Iyer, S. S, and P. Koduru. Unified automation methodology to monitor functional and pnp metrics for use case validation. *DTTC*, 2021.

[3] V. Iyer, R. Angadimani, and F. Fathima. One modular automation for platform (onemap). *DTTC*, 2022.

[4] V. Iyer, S. Bhat, and S. Banik. Triage assistant: Algorithm to classify defects to its signature and assist trage. *SWPC*, 2022.

[5] V. Iyer, S. Lawerence, R. Angadimani, and D. KV. Windows sw debug using machine learning. *Platform Analysis and Technology Summit*, 2018.

[6] V. Iyer and P. K. P. Graphics driver end to end validation on pre-silicon. *Intel Pre-Silicon Software Readiness Summit*, 2018.

[7] V. Iyer, P. K. P, R. Angadimani, and A. Das. Multimedia pre-silicon software: A platform level retrospective. *DTTC*, 2019.

[8] V. Iyer and R. P. The next wave of personal computing: Dual display. *SWPC*, 2020.