**Lab 10: Simple Design using Multiple IPs**

**Exercise 10.1:** Design and implement a unit which computes O = (A\*B) + (C\*D) using Vivado IPs. A, B, C and D are 2-bit inputs. O is a 5-bit output. Implement the design on FPGA and show the outputs using on board LEDs. Assume inputs are connected DIP switches.

**Pin Information:**

**A[1:0] 🡪 [M15, H17]**

**B[1:0] 🡪 [H18, H19]**

**C[1:0] 🡪 [F21, H22]**

**D[1:0] 🡪 [F22, G22]**

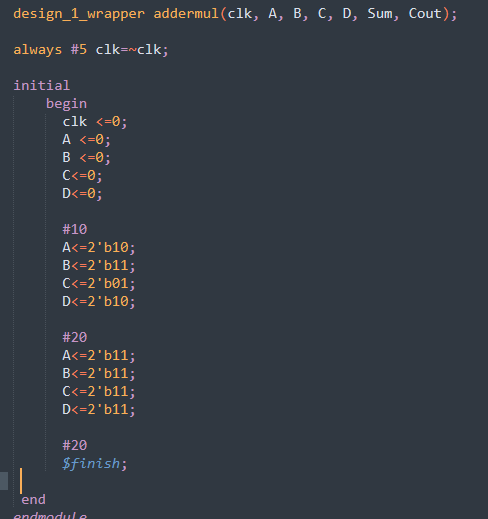
**O[4:0] 🡪 [V22, U21, U22, T21, T22]**

1. **Copy the image of the IP based design:**

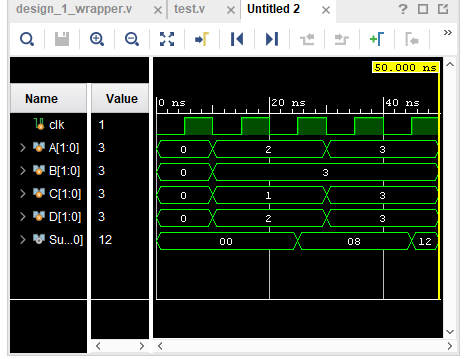
Click here to enter text.

1. Write appropriate test bench and test your module.

**Question: Paste the image test bench code.**

Answer: 

**Question: Paste the image showing the simulated waveforms.**

Answer: 

1. Plan your I/O mapping (using **I/O planning** option) such that actual input **Clk** is connected to internal clock pin **Y9,** all inputs connected to DIP switches and outputs are connected to LEDs (Refer to old documents or CMS for Pin information). Save the mapping information as **design\_1.xdc**.
2. Synthesize (**Run Synthesis**) and Implement the design (**Run Implementation)**.

**Question: Paste the image showing the schematic after synthesis.**

Answer:

**Question: Check the summary report and report hardware utilization for the implementation.** (Note the utilization in your observation book)

Answer:

1. **Generate Bitstream** and port your design on to FPGA (**Open Hardware Manager**🡪 **New Target**🡪… **Program Device**)
2. **Check the output on FPGA.**

**List the concepts you learnt from this lab (Conclusions/Observations)**

Answer: