

# VISHWAS GAUTAM

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## EDUCATION

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**BITS Pilani, Hyderabad Campus**  
*Bachelor of Engineering in Electrical & Electronics*

*August 2019 - Jan 2023*

CGPA: 8.85/10

PS: Successfully completed the 4 year degree in 3.5 years.

## WORK EXPERIENCE

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**Software Development Engineer 1**  
*Advance Micro Devices, Inc. (AMD)*

Hyderabad, India  
*Feb 2023 - Present*

- Working in the Performance Modelling and Architecture Framework group.
- Working on performance estimation and analysis of modern workloads on Xilinx devices.
- Conducting experiments to compare various internal tools and frameworks with production-grade software.

## RESEARCH EXPERIENCE

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**Intern at CFAED, TU Dresden**  
*Bachelor's Thesis at the Chair of Processor Design*

Dresden, Germany  
*June 2022 - Dec 2022*

- Developed an efficient hardware framework for BERT, focusing on minimal resource utilization to enable resource-constrained devices to run large NLP tasks.
- Implemented quantization techniques to reduce memory occupation by model parameters, developed a single matrix multiplier unit based on weight matrix concatenation, and incorporated approximate multiplier units to further optimize resource utilization.
- Created a flexible software-hardware co-design framework, allowing user customization of several parameters based on their specific hardware requirements.
- Successfully tested designs on Avnet Ultra96v2 FPGA board using PYNQ framework for effective deployment on resource-constrained devices.

## RELEVANT PROJECTS

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**Verification of Network-on-Chip systems**  
*Research at BITS Pilani, Hyderabad Campus*

*Jan 2022 - May 2022*

- Developed a feedback guided packet generation technique to improve functional coverage in NoC systems.
- Tested the algorithm for different mesh sizes and compared the results with meta-heuristic based algorithms.

**Convolution using RISC-V processing elements**  
*Research at BITS Pilani, Hyderabad Campus*

*Sept 2021 - Jan 2022*

- Worked on the parallel execution of convolution algorithm to test a RISC-V-based Network-on-Chip processor.
- Developed sequential, loop-unrolled and parallel implementations of the convolution algorithm in RARS.

**Implementation of a RISC-like processor**  
*Independent Project*

*July 2021 - Aug 2021*

- A 32-bit, 5-stage pipelined processor with Fetch, Decode, Execute, Memory, and Write-Back stages in Verilog.
- The processor supports a few R-type, I-type, and B-type instructions from the RISC-V 32I ISA.
- Implemented a forwarding unit and hazard-detection unit for resolving data, stall, and control hazards.

## PUBLICATIONS

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**V. V. Gautam**, R. Loka and A. M. Parimi, "Cubature Kalman Filter and Linear Quadratic Regulator for Load Frequency Control" under review in Electric Power Systems Research (Q1 Journal with IF: 3.8).

Aparna Nair, **Gautam, V.V.**, Revinipati, A., Soumya, J. (2022). "Implementation and Analysis of Convolution Image Filtering with RISC-V Based Architecture," in VLSI Design and Test. VDAT 2022. Communications in Computer and Information Science, vol 1687. Springer, Cham. [doi]

**V. V. Gautam**, R. Loka and A. M. Parimi, "Analysis of Load Frequency Control using Extended Kalman filter and Linear Quadratic Regulator based controller," 2nd International Conference on Power Electronics & IoT Applications in Renewable Energy and its Control (PARC), 2022, pp. 1-5, [doi].

## EXTRACURRICULARS

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### **Hyperloop India — BITS Pilani**

*Oct 2020 - June 2022*

*Subsystem Lead, Electrical and Electronics Subsystem*

- Worked with the Hyperloop India 2020-21 team to design a prototype of the Hyperloop transportation system.
- Proposed a Laser-based communication system for an efficient ground-to-pod communication.
- Simulated the handover techniques in Python for seamless hand-offs in the overlapping regions of the network.

### **Automation & Robotics Club — BITS Hyderabad**

*Jan 2020 - Jan 2021*

*Technical Member*

- Worked on hobbyist grade robotics projects such as 3-DOF inverse kinematic robotic arm and Mario game-controller for exhibitions.
- Prepared material on C-programming, basics of electronics, and Arduino for mentoring students.
- Simulated an autonomous hexacopter in ROS for obstacle avoidance and movement of goods in a warehouse for *Flipkart GRiD 2.0 competition*.

## AWARDS

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1. Financial assistance for bachelor's thesis
2. Round 3 of the Flipkart GRiD 2.0 competition — **Top 64 of 6060 Participants**.

## SKILLS

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### **Programming & Software:**

C, Python, Matlab, Simulink, Verilog, Assembly, LTSpice, Gem5, COMSOL Multiphysics, Vivado, Vitis HLS.

### **Hardware:**

Arduino(AVR), Raspberry Pi, Xilinx Zynq-7000 FPGA kit, Avnet Ultra96v2.

## RELEVANT COURSES

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Computer Architecture (A), Digital Design (A), Microprocessors & Interfacing (A-), FPGA-based System Design (B), Operating Systems (B-), Analog & Digital VLSI Design (A), Digital Communication (A).