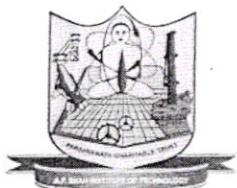


MODULE 5 : SEQUENTIAL LOGIC DESIGN

Flip Flops : SR, JK, D, T, master slave flip flop, Truth Table, excitation table and conversion

Register: Shift register, SISO, SIPO, PISO, PIPO, Bi-directional and universal shift register.

Counters: Design of synchronous and asynchronous ,Modulo Counter, Up Down counter IC 74193, Ring and Johnson Counter



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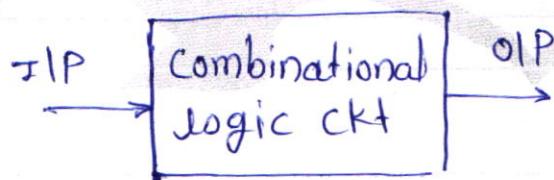
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sequential logic CKT

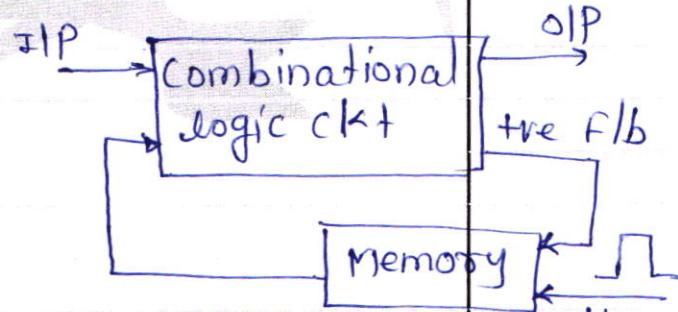
4th Chapter

- * Difference between combinational & sequential CKT.

Combinational logic CKT



Sequential Circuit



- OIP at any instant depends only on present inputs.

- OIP at any instant depends not only on present IP but also on the past OIP



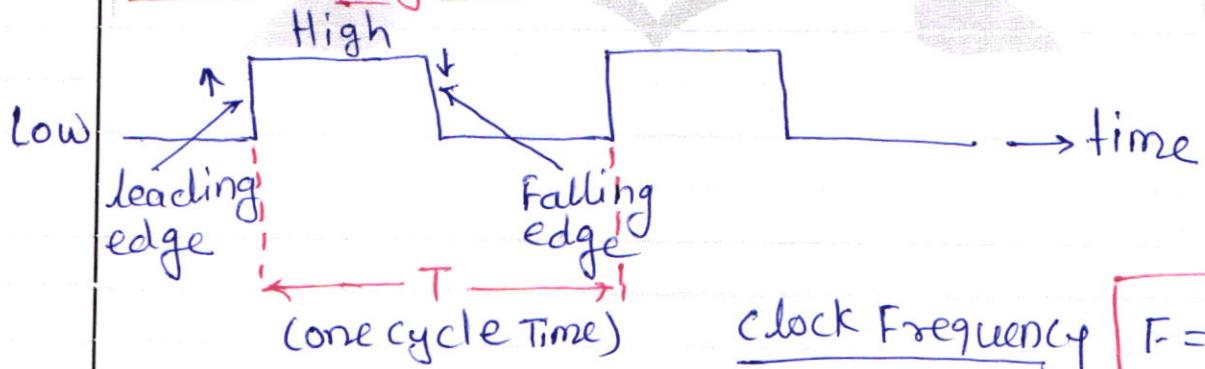
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- | | |
|--|---|
| - It has no memory | - It has memory |
| - CLK i/p - not necess. | - CLK i/p - necessary |
| - No ability to store data | - Ability to store data |
| - Not require any feedback | - Does not require feedback |
| - Mainly used in Arithmetic & Boolean opern | - Mainly used in storing data |
| - examples: Adders, subtractors, code Converters | - Examples : Flip-flop, shift registers, counters |

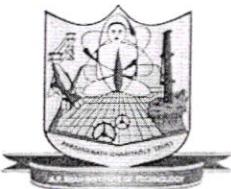
* Clock signal :-



clock Frequency

$$F = 1/T$$

- It is time signal
- Clock is a rectangular signal
- Clock signal repeats itself after every T seconds



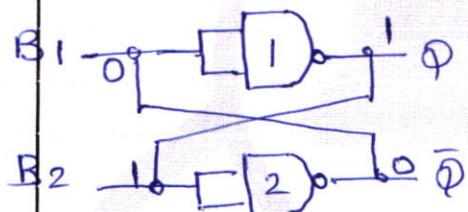
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* Latch:

- F1F is also known as basic digital memory ckt.
- It has two stable states
 - 1] logic 1 state
 - 2] " 0 "
- we can design with
 - 1] NOR gate
 - 2] NAND gate



Here, NAND gates 1 & 2 are acting as inverters. Hence this ckt is called as a cross coupled inverter

- OIP of gate 1 is connected to the iIP of gate 2 & OIP of gate 2 is connected to iIP of gate -1.

oper^n

- Assume \rightarrow OIP of gate 1 i.e. $Q = 1$. Hence $B_2 = 1$.
- AS $B_2 = 1$, OIP of gate-2 i.e. $\bar{Q} = 0$, This makes $B_1 = 0$
- Hence Q continues to be equal to 1

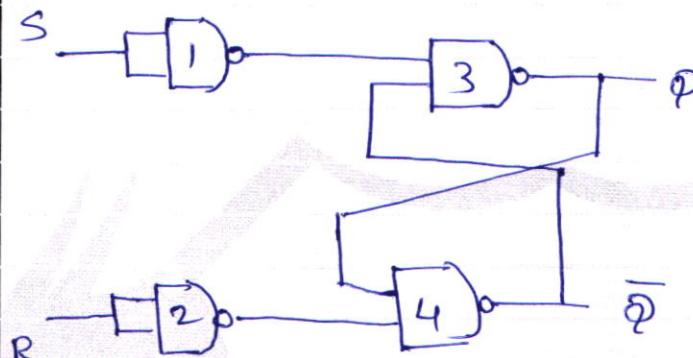


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Latch



NAND gate

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

- It is Capable of locking or latching the information.
- It is called as Latch.

Truth Table

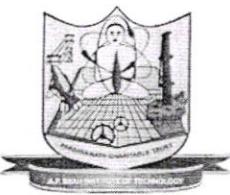
S	R	Q	\bar{Q}	
0	0	0	1	NO Change
0	1	0	1	Reset
1	0	1	0	Set

INFORMATION TECHNOLOGY

Race (Invalid)

Case I $S=R=0$ (No change)

- O/P of gate 1 & 2 will become 1
- Let $Q=0$ & $\bar{Q}=1$.
- Hence both i/p's to gate 3 are 1 & the i/p's to gate 4 are (01)



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- so gate-3 OLP $\varphi = 0$
- & gate-4 OLP $\bar{\varphi} = 1$
- Thus with $S=R=0$ there is no change in the state of OLP's.

Case II : - $S=0$ & $R=1$ (Reset.)

- then one of the IIP's to gate 4 will be 0.
- This will force the $\bar{\varphi}$ OLP to 1.
- Hence both the IIP's to gate 3 will be 1. This Forces φ to 0
- Thus for $S=0$ & $R=1$, the OLP's are $\varphi=0$ & $\bar{\varphi}=1$. This is the reset state or clear state.

Case III : $S=R$ & $R=0$ (Set)

- since $S=1$ & $R=0$, one of the IIP's to gate-3 will be 0, then $\varphi=1$
- Hence both the IIP's to gate-4 will be 1. so $\bar{\varphi}=0$
- Hence $S=1$ & $R=0$, the OLP's are $\varphi=1$ & $\bar{\varphi}=0$. This is set state.



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Case IV:— $s=R=1$ (Invalid [Race/Prohibited/
Forbidden])

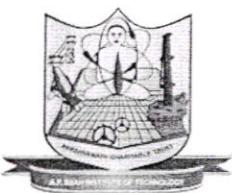
- IF $s=R=1$ then O/P of gates 1 & 2 = 0
- Hence gate 3 ~~or~~ gate 4 will be zero
- So both $Q + \bar{Q} = 0$
- It is not allowed as $Q + \bar{Q}$ should be complementary.
- Hence $s=R=1$ cond'n prohibited.

* Characteristic Equation

- The truth table is also called as excitation table.
- Another way of doing it is to use special type of eq's. called characteristic eq's.
- Characteristic eqⁿ of FLF is the eqⁿ which relates the next state of the FLF or latch Q_{n+1} or \bar{Q}_{n+1} to the current state & ilp's ($Q_n, S \& R$)

$Q_n \& \bar{Q}_n \rightarrow$ Present states

$Q_{n+1} \& \bar{Q}_{n+1} \rightarrow$ Next states .

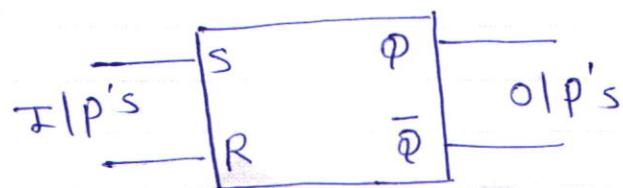


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symbol → S-R latch



Duty cycle:— Ratio of time for which signal is high to the total time

$$\begin{aligned} &= \frac{t_{1/2}}{T} \\ &= 1/2 = 50\% \end{aligned}$$

* Triggering Methods :-

which part of the sequential ckt we have to trigger.

seq. ckt = combinational ckt + memory

stored state in memory will change with clock pulse.

- Trigger memory element. Change in clock will change the memory so this is triggering of FLF.





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Two types

I] Level triggering :-

a) the level triggered :- If the O/P of a Flip-Flop respond to the i/p changes, only when its clock i/p at HIGH (1) level, then it is called as the the level triggered F/F.

b) -ve level triggered :- If the O/P of F/F respond to the i/p changes, only when its clock i/p is at low (0) level, then it is called as the -ve level triggered F/F.

II] Edge triggered :

+ve edge :- When go From Low to High then change in memory element will trigger.

-ve edge :- When go From High to Low then change in memory element will trigger.



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* Types of Flip-Flops

- 1] RS FIF
- 2] JK FIF
- 3] D FIF
- 4] T FIF

Flip-Flop: —

- It is a binary storage device.
- It can store binary bit either 0 or 1.
- It has two stable states i.e. HIGH or LOW or 0 or 1.
- It is also called as bistable multivibrator.
- It stores the data.
- It can be used to keep a record or what value of variable (i/p, o/p or intermediate).

I] RS FIF (Clocked RS FIF or Gated S-R Latch)

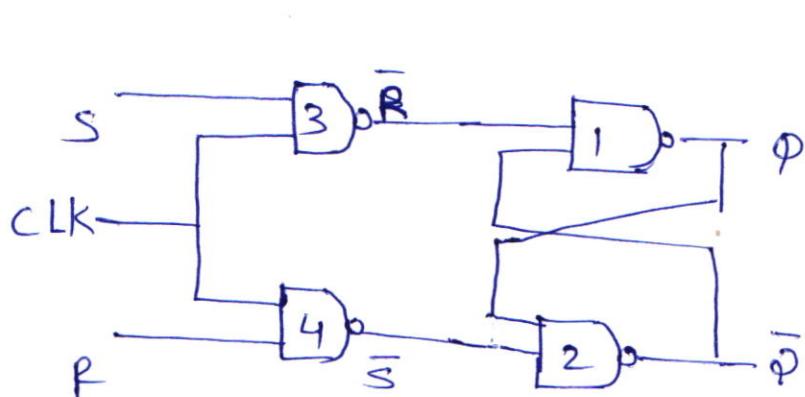
- RS latch FIF required the direct i/p but no clock
- The FIF changes state only when clock pulse is applied depending upon the i/p's.



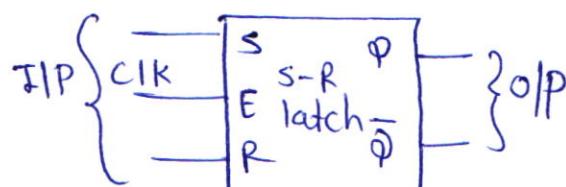
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Symbol



Truth Table

CLK	S	R	Q	\bar{Q}	Comments
0	X	X	No change as $^{(E)} \text{CLK} = 0$		
1	0	0	No change		
1	0	1	0	1	Reset cond ⁿ
1	1	0	1	0	set "
1	1	1	1	1	Not used

Operⁿ

1] $S=R=0$ (No change)

If $S=R=0$ then O/P of NAND gates 3 & 4 are forced to become 1.

- Hence \bar{R} & \bar{S} both will be equal to 1.

- Since S-R latch using NAND gates, there will be no change in the state of O/P's.

2] $S=0, R=1, E=1$

since $S=0$ O/P of NAND-3 gate i.e. $\bar{R}=1$ & $E=1$

the O/P of NAND-4 i.e. $\bar{S}=0$

- Hence $Q=0$ & $\bar{Q}=1$. This is Reset condⁿ.



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3] $S=1, R=0 \& E(CLK)=1$

OIP of NAND-3 i.e. $\bar{R}=0$ & OIP of NAND-4 i.e. $\bar{S}=1$.

Hence OIP of S-R NAND latch is $Q=1$ & $\bar{Q}=0$.
This is set condn.

4] $S=1, R=1 \& E=1$

As $S=1, R=1$ & $E=1$ the OIP of NAND gates 3 & 4 both are 0 i.e. $\bar{S}=\bar{R}=0$

- Hence the Race Cond'n will occur in the basic NAND latch.

Characteristics & Excitation table

1) Characteristics table :- It is also called as truth table

2) Excitation table :- These tables are different from the characteristic tables.

Present state is the state prior to appl'n of CLK pulse & the next state means the state after appl'n of clock pulse.



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Excitation Table

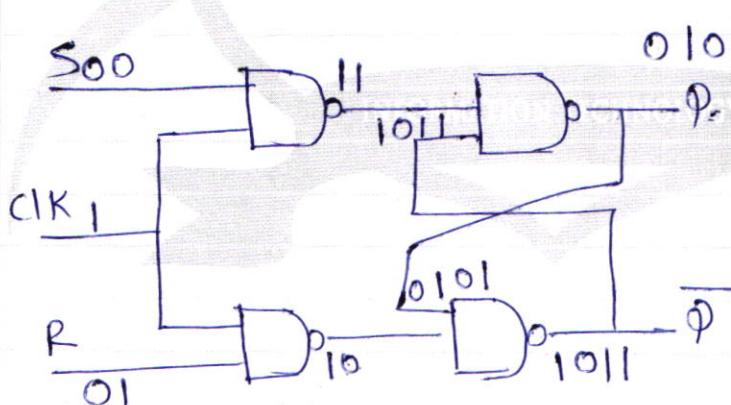
IIP to FIF

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Q_n	SR	00	01	11	10
0	0	0	0	X	1
1	1	D	0	X	C

$$Q_{n+1} = S + Q_n \bar{R}$$

S/R



Q	S	R	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

logic diagram





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1) Truth table For SR F/F

$Q_{n+1} \rightarrow \text{next state}$

clk	S	R	Q_{n+1}	comment
0	X	X		$Q_n \rightarrow \text{Present state}$
1	0	0		$Q_n \rightarrow \text{memory}$
1	0	1	0	0 → Reset
1	1	0	1	1 → Set
1	1	1		Invalid

2) Characteristic table $\text{clk} = \text{high} = 1$

$$Q_{n+1} = SR * \text{Previous state}$$

Q_n	S	R	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

next state = Previous state

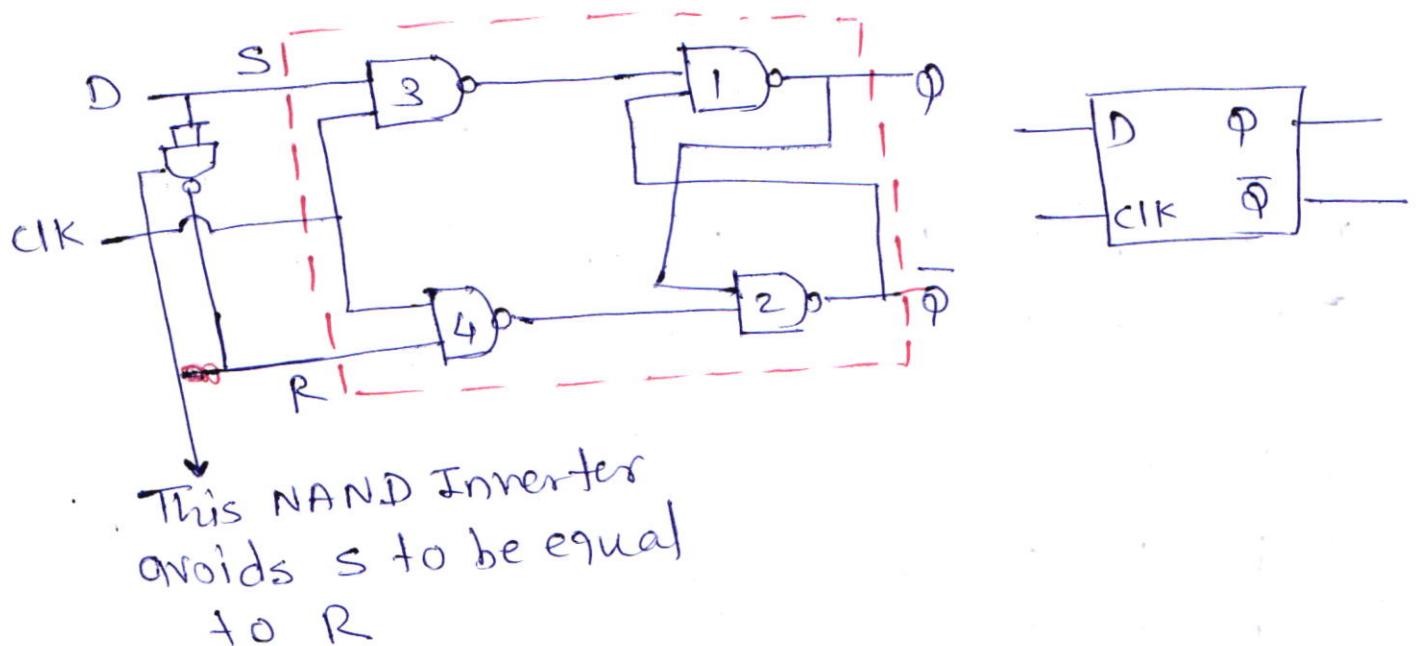
3) Excitation Table

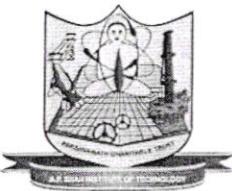
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	1

Q_n	SR	00	01	11	10
0		0	0	X	1
1		1	0	X	1

$$Q_{n+1} = Q_n R + S$$

Gated D latch





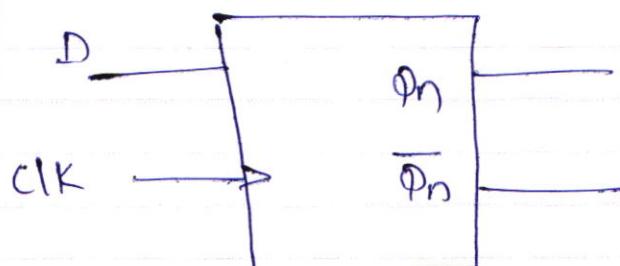
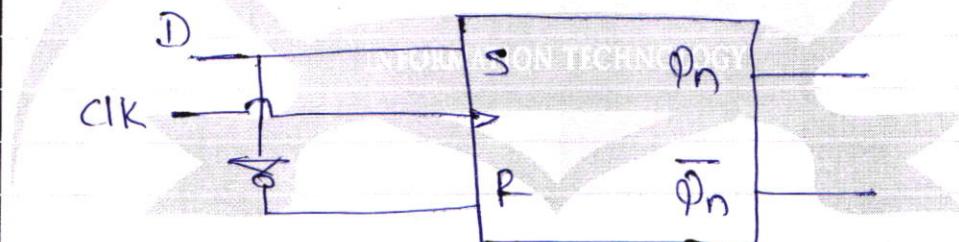
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II] The Gated D Latch (clocked D F/F):-

- D latch is the simple gated S-R Latch with a small modification.
- This latch has only one iIP denoted by D.
- Due to the NAND inverter, S & R iIP's will always be the complements of each other.
IIP cond'n's such as $S=R=0$ or $S=R=1$ will never appear.
- This will avoid the problem associated with $SR=00$ & $SR=11$ cond'n's of SR F/F.



$CLK=0$ will not take

any iIP so

$$Q_{n+1} = Q_n$$

i.e. previous iIP



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Truth Table For D FIF

clk	D	Q_{n+1}
0	X	Q_n
1	0	0
1	1	1

2] Char Table

Q_n	D	Q_{n+1}
0	0	0
0	1	1
1	0	0
1	1	1

$$Q_{n+1} = D$$

3] Excitation Table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

D is single FIF

In SR FIF two iIP, so 4 combinations
but $S=1$ & $R=1$ then not used case



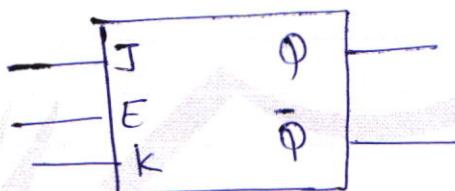
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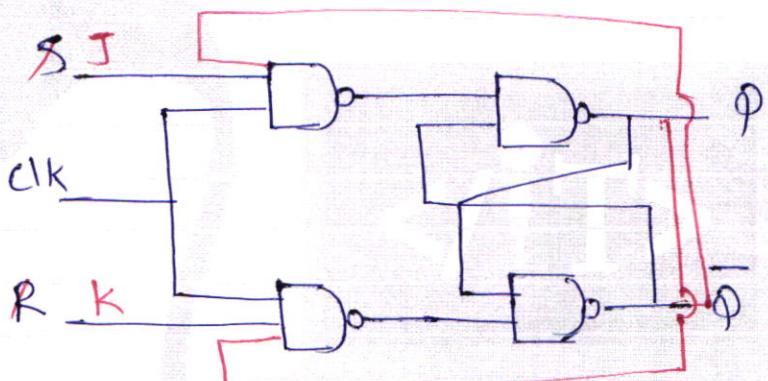
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III] Gated JK latch :- JK FIF

- It is also called as clocked JK FIF.



= symbol



Truth Table For JK FIF

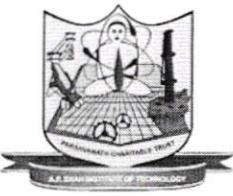
CLK	S	R	Q_{n+1}	Comment
0	X	X	Q_n	memory
1	0	0	Q_n	memory
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	Not used	

CLK = 0 Memory

CLK = 1 J = 1, K = 0, Q = 1, $\bar{Q} = 0$

CLK = 1 J = 0, K = 1, Q = 0, $\bar{Q} = 1$

CLK = 1 J = 1, K = 1
Assume $Q = 0$ & $\bar{Q} = 1$



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1] Truth Table

CLK	J	K	Q_n	Q_{n+1}	next state	comment
0	X	X		Q_n		memory
1	0	0		Q_n		
1	0	1		0		Reset
1	1	0		1		Set
1	1	1		\bar{Q}_n		Toggle

2] Char Table

Q_n	J	K	Q_{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Kmap for - J/K R/F

JK	00	01	11	10
Q_n	0	0	1	1
0	0	0	1	1
1	1	0	0	1

$$Q_{n+1} = \bar{Q}_n J + Q_n \cdot K$$

3] Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Kmap for J

Q_n	0	1
Q_{n+1}	0	1
0	0	1
1	X	X

$$J = Q_n + 1$$

For K-map \rightarrow K

Q_n	0	1
Q_{n+1}	0	1
0	X	X
1	1	0

$$K = \bar{Q}_n + 1$$

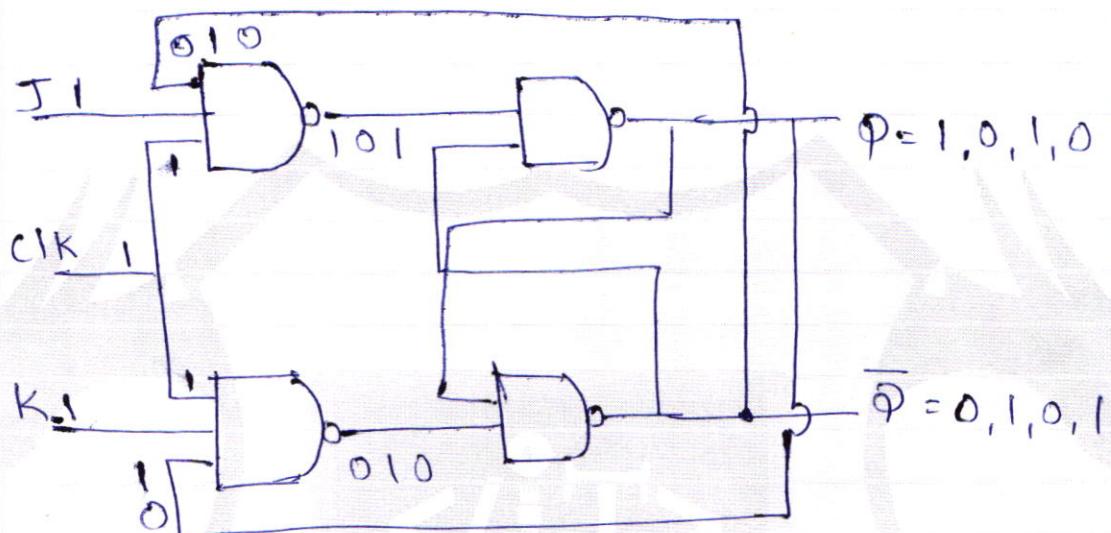


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* Race Around Condition



clk	J	K	Q_{n+1}	\bar{Q}_{n+1}
0	x	x	Q_n	\bar{Q}_n
1	0	0	Q_n	\bar{Q}_n
1	0	1	0	1
1	1	0	1	0
1	1	1	?	?

Toggle can be controlled & Race around can't be controlled

Race around - one has to control using toggling

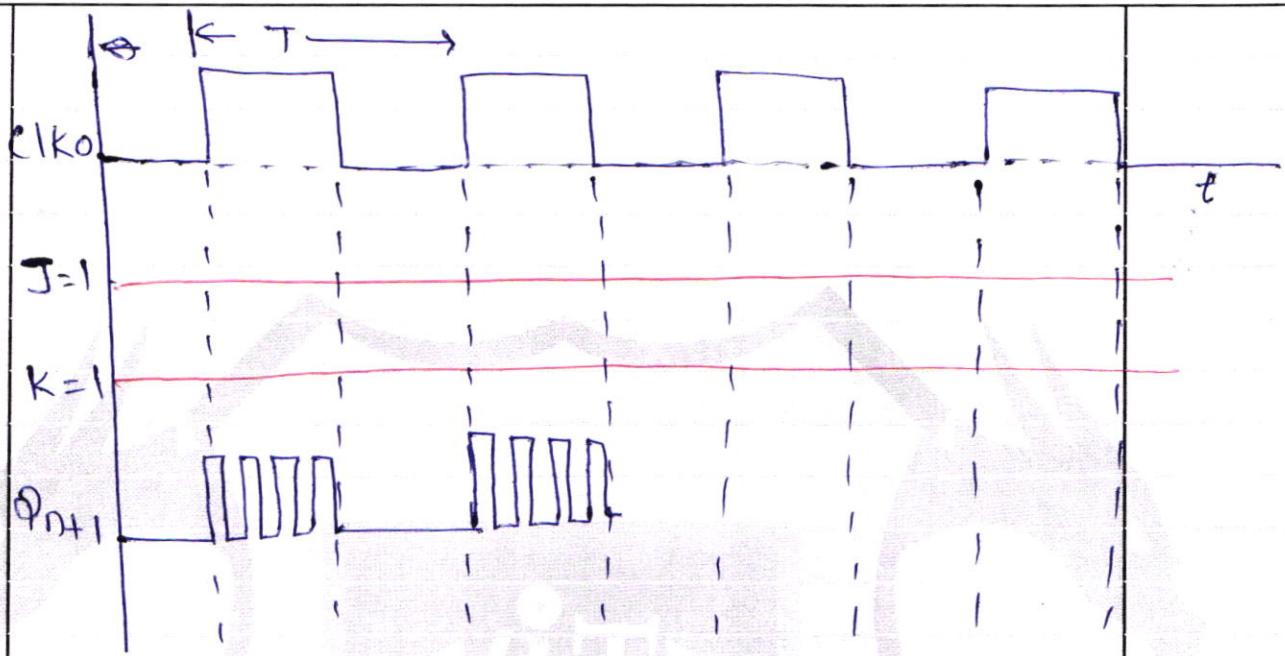
- 1] To avoid - $T_1 < \text{propagation delay of } F/F$
- 2] edge triggering
- 3] Master Slave



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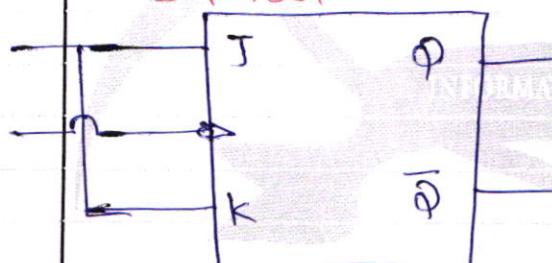
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IV] Gated T FIF | Clocked T FIF (Toggle)
T FlipFlop.

1] Truth table T FIF

symbol



CLK	T	Q_{n+1}
0	X	Q_n (memory)
1	0	Q_n (memory)
1	1	\overline{Q}_n (toggling)

2] Ch Table

Q_n	T	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1} = Q_n \oplus T$$

3] Excitation Table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

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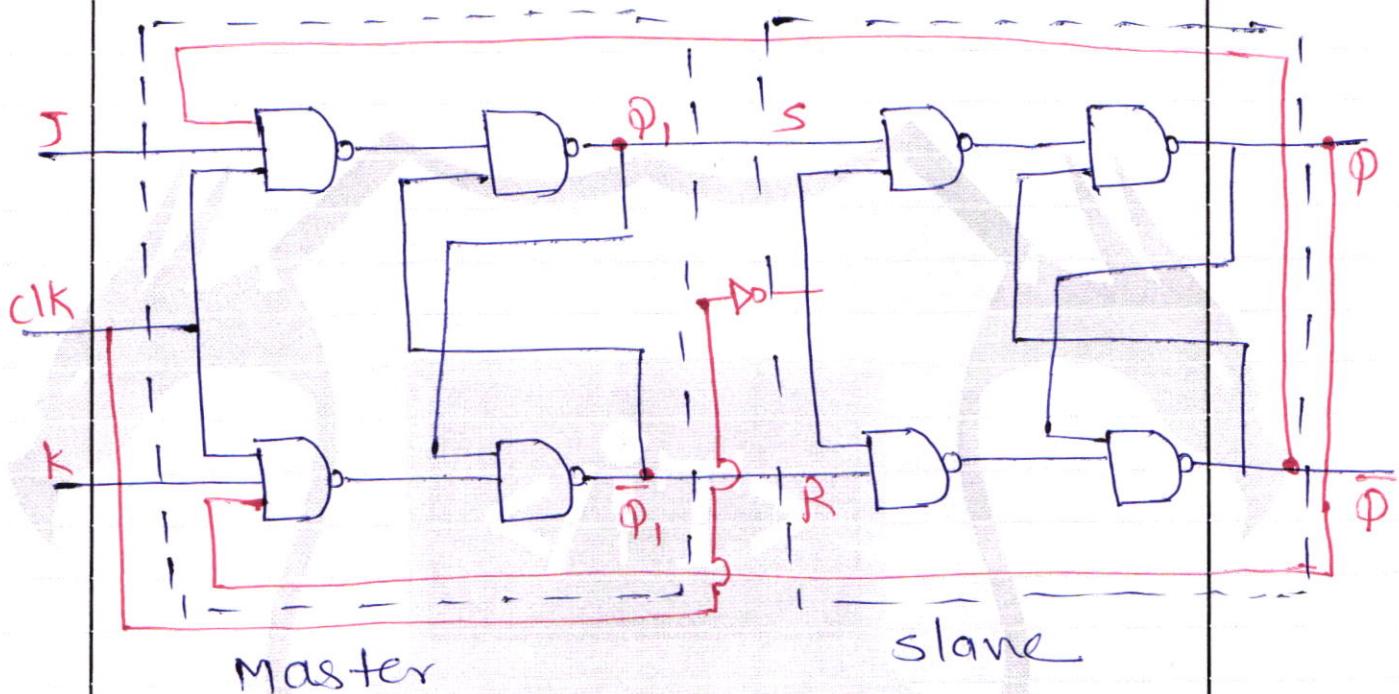


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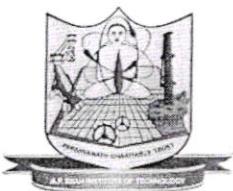
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Master-slave (Ms) JK Flip Flop



- It is the combination of a clocked JK latch & clocked SR latch.
- The clocked JK latch acts as the **Master**
- " " SR " " " Slave
- Master** is the level triggered level
- slave** - due to the presence of the inverter in the clock line, the slave will respond to the -ve level.
- When $\text{clk} = 1$ (the level)
then **Master** is active &
slave is inactive.



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When $\text{Clk} = 0$ (low level)

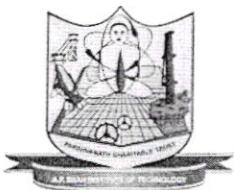
Master is inactive

Slave is active

Truth Table for MS FLF

Case	JIP's			OIP		Remark
	Clk	J	K	Q_{n+1}	\bar{Q}_{n+1}	
I	X	0	0	Q_n	\bar{Q}_n	No Change
II	$\Sigma L(1)$	0	0	Q_n	\bar{Q}_n	No Change
III	$\Sigma L(1)$	0	1	0	1	Reset
IV	$\Sigma L(1)$	1	0	1	0	Set
V	$\Sigma L(1)$	1	1	\bar{Q}_n	Q_n	Toggle

INFORMATION TECHNOLOGY

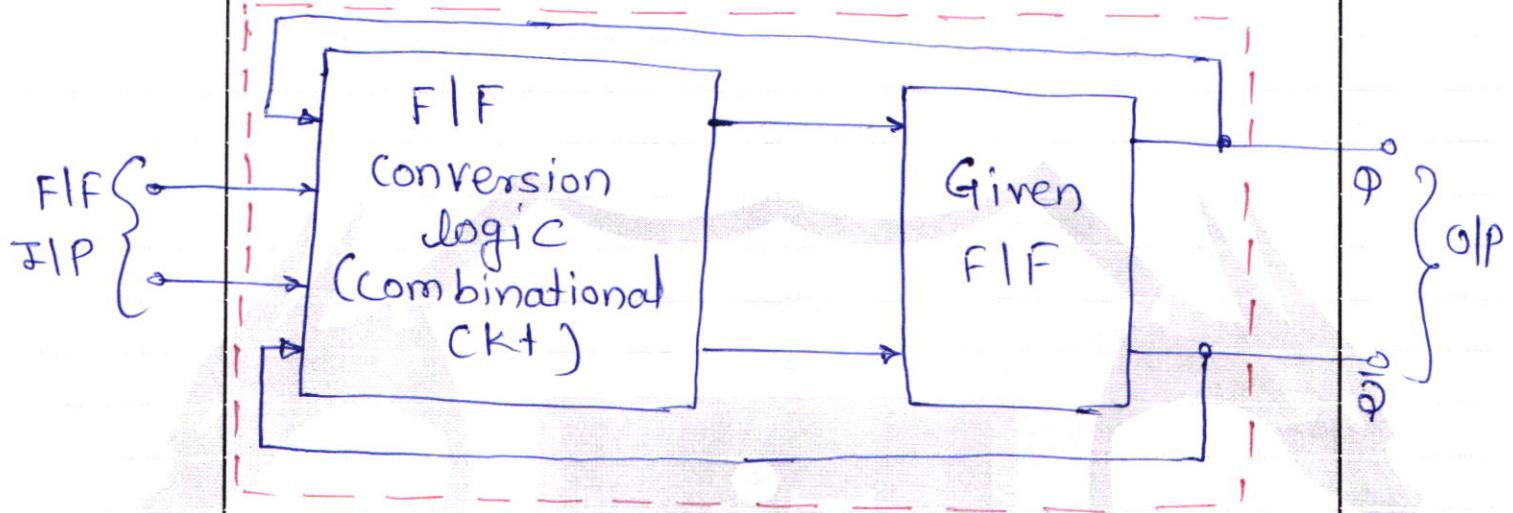


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* Conversion of F/F



- It is the combination of Excitation tables of both F/F [Given F/F & Required F/F]
- Flip flop conversion logic are, the flip flop data i/p's & the o/p's of the given F/F.
i.e. the given F/F & Required F/F.
- Make the truth table of flip-flops with the help of excitation table of them.
- Then we draw the k-map for each o/p & obtain the simplified expressions.



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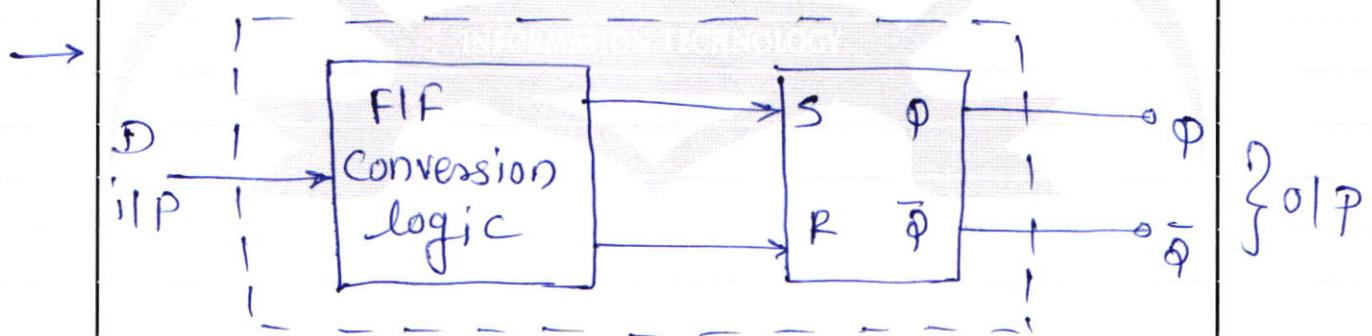
- At last, draw the logic diagram for FIF's.

~~Ex-1~~

Excitation Table

present state Q_n	Next state Q_{n+1}	SR FIF		JK FIF		T	D
		S	R	J	K		
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	1	0
1	1	X	0	X	0	0	1

~~Ex-1~~] conversion from SR FIF to D FIF



D FIF

Step 1 Write truth table for conversion

D	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	0	1	1	0
1	1	0	0	1



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Step 2 :- K-map & simplification

K-map for S

D	\bar{Q}_n
0	0
1	X

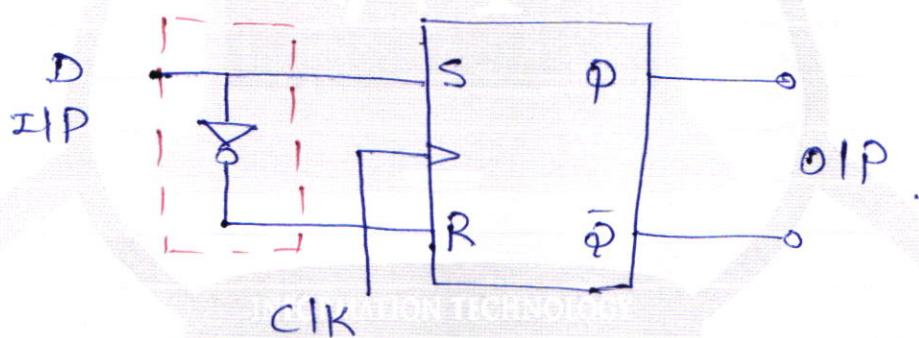
$$S = D$$

K-map for R

D	\bar{Q}_n
X	1
0	0

$$R = \bar{D}$$

Logic Diagram



Ex2] conversion of JK to T FIF

→ step 1 → Truth Table

T	\bar{Q}_n	Q_{n+1}	J	K
0	0	0	0	X
1	0	1	1	X
1	1	0	X	1
0	1	1	X	0

← Excitation Table → for T ← Excitation Table for JK →



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Academic Year: _____

Step II: — k-map & simplification

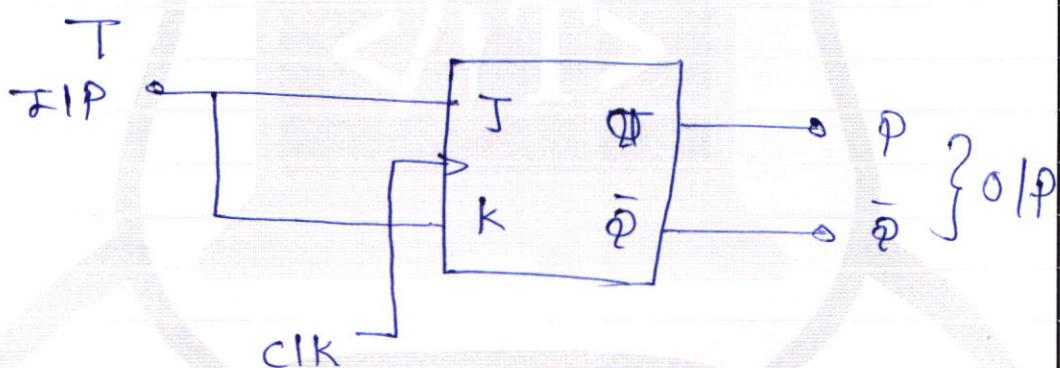
for-J	
0	X
1	X

$$J = K$$

for-K	
X	0
X	1

$$K = T$$

Step III: — logic diagram



Ex 3] Conversion of SR FIF to T FIF

→ Step I: — Truth Table

TIP's			OIP's	
T	Q _n	Q _{n+1}	S	R
0	0	0	0	X
1	0	1	1	0
1	1	0	0	1
0	1	1	X	0



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Step II : - k-map & simplification

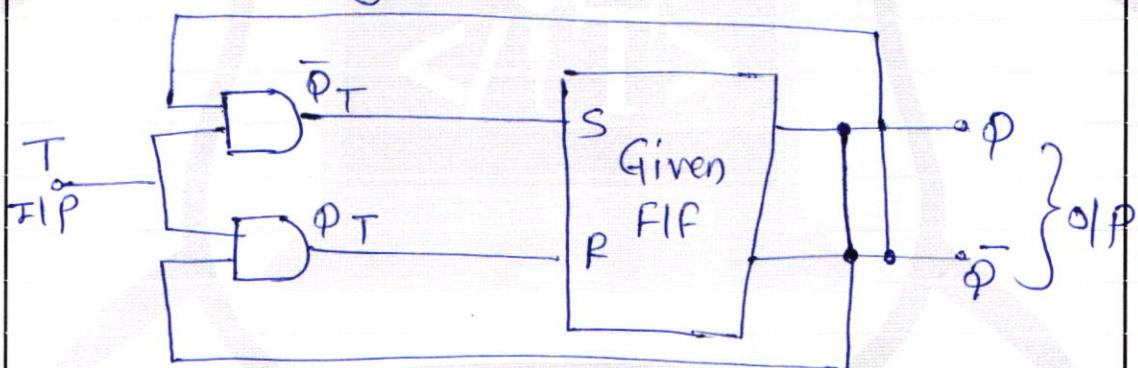
		For S	
		0	1
0		0	X
1	0	1	0
1	1		

		For R	
		0	1
0		X	0
1	0	0	1
1	1		

$$S = T \bar{\Phi}_n$$

$$R = T \Phi_n$$

Step III: logic diagram



Ex 4] Conversion of SR FIF to JK FIF

Step I I/I/P D/I/P

J	K	Φ_n	$\Phi_n + \bar{I}$	S	R
0	0	0	0	0	X
0	1	0	0	0	X
1	0	0	1	1	0
1	1	0	1	1	0
0	1	1	0	0	1
1	1	1	0	0	1
0	0	1	1	X	0
1	0	1	1	X	0



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Step II: —

K-map for S

J	K ϕ_n	00	01	11	10
0	0	X	0	0	.
1	1	X	0	1	.

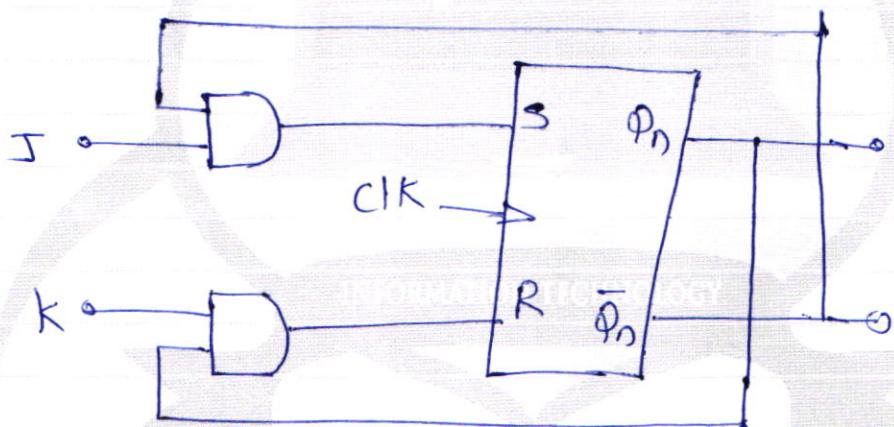
$$S = J\bar{\phi}_n$$

K-map for R

J	K ϕ_n	00	01	11	10
0	X	0	1	X	.
1	0	0	1	0	.

$$R = K\phi_n$$

Step III: :





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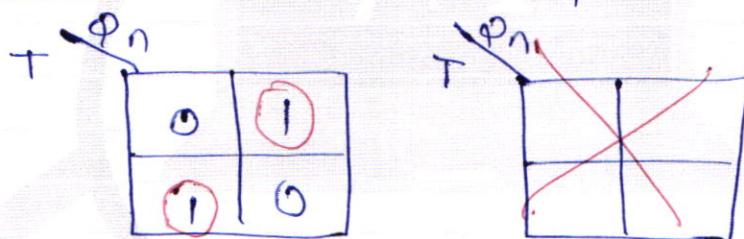
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ex5] conversion of D to T FIF

→ Step I: Truth Table

T	\bar{Q}_n	Q_{n+1}	D
0	0	0	0
1	0	1	1
1	1	0	0
0	1	1	1

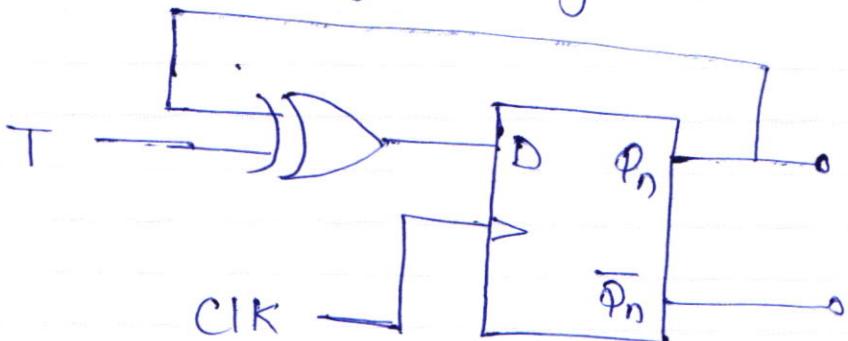
Step II: Kmap & simplification



$$D = T\bar{Q}_n + \bar{T}Q_n$$

$$D = T \oplus Q_n$$

Step III: Logic diagram





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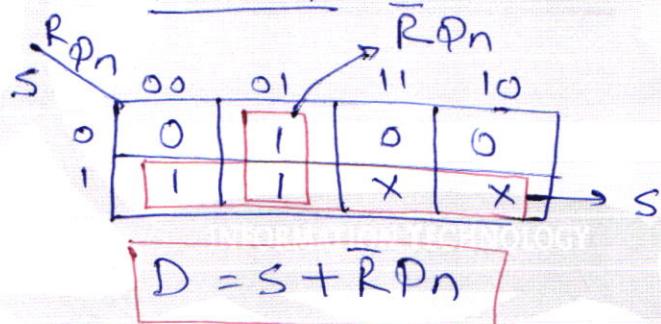
Academic Year: _____

Ex 6] D FIF to SR FIF Conversion

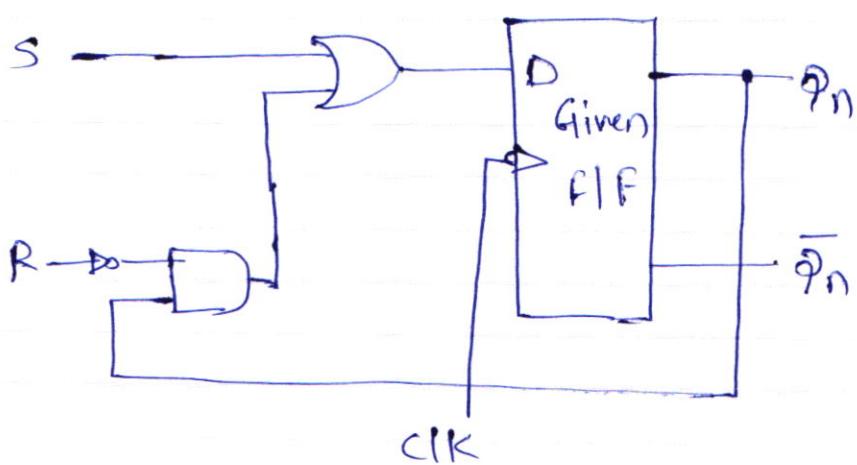
→ Step I :- Truth Table

S	R	Q_n	Q_{n+1}	D
0	0	0	0	0
0	1	0	0	0
1	0	0	1	1
0	1	1	0	0
0	0	1	1	1
1	0	1	1	1

Step II K-map



Step III: Logic diagram for D to SR FIF





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Assignment example

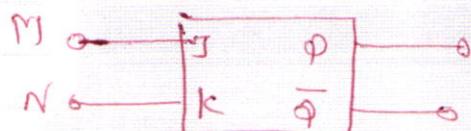
1] T FIF to SR FIF

2] D FIF to J-K FIF

3] JK FF to SR FIF

ex 4] JK FIF to D FIF

ex 5] Consider the MN FIF as shown in Fig. obtain its characteristics table, characteristics eqⁿ & excitation table



⇒ Characteristics Table

N	M	Q _n	Q _{n+1}
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



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Excitation Table

N	M	$\bar{\Phi}_n$	Φ_{n+1}	J	K
0	0	0	1	1	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	1	X	0
1	0	0	1	1	X
1	0	1	0	X	1
1	1	0	0	0	X
1	1	1	0	X	1

K-map

$M_{\bar{\Phi}_n}$

1	X	X	0
1	X	X	0

$$J = \overline{M}$$

M_{Φ_n}

X	0	0	X
X	1	1	X

$$K = N$$

Characteristic eqⁿ

$$\Phi_{n+1} = \overline{M}\Phi_n + N\bar{\Phi}_n$$

* APPN OF FIR

- 1] In registers
- 2] In counters
- 3] In memory element

Shift Register

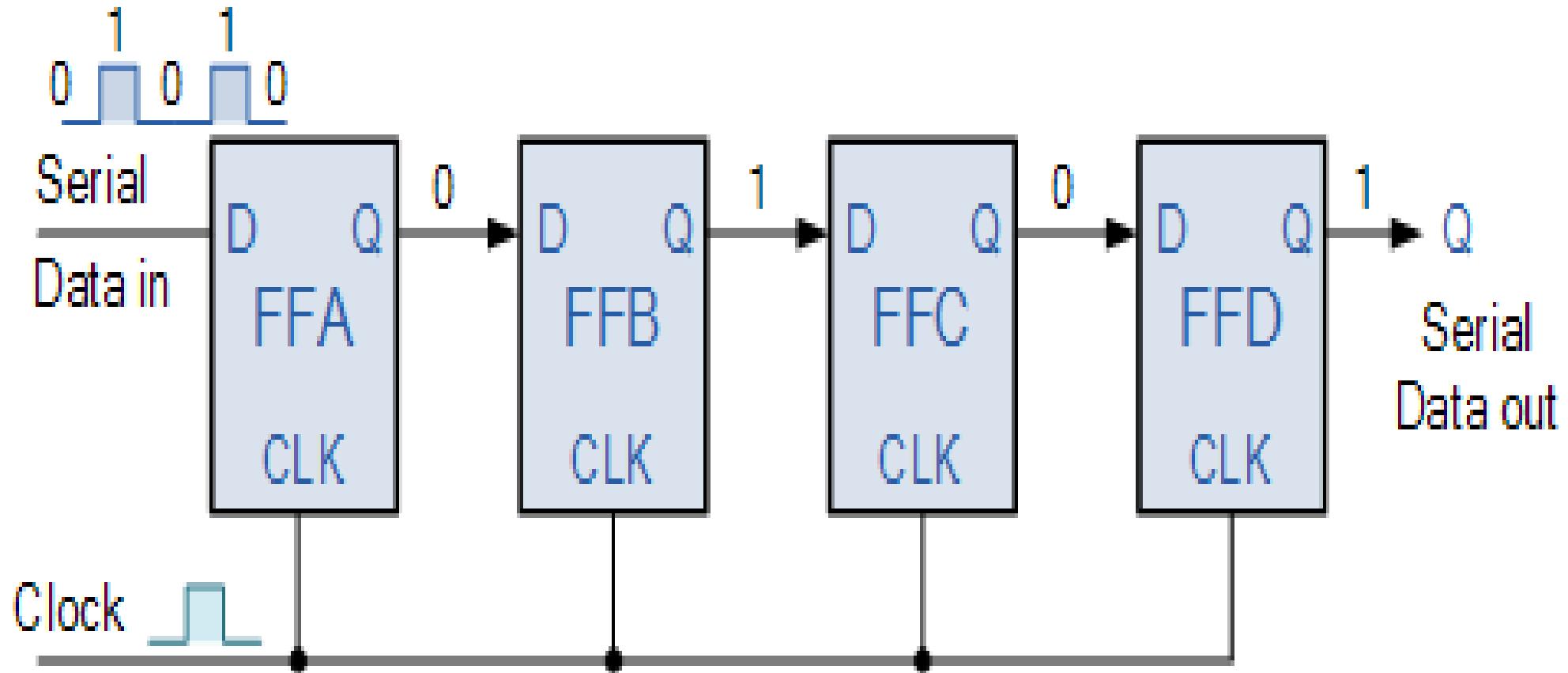
Introduction

- The **Shift Register** is another type of sequential logic circuit that can be used for the storage or the transfer of data in the form of binary numbers.
- This sequential device loads the data present on its inputs and then moves or “shifts” it to its output once every clock cycle, hence the name **Shift Register**.
- A shift register basically consists of several single bit “D-Type Data Latches”, one for each data bit, either a logic “0” or a “1”, connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.

Basically shift registers are of 4 types

1. Serial In Serial Out shift register
2. Serial In parallel Out shift register
3. Parallel In Serial Out shift register
4. Parallel In parallel Out shift register

Serial In Serial Out shift (SISO) register



Truth Table (SISO)

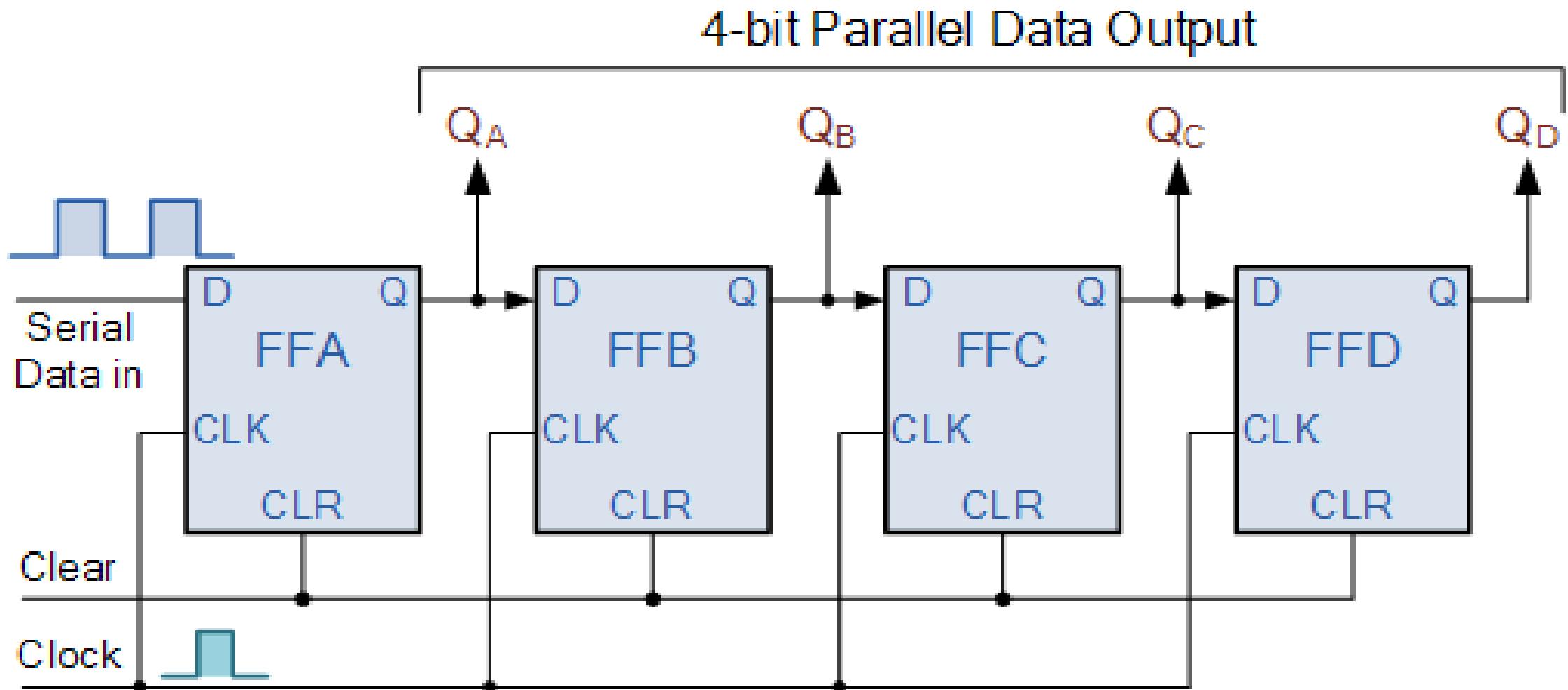
	CLK	$D_n = Q_s$	$Q_s = D_s$	$Q_s = D_i$	$Q_i = D_o$	Q_o
Initially			0	0	0	0
(i)	↓	1	1	0	0	0
(ii)	↓	1	1	1	0	0
(iii)	↓	1	1	1	1	0
(iv)	↓	1	1	1	1	1

→ Direction of data travel

Serial In Serial Out shift (SISO) register

- there is only one output, the DATA leaves the shift register one bit at a time in a serial pattern, hence the name **Serial-in to Serial-Out Shift Register** or **SISO**.
- SISO shift register if the output data is exactly the same as the input data. Well this type of **Shift Register** also acts as a temporary storage device or it can act as a time delay device for the data, with the amount of time delay being controlled by the number of stages in the register, 4, 8, 16 etc or by varying the application of the clock pulses.

Serial-in to Parallel-out (SIPO) Shift Register



Serial-in to Parallel-out (SIPo) Shift Register

- The operation is as follows. Lets assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs Q_A to Q_D are at logic level “0” ie, no parallel data output.
- If a logic “1” is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting Q_A will be set HIGH to logic “1” with all the other outputs still remaining LOW at logic “0”. Assume now that the DATA input pin of FFA has returned LOW again to logic “0” giving us one data pulse or 0-1-0.
- The second clock pulse will change the output of FFA to logic “0” and the output of FFBand Q_B HIGH to logic “1” as its input D has the logic “1” level on it from Q_A . The logic “1” has now moved or been “shifted” one place along the register to the right as it is now at Q_A .

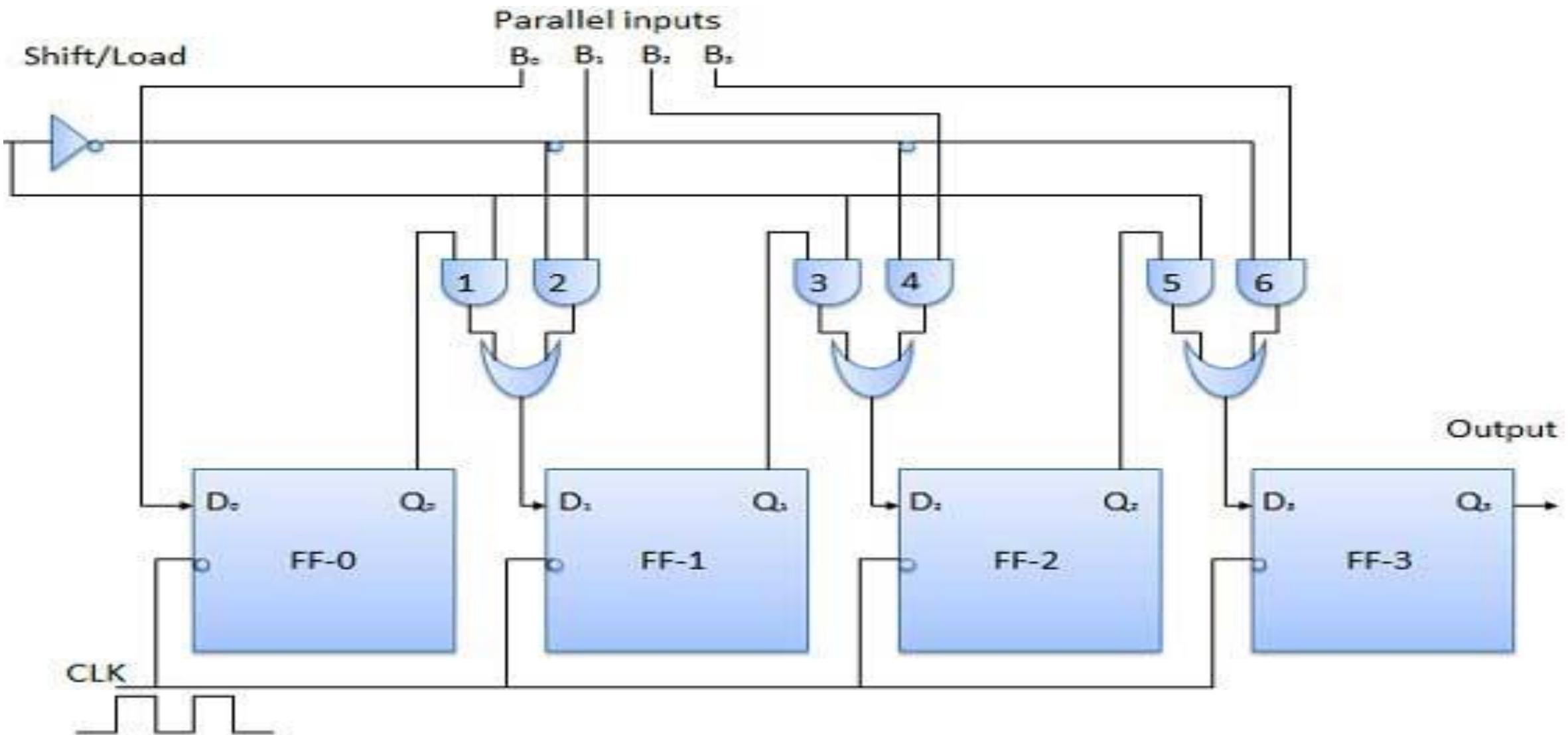
Serial-in to Parallel-out (SIPO) Shift Register

- When the third clock pulse arrives this logic “1” value moves to the output of FFC (Q_C) and so on until the arrival of the fifth clock pulse which sets all the outputs Q_A to Q_D back again to logic level “0” because the input to FFA has remained constant at logic level “0”.
- The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of Q_A to Q_D .
- Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic “1” through the register from left to right as follows.

Parallel-in to Serial-out (PISO) Shift Register

- The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins P_A to P_D of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present at P_A to P_D .
- This data is outputted one bit at a time on each clock cycle in a serial format. It is important to note that with this type of data register a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.

Parallel-in to Serial-out (PISO) Shift Register



Parallel-in to Serial-out (PISO) Shift Register

- In this mode the bits are entered in Parallel into a shift register.
- This ckt is four bit PISO register.
- Output of Previous FF is connected to the input of the next one via a combinational ckt.
- The binary input B, B_1, B_2, B_3 is applied through the same combinational ckt.
- There are two modes in which ckt i.e. Shift or Load mode.

Parallel-in to Serial-out (PISO) Shift Register

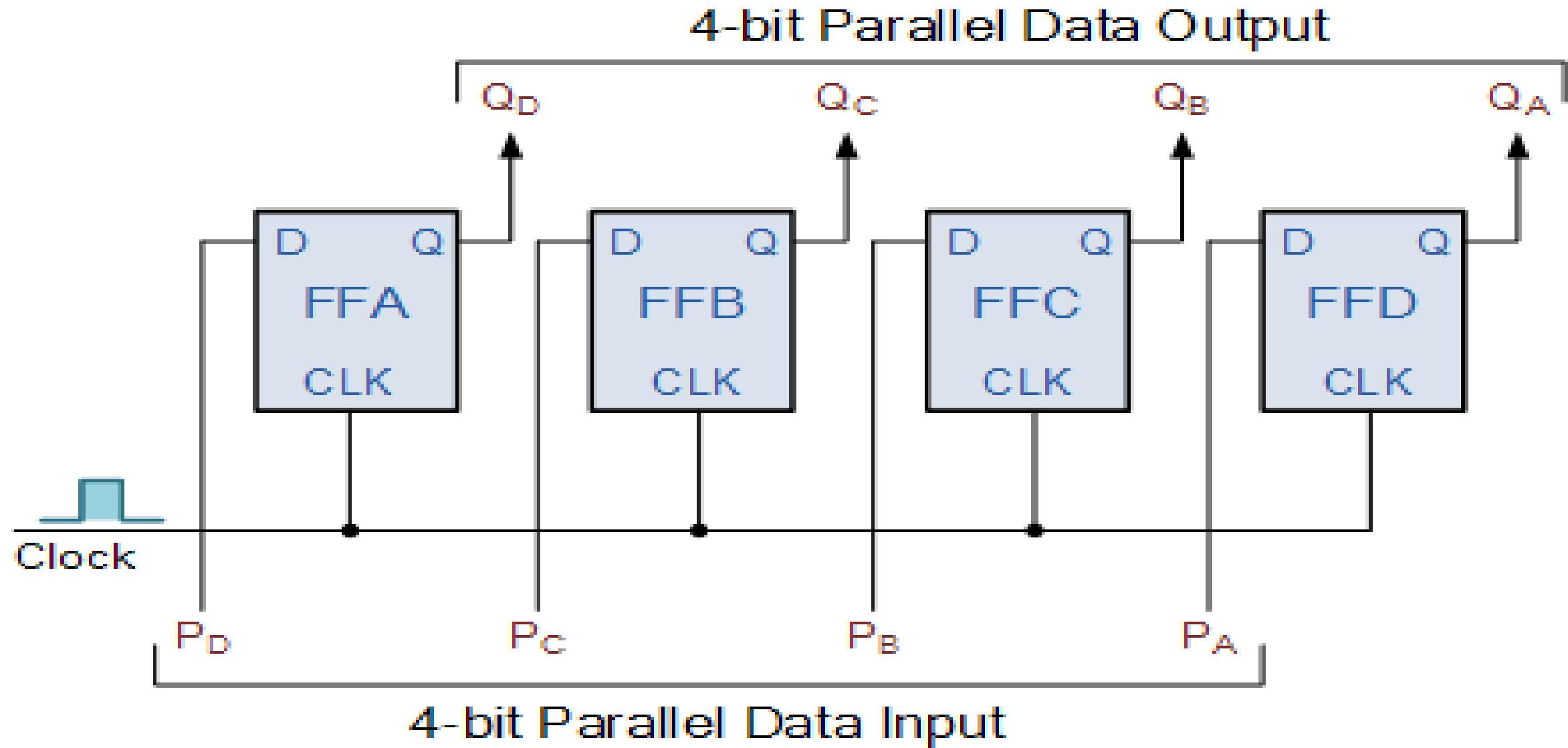
- **Load mode**

When the shift/load bar line is low (0), the AND gate 2, 4 and 6 become active they will pass B_1 , B_2 , B_3 bits to the corresponding flip-flops. On the low going edge of clock, the binary input B_0 , B_1 , B_2 , B_3 will get loaded into the corresponding flip-flops. Thus parallel loading takes place.

- **Shift mode**

When the shift/load bar line is low (1), the AND gate 2, 4 and 6 become inactive. Hence the parallel loading of the data becomes impossible. But the AND gate 1,3 and 5 become active. Therefore the shifting of data from left to right bit by bit on application of clock pulses. Thus the parallel in serial out operation takes place.

Parallel-in to Parallel-out (PIPO) Shift Register



Parallel-in to Parallel-out (PIPO) Shift Register

- The final mode of operation is the Parallel-in to Parallel-out Shift Register.
- This type of shift register also acts as a temporary storage device or as a time delay device similar to the SISO configuration above.
- The data is presented in a parallel format to the parallel input pins P_A to P_D and then transferred together directly to their respective output pins Q_A to Q_D by the same clock pulse.
- Then one clock pulse loads and unloads the register. This arrangement for parallel loading and unloading is shown Above.

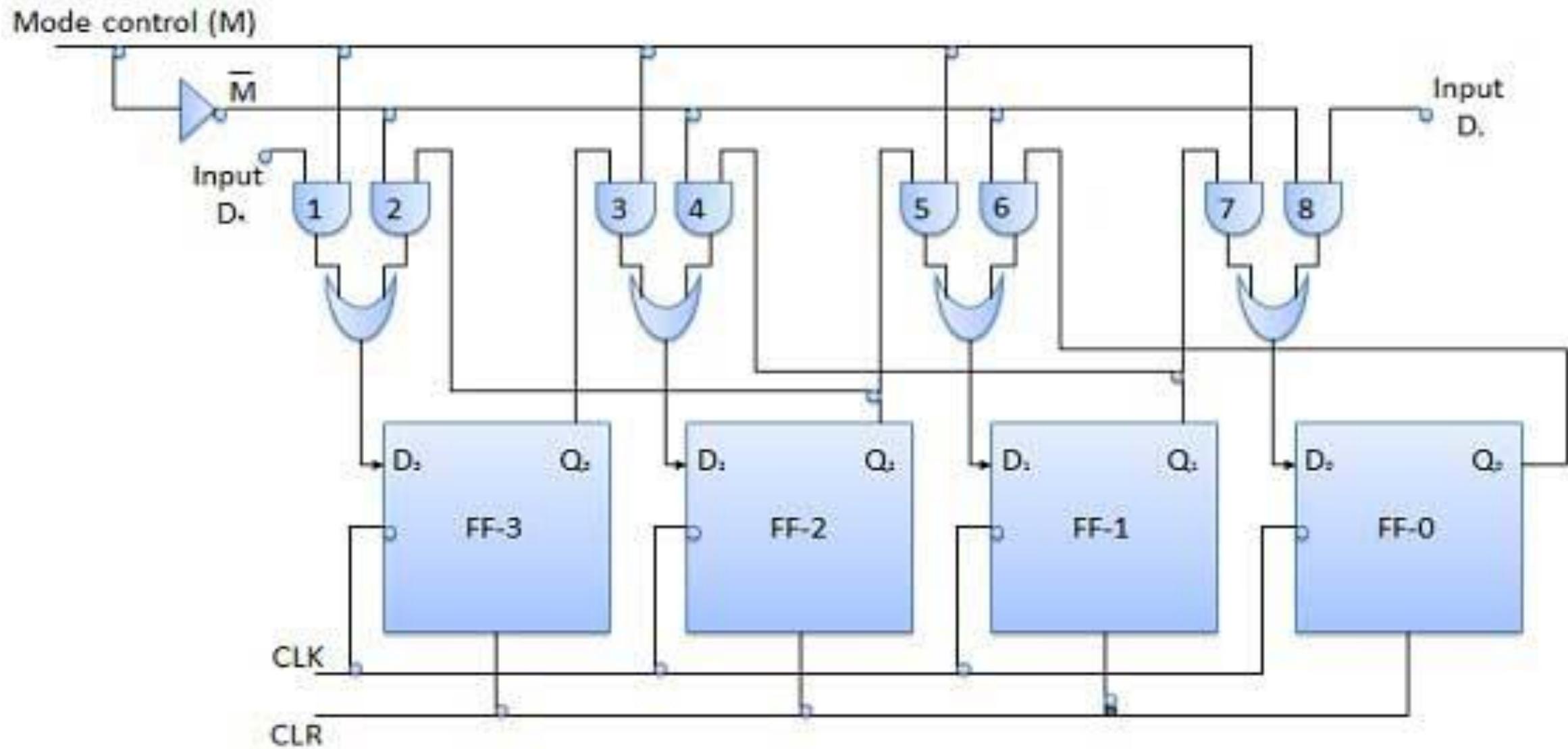
Parallel-in to Parallel-out (PIPO) Shift Register

- The PIPO shift register is the simplest of the four configurations as it has only three connections, the parallel input (PI) which determines what enters the flip-flop, the parallel output (PO) and the sequencing clock signal (Clk).
- Similar to the Serial-in to Serial-out shift register, this type of register also acts as a temporary storage device or as a time delay device, with the amount of time delay being varied by the frequency of the clock pulses. Also, in this type of register there are no interconnections between the individual flip-flops since no serial shifting of the data is required.

Bidirectional Shift Register

- If a binary number is shifted left by one position then it is equivalent to multiplying the original number by 2. Similarly if a binary number is shifted right by one position then it is equivalent to dividing the original number by 2.
- Hence if we want to use the shift register to multiply and divide the given binary number, then we should be able to move the data in either left or right direction.
- Such a register is called bi-directional register. A four bit bi-directional shift register is shown in fig.
- There are two serial inputs namely the serial right shift data input DR, and the serial left shift data input DL along with a mode select input (M).

Bidirectional Shift Register



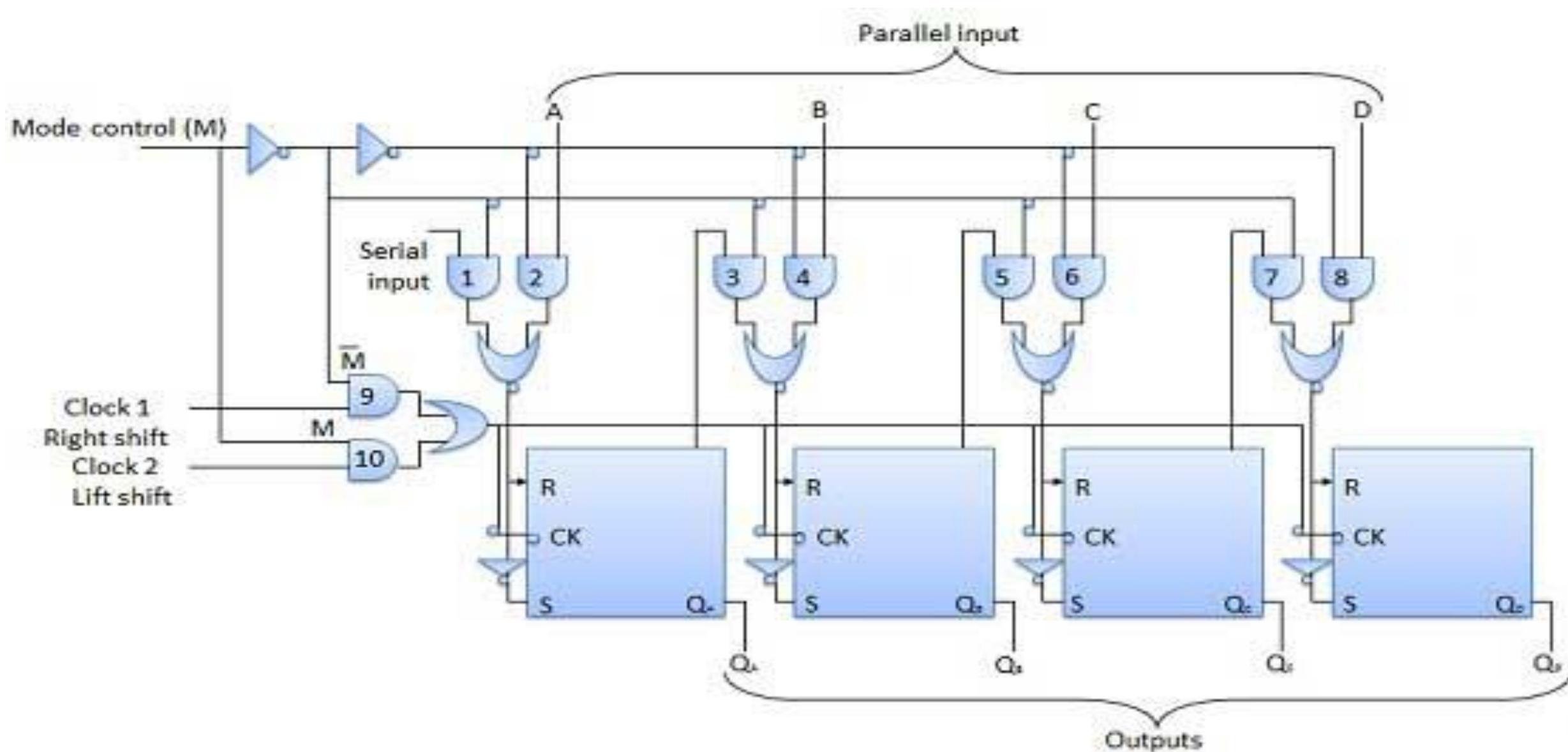
Bidirectional Shift Register

S. N.	Condition	Operation
1	With $M = 1$ – Shift right operation	<p>If $M = 1$, then the AND gates 1, 3, 5 and 7 are enabled whereas the remaining AND gates 2, 4, 6 and 8 will be disabled.</p> <p>The data at D_R is shifted to right bit by bit from FF-3 to FF-0 on the application of clock pulses. Thus with $M = 1$ we get the serial right shift operation.</p>
2	With $M = 0$ – Shift left operation	<p>When the mode control M is connected to 0 then the AND gates 2, 4, 6 and 8 are enabled while 1, 3, 5 and 7 are disabled.</p> <p>The data at D_L is shifted left bit by bit from FF-0 to FF-3 on the application of clock pulses. Thus with $M = 0$ we get the serial left shift operation.</p>

Universal Shift Register

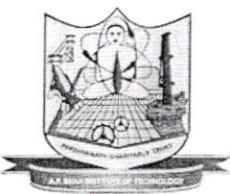
- A shift register which can shift the data in only one direction is called a uni-directional shift register. A shift register which can shift the data in both directions is called a bi-directional shift register. Applying the same logic, a shift register which can shift the data in both directions as well as load it parallelly, is known as a universal shift register. The shift register is capable of performing the following operation –
- Parallel loading
- Left shifting
- Right shifting
- The mode control input is connected to logic 1 for parallel loading operation whereas it is connected to 0 for serial shifting. With mode control pin connected to ground, the universal shift register acts as a bi-directional register. For serial left operation, the input is applied to the serial input which goes to AND gate-1 shown in figure. Whereas for the shift right operation, the serial input is applied to D input.

Universal Shift Register



Applications of Shift Registers

- Temporary data storage
- Data transfer
- Data manipulation
- As counters.
- Shift registers are used in computers as memory elements. All the digital systems need to store large amount of data, in an efficient manner; there we use storage elements like RAM and other type of registers.
- Many of the digital system operations like division, multiplication are performed by using registers. The data is transferred through serial shift registers and other type.
- Counters are used as Digital clocks, Frequency counters, Binary counters etc.
- Serial in – serial out register are used for time delays.
- Serial in – parallel out registers are used for converting the data from serial form to parallel form. So these are also called “Serial to parallel converters”.
- Parallel in – serial out registers are used for converting the data from parallel form to serial form. So these are also called “Parallel to serial converters”.



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* Counters: —

- Digital ckt used for counting pulses is known as counter.
- It is sequential ckt.
- It is used for FIF.
- It counts the number of clk pulses.
- It is sometime used for measuring freqn.

⇒ Types of Counters

- 1] Asynchronous counter [Ripple counter]
- 2] Synchronous counter.

Depending on the way in which Counting progress

1] Up Counter :- Count from small to large (big) count.

- O/P goes on increasing as they receive clock pulses.

ex:- Counter will be 0, -1, 2, 3 . . .

2] Down Counter: - count from big to small count.

- O/P goes on decreasing as they receive clock pulses.

ex:- Counter will be 7-6-5-4 . . .



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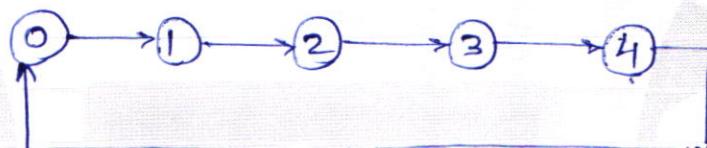
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* Design Counters: —

1] Design module 5 ripple Counter using 3-bit ripple counter

⇒ Step 1: — state diagram of Counter



state diag. of MOD-5 ripple counter

Step 2: — Truth Table for reset logic

State	F1F outputs			O/P of reset logic
	Φ_C	Φ_B	Φ_A	
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	0
6	1	1	0	0
7	1	1	1	0

} valid states } Invalid states

Step 3: k-map for y

Φ_C

1	1	1	1
1	0	0	0

$$y = \overline{\Phi}_C + \overline{\Phi}_B \overline{\Phi}_A$$

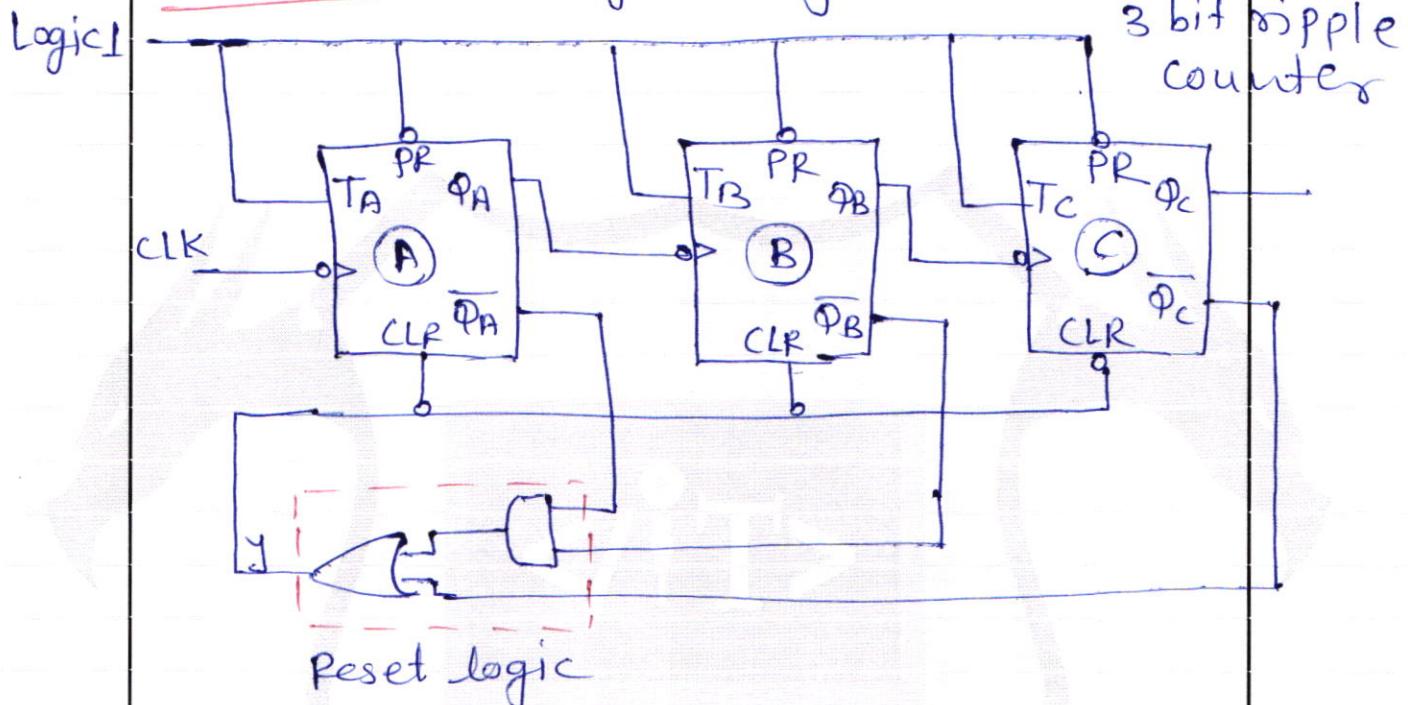


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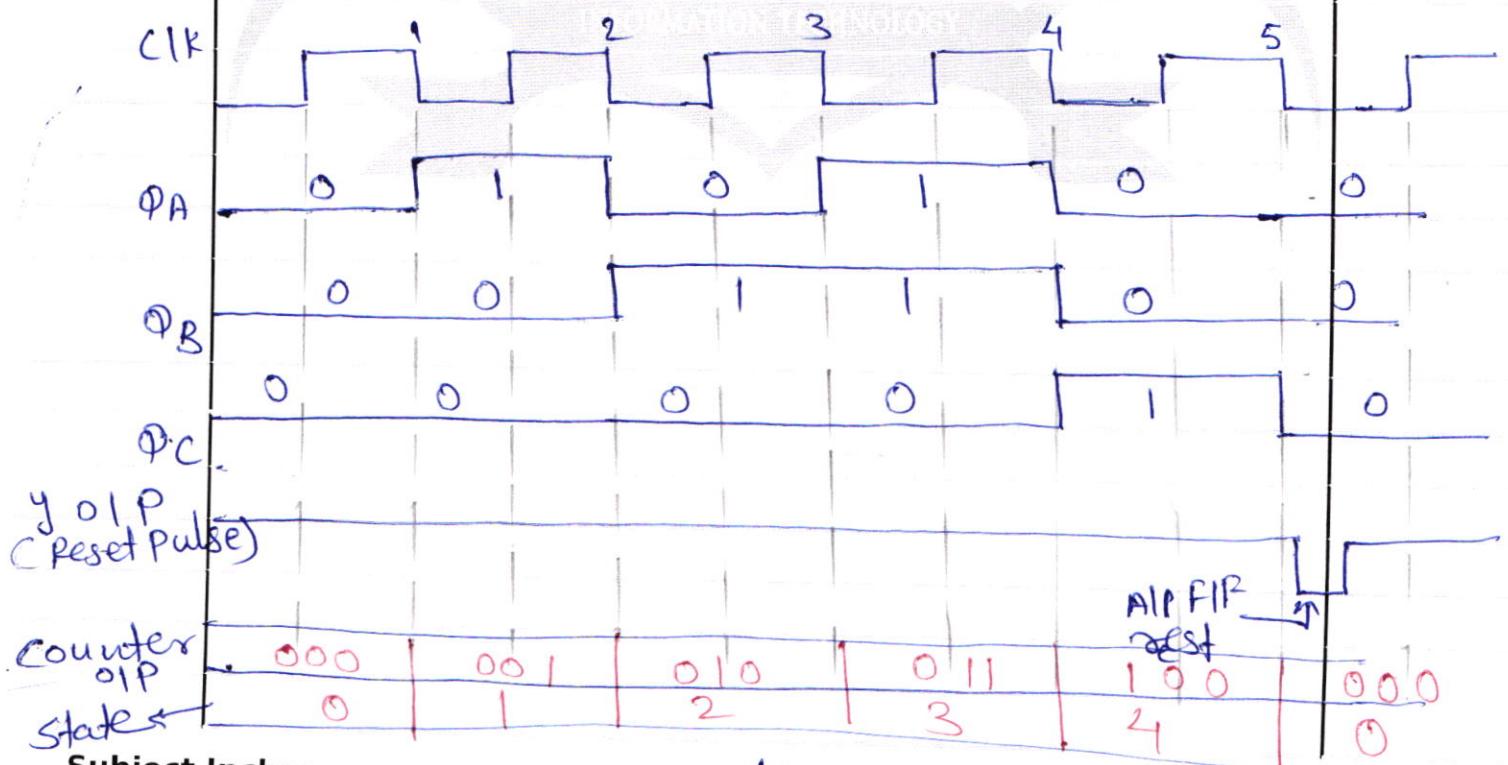
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Step IV :- Logic Diagram



Logic diagram of MOD-5 ripple Counter

Step V - Timing Diagram





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2] MOD - 11 A synchronous Counter, use TFI/F
If the O/P freqn is 11 kHz. what is the clock i/p.?

⇒ Step I :- Truth Table

Q_D	Q_C	Q_B	Q_A	Y
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

} Invalid states

Step II K-map

	$Q_B Q_A$	00	01	11	10
$Q_D Q_C$	00	1	1	1	1
01	1	1	1	1	1
11	0	0	0	0	0
10	1	1	0	1	1

$$y = \bar{Q}_D + \bar{Q}_C \bar{Q}_A + \bar{Q}_C \bar{Q}_B$$

$$y = \bar{Q}_D + \bar{Q}_C (\bar{Q}_A + \bar{Q}_B)$$

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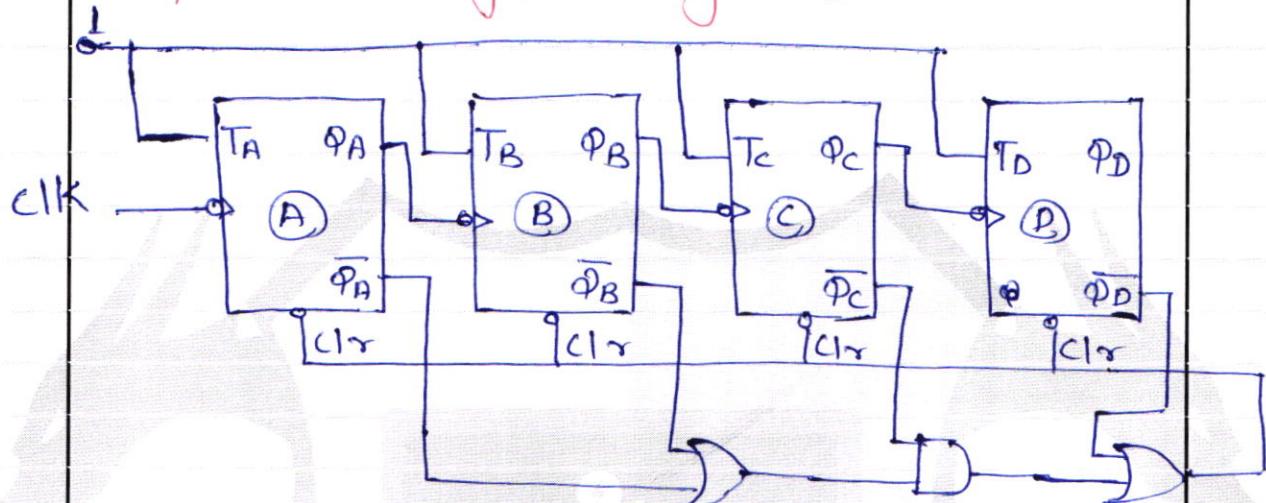


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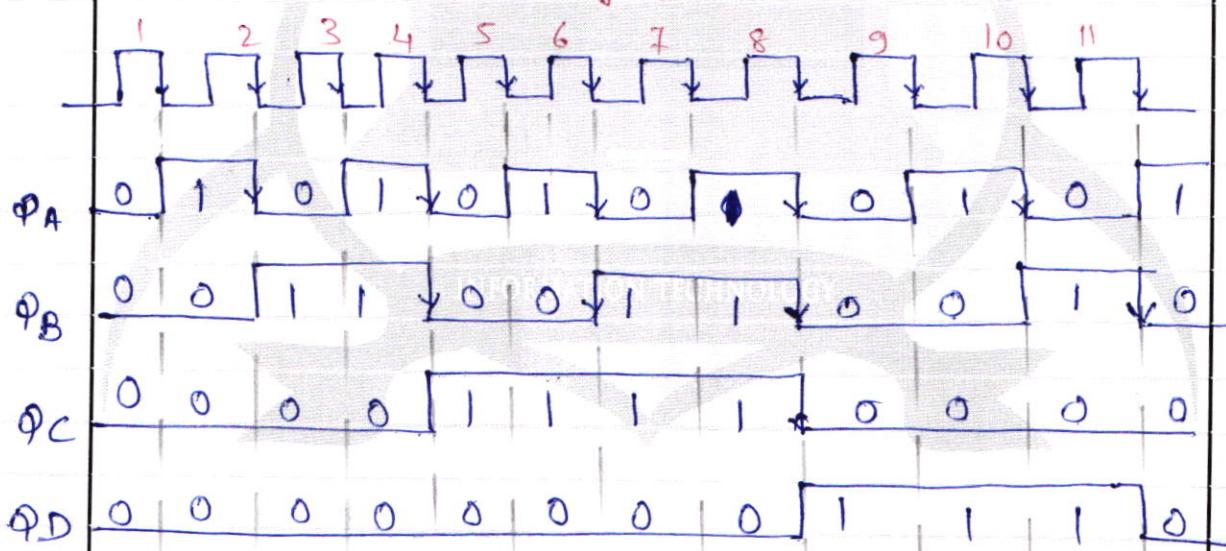
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Step III :- logic Diagram



Step IV :- Timing Diagram



Counter Output State	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	0000
state	0	1	2	3	4	5	6	7	8	9	10	0

In above Counter if O/P freq is 11 kHz
 What is CLK ?

$$F_o = \frac{F_{CLK}}{11} \Rightarrow F_{CLK} = 11 \times F_o = 11 \times 11 = 121 \text{ kHz}$$



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*

up|down Counter (Asynchronous)

- All the FIF's operate in the toggle mode. So either T flip flops or JK FFs are to be used.
- The LSB FIF receives CLK directly.
- But the CLK to every other FIF is obtained from Q or \bar{Q} OIP of the previous FIF.

Up Counting Mode ($M=0$)

Down Counting Mode ($M=1$)

ex 1] Design 3-bit binary up/down ripple counter.

⇒ Let the setⁿ of Q & \bar{Q} OIP of the preceding FF be controlled by the mode control iIP M such that.

If $M=0$ up counting. So Connect Q to CLK

If $M=1$ Down counting. " " \bar{Q} to CLK.

Now, design a combinational logic to satisfy all the requirements stated above.



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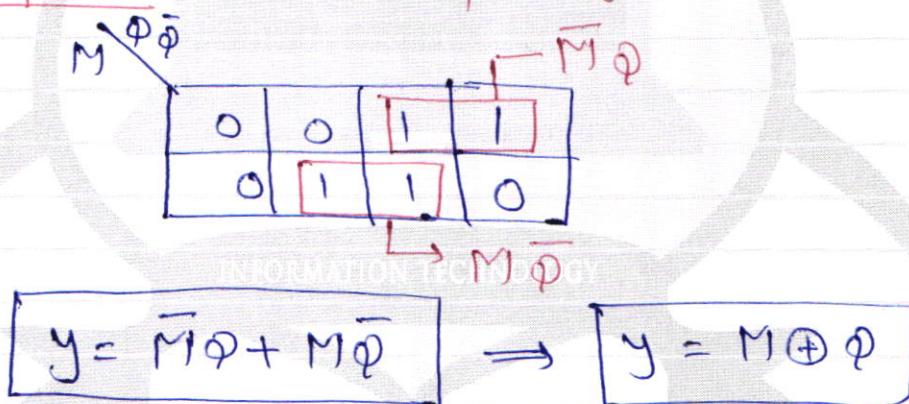
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Step I : Truth table for mode control

		FIP	OIP	
M	Q	\bar{Q}	Y	
0	0	0	0	$y = Q$
	0	1	0	
	1	0	1	
	1	1	1	
1	0	0	0	$y = \bar{Q}$
	0	1	1	
	1	0	0	
	1	1	1	

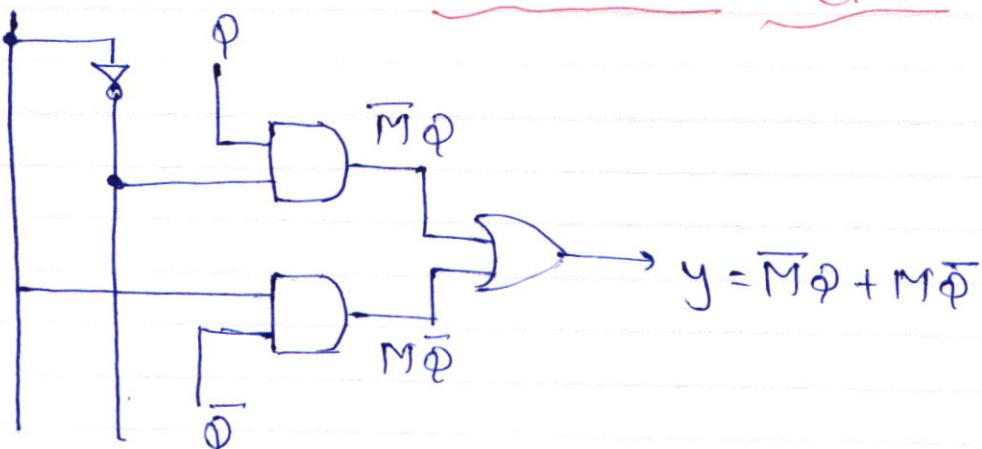
Up Counting
Down Counting

Step II : k-map & logic ckt



M

Combinational Ckt



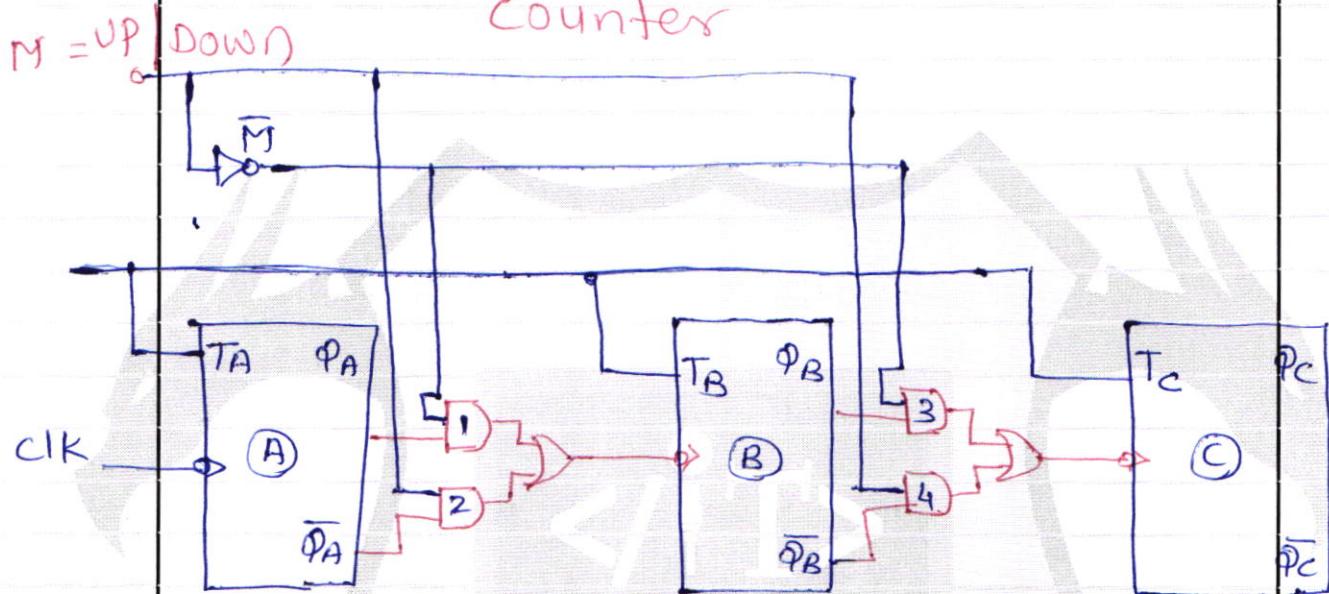


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Step III :- Logic diag. of 3-bit up/down Counter



operation \Rightarrow 3-bit up down ripple counter

I] with $M=0$ (Up counting mode)

a] $M=0 \quad \bar{M}=1$

then the AND gate 1 & 3 will be enabled whereas the AND gates 2 & 4 will be disabled

b] with $M=1$ (Down counting mode)

IF $M=1$

then

AND gate 2 & 4 \rightarrow enabled

" " 1 & 3 \rightarrow disabled



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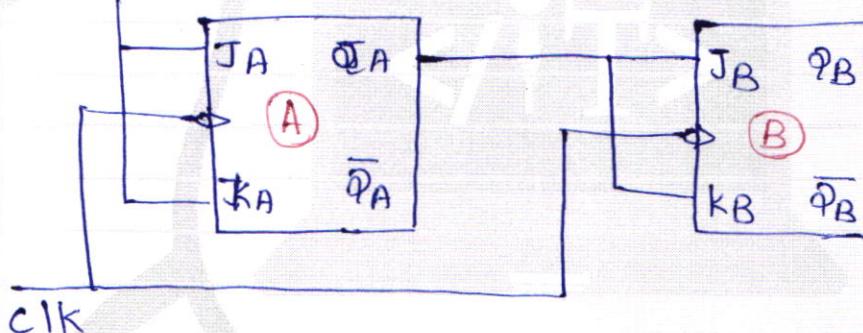
Synchronous Counter:

- When a counter is clocked such that each FF will triggered at the same time the counter is called as Synchronous Counter.

1]

2-bit Synchronous Counter:

Logic I



- Here CLK is connected in "I" to CLK i/p of both FF
- Q_n O/P of First stage is connected J & K i/p of second stage.
- Initially Q_A = Q_B = 0, at -ve edge of CLK signal.
- FFA will toggle as J_A = K_A = 1 O/P Q_A = 1 Q_B = 0
because J_B = K_B = 0



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- At 2nd stage -ve edge of clk pulse both FF will toggle as both have toggle cond'n at their i/p.
- Thus, after 2nd clk pulse $Q_A = 0$ & $Q_B = 1$ & so on.

Initially $Q_A, Q_B = 00$

After 1st CLK pulse $Q_A, Q_B = 01$

" 2nd " " $Q_B, Q_A = 10$

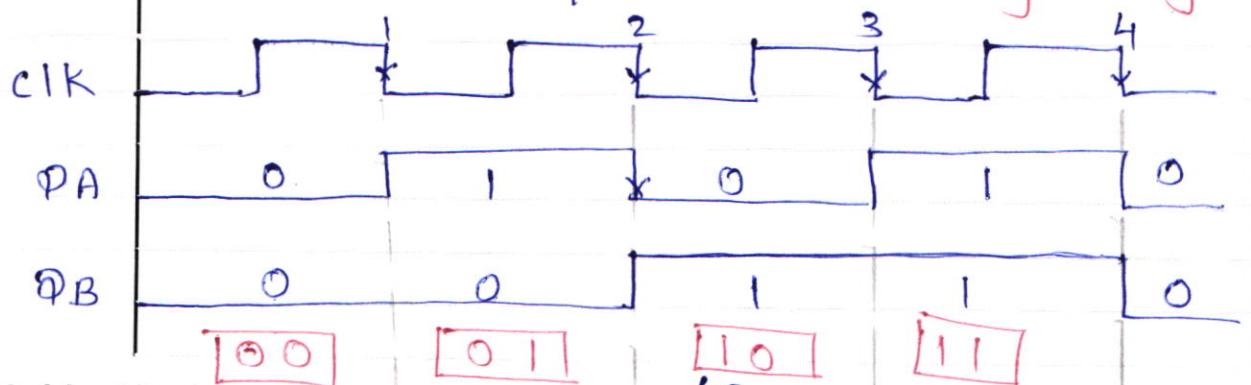
" 3rd " " $Q_B, Q_A = 11$

" 4th " " $Q_B, Q_A = 00$

CLK	Counter Output	
	Q_B (MSB)	Q_A (LSB)
Initially	0	0
1	0	1
2	1	0
3	1	1
4	0	0

oper'n of 2-bit
synchronous
counter

Timing diagram





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*

Modulo - N Synchronous Counters

steps

- 1] Decide the no. of FFs & type of FF to be used.
- 2] Write the ckt excitation table
- 3] From the ckt excitation table write down the k-maps & obtain simplified expressions for the o/p's.
- 4] Draw the logic diagram & timing diagram.

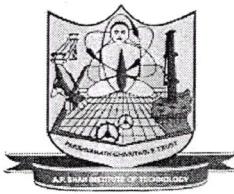
ex 1] Design MOD 5- Synchronous Counter using T FIF

→ step I: The no. of states is 5 so, need 3 FIF & T FF is used

$$2^3 = 8$$

step 2 Excitation table TFF

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0



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Excitation Table for Counter

Present state			Next state			FF IIPs.		
Φ_n			Φ_{n+1}			T_c	T_B	T_A
Φ_C	Φ_B	Φ_A	Φ_{C+1}	Φ_{B+1}	Φ_{A+1}			
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	0
1	0	0	0	0	0	1	0	0
1	0	1	0	0	0	1	0	1
1	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	1	1

Step 3 → K-map

Φ_C	$\Phi_B \Phi_A$	$\Phi_B \Phi_A$
0	0 0	1 0
1	1 1	1 1

TECHNOLOGY

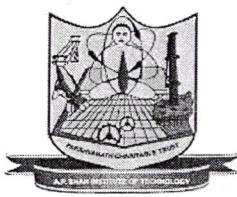
$$T_C = \Phi_C + \Phi_B \Phi_A$$

Φ_C	$\Phi_B \Phi_A$	$\bar{\Phi}_C \Phi_A$
0	0 1	1 1
0	0 0	1 1

$$T_B = \bar{\Phi}_C \Phi_A + \Phi_C \Phi_B$$

Φ_C	$\bar{\Phi}_C \Phi_A$	$\Phi_C \Phi_B$
1	1 1	1 1
0	1 1	0

$$T_A = \Phi_A + \bar{\Phi}_C$$



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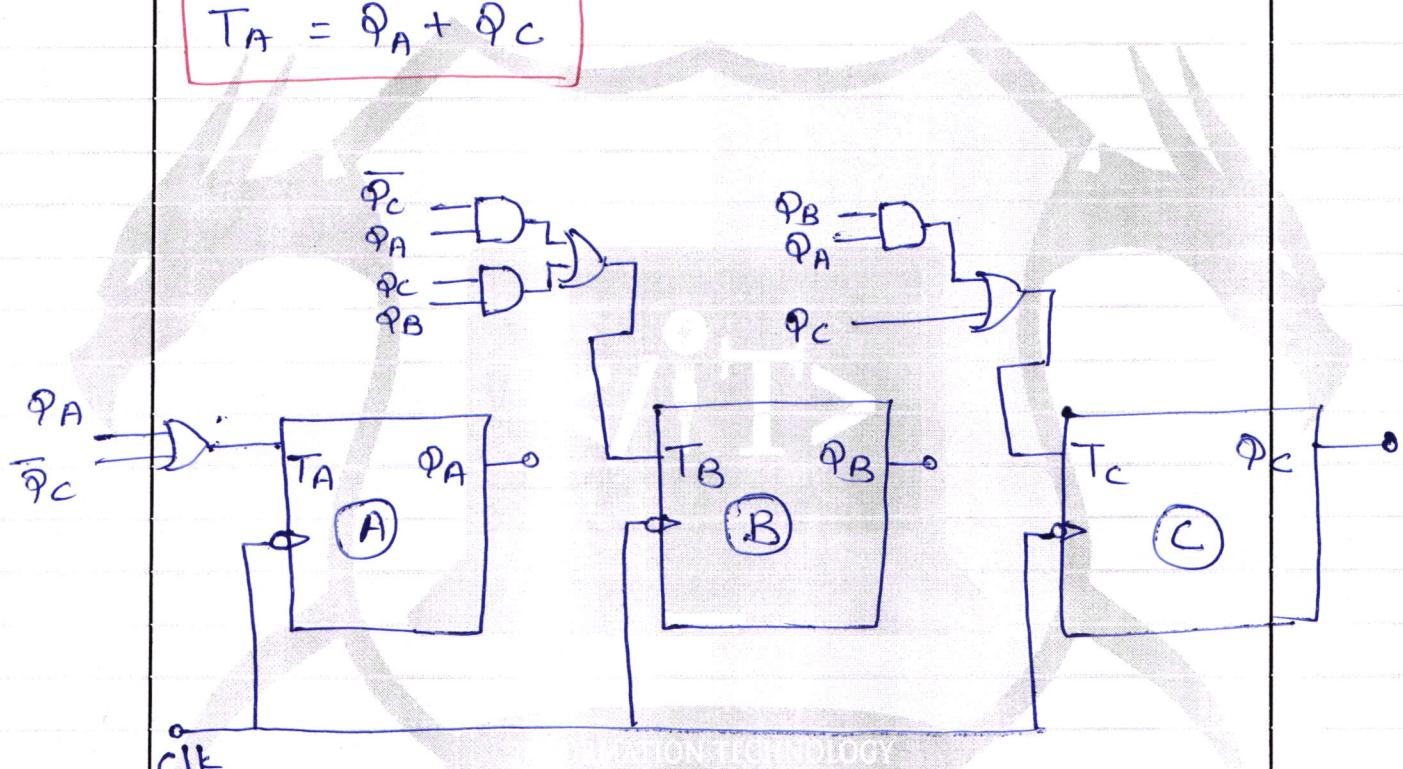
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Step 4 logic diagram.

$$T_C = \bar{Q}_C + Q_B Q_A$$

$$T_B = \bar{Q}_C Q_A + Q_C Q_B$$

$$T_A = Q_A + \bar{Q}_C$$



MOD-5 Synchronous Counter using T FIF



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* up/down synchronous counter:-

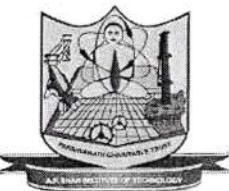
ex:- 3-bit updown synchronous counter
using TFF.

→ step I:- ckt excitation table

Mode M	Present state			next state			F	I	P	S
	Φ_C	Φ_B	Φ_A	Φ_{C+1}	Φ_{B+1}	Φ_{A+1}	T_c	T_B	T_A	
0	0	0	0	0	0	1	0	0	1	
0	0	0	1	0	1	0	0	1	1	
0	0	1	0	0	1	1	0	0	1	
0	0	1	1	1	0	0	1	1	1	
0	1	0	0	1	0	1	0	0	1	
0	1	0	1	1	1	0	0	1	1	
0	1	1	0	0	1	1	1	0	0	
0	1	1	1	1	0	0	0	1	1	
1	0	0	0	1	1	1	1	1	1	
1	0	0	1	0	0	0	0	0	1	
1	0	1	0	0	0	1	0	1	1	
1	0	1	1	0	1	0	0	0	1	
1	1	0	0	0	1	1	1	1	1	
1	1	0	1	1	0	0	0	0	1	
1	1	1	0	1	0	1	0	1	1	
1	1	1	1	1	1	0	0	0	1	

up
Counting

Down
Counting



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Step 2: - K-map

$M\bar{Q}_C$	$\bar{Q}_B\bar{Q}_A$	00	01	11	10
00	0 0 1 0	0	0	1	0
01	0 0 1 0	0	0	1	0
11	1 0 0 0	1	0	0	0
10	1 0 0 0	1	0	0	0

$M\bar{Q}_C$	$\bar{Q}_B\bar{Q}_A$	00	01	11	10
00	0 1 1 0	0	1	1	0
01	0 1 1 0	0	1	1	0
11	1 1 0 0	1	1	0	0
10	1 1 0 0	1	1	0	1

$M\bar{Q}_C$	$\bar{Q}_B\bar{Q}_A$	00	01	11	10
00	1 1 1 1	1	1	1	1
01	1 1 1 1	1	1	1	1
11	1 1 1 1	1	1	1	1
10	1 1 1 1	1	1	1	1

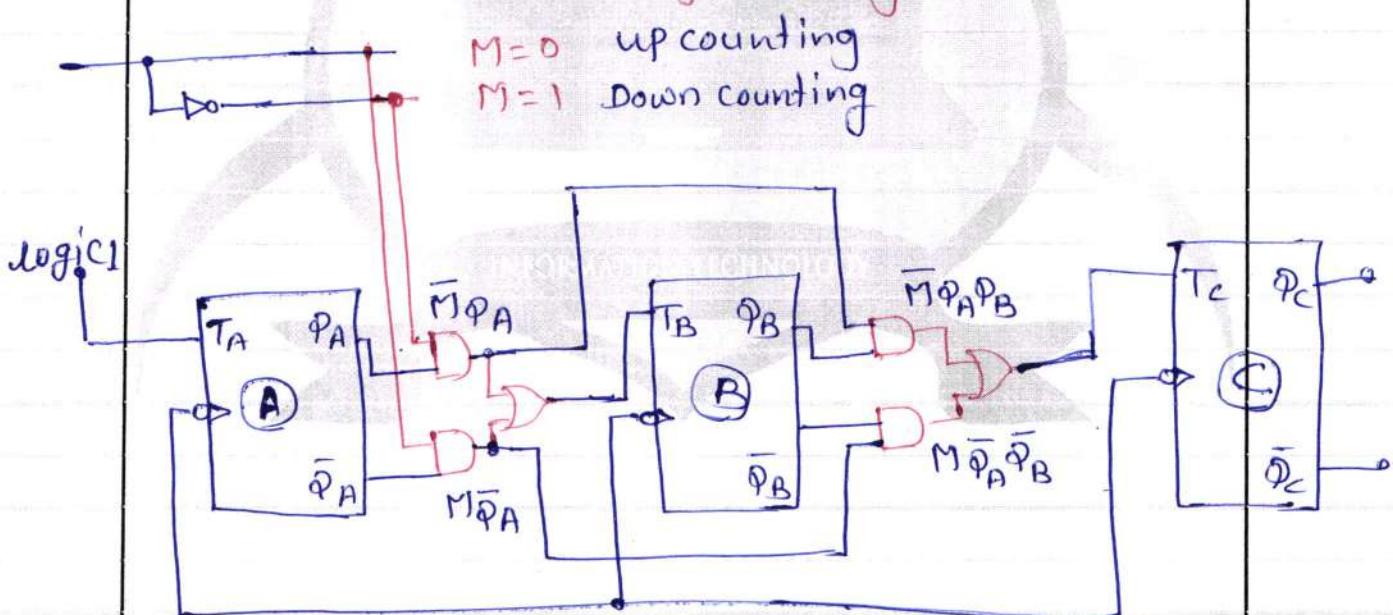
$$T_C = \bar{M}Q_B\bar{Q}_A + M\bar{Q}_B\bar{Q}_A$$

$$T_B = \bar{M}Q_A + M\bar{Q}_A$$

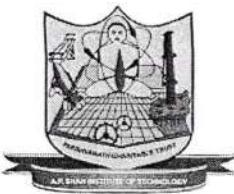
$$T_A = 1$$

$$= M \oplus Q_A$$

Step 3: - Draw logic diagram



Logic diag of a 3-bit synchronous updown counter.



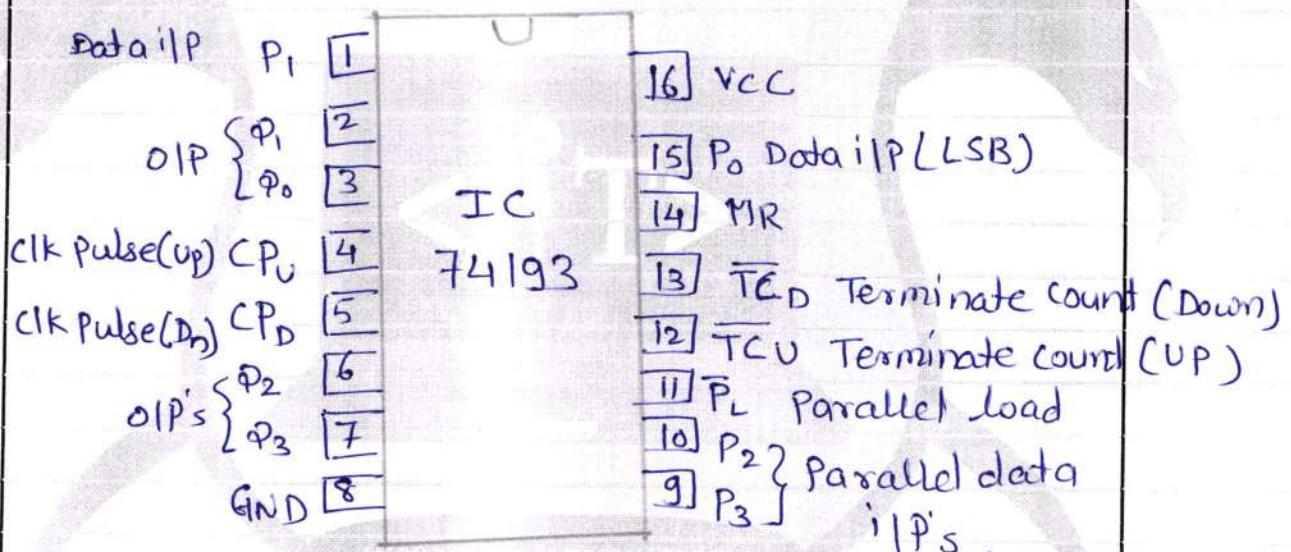
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* up Down Counter IC 74193 :-

- IC 74193 is an UP/Down Modulo - 16 binary counter.



Mode select Table

MR	JIP's	C _{Pu}	C _{PD}	Mode
1	X	X	X	Reset
0	0	X	X	Parallel loading (Preset)
0	1	1	1	No Change
0	1	1	1	Count up
0	1	H	1	Count down

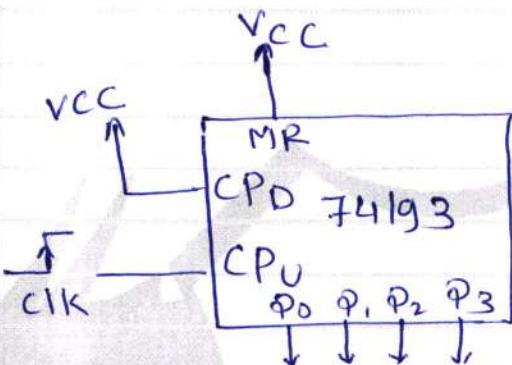


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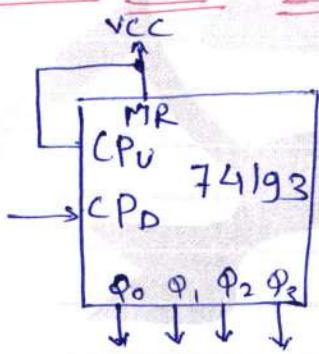
Count up mode :-



- with $MR=0, \overline{PL}=1$ the reset & parallel loading mode are disabled
- Connect CP_D to HIGH to make it inactive & apply the clk pulses to the up counter CLK_{CPU}

- Counter will count 0 to 15. The conn's of 74193 for Count up mode, as shown in fig.

Count down mode :-



- Connect $MR=0, \overline{PL}=1$ to disable the reset & parallel load modes.
- Connect CP_U to HIGH to make it inactive & supply the clk pulses to the down counter CLK_{CP_D} .

- The counter counts down from 15 to 0. The conn's for 74193 for count down mode are as shown in fig.



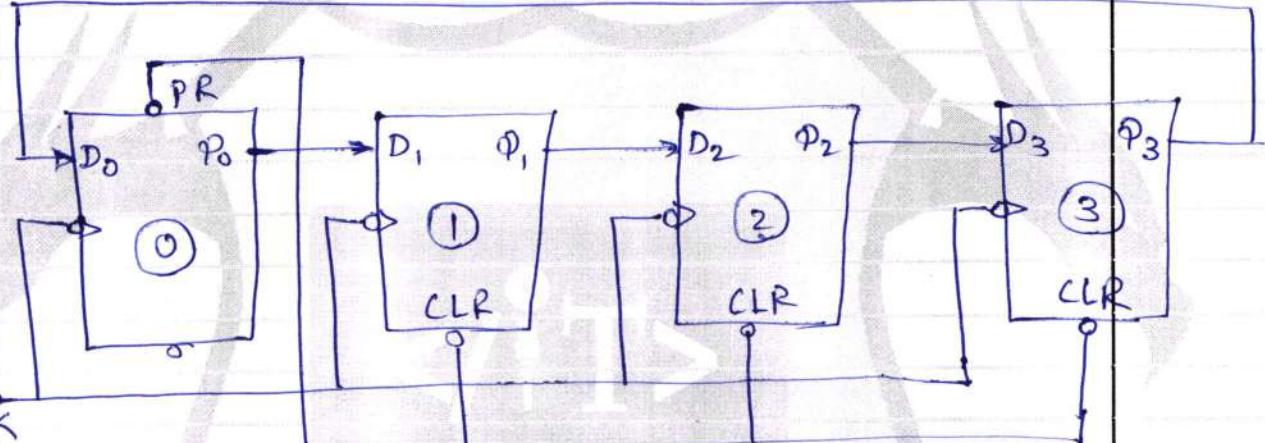
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* Ring Counter: —

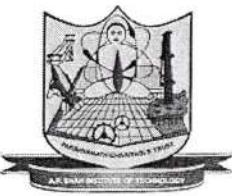
- It is the appl' of shift register called Ring counter.



A - 4 - bit Ring Counter

Truth Table (Oper^n)

Mode	Q_0	Q_1	Q_2	Q_3
1	1	0	0	0
0	0	1	0	0
0	0	0	1	0
0	0	0	0	1
0	1	0	0	0

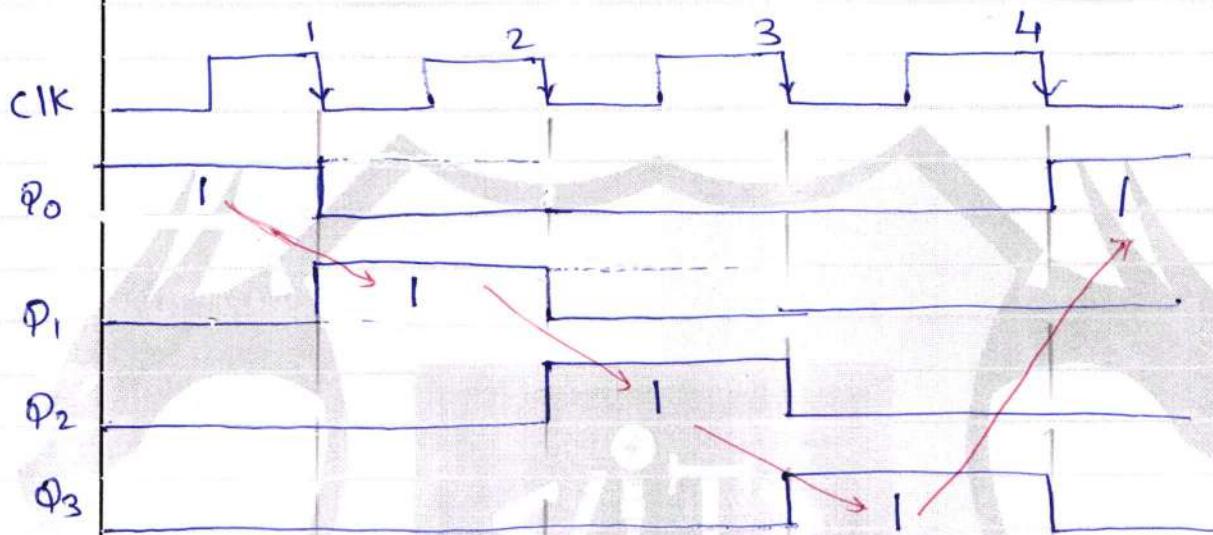


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Waveforms of Ring Counter.



waveforms of a four bit ring counter

- The waveforms shift one bit per clock cycle & forms a ring. Hence the name ring counter.
- The conn's are similar to the conn's for shift right operⁿ, except for one change.
- o/p of FF③ is connected to data input D₀ of FF① Ring counter is a special type of shift register.



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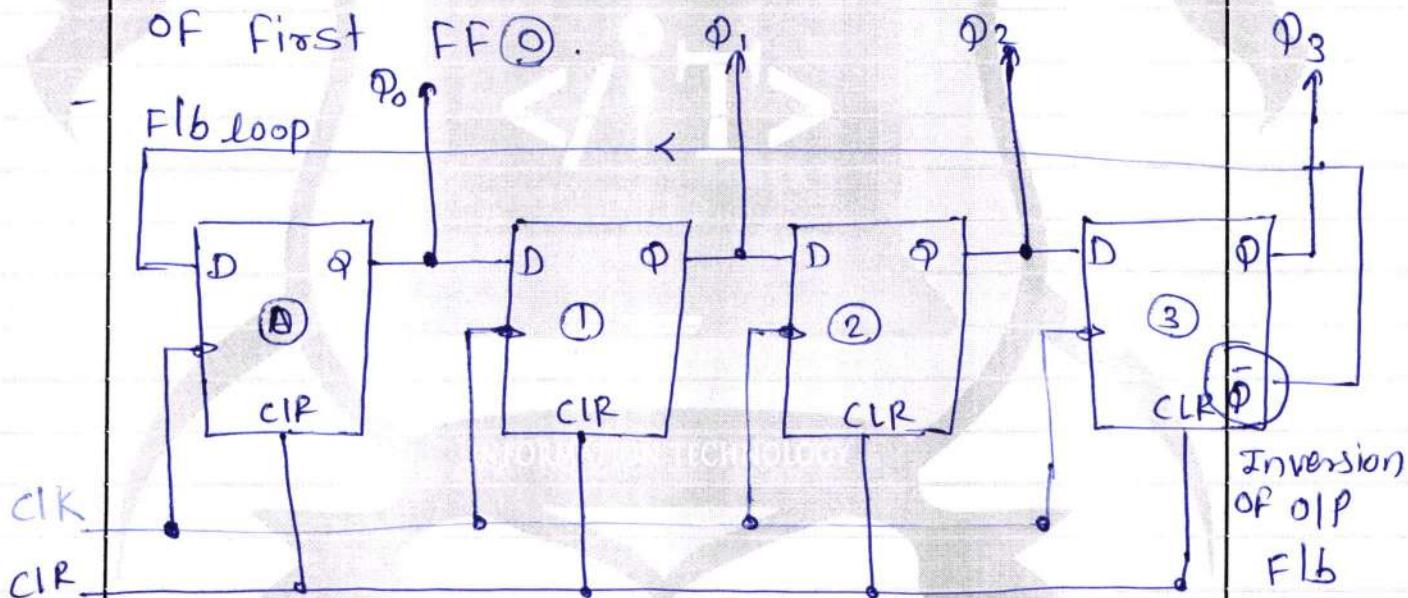
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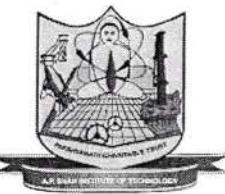
Johnson's Counter (Twisted | switch Tail Ring Counter)

- In the Ring counter the o/p's of FF₃ were connected directly to the i/p's of FF₀
- Feedback inverted o/p \bar{Q} of the FF₃ is now connected back to the i/p D of first FF₀.



Truth Table 4-bit Johnson Counter

Mode	CLK	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0	0
1	1	1	0	0	0
1	2	1	1	0	0
1	3	1	1	1	0
1	4	1	1	1	1
1	5	0	1	1	1
1	6	0	0	1	1
1	7	0	0	0	0

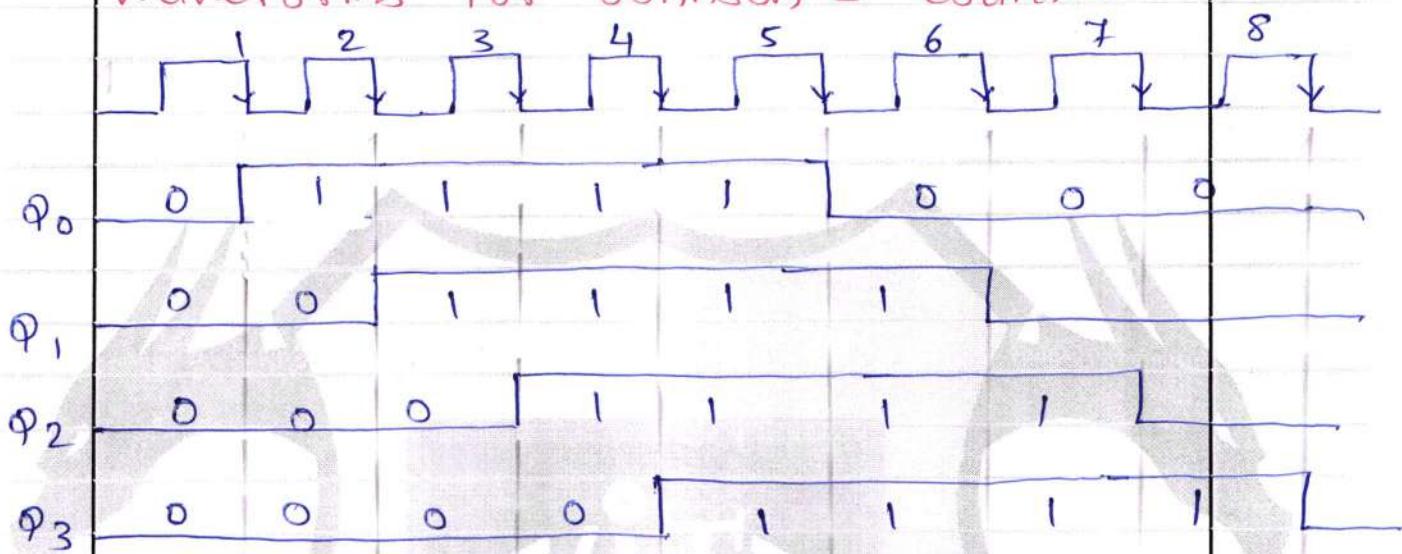


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Waveforms For Johnson's Counter.



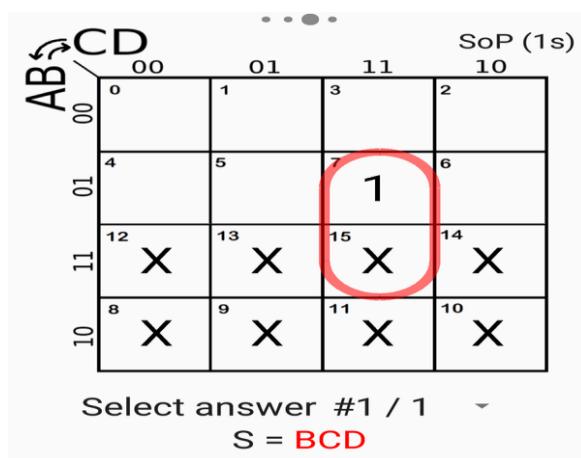
Waveforms of Johnson Counter

Design mod 10 synchronous counter using SR Flip flop

Excitation Table for SR FF									
$Q_n \rightarrow Q_{n+1}$		S_n	R_n						
0	0	0	X						
0	1	1	0						
1	0	0	1						
1	1	X	0						

S	Present State				Next State											
	Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	S_3	R_3	S_2	R_2	S_1	R_1	S_0	R_0
S_0	0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	0
S_1	0	0	0	1	0	0	1	0	0	X	0	X	1	0	0	1
S_2	0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	0
S_3	0	0	1	1	0	1	0	0	0	X	1	0	0	1	0	1
S_4	0	1	0	0	0	1	0	1	0	X	X	X	0	X	1	0
S_5	0	1	0	1	0	1	1	0	0	X	X	X	0	X	1	0
S_6	0	1	1	0	0	1	1	1	0	X	X	X	0	X	1	0
S_7	0	1	1	1	1	0	0	0	1	0	0	0	1	0	1	0
S_8	1	0	0	0	1	0	0	1	X	0	0	0	X	0	X	1
S_9	1	0	0	1	1	0	1	0	X	0	0	0	X	1	0	0

The expression for all four SR flip flops are obtained as below. In following K-map $Q_3Q_2Q_1Q_0 = ABCD$



$$S_3 = Q_2Q_1Q_0$$

		CD		SoP (1s)			
		00	01	11	10		
AB	00	X	X	X	X		
	01	X	X		X		
AB	11	X	X	X	X		
	10			X	X		

Select answer #1 / 1

$$S = 0$$

$$R_3=0$$

		CD		SoP (1s)			
		00	01	11	10		
AB	00			1			
	01	X	X		X		
AB	11	X	X	X	X		
	10			X	X		

Select answer #1 / 1

$$S = \bar{B}CD$$

$$S_2 = \overline{Q_2}Q_1Q_0$$

		CD		SoP (1s)			
		00	01	11	10		
AB	00	X	X		X		
	01			1			
AB	11	X	X	X	X		
	10	X	X	X	X		

Select answer #1 / 1

$$S = BCD$$

$$R_2=Q_2Q_1Q_0$$

		CD		SoP (1s)			
		00	01	11	10		
AB	00	1		3	2	\times	
	01		1	7	6	\times	
AB	11	\times	\times	\times	\times	\times	
	10	8	9	11	10	\times	

Select answer #1 / 1
 $S = \bar{C}D$

$$S_1 = \overline{Q_1}Q_0$$

		CD		SoP (1s)			
		00	01	11	10		
AB	00	\times		1	2		
	01	\times		1	6		
AB	11	\times	\times	\times	\times	\times	
	10	\times		11	10	\times	

Select answer #1 / 1
 $S = CD$

$$R_1 = Q_1 Q_0$$

		CD		SoP (1s)			
		00	01	11	10		
AB	00	1		1	1		
	01	1			1		
AB	11	\times	\times	\times	\times	\times	
	10	1		\times	\times	\times	

Select answer #1 / 1
 $S = \bar{D}$

$$S_0 = \overline{Q_0}$$

AB		CD		SoP (1s)
00	01	11	10	
00	1	1	2	
01	5	7	6	
11	X	X	X	X
10	1	X	X	

Select answer #1 / 1

$$S = D$$

$$R_0 = Q_0$$

The following is the complete logic diagram for decade counter using SR FF.

