Analog IC Design : Assignment-1

Monsoon 2022, CVEST, IIIT Hyderabad (Instructor: Prof. Abhishek Srivastava)

Due date : 14 Aug, 2022 (18:00 hrs)

Instructions:

1. Submit your assignment as a single pdf (Name_RollNo.pdf) at moodle on or before the due date
2. Hand-written/typed (latex/word) submissions are allowed
3. Report should be self explanatory and must carry complete solution - Answers with schematics, netlist, annotated waveforms, inference/discussion on results
4. Print your name and roll number in your graphs using set curplottitle command in your netlist
5. Use the 180 nm TSMC technology file given in tutorial for NGSPICE simulations
6. Any form of **copying/cheating** will result in immediate **F** grade

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1. Install NGSPICE. Run the given net-lists (in tutorial) and observe the results (no need to submit this part).
2. Use the net-list q2_2022.cir and answer the following.
   (a) Draw the schematic corresponding to the given netlist clearly showing absolute sizes of the devices and signal levels, frequency.
   (b) Find 1^{st}, 2^{nd} and 3^{rd} harmonics for small and large input levels.
   (Make a table, write harmonic strengths for different input levels (5-6 values))
   (c) At what input level THD (given by Fourier analysis used in netlist) reaches more than 10%. More than 20%?
   (d) How can you linearise the circuit for the input levels obtained in part (c). Show the modification so that THD reduces for a given input level obtained in part (c). What is the trade-off, explain?
3. Plot I_D vs V_{GS} for $\frac{1.8\mu}{0.18\mu}$ NMOS transistor and estimate its V_T from the graph for the following cases : (Suggested read: Operation and Modeling of the MOS Transistor, second ed, by Tsividis (sections 10.4 and 4.10))
   (a) V_{DS} = 50 mV and V_{GS} is swept from 0 to 1.8 V in a step of 0.1 V
   (b) V_{DS} = 1.8 V and V_{GS} is swept from 0 to 1.8 V in a step of 0.1 V
   (c) Do you observe any difference in V_T values in case (a) and (b) ? If yes, explain why and which one will you use for hand calculations with simple MOS models?
   (d) Estimate technology parameter μC_{ox} from simulations and simple MOS models.
   (e) Plot $\log(I_D)$ vs V_{GS} for V_{DS} = 50 mV and V_{DS} = 1.8 V. Clearly mark subthreshold region on graphs. From plots and using simple exponential relationship $I_D = I_0 exp(\frac{V_{GS}}{\eta V_{Thermal}})$, estimate the process parameter η.
4. Finding f_T of technology node.
   (a) Find the f_T (unity current gain frequency, where $\frac{|i_d|}{|i_g|} = 1$) for the 180 nm TSMC, 180 nm SCL and 130 nm IBM technology. You are expected to show the method, plots and your explanation.

(b) Suggest a method to compare the intrinsic gains ($g_m r_o$) of minimum size transistors for the three model files given to you. Show the schematic, netlist, simulation results with necessary discussions.

5. Using TSMC model file, write a net-list for an analog amplifier using complementary NMOS (5μm/1μm), PMOS (10μm/ 1μm) configuration discussed in class. Use only one DC source $V_{DD} = 1.8$V and generate other voltages using resistive dividers. From simulations find out the bias point and maximum input amplitude for the maximum gain and THD$<10\%$. Report the bias point and the maximum gain. How will you cascade two such amplifiers ? Show the scheme with the exact schematic and simulation results (gain and THD) for the cascaded amplifier also.
