

# A Study of Graph Analytics for Massive Datasets on Distributed Multi-GPUs

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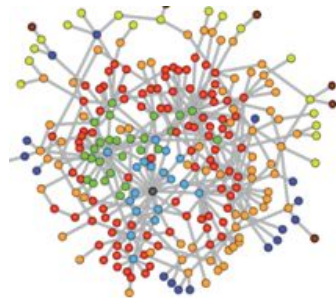
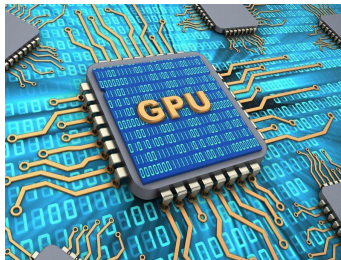
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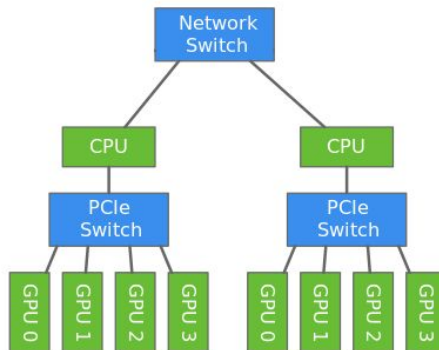
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# Motivation



Graph Analytics



- **Data Growth!**
  - Clueweb is ~ 1 TB  
42.5 B edges
- **Limited GPU Memory**
  - NVIDIA P100 has  
16 GB memory

Distributed Multi-GPUs



# Study of Graph Analytics on Distributed GPUs

## Limitations of Prior Studies

Customized for few applications  
Scalable BFS [**Pan et al. IPDPS'18**]

Focused only for CPUs  
Partitioning study [**Gill et al. PVLDB'18**]

Restricted for single GPUs  
Graph survey [**Shi et al. Comput.'18**]

Not exhaustive  
[**Gluon PLDI'18, Lux PVLDB'17**]

## Contributions of Our Study

Shows impact of partitioning,  
computation, and communication

Analyzes massive graphs using  
state-of-the-art D-IrGL

Provides key suggestions  
for designers

Identifies scope for improvements

# Distributed Graph Analytics

Input Graph  $G$

(1) Partition Graph

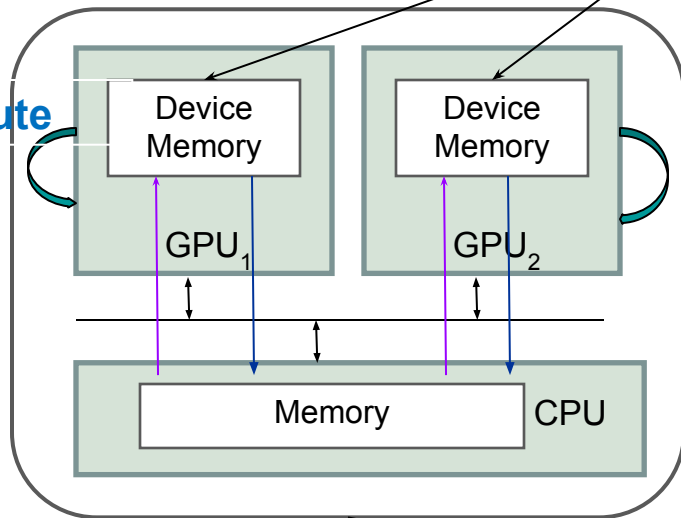
$G_1$

$G_2$

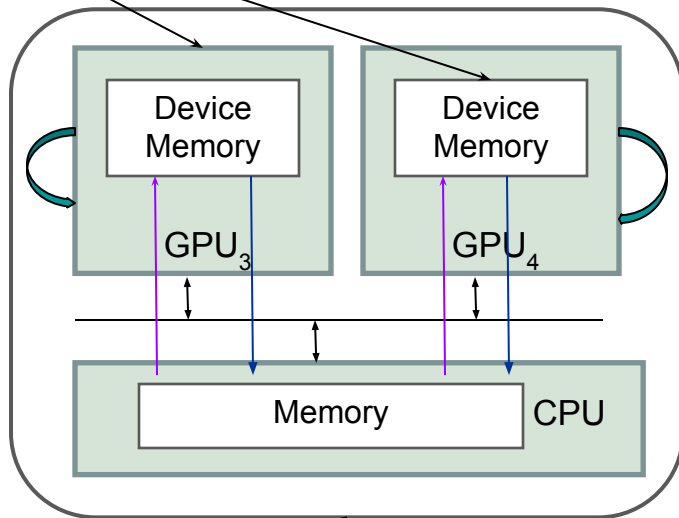
$G_3$

$G_4$

(2) Compute



Node<sub>1</sub>



Node<sub>2</sub>

Network

(3) Synchronize

# Evaluated Techniques in The Study

## Partitioning

CuSP [Hoang et al. IPDPS'19]

- Incoming Edge Cut<sup>1,2</sup> (IEC)
- Outgoing Edge Cut<sup>2,3</sup> (OEC)
- Cartesian Vertex Cut<sup>2,4</sup> (CVC)
- Hybrid Vertex Cut<sup>5</sup> (HVC)

## Computation

- Thread/Warp/CTA Distribution<sup>3,6,7</sup> (TWC)
- Adaptive Load Balancer (ALB)<sup>8</sup>

## Synchronization

- Execution Model
  - Bulk-Synchronous Parallel<sup>1,2,9</sup> (BSP)
  - Bulk-Asynchronous Parallel<sup>10</sup> (BASP)
- Communication
  - Update-Only<sup>2</sup>
  - All-Shared<sup>1</sup>

<sup>1</sup>Lux PVLDB'17, <sup>2</sup>Gluon PLDI'18, <sup>3</sup>Gunrock IPDPS'17, <sup>4</sup>Boman et al. SC'13, <sup>5</sup>PowerLyra EuroSys' 15, <sup>6</sup>IrGL OOPSLA'16, <sup>7</sup>Merill et al. PPOPP'12, <sup>8</sup>Jatalla et al. Arxiv'19, <sup>9</sup>Valiant CACM'90, <sup>10</sup>Gluon-Async PACT'19,

# Experimental Setup

## Hardware

Bridges Supercomputer  
 32 (machines) \* 2 (NVIDIA P100 GPUs)

## Benchmarks

**bfs**, sssp, **cc**, **pagerank**, and kcore

## Frameworks

D-IrGL and Lux (Distributed Multi-GPU Frameworks)

## Inputs

Inputs (Medium)	V	E	Input (Large)	V	E
twitter50	51 M	1,963 M	<b>clueweb12</b>	978 M	42.5 B
<b>friendster</b>	66 M	1,806 M	<b>uk14</b>	788 M	47.6 B
<b>uk07</b>	106 M	3,739 M	wdc14	1725 M	64.4 B

# Results: Computation and Synchronization

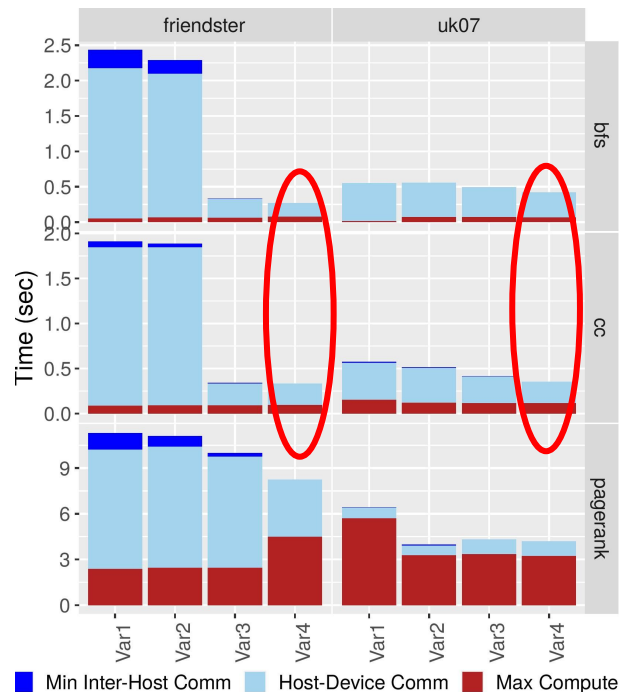


Variant	Optimizations
Var1	TWC + All Shared + Sync
Var2	ALB + All Shared + Sync
Var3	ALB + Update Only + Sync
Var4 (default)	ALB + Update Only + Async

All variants (even Lux) use same partitioning policy (IEC).

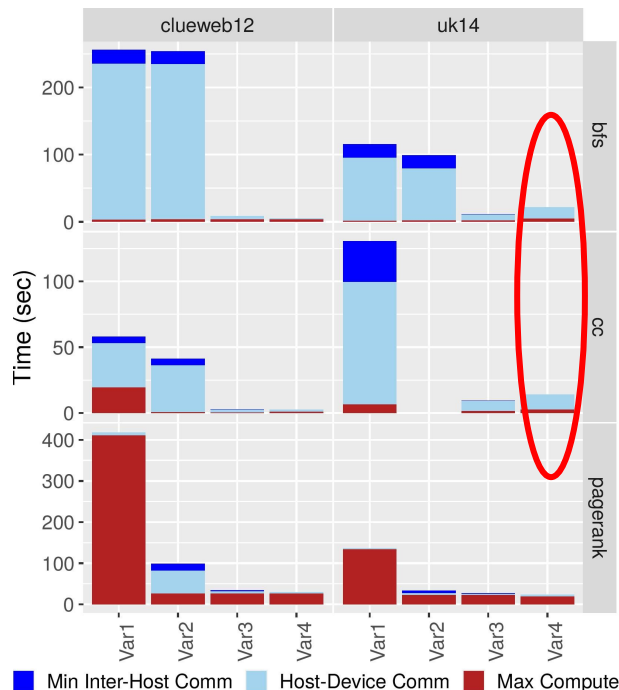
# Analyzing Computation and Synchronization

32 GPUs



**Host-device** time is significant

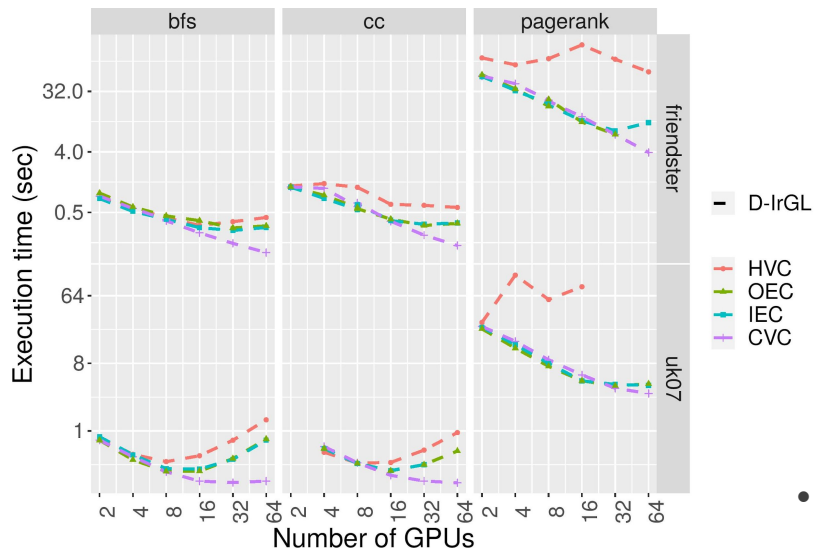
64 GPUs



**Asynchronous** behavior should be **throttled**



# Analyzing Partitioning Schemes



Benchmark	Partition	uk07 on 32 GPUs		uk14 on 64 GPUs		
		Static	Dynamic Memory	Static	Dynamic Memory	Static
bfs	CVC	1.15	1.17	1.15	1.15	1.11
	HVC	1.10	1.20	1.08	1.40	1.38
	IEC	1.00	1.14	1.04	1.00	1.08
	OEC	1.00	1.20	1.02	1.00	1.03
cc	CVC	1.03	1.18	1.05	1.12	1.13
	HVC	1.09	1.30	1.08	1.11	1.34
	IEC	1.00	1.27	1.02	1.00	1.24
	OEC	1.00	1.29	1.02	1.00	1.22
pagerank	CVC	1.16	1.04	1.15	1.15	1.02
	IEC	1.00	1.09	1.04	1.00	1.09
	OEC	1.00	1.10	1.03	1.00	1.08

- CVC outperforms other schemes on **16 or more GPUs**
  - fewer** communication partners

- Static load imbalance not correlated to dynamic load imbalance
- Static load imbalance is **correlated** to **memory** usage
  - Critical for **GPUs** due to **limited memory**

## Conclusion

- Detailed analysis of distributed multi-GPU graph analytics
- Lessons:
  - CVC is crucial for scaling
  - Static load balance is important for GPUs
- Scope for Improvements:
  - Reduce host-device communication time through GPUDirect
  - Control asynchrony in Bulk-Asynchronous execution

Please contact authors for any questions. Thank you!

<http://iss.oden.utexas.edu/?p=projects/galois>

Galois 