CSCI 516 - Fundamental Concepts in Computing and Machine Organization
Homework Assignment 2 Solutions

Questions

1. What is the CPU Time? Which two parts are included in CPU Time?

- CPU execution time or simply CPU time, is the time the CPU spends computing for the task and does not include time spent waiting for I/O or running other programs.
- CPU time can be further divided into **user CPU time** and **system CPU time**.
  - user CPU time: the CPU time spent in the program.
  - system CPU time: the CPU time spent in the operating system performing tasks on behalf of the program.

2. What are the hardware or software components which affect the performance of a program? What do these components affect? And how? (Hint: check a table in section 1.6 in the textbook.)

Hardware or software component	Affects what?	How?
Algorithm	Instruction count, possibly CPI	The algorithm determines the number of source program instructions executed and hence the number of processor instructions executed. The algorithm may also affect the CPI, by favoring slower or faster instructions. For example, if the algorithm uses more divides, it will tend to have a higher CPI.
Programming language	Instruction count, CPI	The programming language certainly affects the instruction count, since statements in the language are translated to processor instructions, which determine instruction count. The language may also affect the CPI because of its features; for example, a language with heavy support for data abstraction (e.g., Java) will require indirect calls, which will use higher CPI instructions.
Compiler	Instruction count, CPI	The efficiency of the compiler affects both the instruction count and average cycles per instruction, since the compiler determines the translation of the source language instructions into computer instructions. The compiler's role can be very complex and affect the CPI in varied ways.
Instruction set architecture	Instruction count, clock rate, CPI	The instruction set architecture affects all three aspects of CPU performance, since it affects the instructions needed for a function, the cost in cycles of each instruction, and the overall clock rate of the processor.

3. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (classes A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2.
Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D)

a. which is faster: P1 or P2?

Instruction Count of Class A: $10\% * 10^6 = 1 * 10^5$
Instruction Count of Class B: $10\% * 10^6 = 2 * 10^5$
Instruction Count of Class C: $10\% * 10^6 = 5 * 10^5$
Instruction Count of Class D: $10\% * 10^6 = 2 * 10^5$

$$\begin{aligned} CPU\ Time_{P1} &= \frac{InstructionCount * CPI}{ClockRate} \\ &= \frac{(1 * 10^5 * 1 + 2 * 10^5 * 2 + 5 * 10^5 * 3 + 2 * 10^5 * 3)}{2.5 * 10^9} \\ &= 10.4 * 10^{-4} s \end{aligned} \tag{1}$$

$$\begin{aligned} CPU\ Time_{P2} &= \frac{InstructionCount * CPI}{ClockRate} \\ &= \frac{(1 * 10^5 * 2 + 2 * 10^5 * 2 + 5 * 10^5 * 2 + 2 * 10^5 * 2)}{3 * 10^9} \\ &= 6.66 * 10^{-4} s \end{aligned} \tag{2}$$

b. What is the global CPI for each implementation?

$$CPI_{P1} = 0.1 * 1 + 0.2 * 2 + 0.5 * 3 + 0.2 * 3 = 2.6 \tag{3}$$

$$CPI_{P2} = 0.1 * 2 + 0.2 * 2 + 0.5 * 2 + 0.2 * 2 = 2.0 \tag{4}$$

c. Find the clock cycles required in both cases.

$$\begin{aligned} ClockCycles &= InstructionCount * CPI \\ &= 1 * 10^5 * 1 + 2 * 10^5 * 2 + 5 * 10^5 * 3 + 2 * 10^5 * 3 \\ &= 26 * 10^5 \end{aligned} \tag{5}$$

$$\begin{aligned} ClockCycles &= InstructionCount * CPI \\ &= 1 * 10^5 * 2 + 2 * 10^5 * 2 + 5 * 10^5 * 2 + 2 * 10^5 * 2 \\ &= 20 * 10^5 \end{aligned} \tag{6}$$

4. Another pitfall cited in Section 1.10 is expecting to improve the overall performance of a computer by improving only one aspect of the computer. Consider a computer running a program that requires 250 s, with 70 s spent executing FP instructions, 85 s executed L/S instructions, and 40 s spent executing branch instructions.

We assume that there are 4 kinds of instructions: INT instructions, FP instructions, L/S instructions, and branch instructions

1.13.1 By how much is the total time reduced if the time for FP operations is reduced by 20%?
$T_{fp} = 70 * 0.8 = 56s$
$T_{INT} = 250 - 70 - 85 - 40 = 55s$
$T_{new} = 56 + 85 + 40 + 55s = 236s$
Therefore, the total CPU Time is reduced by $(250 - 236)/250 = 5.6\%$

1.13.2 By how much is the time for INT operations reduced if the total time is reduced by 20%?
New total execution time: 250 * 0.8 = 200s
Execution time except INT instruction: 70 + 85 + 40 = 195s
New INT instruction execution time: 200 - 195 = 5s.
Then, the reduction is: (55 - 5) / 55 * 100% = 90.1%

1.13.3 Can the total time can be reduced by 20% by reducing only the time for branch instructions?

$$\frac{4}{5} * 250 = \frac{40s}{x} + 210 \tag{7}$$

where x is the improvement factor. x here is a negative number. Therefore, it is not possible to reduce total CPU Time by reducing the time of branch instructions.

5. The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power.

The Core i5 Ivy Bridge, released in 2012, has a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.

- 1.8.1 For each processor find the average capacitive loads.
  - C = $2 * DynamicPower/(V^2 * Frequency)$
  - Pentium 4: $C = 2 * 90w/(1.25^2 * 3.6GHz) = 3.2 * 10^{-8}$
  - Core i5 Ivy Bridge: $C = 2 * 40w/(0.9^2 * 3.4GHz) = 2.9 * 10^{-8}$
- 1.8.2 Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.
  - Pentium 4: $10/(10 + 90) = 10\%$
  - Core i5 Ivy Bridge: $30/(30 + 40) = 42.9\%$
- 1.8.3 If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current? Note: power is defined as the product of voltage and current.

- $\frac{Static_{new} + Dynamic_{new}}{Static_{old} + Dynamic_{old}} = 0.90$;
- from equation in the textbook/slides: $D_{new} = C * V_{new}^2 * F$
- "Note: power is defined as the product of voltage and current": $S = V * I$

Then:

- $V_{new} = [D_{new}/(C * F)]^{\frac{1}{2}}$
- $D_{new} = 0.90 * (S_{old} + D_{old}) - S_{new}$
- $S_{new} = V_{new} * (S_{old}/V_{old})$

Pentium 4:

- $S_{new} = V_{new} * (10/1.25) = V_{new} * 8$
- $D_{new} = 0.90 * 100 - V_{new} * 8 = 90 - V_{new} * 8$
- $V_{new} = [(90 - V_{new} * 8)/(3.2 * 10^{-8} * 3.6 * 10^9)]^{\frac{1}{2}}$
- $V_{new} = 0.85V$

Core i5:

- $S_{new} = V_{new} * (30/0.9) = V_{new} * 33.3$
- $D_{new} = 0.90 * 70 - V_{new} * 33.3 = 63 - V_{new} * 33.3$
- $V_{new} = [(63 - V_{new} * 33.3)/(32.9 * 10^{-8} * 3.4 * 10^9)]^{\frac{1}{2}}$
- $V_{new} = 0.64V$