CSCI 516: Fundamental Concepts in Computing and Machine Organization
Homework Assignment 7

Requirement

- You need to show the **steps of calculation**, instead of giving the final result only.
- You need to do your assignment **individually**
- You need to submit **'.pdf'** file which contains your solutions to the Blackboard.

1. Problem 5.5 from Textbook.

5.5 For a direct-mapped cache design with a 64-bit address, the following bits of the address are used to access the cache.

Tag	Index	Offset
63–10	9–5	4–0

5.5.1 [5] <§5.3> What is the cache block size (in words)?

5.5.2 [5] <§5.3> How many blocks does the cache have?

5.5.3 [5] <§5.3> What is the ratio between total bits required for such a cache implementation over the data storage bits?

Beginning from power on, the following byte-addressed cache references are recorded.

Address												
Hex	00	04	10	84	E8	A0	400	1E	8C	C1C	B4	884
Dec	0	4	16	132	232	160	1024	30	140	3100	180	2180

5.5.4 [20] <§5.3> For each reference, list (1) its tag, index, and offset, (2) whether it is a hit or a miss, and (3) which bytes were replaced (if any).

5.5.5 [5] <§5.3> What is the hit ratio?

5.5.6 [5] <§5.3> List the final state of the cache, with each valid entry represented as a record of <index, tag, data>. For example,

```
<0, 3, Mem[0xC00]-Mem[0xC1F]>
```

Solution:

5.5.1. There are 5 bits in the data offset field. Then:
there are 2^5 bytes for each cache block/line $\rightarrow 2^3$ = 8 words

5.5.2. There are 5 bits in the cache index field. Then:
There are $2^5 = 32$ cache blocks/lines in this cache.

5.5.3.
Total bits = number of cache lines * (tag bits + valid bit + data bits)
= $2^5 * (54 + 1 + 2^5 * 8) = 9952$ bits
Data bits = number of cache lines * data bits
= $2^5 * (2^5 * 8) = 8192$ bits
Ratio = $\frac{Totalbits}{Databits}$ = $\frac{9952}{8192} = 1.21$

5.5.4

Byte Address	Binary Address	Tag	Index	Offset	Hit/Miss	Bytes Replaced
0x00	0000 0000 0000	0x0	0x00	0x00	M	
0x04	0000 0000 0100	0x0	0x00	0x04	H	
0x10	0000 0001 0000	0x0	0x00	0x10	H	
0x84	0000 1000 0100	0x0	0x04	0x04	M	
0xe8	0000 1110 1000	0x0	0x07	0x08	M	
0xa0	0000 1010 0000	0x0	0x05	0x00	M	
0x400	0100 0000 0000	0x1	0x00	0x00	M	0x00-0x1F
0x1e	0000 0001 1110	0x0	0x00	0x1e	M	0x400-0x41F
0x8c	0000 1000 1100	0x0	0x04	0x0c	H	
0xc1c	1100 0001 1100	0x3	0x00	0x1c	M	0x00-0x1F
0xb4	0000 1011 0100	0x0	0x05	0x14	H	
0x884	1000 1000 0100	0x2	0x04	0x04	M	0x80-0x9f

5.5.5. Hit Ratio = $\frac{4}{12} * 100\% = 33.33\%$
5.5.6.

```
<index, tag, data>
<0, 3, Mem[0xC00]-Mem[0xC1F]>
<4, 2, Mem[0x880]-Mem[0x89f]>
<5, 0, Mem[0x0A0]-Mem[0x0Bf]>
<7, 0, Mem[0x0e0]-Mem[0x0ff]>
```

2. Problem 5.10 from Textbook.

5.10 In this exercise, we will look at the different ways capacity affects overall performance. In general, cache access time is proportional to capacity. Assume that main memory accesses take 70 ns and that 36% of all instructions access data memory. The following table shows data for L1 caches attached to each of two processors, P1 and P2.

	L1 Size	L1 Miss Rate	L1 Hit Time
P1	2 KiB	8.0%	0.66 ns
P2	4 KiB	6.0%	0.90 ns

5.10.1 [5] <§5.4> Assuming that the L1 hit time determines the cycle times for P1 and P2, what are their respective clock rates?

5.10.2 [10] <§5.4> What is the Average Memory Access Time for P1 and P2 (in cycles)?

5.10.3 [5] <§5.4> Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 and P2? Which processor is faster? (When we say a "base CPI of 1.0", we mean that instructions complete in one cycle, unless either the instruction access or the data access causes a cache miss.)

For the next three problems, we will consider the addition of an L2 cache to P1 (to presumably make up for its limited L1 cache capacity). Use the L1 cache capacities and hit times from the previous table when solving these problems. The L2 miss rate indicated is its local miss rate.

L2 Size	L2 Miss Rate	L2 Hit Time
1 MiB	95%	5.62 ns

5.10.4 [10] <§5.4> What is the AMAT for P1 with the addition of an L2 cache? Is the AMAT better or worse with the L2 cache?

5.10.5 [5] <§5.4> Assuming a base CPI of 1.0 without any memory stalls, what is the total CPI for P1 with the addition of an L2 cache?

5.10.6 [10] <§5.4> What would the L2 miss rate need to be in order for P1 with an L2 cache to be faster than P1 without an L2 cache?

5.10.7 [15] <§5.4> What would the L2 miss rate need to be in order for P1 with an L2 cache to be faster than P2 without an L2 cache?

Solution:

5.10.1.

$Clock\ Rate_{P1} = 1 / 0.66ns = 1.52\ GZ$

$Clock\ Rate_{P2} = 1 / 0.90ns = 1.11\ GZ$

5.10.2. AMAT = Access Time of Hit + Penalty of Miss

Cycles for Penalty of P1: $\frac{70ns}{0.66ns}$ = 107 cycles

$AMAT_{P1}$ = 1 + 0.08 * 107 = 9.56 cycles

Cycles for Penalty of P2: $\frac{70ns}{0.90ns}$ = 78 cycles

$AMAT_{P2}$ = 1 + 0.06 * 78 = 5.67 cycles

5.10.3. $Total\ CPI = CPI_{NoStall} + Penalty\ of\ Miss$

Moreover, 36% of all instructions access data memory. Therefore:

$Total\ CPI_{P1} = 1 + 0.08 * 107 + 0.08 * 0.36 * 107 = 12.64\ cycles$

$Total\ CPI_{P2} = 1 + 0.06 * 78 + 0.06 * 0.36 * 78 = 7.36\ cycles$

5.10.4.

Average memory access time = (access time on L1 hit) + (L1 miss penalty)*(L1 miss rate)

L1 miss penalty = (access time in L2 on hit) * (hit rate in L2) + (L2 miss penalty)*(L2 miss rate)

L2 requires $\frac{5.62ns}{0.66ns}$ = 9 cycles. Therefore:

AMAT = 1 + 0.08 * (9 + 0.95 * 107) = 9.85 cycles. The result is even worse than one level cache.

5.10.5.

CPI = 1 + 0.08 * (1 + 0.36) * (9 + 0.95 * 107) = 13.04 cycles.

5.10.6.

AMAT with L2 < AMAT with L1 only

1 + 0.08[9 + m*107] < 9.56

This happens when m< 0.916.

5.10.7.

AMAT of P1 with L2 < AMAT of P2 with L1 only

1 + 0.08[9 + m*107] < 5.67

This happens when m < 0.4614