Header H1			
	1	2	
	3	4	
USER_1_1	5	6	USER_1_2
SPI_1_CS2	7	8	USER_1_4
SPI_1_CS1	9	10	SPI_1_MOSI
SPI_1_CLK	11	12	SPI_1_MISO
UART_1_TX	13	14	UART_1_CTS
UART_1_RX	15	16	UART_1_RST
UART_RCS_1_TX	17	18	UART_RCS_1_CTS
UART_RCS_1_RX	19	20	UART_RCS_1_RST
I2C_1_SCL	21	22	I2C_1_SDA
CAN_1_H	23	24	CAN_1_L
GLO_SYNC	25	26	GLO_FAULT
CPU_WD_1	27	28	CPU_WD_2
-	29	30	CPU_MODE
-	31	32	-
GND	33	34	GND
GLO_KS_1	35	36	GLO_KS_2
-	37	38	-
USER_3_1	39	40	USER_3_2
USER_3_3	41	42	USER_3_4
USER_5_1	43	44	USER_5_2
USER_5_3	45	46	USER_5_4
	47	48	
	49	50	
	51	52	

Header H2			
	1	2	
	3	4	
USER_2_1	5	6	USER_2_2
SPI_2_CS2	7	8	USER_2_4
SPI_2_CS1	9	10	SPI_2_MOSI
SPI_2_CLK	11	12	SPI_2_MISO
UART_2_TX	13	14	UART_2_CTS
UART_2_RX	15	16	UART_2_RST
UART_RCS_2_TX	17	18	UART_RCS_2_CTS
UART_RCS_2_RX	19	20	UART_RCS_2_RST
I2C_2_SCL	21	22	I2C_2_SDA
CAN_2_H	23	24	CAN_2_L
SUP_5V	25	26	SUP_5V
SUP_3V3	27	28	SUP_3V3
GND	29	30	GND
-	31	32	GND
-	33	34	-
-	35	36	-
-	37	38	-
USER_4_1	39	40	USER_4_2
USER_4_3	41	42	USER_4_4
USER_6_1	43	44	USER_6_2
-	45	46	-
USER_6_3	47	48	USER_6_4
	49	50	
	51	52	