Experience of using OpenROAD Flow Scripts on a Complex enough Ibex and tiny design of 1-bit Full Adder

Mohammed Zakir Hussain
Assistant Professor, Department of ECE
zakir.hussain.work@gmail.com, +91-9949426362
Muffakham Jah College of Engineering and Technology
Hyderabad-500034, Telangana State, India.

Abstract—In this paper, I am going to discuss my experience with the OpenRoad flow scripts. As a physical design engineer, how this tool is friendly to use and how efficient in terms of physical design flow will be considered for presenting the experience.

Keywords— OpenROAD Flow Scripts, RTL-to-GDSII flow, open-source tools, automated design, no-human-in-the-loop.

I. INTRODUCTION

For an VLSI enthusiastic student, startups, Institutes, and even companies often find it difficult to get EDA tools because of EDA tools are often Proprietary software and maintaining their licences is quite costly job. In addition to these costly EDA tools, getting product-based Process Design Kits is also a costlier job.

With such a costlier EDA tool and PDKs most of the talented VLSI enthusiasts are unable to see their ideas being materialized. But, now thanks to the slogan now a days coming to hear “Democratization of IC Design” which is with the advent of open-source EDA tools such as OpenROAD and open PDKs such as Sky130 now anyone can put their ideas to test.

II. EXPERIENCE OF THE DESIGN FLOW

For experiencing OpenROAD app flow from RTL-to-GDSII, I have taken two design examples, one is ibex which had come with the local installation of the Openroad itself and the second design example is very tiny that is 1-bit full adder.

The experience with ready-made design in my case ibex was quite satisfactory but when I was trying with my own design there where I found it bit difficult for these reasons, 1. Needs to remember variable names as a designer I feel remembering them by following exact needed syntax is difficult 2. It is also bit difficult to remember and to make the changes according to TCL syntax in configuration file. 3. As a designer I wish to keep my own design in any of the directory that I wish, but here I have to strictly follow directory structure when I create any design of my own.

III. STRENGTH OR LIMITATION IN THE TOOL

The strength of the OpenROAD app flow is quite impressive in the sense it is pretty much comparable with the commercial EDA tools such as cadence in adopting the design flow steps from RTL-to-GDSII with the one limitation that I feel is lack of Design for Testability tool set.

IV. PROPOSED PLAN

I am planning in this contest to work on flow methodology to enhance either PPA or runtime on the already facilitated design which is RISC-V32i.

V. CONCLUSION AND RECOMMENDATIONS

In the conclusion, I strongly appeal the developers to keep continuing to accomplish the slogan “Democratization of IC Design” be materialized with open-source EDA tools through which bright minds can contribute towards the sophisticated technology. My recommendations are as I said in section II, there must be some means through which designer only changes the numerical values instead bothering about the syntax of the variable and also the TCL syntax.

REFERENCES

[1] https://github.com/The-OpenROAD-Project/OpenROAD

[2] https://openroad.readthedocs.io/en/latest/