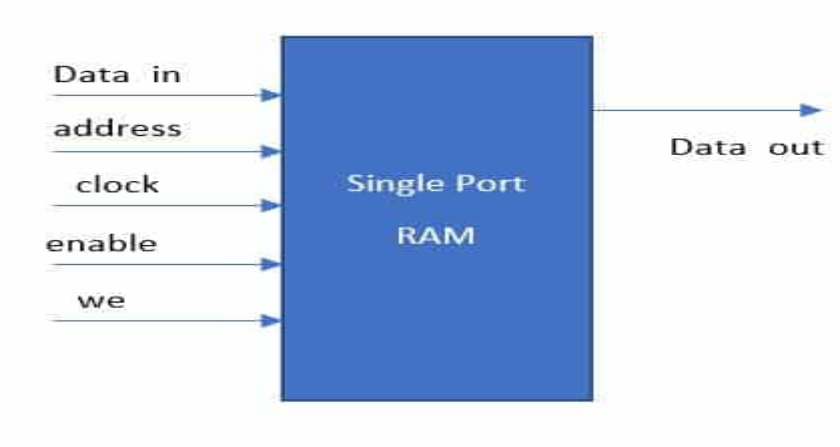
ASIC Design and Verification of RAM Verification

Abstract: The project aims to design and verify a custom Random Access Memory (RAM) module for integration into an Application-Specific Integrated Circuit (ASIC). This endeavour is divided into two distinct phases. Phase-1 focuses on comprehending the RAM specifications, developing the Register-Transfer Level (RTL) using Verilog HDL, and validating its correctness through functional simulation in SystemVerilog. Additionally, synthesis will be performed using the SKY130 Standard-cell library from Skywater Technologies. Phase-2 entails the completion of the backend process, encompassing floorplanning, placement, clock tree synthesis, routing, and ultimately, the generation of the GDSII file. OpenLane will be employed for this phase.

Introduction: Random Access Memory (RAM) plays a pivotal role in modern computing systems, serving as a high-speed, volatile data storage medium. The project endeavours to design a custom RAM module tailored for integration within an ASIC. This endeavour is essential for optimizing memory access and improving overall system performance.

Problem Statement:
The current landscape of memory solutions poses limitations in terms of speed, power efficiency, and integration within specialized applications. By designing a custom RAM module, we aim to address these challenges, optimizing memory access patterns for specific applications and achieving superior performance metrics.

Block diagram:



Phase-1: Understanding RAM and its Specifications
In this initial phase, a thorough understanding of RAM specifications is imperative. This involves a comprehensive study of various RAM architectures, including SRAM, DRAM, and their respective characteristics. Critical parameters such as access time, power consumption, and bit cell layout will be investigated to inform the subsequent design process.

Phase-1 Tasks:
1. Understanding the RAM and its Specifications: This task involves an in-depth exploration of various RAM architectures and their associated characteristics, providing the foundational knowledge required for the subsequent design phase.

2. Developing RTL using Verilog HDL: Leveraging Verilog HDL, the Register-Transfer Level (RTL) description of the RAM module will be constructed. This step is crucial in defining the functionality and behavior of the memory unit.
3. Ensuring RTL Correctness through Functional Simulation: SystemVerilog will be employed for functional simulation, allowing for rigorous testing and validation of the RTL description. This step is pivotal in identifying and rectifying any potential design flaws or discrepancies.
4. Performing Synthesis using SKY130 Standard-cell Library: The RTL description will be synthesized using the SKY130 Standard-cell library from Skywater Technologies. This step facilitates the generation of a gate-level netlist, a critical milestone in the ASIC design process.

Phase-1 EDA Tools:
1. iverilog for Functional Simulation: Iverilog will be utilized for functional simulation, providing a robust platform for validating the RTL description against various test cases.
2. yosys for Synthesis: Yosys will be employed for synthesis, facilitating the transformation of the RTL description into a gate-level netlist.

Phase-2: Complete Backend Process
The second phase focuses on the completion of the backend process, encompassing floorplanning, placement, clock tree synthesis, routing, and the ultimate generation of the GDSII file. This phase is pivotal in ensuring the physical realization of the designed RAM module.

Phase-2 Tasks:
1. Floorplanning: The initial step involves strategically placing various components within the chip, optimizing for factors such as power distribution, signal routing, and overall chip size.
2. Placement: The placement phase involves determining the precise location of each component on the chip, adhering to design constraints and optimizing for performance metrics.
3. Clock Tree Synthesis: This task involves the generation of a clock distribution network, ensuring synchronized clock signals across the entire chip.
4. Routing: The routing phase focuses on establishing interconnects between various components, enabling seamless communication and data transfer.
5. Generation of GDSII: The final step involves the creation of the GDSII file, which serves as the blueprint for fabrication.

Phase-2 EDA Tool:
OpenLane: OpenLane will be employed for the entirety of Phase-2, providing a comprehensive suite of tools for floorplanning, placement, clock tree synthesis, routing, and GDSII generation.

Conclusion: Through the meticulous execution of these two phases, the project aims to culminate in the successful design and verification of a custom RAM module, poised for integration within an ASIC. This endeavour holds immense potential in enhancing memory access and overall system performance for specialized applications.