ASIC Design of High-Performance Multiplier using SKY130 PDK

Abstract: The project aims to design a high-performance multiplier using the SKY130 Process Development Kit (PDK) for Application-Specific Integrated Circuit (ASIC) development. This endeavor addresses the critical need for efficient and fast arithmetic units in modern digital systems. The project encompasses two phases: Phase-1 focuses on architectural exploration, RTL development, correctness verification, and synthesis, while Phase-2 encompasses backend tasks including floorplanning, placement, clock tree synthesis, routing, and GDS2 file generation.

Introduction: In contemporary digital systems, multipliers are indispensable components, extensively employed in various applications such as signal processing, graphics rendering, and cryptography. The efficiency and speed of a multiplier play a pivotal role in determining the overall performance of these systems. The utilization of an optimized PDK like SKY130 offers a strategic advantage in achieving high-performance ASIC designs. This project endeavors to leverage the SKY130 PDK to develop an ASIC multiplier with exceptional efficiency.

Problem Statement: The existing multipliers often face challenges in meeting the escalating demands of modern applications that necessitate rapid and accurate multiplication operations. Conventional designs may fall short in terms of speed, power efficiency, or area utilization. This project addresses these concerns by implementing a state-of-the-art multiplier design using SKY130 PDK, aiming to achieve superior performance metrics compared to conventional counterparts.

Scheduled Tasks:

Phase-1:

1. Understanding the Various Multiplier Architectures:
   - Comprehensive study and analysis of diverse multiplier architectures to identify the most suitable approach for high-performance requirements.

2. Developing RTL using Verilog HDL:
   - Implementing the chosen multiplier architecture in Register-Transfer Level (RTL) using Verilog Hardware Description Language (HDL).

3. Ensuring RTL Correctness through Functional Simulation:
   - Rigorous simulation and verification of RTL code to guarantee its correctness and adherence to the design specifications.

4. Performing ASIC-Based Synthesis Flow:
   - Utilizing the Yosys open-source synthesis tool to convert RTL code into a gate-level netlist, optimizing for performance, power, and area.

Tools used in Phase-1:

- Yosys open-source synthesis tool

Phase-2:

1. Complete Backend Tasks:
   - Floorplanning: Defining the placement of various logical blocks to optimize for performance and minimize wirelength.
   - Placement: Allocating physical locations to different logic elements while adhering to design constraints.
   - Clock Tree Synthesis: Ensuring efficient distribution of clock signals to minimize skew and maintain synchronization.
   - Routing: Establishing interconnections between placed elements while minimizing congestion and ensuring signal integrity.

2. Generation of GDS2 File:
   - Producing the final Graphic Data System 2 (GDS2) file, a standard format for describing the physical layout of an integrated circuit.

Tools used in Phase-2:

- OpenLane tool chain

Conclusion: By systematically executing these tasks over the two defined phases, this project endeavors to deliver a high-performance ASIC multiplier design, leveraging the capabilities of the SKY130 PDK. This endeavor holds the potential to significantly enhance the computational capabilities of digital systems, catering to the demands of contemporary applications.