

INTRO

Tuesday, April 26, 2022 7:14 AM

Counters.

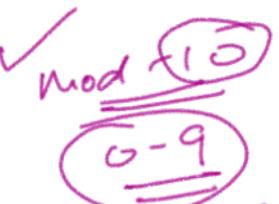
Registers counting no. of clock pulses.

0
1
2
3

$\frac{1}{T_C}$



+ve ✓
-ve ✓



mod - 6
0 - 5

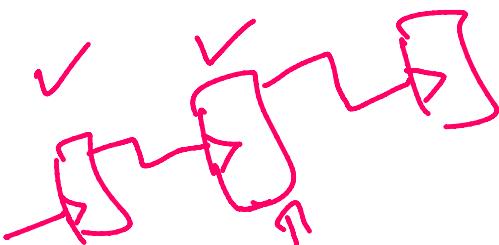
{ Single-mode operation ✓
Multi-mode operation ✓
updown.



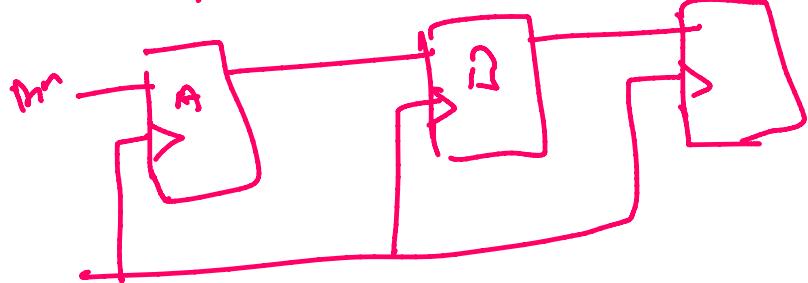
Modulus
Total no. of counts
counter can indicate

16 (0-15)

Async



Sync

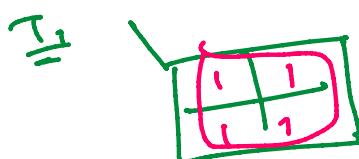
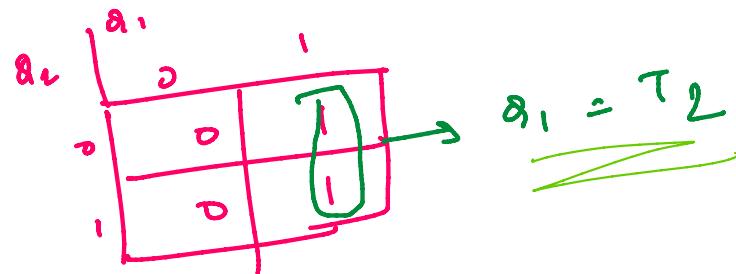


UP COUNTER

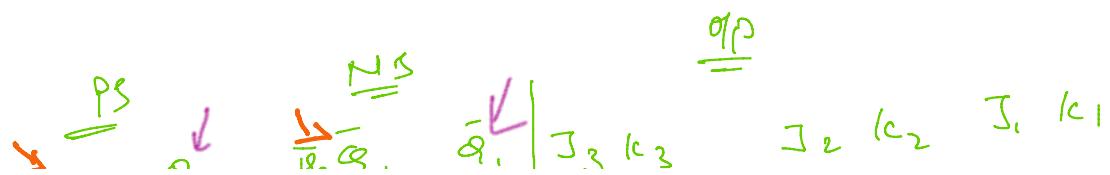
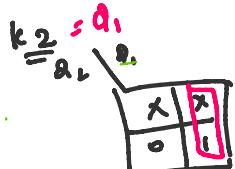
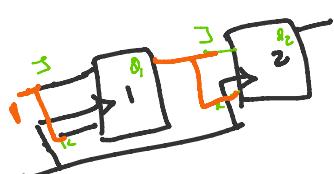
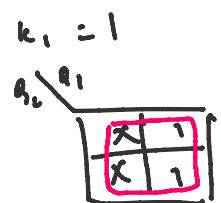
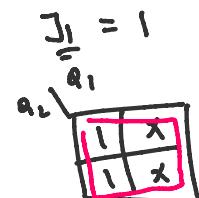
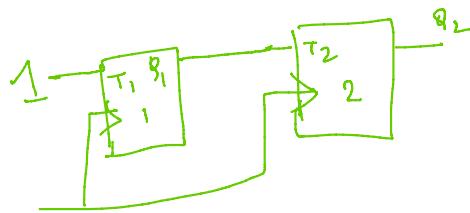
Tuesday, April 26, 2022 7:31 AM

State Table with excitation table

Present State	Next State	Flip Flop			
Q_2	Q_1	Q'_2	Q'_1	T_2	T_1
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1



$$T_1 = 1$$



$\overrightarrow{q_3}$	$\overleftarrow{q_2}$	$\overrightarrow{q_1}$	$\overleftarrow{q_3} \overleftarrow{q_2}$	$\overleftarrow{q_1}$	J_3	k_3	J_2	k_2	J_1	k_1
0 0	0 0	1 0	0 0	1	0	x	0	x	1	x
0 0	1 1	2 0	0 1	0	0	x	1	x	x	1
0 1	0	0 1	1	1	0	x	x	0	1	x
0 1	1	1 0	0	0	1	x	0	1	x	1
1 0	0	1	0 1	1	x	0	0	x	1	x
1 0	1	1 1	0	0	x	0	x	0	1	x
1 1	0	2 1	1 1 1	1	x	1	x	0	x	1
1 1	1	2	0 0 0	0	x	1	x	1	x	1

$\overrightarrow{q_3}$	$\overleftarrow{q_2}$	$\overrightarrow{q_1}$	$\overleftarrow{q_3} \overleftarrow{q_2}$	$\overrightarrow{q_1}$	S_2	R_2	S_1	R_1
0 0	0	1	0	1	0	x	1	0
0 1	1	0	1	0	1	0	0	1
1 0	0	1	1	1	x	0	1	0
1 1	1	0	0	0	0	1	0	1

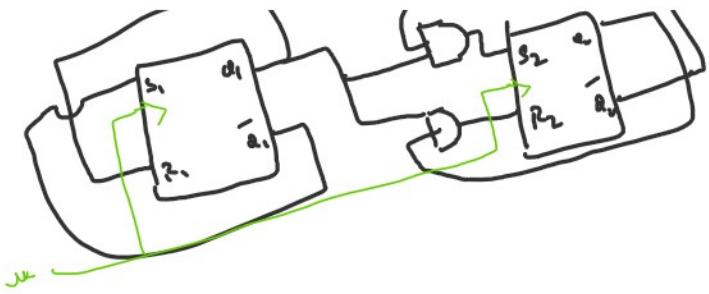
$$S_2 = \overline{a}_2 q_1$$

$$R_2 = a_1 a_2$$

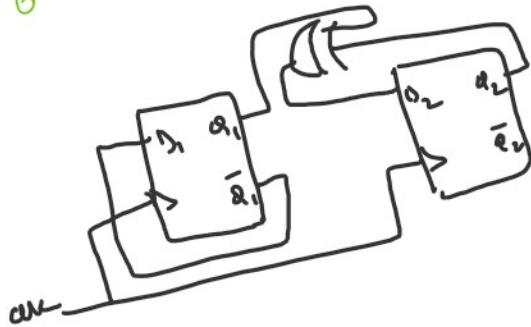
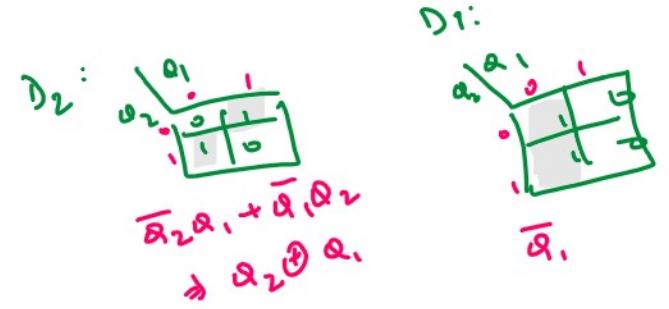
$$S_1 = \overline{a}_1$$

$$R_1 = a_1$$





$\overline{q_1}$	q_1	$\overline{q_2}$	q_2	d_1	d_2
0	0	0	1	0	1
0	1	1	0	1	0
1	0	1	1	0	0
1	1	0	0	0	0



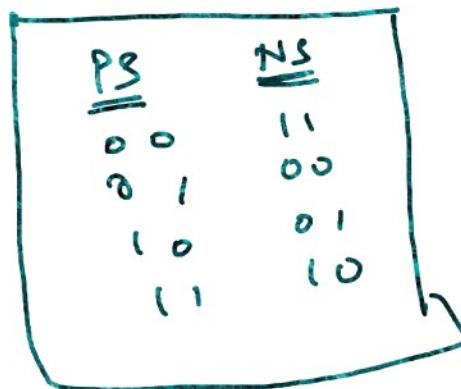
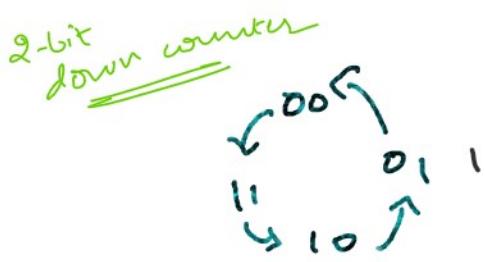
Up



Down

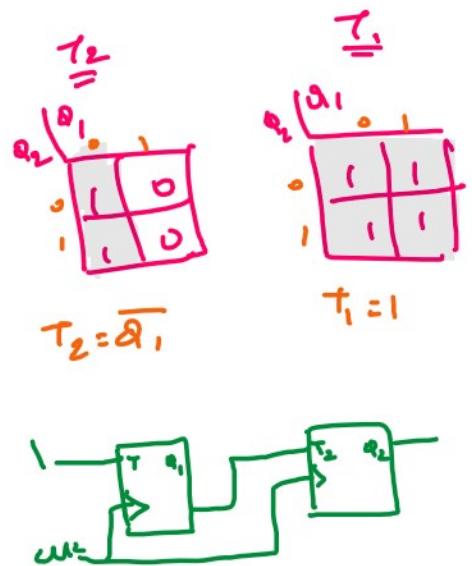


DOWN COUNTER

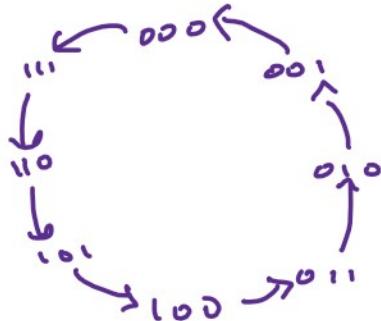


using T FF

PS	NS	D/P	T ₂	T ₁
q ₂ q ₁	q ₂ ' q ₁ '			
0 0	1 1		1	1
0 1	0 0		0	1
1 0	0 1		1	0
1 1	1 0		0	1



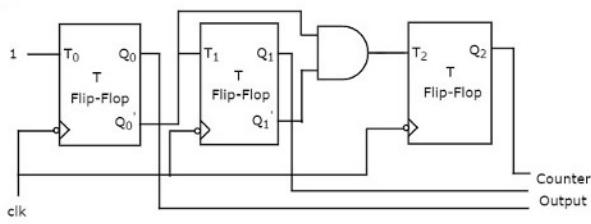
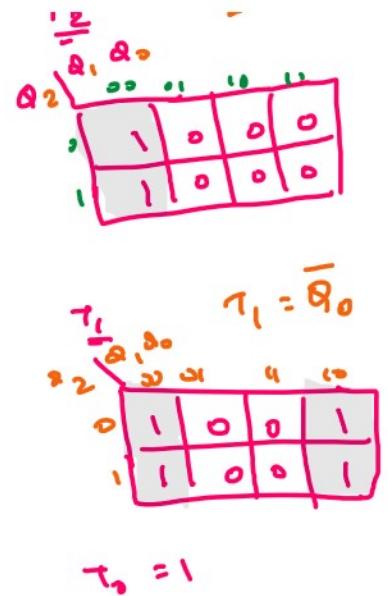
3-bit down counter



PS	NS	D/P	T ₂	T ₁	T ₀
q ₂ q ₁ q ₀	q ₂ ' q ₁ ' q ₀ '				
000	001				
001	010				
010	011				
011	100				
100	101				
101	000				

$T_2 = \bar{q}_2 \bar{q}_1 \bar{q}_0$

<u>PS</u>	$Q_2' Q_1' Q_0'$	$Q_2' Q_1' Q_0'$	T_2	T_1	T_0
0 0 0	1 1 1		1	1	1
0 0 1	0 0 0		0	0	1
0 1 0	0 0 1		0	1	1
0 1 1	0 1 0		0	0	1
1 0 0	0 1 1		1	1	1
1 0 1	1 0 0		0	0	1
1 1 0	1 0 1		0	1	1
1 1 1	1 1 0		0	0	1



MODULO COUNTER

Design for Mod-N counter :

The steps for the design are –

Step 1 : Decision for number of flip-flops –

Example : If we are designing mod N counter and n number of flip-flops are required then n can be found out by this equation.

$$N \leq 2^n$$

Here we are designing Mod-10 counter Therefore, $N=10$ and number of Flip flops(n) required is

For $n=3$, $10 \leq 8$, which is false.

✓ For $n=4$, $10 \leq 16$, which is true.

Therefore number of FF required is 4 for Mod-10 counter.

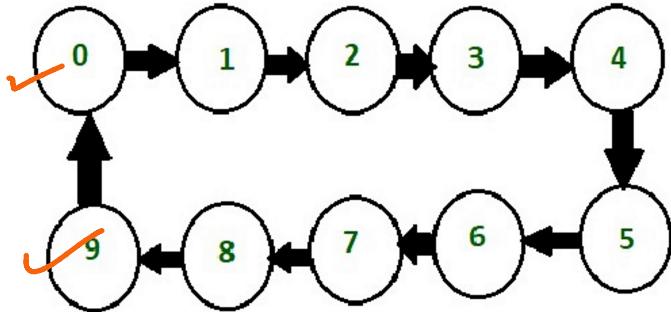
Step 2 : Write excitation table of Flip flops –

Here T FF is used

Previous state(Q _n)	Next state(Q _{n+1})	T
0	0	0
0	1	1
1	0	1
1	1	0

Excitation table of T FF.

Step 3 : Draw state diagram and circuit excitation table –



Counting Sequence of Decade counter

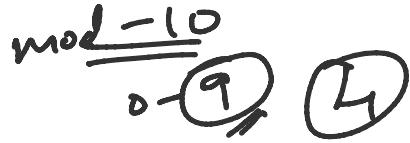
A decade counter is called as mod -10 or divide by 10 counter. It counts from 0 to 9 and again reset to 0. It counts in natural binary sequence. Here 4 T Flip flops are used. It resets after $Q_3 Q_2 Q_1 Q_0 = 1001$.

Circuit excitation table –

Here $Q_3 Q_2 Q_1 Q_0$ are present states of four flip-flops and $Q^{*3} Q^{*2} Q^{*1} Q^{*0}$ are next counting state of 4 Flip flops. If there is a transition in current state i.e if Q_3 value changes from 0 to 1 or 1 to 0 then there's corresponding T(toggle) bit is written as 1 otherwise 0.

Q_3	Q_2	Q_1	Q_0	Q^{*3}	Q^{*2}	Q^{*1}	Q^{*0}	T_3	T_2	T_1	T_0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	0	0	0	0	1	0	0	1

Circuit excitation table.



0-7



Step 4 : Create Karnaugh map for each FF input in terms of flip-flop outputs as the input variable –

Simplify the K map –

		$Q_1 Q_0$	$Q_3 Q_2$		
		00	01	11	10
$Q_3 Q_2$	00	0	0	0	0
01	0	0	1	0	
11	X	X	X	X	
10	0	1	X	X	

$$T_3 = Q_3 Q_0 + Q_2 Q_1 Q_0$$

		$Q_1 Q_0$	$Q_3 Q_2$		
		00	01	11	10
$Q_3 Q_2$	00	0	0	1	0
01	0	0	1	0	
11	X	X	X	X	
10	0	0	X	X	

$$T_2 = Q_1 Q_0$$

		$Q_1 Q_0$	$Q_3 Q_2$		
		00	01	11	10
$Q_3 Q_2$	00	0	1	1	0
01	0	1	1	0	
11	X	X	X	X	
10	0	0	X	X	

$$T_1 = Q'_3 Q_0$$

		$Q_2 Q_1$	$M Q_3$		
		00	01	11	10
$Q_2 Q_1$	00	1	1	1	1
01	1	1	1	1	
11	1	1	1	1	
10	1	1	1	1	

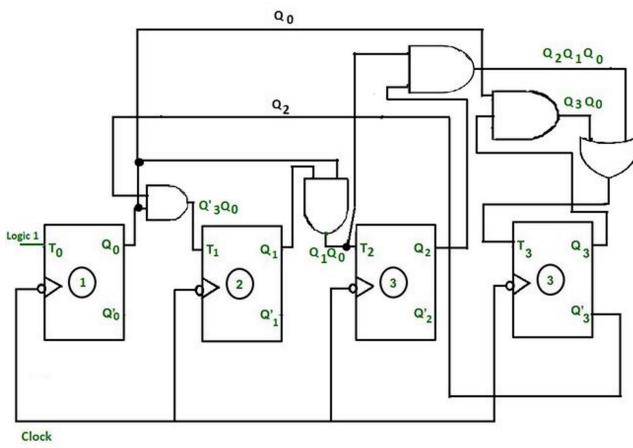
$$T_0 = 1$$

K map for finding minimal expressions.

Step 5 : Create circuit diagram –

Here negative edge triggered clock is used for toggling purpose.

- The clock is provided to every Flip flop at same instant of time.
- The toggle(T) input is provided to every Flip flop according to the simplified equation of K map.



Circuit diagram

MOD 5 COUNTER - JK

Step 1:

Determine the number of flip flop needed

Flip flop required are

$$2^n \geq N \quad 2^n \geq 5$$

Mod 5 hence $N=5$

3 flip flop are required



✓ Mod-5
≡

0 - 4

100

3 variables -

3 JFF

Step 2:

Type of flip flop to be used: JK flip flop

Step 3:

1) Excitation table for JK flip flop

$Q_n Q_n$	$Q_{n+1} Q_{n+1}$	J	K
0	0	0	xx
0	1	1	xx
1	0	xx	1

Now, we can derive excitation table for counter using above table as follows:

2) Excitation table for counter

Present state			Next state			Flip flop Input					
Q_c	Q_B	Q_A	Q_{c+1}	Q_{B+1}	Q_{A+1}	J_c	K_c	J_B	K_B	J_A	K_A
0	0	0	0	0	1	x	0	0	x	1	x
0	0	1	0	1	0	x	1	1	x	x	1
0	1	0	0	1	1	x	x	x	0	1	x
0	1	1	1	0	0	x	x	x	x	1	x
1	0	0	0	0	0	1	0	0	x	0	x
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

Step 4

K-map simplification

For $J_c J_c$

$\diagdown Q_B Q_A$	00	01	11	10
Q_C	0	0	0	0
1	x	x	x	x

$$J_c = Q_B Q_A J_c = Q_B Q_A$$

For $K_c K_c$

$\diagdown Q_B Q_A$	00	01	11	10
Q_C	x	x	x	x
1	1	x	x	x

$$K_c = 1 \quad K_c = 1$$

For $J_B J_B$

$\diagdown Q_B Q_A$	00	01	11	10
Q_C	1	x	x	x
1	x	x	x	x

$$J_B = Q_A J_B = Q_A$$

For $K_B K_B$

$\diagdown Q_B Q_A$	00	01	11	10
Q_C	x	x	1	0
1	x	x	x	x

$$K_B = Q_A K_B = Q_A$$

For JAJA

$\begin{matrix} Q_B \\ Q_A \\ Q_C \end{matrix}$	00	01	11	10
0	1	x	x	1
1	0	x	x	x

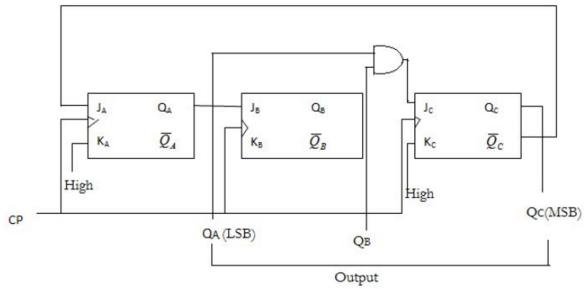
$$J_A = Q_C \cdot \bar{Q}_A \cdot \bar{Q}_B$$

For KA KA

$\begin{matrix} Q_B \\ Q_A \\ Q_C \end{matrix}$	00	01	11	10
0	x	1	1	x
1	x	x	x	x

$$K_A = 1 \quad K_B = 1$$

Step 5 Logic Diagram



UP/DOWN COUNTER

Steps to design Synchronous 3 bit Up/Down Counter :

1. Decide the number and type of FF –

- Here we are performing 3 bit or mod-8 **Up or Down counting**, so 3 Flip Flops are required, which can count up to $2^3 - 1 = 7$.
- Here T Flip Flop is used.

2. Write excitation table of Flip Flop –

Previous state(Q _n)	Next state(Q _{n+1})	T
0	0	0
0	1	1
1	0	1
1	1	0

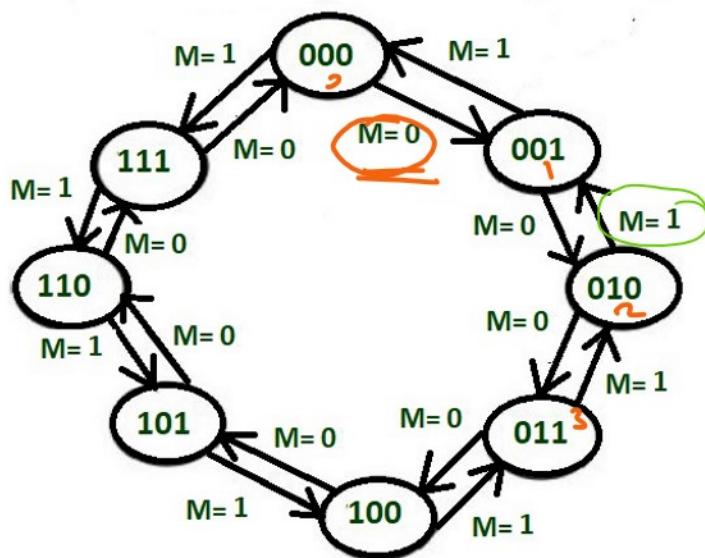
Excitation table of TFF

3. Decision for Mode control input M –

- When M=0 ,then the counter will perform up counting.
- When M=1 ,then the counter will perform down counting.

4. Draw the state transition diagram and circuit excitation table –

Gr. var



State transition diagram for 3 bit up/down counting.

5. Circuit excitation table –

The circuit excitation table represents the present states of the counting sequence and the next states after the clock pulse is applied and input T of the flip-flops. By seeing the transition between the present state and the next state, we can find the input values of 3 Flip Flops using the Flip Flops excitation table. The table is designed according to the required counting sequence.

M	Q ₃	Q ₂	Q ₁	Q ₃ [*]	Q ₂ [*]	Q ₁ [*]	T ₃	T ₂	T ₁
0	0	0	0	0	0	1	0	0	1
0	0	0	1	0	1	0	0	1	1
0	0	1	0	0	1	1	0	0	1
0	0	1	1	1	0	0	1	1	1
0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1

0	1	0	0	1	0	1	0	0	1
0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	1	1	0	0	1
0	1	1	1	0	0	0	1	1	1
1	0	0	0	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	1
1	0	1	0	0	0	1	0	1	1
1	0	1	1	0	1	0	0	0	1
1	1	0	0	0	1	1	1	1	1
1	1	0	1	1	0	0	0	0	1
1	1	1	0	1	0	1	0	1	1
1	1	1	1	0	1	0	0	0	1

Circuit excitation table

If there is a change in the output state of a flip flop (i.e. 0 to 1 or 1 to 0), then the corresponding T value becomes 1 otherwise 0.

6. Find a simplified equation using k map –

Here we are finding the minimal Boolean expression for each Flip Flop input T using k map.

M Q ₃	Q ₂ Q ₁	00	01	11	10
00	0	0	1	0	
01	0	0	1	0	
11	1	0	0	0	
10	1	0	0	0	

$$T_3 = M'Q_2Q_1 + MQ'_2Q'_1$$

M Q ₃	Q ₂ Q ₁	00	01	11	10
00	0	1	1	0	
01	0	1	1	0	
11	1	0	0	0	1
10	1	0	0	0	1

$$T_2 = M'Q_1 + MQ'_1$$

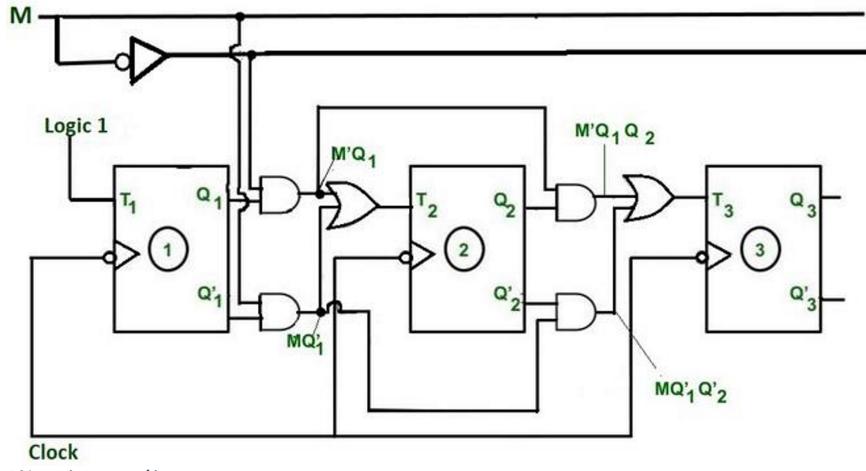
M Q ₃	Q ₂ Q ₁	00	01	11	10
00	1	1	1	1	
01	1	1	1	1	
11	1	1	1	1	
10	1	1	1	1	

$$T_1 = 1$$

Simplified equation for K map

7. Create a circuit diagram –

The simplified expression for Flip Flops is used to design circuit diagrams. Here all the connections are made according to simplified expressions for Flip Flops.



3 bit synchronous up/down counter.

Using positive edge triggered SR Flip-flop, design a counter which counts the following sequence :
000,111, 110, 101, 100, 011, 010, 001, 000.....

0 7 6 4 3 2 1 0

000, 111, 110, 101, 100, 011, 010, 001, 000, ...
Solution :

Step 1 : Determine the number of flip-flops needed

We know that $2^n \geq N$. Here, $N = 8 \therefore n = 3$

Step 2 : Type of flip-flop to be used : SR

Step 3 : Determine the excitation table for counter.

Here, the next state for each present state is written according to given sequence. For example, the next state for the present state 000 is 111.

0 7 6 4 2 1

(3) (5)

000

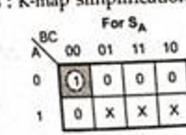
Q _n		S	R
Q _n	Q _{n+1}		
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Table 7.4.7 Excitation table of SR flip-flop

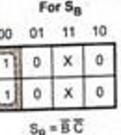
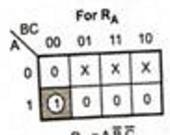
Present state		Next state		Flip-flop inputs							
A	B	C	A ⁺	B ⁺	C ⁺	S _A	R _A	S _B	R _B	S _C	R _C
0	0	0	1	1	1	1	0	1	0	1	0
0	0	1	0	0	0	x	0	x	0	1	
0	1	0	0	1	0	x	0	1	1	0	
0	1	1	0	1	0	x	x	0	0	1	
1	0	0	1	1	0	1	1	0	1	0	
1	0	1	1	0	0	x	0	0	x	0	1
1	1	0	1	0	1	x	0	0	1	1	0
1	1	1	1	1	0	x	0	x	0	0	1

Table 7.4.8 Excitation table for counter

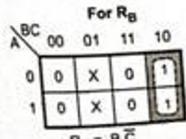
Step 4 : K-map simplification.



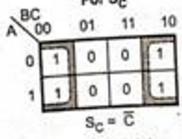
$$S_A = \bar{A} \bar{B} \bar{C}$$



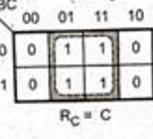
$$S_B = \bar{B} \bar{C}$$



$$R_B = B \bar{C}$$



$$S_C = \bar{C}$$



$$R_C = C$$

Fig. 7.4.14 (a)

Step 5 : Draw logic diagram

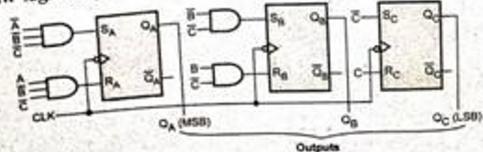


Fig. 7.4.14 (b) Logic diagram