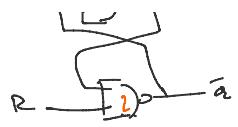


SR



(a) $S=1, R=0$ any $Q_P=0, Q_D=1 \Rightarrow Q=0$
 $\bar{Q}=1$
 $S=1, R=1$ if $S=1, R=1$, both $Q_P=1, Q_D=0$
 $S=1, Q=0 \Rightarrow Q=0$

$$S=1 \quad | \quad \begin{cases} Q=0 \\ Q=1 \end{cases}$$

$$R=0 \quad | \quad \begin{cases} Q=0 \\ Q=1 \end{cases}$$

(b) $S=1, R=1$ if $S=1, R=1$, both $Q_P=1, Q_D=0$
 $S=1, Q=0 \Rightarrow Q=0$

(c) $S=0, R=1$ any $Q_P=0, Q_D=1 \Rightarrow Q=0$
 $R=1 \quad | \quad \begin{cases} Q=1 \\ Q=0 \end{cases}$

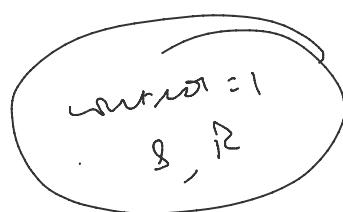
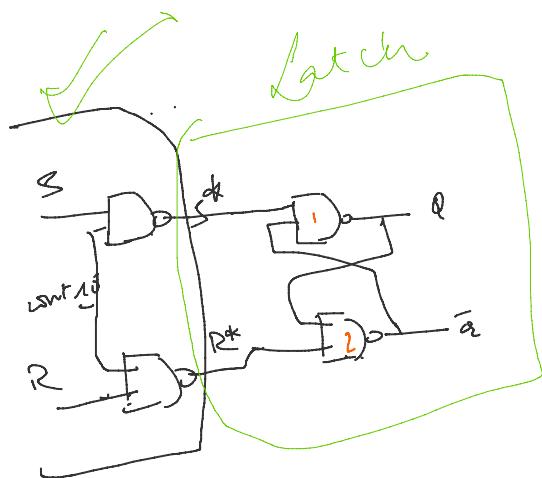
(d) $S=1, R=1$ $Q_P=0, Q_D=1 \Rightarrow Q=0$
 $R=1 \quad | \quad \begin{cases} Q=0 \\ Q=1 \end{cases}$

(e) $S=0, R=0$

Any $Q_P=0, Q_D=1 \quad S=0 \quad | \quad \begin{cases} Q=1 = \bar{Q} \Rightarrow \text{Invald} \\ Q=0 \end{cases}$

1.1 of SR Latch
using NAND Gates

S	R	Q	\bar{Q}
0	0	invalid	
0	1	1	0
1	0	0	1
1	1	memory	



Latch

(a) Basic building block.

(b) Level triggered
+ve
-ve

(c) Latch responds to Q_P , until
active level is maintained
the time



if

(a) Built by connecting additional
components around basic

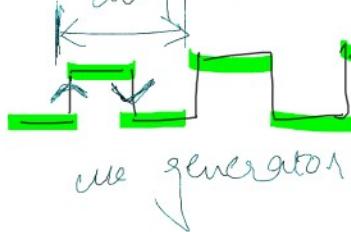
(b) Edge triggered
+ve
-ve

(c) Responds to Q_P only at
specified edges.

active time is known as

as the period.

ie.



(T)

duty cycle
freq divider

Species - >

freq : / time period