System Verilog Lab3

After completing this lab, you should be able to:

Understand how to collect the output of DUT

Use queues to store the read data.

Implement generic code to capture the dut output.

Verify DUT behaviour with waveform.

LAB3:

Copy the lab2 code as lab3

Step 1: Collect the output from dut in testbench.

1. Define queue named dut_out[$] in testbench.sv
2. Add the below code in Section 1 in testbench.sv

```
reg [7:0] dut_out[$];
```

3. Wait on signal rdata in teetbench to detect the output from dut.
   Add this code in Section 7

```
initial begin // Add this code in Section 8
  forever begin
  @(rdata);
  dut_out.push_back(rdata).
  $display("[Rdata] Rdata = %0d at mem address = %0d",rdata,addr);
  end
end
```

Step 2: Add the display to initial block.

1. Add the below code into Section 6 in testbench.sv

   $display("[Dut values] Data = %0p",dut_out);

Step 3: Simulating the design and Validate the output

```
# [Testbench] Reset applied to DUT
# [Testbench] Reset completed
# [Rdata] Rdata = 10 at mem address = 1
# [Rdata] Rdata = 20 at mem address = 3
# [Rdata] Rdata = 30 at mem address = 4
# [Rdata] Rdata = 40 at mem address = 4
# [Golden Values] Data = 10 20 30 40
# [Dut values] Data = 10 20 30 40
```