SEQUENTIAL EXAM - 1

1. Design synchronous 3-bit up/down counter ?
2. Design a 4-bit universal shift register.
3. Design the SR NAND Gate Latch and explain its working
4. Design a circuit which takes 4 bit data serially and double the value and sends out the data serially
5. The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset. The counter corresponding to this circuit is _____