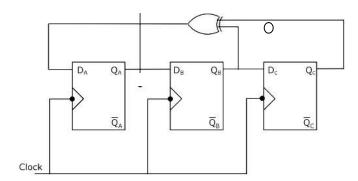
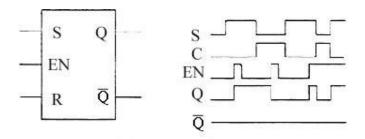
SEQUENTIAL ASSIGNMENT 1

1. Assuming that all flip-flops are in reset condition initially, the count sequence observed at Q_A in the circuit shown is



- 2. (a) Difference between latch and flip flop
 - (b) What is the difference between asynchronous counter and synchronous counter?
- 3. I) A bidirectional 4-bit shift register is storing the nibble 1110. Its input is LOW. The nibble 0111 is waiting to be entered on the serial data-input line. After two clock pulses, the shift register is storing
- a) 1110 b) 0111 c) 1000 d) 1001
- II) Assume there is a mod6 up counter, current state is 101. After 17 clock pulses, what is the state?
- 4. What does the triangle on the clock input of a *J-K* flip-flop mean?
- a. Level enabled
- b. Edge-triggered
- 5. A gated S-R latch and its associated waveforms are shown below. What, if anything, is wrong and what could be causing the problem?



- 6. How many Flip Flops are required to make Mod 32 Bit Counter?
 - a. 4
- b. 45
- c. 3
- d. 5