Designing Exercise: *Grand test*

Time : 120 min Marks : 100

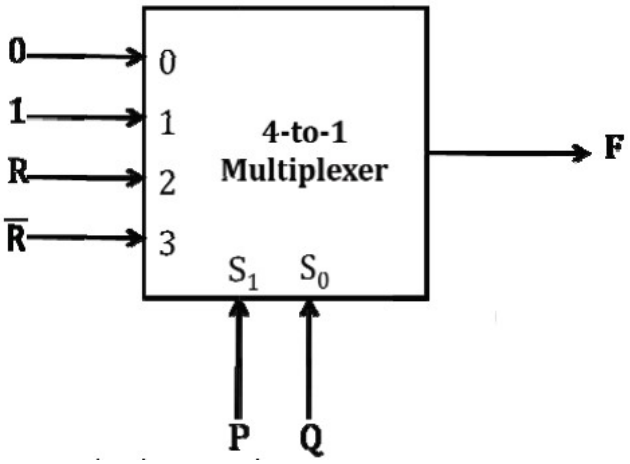
1. (a) Define duality property and State De Morgan's theorem.
   (b) Solve the following -
   I. Reduce A.A'C
   II. Reduce A(A + B)
   III. Reduce A'B'C' + A'BC' + A'BC
   IV. Reduce AB + (AC)' + AB'C(AB + C)
   V. Simplify the following expression Y = (A + B)(A + C')(B' + C')
   VI. Simplify the following using De Morgan's theorem [((AB)'C)'' D]'
   VII. Show that (X + Y' + XY)(X + Y')(X'Y) = 0

2. (a) Convert (634) 8 to binary
   (b) Convert (9 B 2 - 1A) H to its decimal equivalent.
   (c) Convert decimal number 22.64 to hexadecimal number.
   (d) Convert gray code 101011 into its binary equivalent.
   (e) Convert 10111011 is binary into its equivalent gray code.

3. Design logic gates using Nand gate.

4. Using 4 to 1 MUX implement the following 2-input gates:
   (a) OR (b) AND (c) NOR (d) NAND (e) XOR (f) XNOR (g) NOT.

5. (a) Consider a 4-to-1 multiplexer with two select lines S1 and S0, given below.



Write the minimal SOP form of boolean expression.

(b) Implement full adder using 3 : 8 decoder.

6. Design mod-6 Synchronous counter using JK flip-flop.
7. Design divide by 6 using T flip-flop. Write state table and reduce the expression using K-map.
8. Uisng positive edge triggered SR Flip-flop, design a counter which counts the following sequence : 000,111, 110,100,011,010,001,000…..
9. Design a 4-bit Universal shift register and explain its operation.
10. Design a moore sequence detector to detect the sequence – 1001. (non-overlapping and overlapping)