LAB NO 01

1..draw logic diagram on logisim for following Boolean function without simplification (use only two ip gate)

i)F(A,B,C)= Σ(1,4,5,6,7)

ii)F(A,B,C,D)= Σ(2,4,7,10,12,14)

iii)F(u,x,y)= ux+u'x'+x

2 .Draw a logic diagram for following Boolean function with simplification (use only two ip gate)

a	b	C	F1	F2
0	0	0	1	1
0	0	1	0	1
0	1	0	1	0
0	1	1	1	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	0
1	1	1	1	1

fig2

3.Design the logic diagram for shaded region of fig2 on Logisim here a,b,c are the input(use only two ip gate) .....

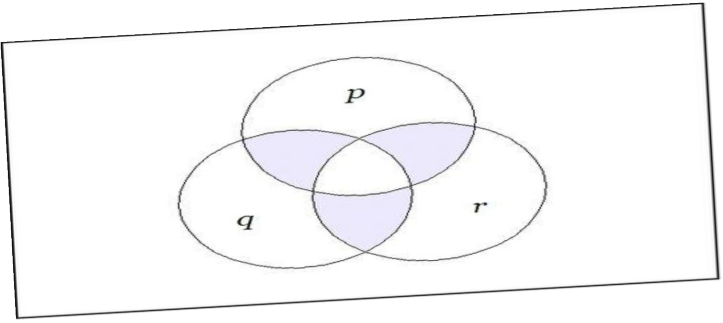

Fig2

4.Implement the logic diagram on logisim for following question (use only two ip gate)..

i)F(x,yz)=1 whenever x,y,z are different and 0 otherwise.....

LAB NO 02

1.Design following on logisim
i)Half adder
ii)Full adder
iii)half substractor
iv)full substractor

2.
i)Design a full adder using half adder and a OR gate on logisim
ii)Design a full substractor using half substactor and a OR gate on logisim

3.
Design a full adder and full substracor using NAND gate only….

LAB NO 03

1.Design 2:1 mux using only basic gate on logisim…….
2.Design 4:1 mux using 2:1 mux on logisim….
3.design the two input XOR, XNOR gate using mux on logisim

LAB NO 04

1.
i)Design 1:2 Demux using basic gate only on logisim
ii)Design 1:4 Demux using 1:2 Demux on logisim
2.Design 2:4 encoder using basic gate only on logisim
3. design the logic diagram for following converter on logisim
i)binary to gray
ii)gray to binary

LAB NO 05

1.Design Clocked SR flip flop using basic gate on logisim
2.Design JK ,SR,T,D FF using SR FF on logisim
3. Design D FF using mux
4.Design T FF using MUX