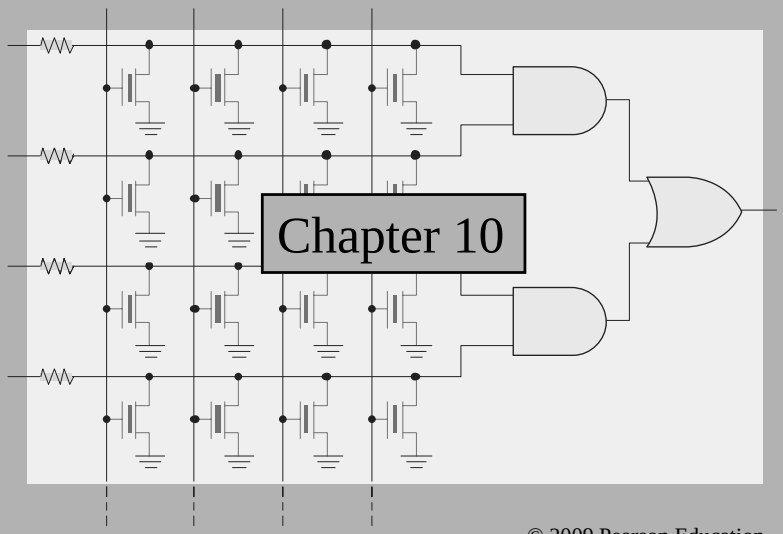
Digital Fundamentals

with PLD Programming

Floyd



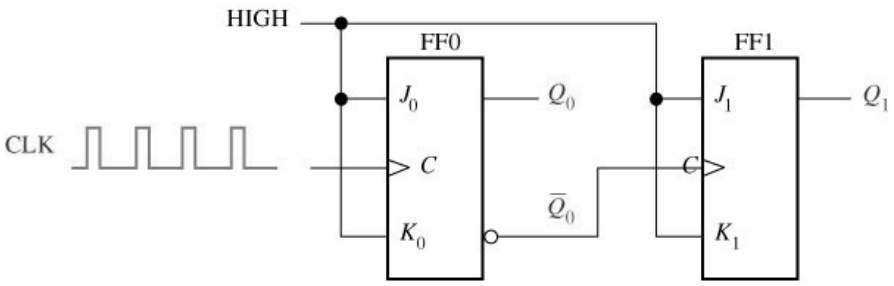
Contadores

Grupo de biestables que generan una **cuenta** (secuencia de números binarios).

El número de biestables y la forma de conectarlos determina el número estados (**módulo**) y la **secuencia** de estados por los que pasa en un ciclo completo.

Clasificación según el reloj:
(1) **asíncrono** (contador en cascada), el reloj sincroniza el primer biestable, y el resto se sincroniza con la salida del anterior.
(2) **síncrono**: todos los biestables sincronizados por el reloj.

Contador binario asíncrono de dos bits



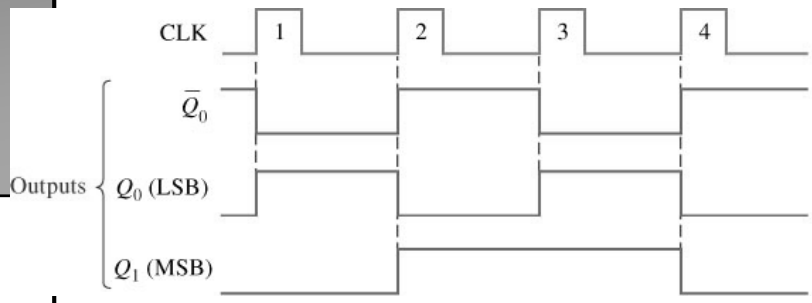


Diagrama de tiempo

CLOCK PULSE	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0

Secuencia de estados

Summary

Counting in Binary

As you know, the binary count sequence follows a familiar pattern of 0's and 1's as described in Section 2-2 of the text.

0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
1 1 1

LSB changes on every number.

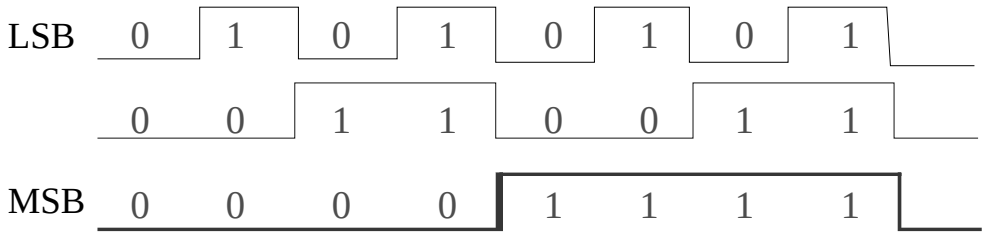
The next bit changes on every other number.

The next bit changes on every fourth number.

Summary

Counting in Binary

A counter can form the same pattern of 0's and 1's with logic levels. The first stage in the counter represents the least significant bit – notice that these waveforms follow the same pattern as counting in binary.

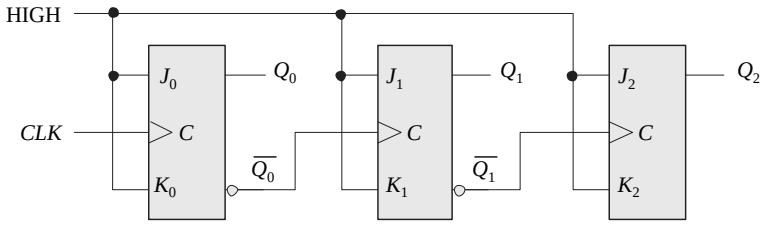


Summary

Three bit Asynchronous Counter

In an asynchronous counter, the clock is applied only to the first stage. Subsequent stages derive the clock from the previous stage.

The three-bit asynchronous counter shown is typical. It uses J-K flip-flops in the toggle mode.



Waveforms are on the following slide…

Summary

Three bit Asynchronous Counter

Notice that the Q_0 output is triggered on the leading edge of the clock signal. The following stage is triggered from $\overline{Q}_0$. The leading edge of $\overline{Q}_0$ is equivalent to the trailing edge of Q_0. The resulting sequence is that of an 3-bit binary up counter.

TABLE 9–2

Binary state sequence for a 3-bit binary counter.

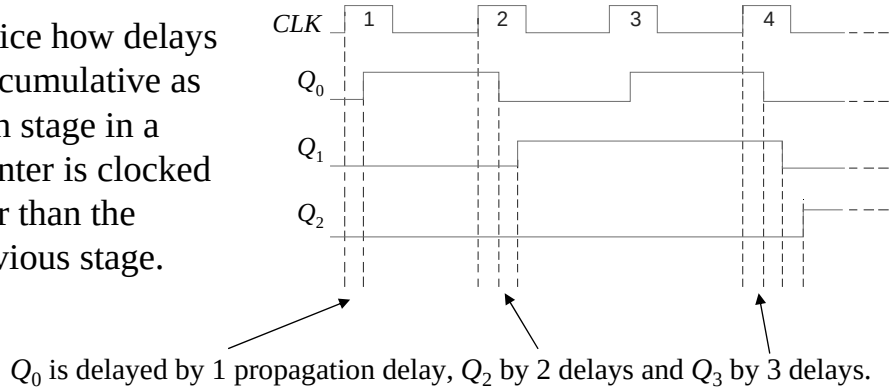
CLOCK PULSE	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

Summary

Propagation Delay

Asynchronous counters are sometimes called **ripple** counters, because the stages do not all change together. For certain applications requiring high clock rates, this is a major disadvantage.

Notice how delays are cumulative as each stage in a counter is clocked later than the previous stage.



Q_0 is delayed by 1 propagation delay, Q_2 by 2 delays and Q_3 by 3 delays.

Contadores con secuencia truncada

Módulo de un contador: el número de estados únicos por los que pasa.

Módulo **máximo** = 2^n con n biestables.

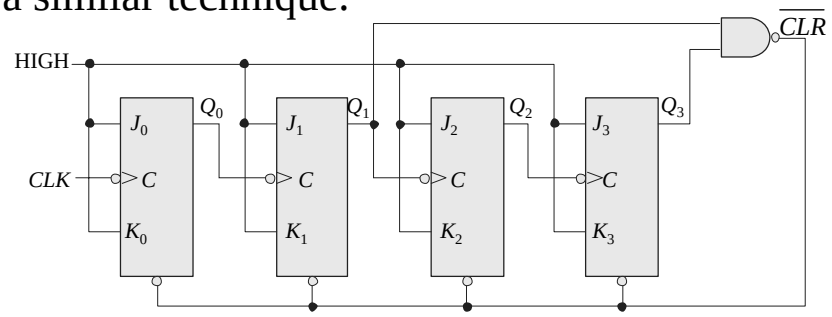
Se pueden diseñar contadores con n biestables con un módulo menor que n → **secuencia truncada**.

Esto se consigue haciendo que el contador vuelva al estado inicial, mediante la entrada asíncrona de CLEAR, antes de llegar al final de la cuenta.

Summary

Asynchronous Decade Counter

This counter uses partial decoding to recycle the count sequence to zero after the 1001 state. The flip-flops are trailing-edge triggered, so clocks are derived from the *Q* outputs. Other truncated sequences can be obtained using a similar technique.

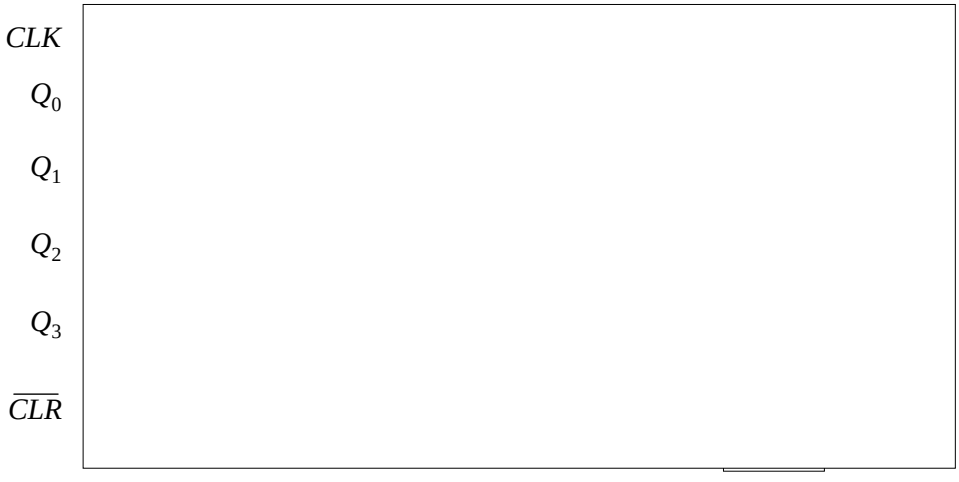


Waveforms are on the following slide…

Summary

Asynchronous Decade Counter

When Q_1 and Q_3 are HIGH together, the counter is cleared by a "glitch" on the $\overline{CLR}$ line.

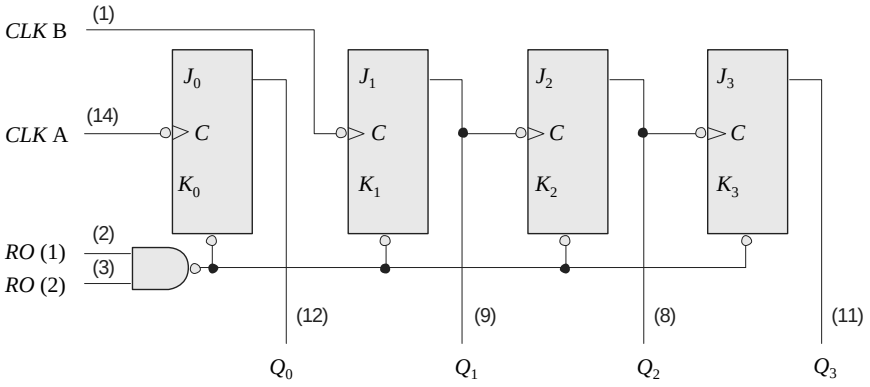


Summary

The 74LS93A Asynchronous Counter

The 74LS93A has one independent toggle J-K flip-flop driven by *CLK* A and three toggle J-K flip-flops that form an asynchronous counter driven by *CLK* B.

The counter can be extended to form a 4-bit counter by connecting Q_0 to the *CLK* B input. Two inputs are provided that clear the count.



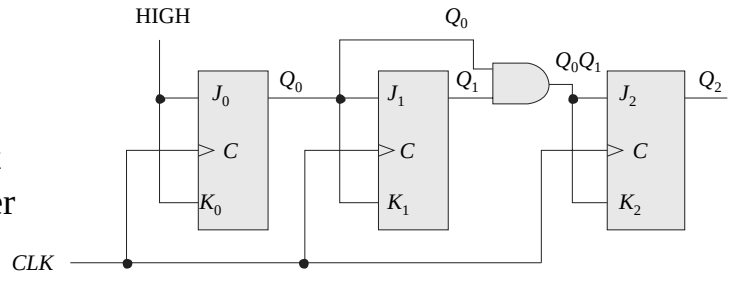
All J and K inputs are connected internally HIGH

Summary

Synchronous Counters

In a **synchronous counter** all flip-flops are clocked together with a common clock pulse. Synchronous counters overcome the disadvantage of accumulated propagation delays, but generally they require more circuitry to control states changes.

This 3-bit binary synchronous counter has the same count sequence as the 3-bit asynchronous counter shown previously.



The next slide shows how to analyze this counter by writing the logic equations for each input. Notice the inputs to each flip-flop…

Summary

Analysis of Synchronous Counters

A tabular technique for analysis is illustrated for the counter on the previous slide. Start by setting up the outputs as shown, then write the logic equation for each input. This has been done for the counter.

1. Put the counter in an arbitrary state; then determine the inputs for this state.	2. Use the new inputs to determine the next state: Q_2 and Q_1 will latch and Q_0 will toggle.	3. Set up the next group of inputs from the current output.

Outputs	Logic for inputs					
$Q_2\,Q_1\,Q_0$	$J_2 = Q_0Q_1$	$K_2 = Q_0Q_1$	$J_1 = Q_0$	$K_1 = Q_0$	$J_0 = 1$	$K_0 = 1$
0 0 0	0	0	0	0	1	1
0 0 1	0	0	1	1	1	1
0 1 0						

4. Q_2 will latch again but both Q_1 and Q_0 will toggle.

Continue like this, to complete the table. The next slide shows the completed table…

Summary

Analysis of Synchronous Counters

Outputs	Logic for inputs					
$Q_2\,Q_1\,Q_0$	$J_2 = Q_0Q_1$	$K_2 = Q_0Q_1$	$J_1 = Q_0$	$K_1 = Q_0$	$J_0 = 1$	$K_0 = 1$
0 0 0	0	0	0	0	1	1
0 0 1	0	0	1	1	1	1
0 1 0	0	0	0	0	1	1
0 1 1	1	1	1	1	1	1
1 0 0	0	0	0	0	1	1
1 0 1	0	0	1	1	1	1
1 1 0	0	0	0	0	1	1
1 1 1	1	1	1	1	1	1
0 0 0						

At this points all states have been accounted for and the counter is ready to recycle…

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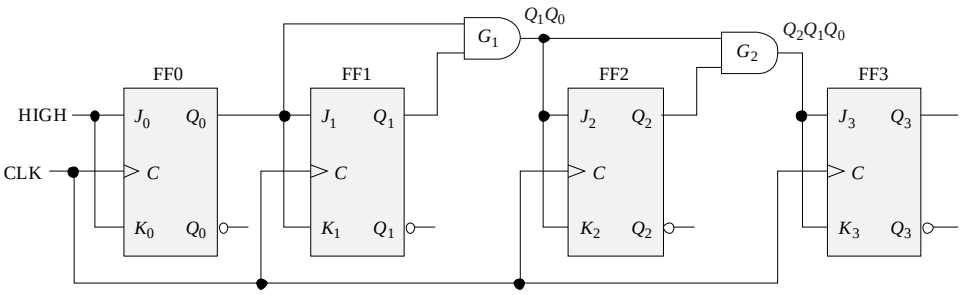
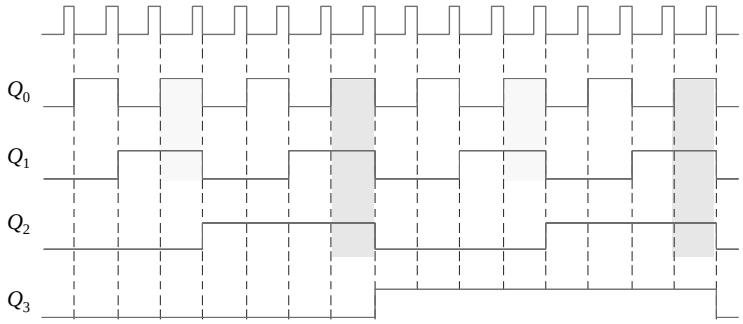
Summary

A 4-bit Synchronous Binary Counter



The 4-bit binary counter has one more AND gate than the 3-bit counter just described. The shaded areas show where the AND gate outputs are HIGH causing the next FF to toggle.

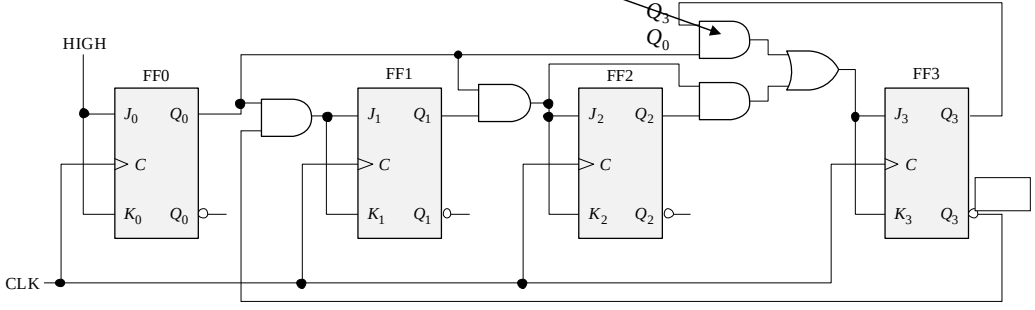


Summary

BCD Synchronous Decade Counter

With some additional logic, a binary counter can be converted to a BCD synchronous decade counter. After reaching the count 1001, the counter recycles to 0000.

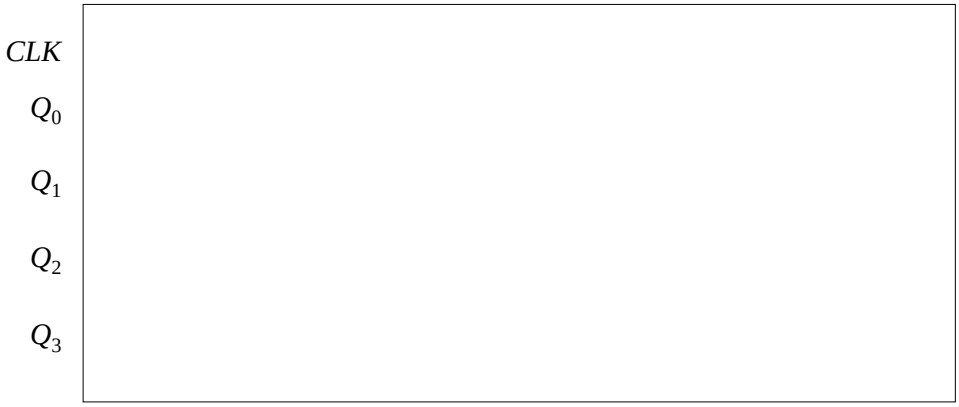
This gate detects 1001, and causes FF3 to toggle on the next clock pulse. FF0 toggles on every clock pulse. Thus, the count starts over at 0000.



Summary

BCD Decade Counter

Waveforms for the decade counter:

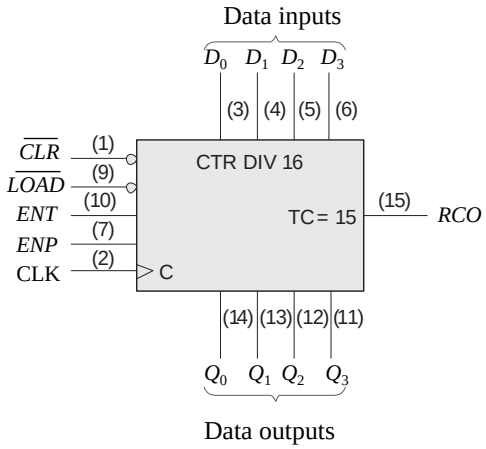


These same waveforms can be obtained with an asynchronous counter in IC form – the 74LS90. It is available in a dual version – the 74LS390, which can be cascaded. It is slower than synchronous counters (max count frequency is 35 MHz), but is simpler.

Summary

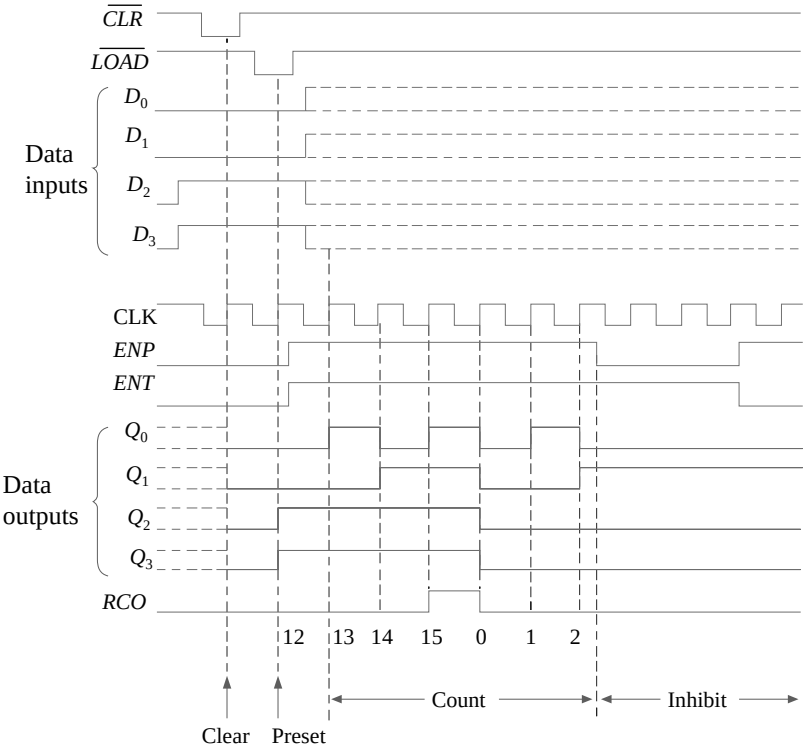
A 4-bit Synchronous Binary Counter

The 74LS163 is a 4-bit IC synchronous counter with additional features over a basic counter. It has parallel load, a $\overline{CLR}$ input, two chip enables, and a ripple count output that signals when the count has reached the terminal count.



Example waveforms are on the next slide…

Summary



Summary

Up/Down Synchronous Counters

An up/down counter is capable of progressing in either direction depending on a control input.

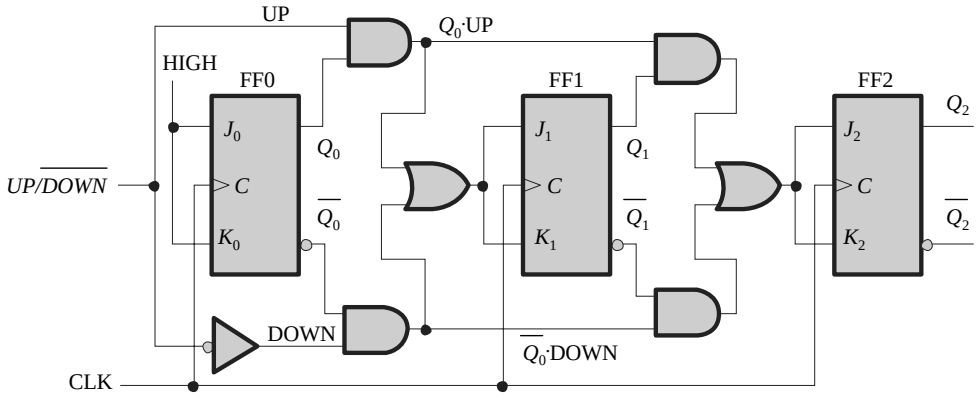
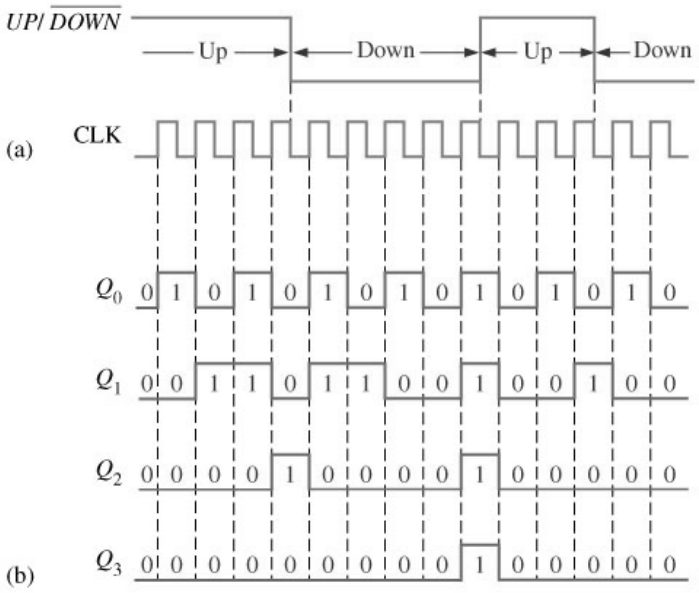


TABLE 9–5

Up/Down sequence for a 3-bit binary counter.

CLOCK PULSE	UP	Q_2	Q_1	Q_0	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

Ejemplo de funcionamiento



Q_3	Q_2	Q_1	Q_0	
0	0	0	0	
0	0	0	1	
0	0	1	0	UP
0	0	1	1	
0	1	0	0	
0	0	1	1	
0	0	1	0	
0	0	0	1	DOWN
0	0	0	0	
1	1	1	1	
0	0	0	0	
0	0	0	1	UP
0	0	1	0	
0	0	0	1	DOWN
0	0	0	0	

Diseño de contadores síncronos

Pasos:
(1) **Diagrama de estados**: representación gráfica de la secuencia de estados.
(2) **Tabla de estado siguiente**: para cada estado; utilizando el diagrama anterior.
(3) **Tabla de transiciones** de los biestables: valor de las entradas para cada una de las posibles transiciones.
(4) **Mapas de Karnough**: las entradas de los biestables en función de los estados; utilizando las dos tablas anteriores.
(5) **Expresiones lógicas** de las entradas: obtenidas por Karnough.
(6) **Implementación** del contador: realización con puertas lógicas y los biestables.

Step 1: State Diagram

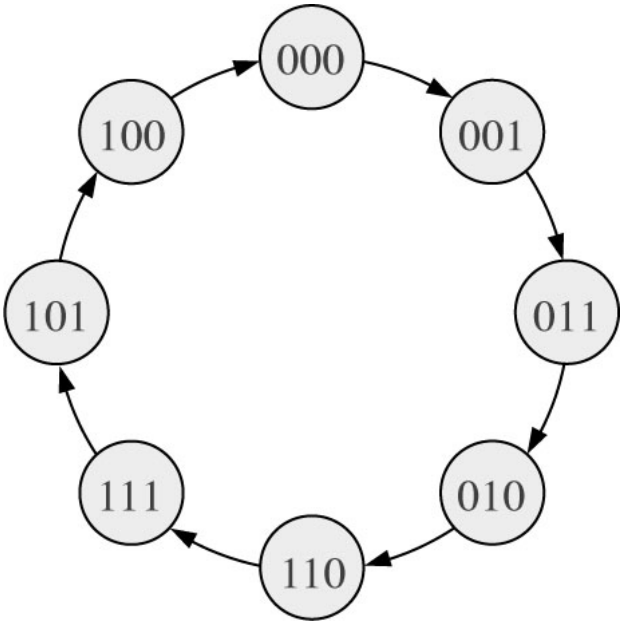


Figure 9--28 State diagram for a 3-bit Gray code counter.

Step 2: Next-State Table

TABLE 9–7

Next-state table for 3-bit Gray code counter.

PRESENT STATE			NEXT STATE		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Step 3: Flip-Flop Transition Table

TABLE 9–8

Transition table for a J-K flip-flop.

OUTPUT TRANSITIONS			FLIP-FLOP INPUTS	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Q_N: present state

Q_{N+1}: next state

X: "don't care"

Step 4: Karnaugh Maps

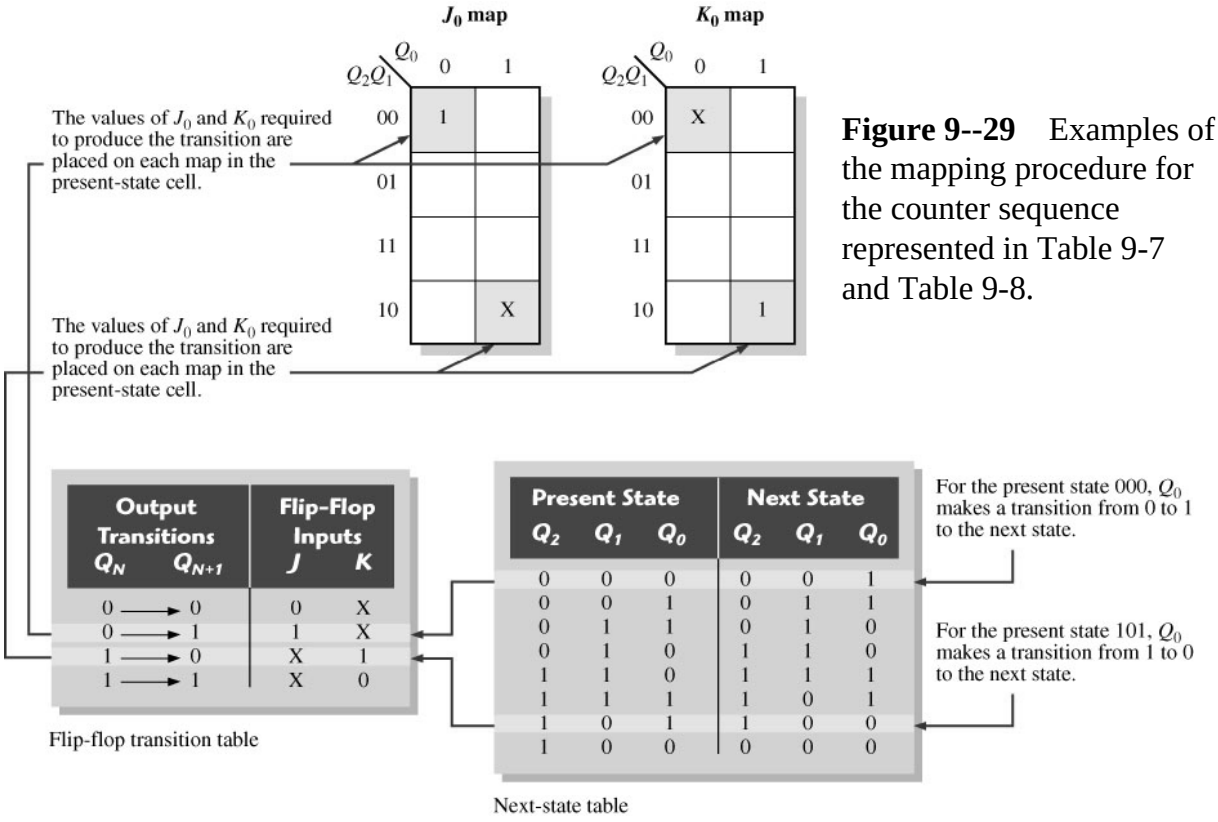


Figure 9--29 Examples of the mapping procedure for the counter sequence represented in Table 9-7 and Table 9-8.

Step 5: Logic Expressions for Flip-Flop Inputs

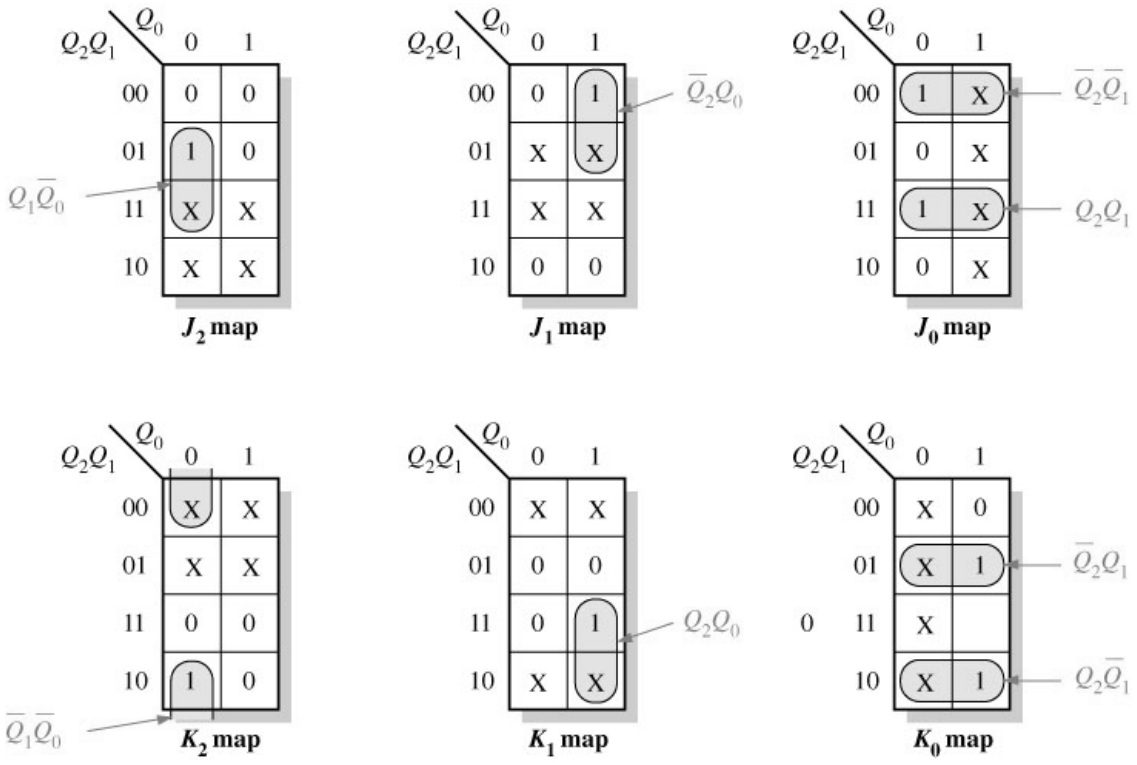


Figure 9--30 Karnaugh maps for present-state *J* and *K* inputs.

Step 6: Counter Implementation

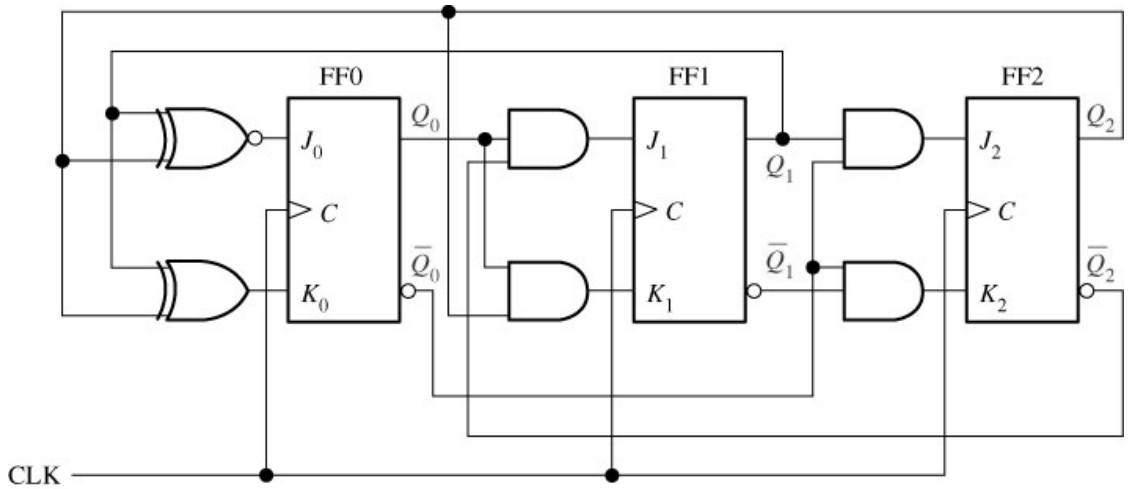
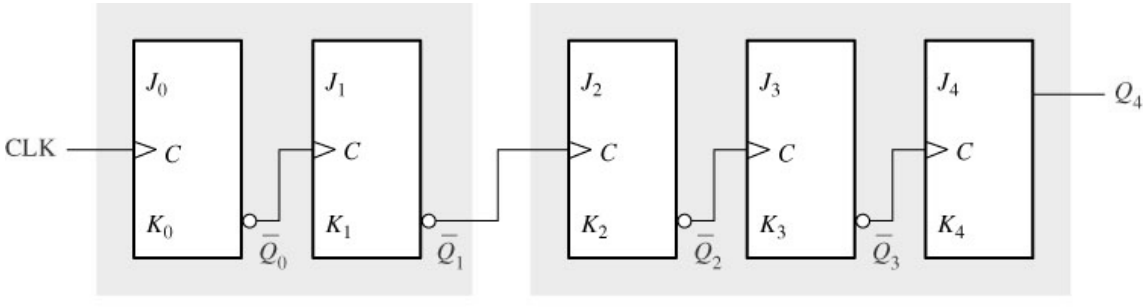
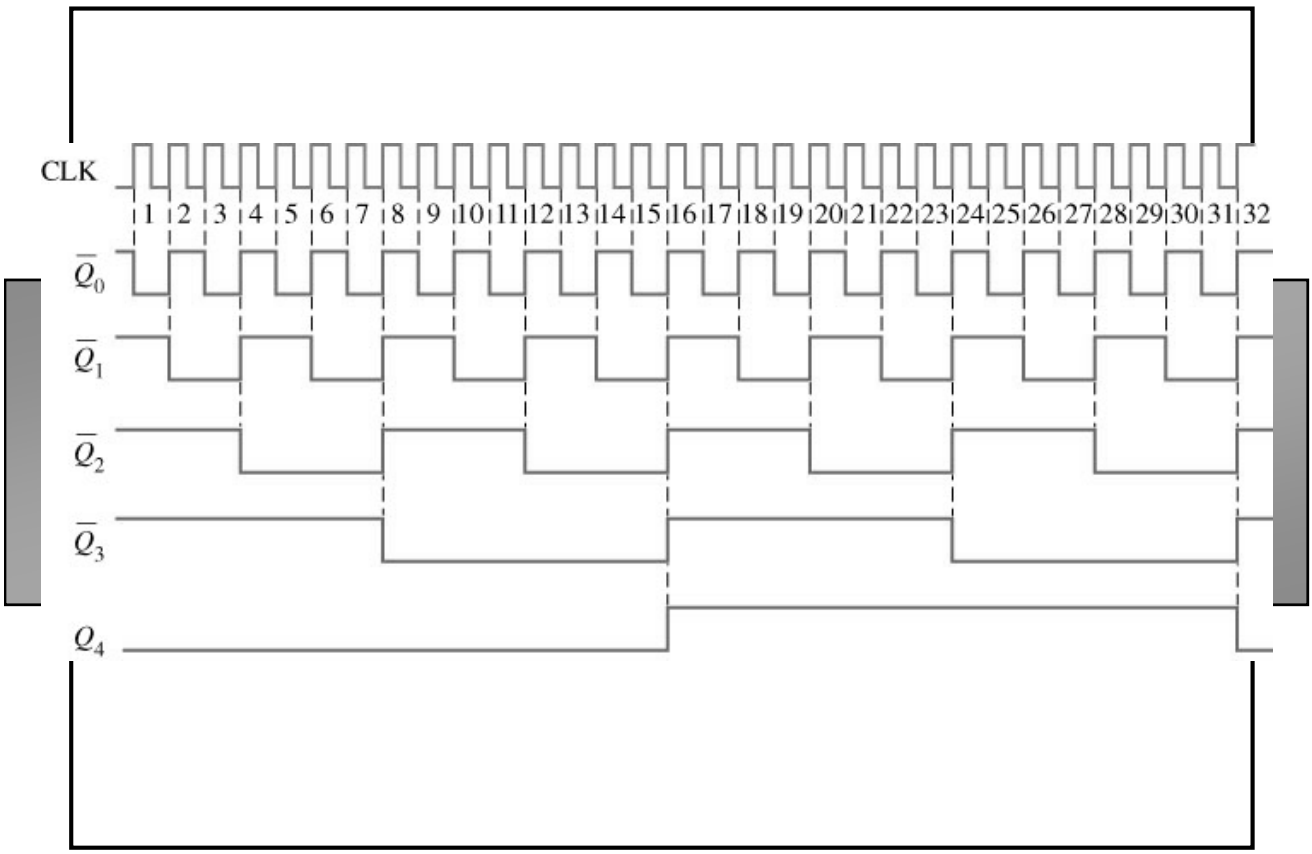


Figure 9--31 Three-bit Gray code counter.

Contadores en cascada

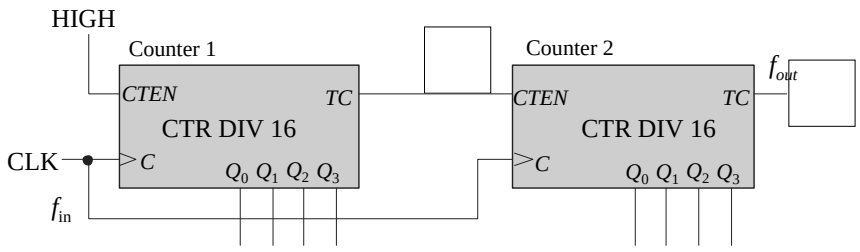
Para trabajar con módulos mayores





Circuitos contadores integrados en cascada

For synchronous IC counters, the next counter is enabled only when the terminal count of the previous stage is reached.



Example

a) What is the modulus of the cascaded DIV 16 counters?
b) If f_{in} =100 kHz, what is f_{out}?

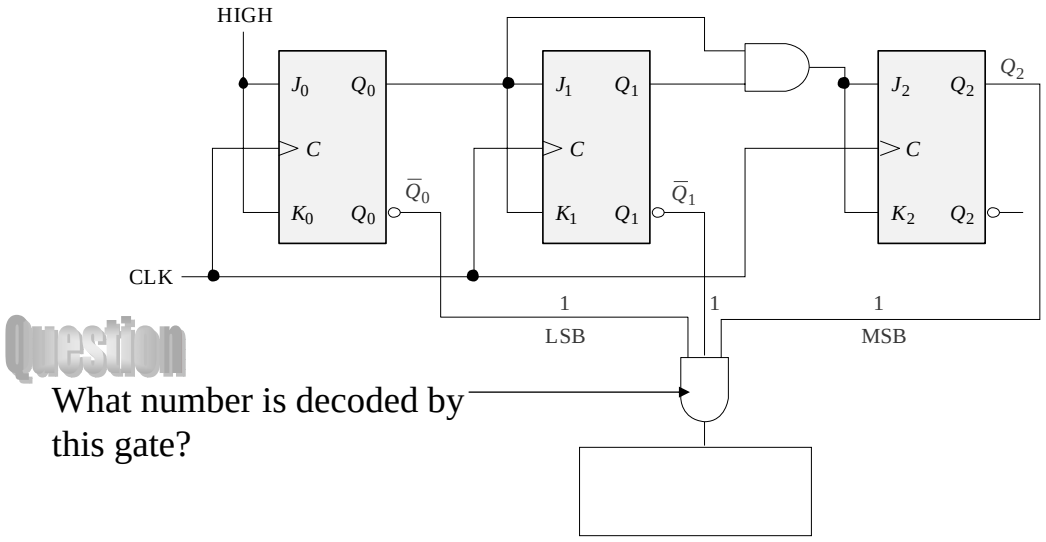
Solution

a) Each counter divides the frequency by 16. Thus the modulus is $16^2 = 256$.
b) The output frequency is 100 kHz/256 = 391 Hz

Summary

Counter Decoding

Decoding is the detection of a binary number (state) and can be done with an AND gate.



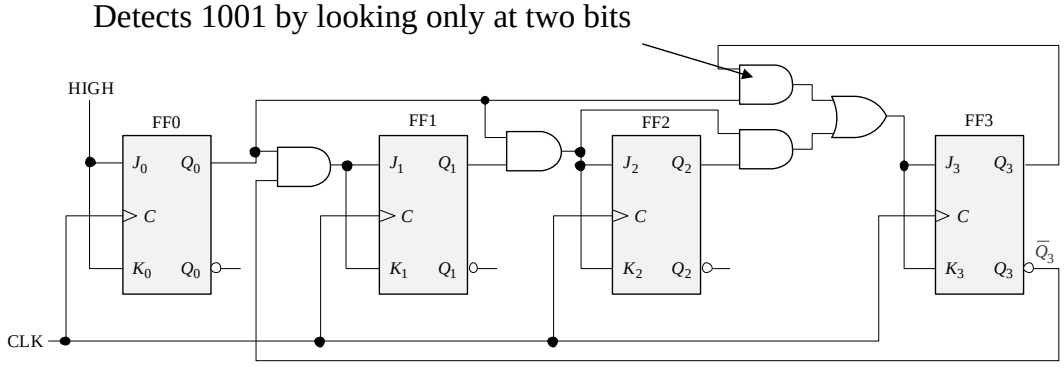
Question

What number is decoded by this gate?

Summary

Partial Decoding

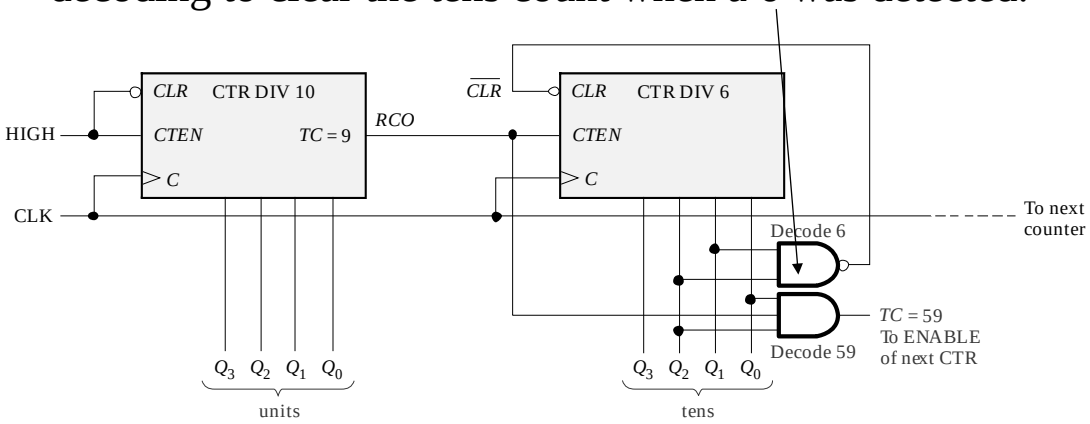
The decade counter shown previously incorporates *partial decoding* (looking at only the MSB and the LSB) to detect 1001. This was possible because this is the first occurrence of this combination in the sequence.



Summary

Resetting the Count with a Decoder

The divide-by-60 counter in the text also uses partial decoding to clear the tens count when a 6 was detected.



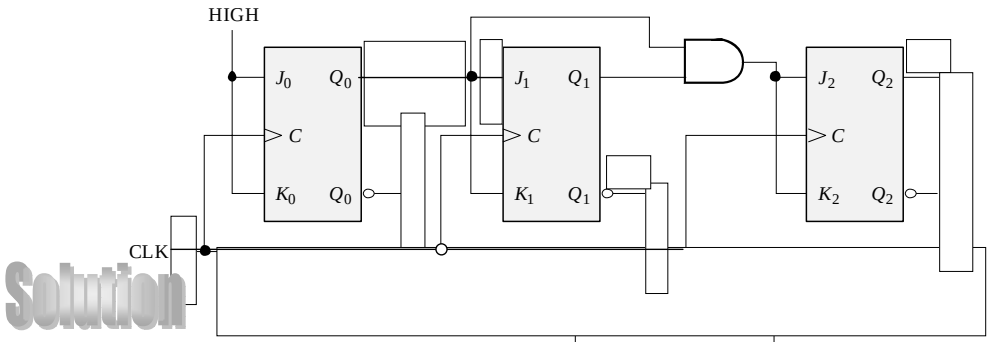
The divide characteristic illustrated here is a good way to obtain a lower frequency using a counter. For example, the 60 Hz power line can be converted to 1 Hz.

Summary

Counter Decoding

Example

Show how to decode state 5 with an active LOW output.



Solution

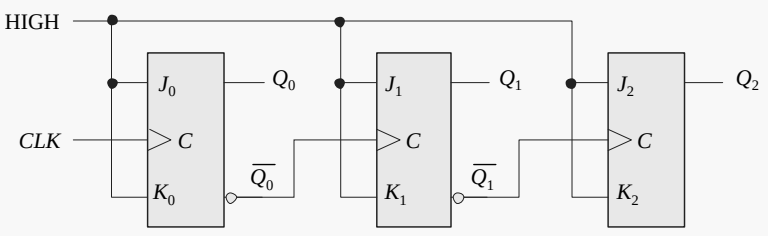
Notice that a NAND gate was used to give the active LOW output.

Selected Key Terms

Asynchronous	Not occurring at the same time.
Modulus	The number of unique states through which a counter will sequence.
Synchronous	Occurring at the same time.
Terminal count	The final state in a counter's sequence.
State machine	A logic system exhibiting a sequence of states or values.
Cascade	To connect "end-to-end" as when several counters are connected from the terminal count output of one to the enable input of the next counter.

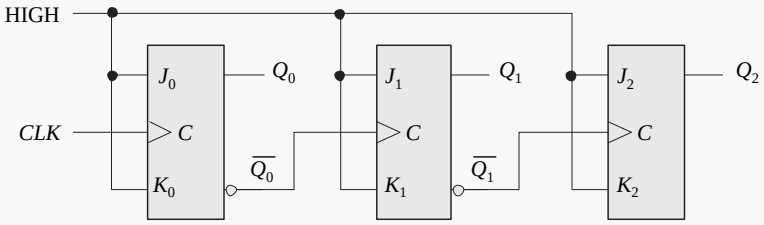
Quiz

1. The counter shown below is an example of
   a. an asynchronous counter
   b. a BCD counter
   c. a synchronous counter
   d. none of the above



Quiz

2. The Q_0 output of the counter shown
   a. is present before Q_1 or Q_2
   b. changes on every clock pulse
   c. has a higher frequency than Q_1 or Q_2
   d. all of the above



Quiz

3. To cause a D flip-flop to toggle, connect the
   a. clock to the *D* input
   b. *Q* output to the *D* input
   c. $\overline{Q}$ output to the *D* input
   d. clock to the preset input

Quiz

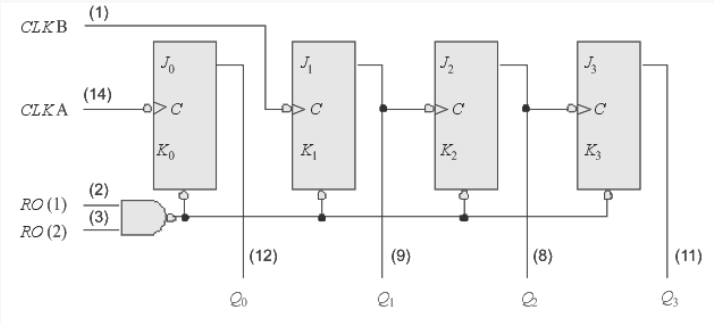
4. The 7493A asynchronous counter diagram is shown (*J*'s and *K*'s are HIGH.) To make the count have a modulus of 16, connect

   a. Q_0 to RO(1) and RO(2) to

   b. Q_3 to RO(1) and RO(2)

   c. *CLK* A and *CLK* B together

   d. Q_0 to *CLK* B



Quiz

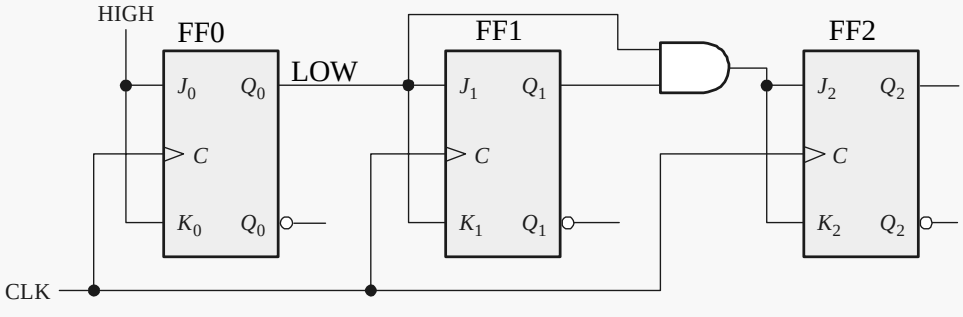
5. Assume Q_0 is LOW. The next clock pulse will cause

   a. FF1 and FF2 to both toggle

   b. FF1 and FF2 to both latch

   c. FF1 to latch; FF2 to toggle

   d. FF1 to toggle; FF2 to latch



Quiz

6. A 4-bit binary counter has a terminal count of
   a. 4
   b. 10
   c. 15
   d. 16

Quiz

7. Assume the clock for a 4-bit binary counter is 80 kHz. The output frequency of the fourth stage (Q_3) is
   a. 5 kHz
   b. 10 kHz
   c. 20 kHz
   d. 320 kHz

Quiz

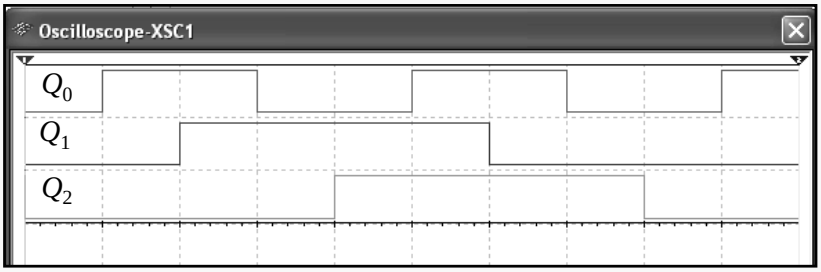
8. A 3-bit count sequence is shown for a counter (Q_2 is the MSB). The sequence is

a. 0-1-2-3-4-5-6-7-0 (repeat)

b. 0-1-3-2-6-7-5-4-0 (repeat)

c. 0-2-4-6-1-3-5-7-0 (repeat)

d. 0-4-6-2-3-7-5-1-0 (repeat)



Quiz

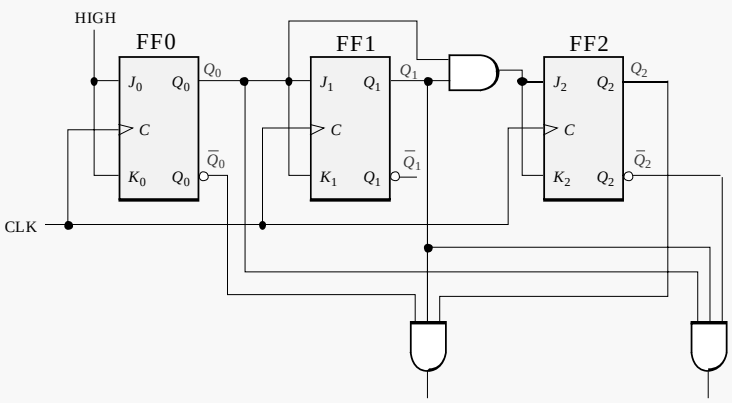
9. FF2 represents the MSB. The counts that are being decoded by the 3-input AND gates are

a. 2 and 3

b. 3 and 6

c. 2 and 5

d. 5 and 6



Quiz

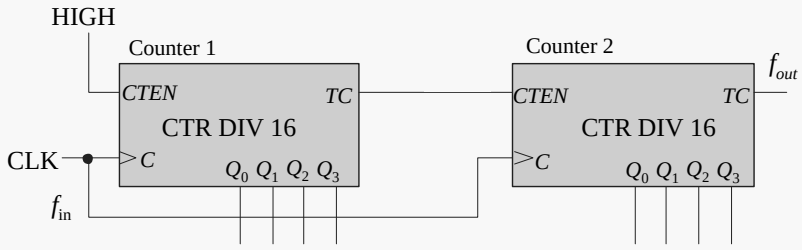
10. Assume the input frequency (f_{in}) is 256 Hz. The output frequency (f_{out}) will be

a. 16 Hz

b. 1 kHz

c. 65 kHz

d. none of the above



Quiz

Answers:

1. a	6. c
2. d	7. a
3. c	8. b
4. d	9. b
5. b	10. d