Sudharshan Viswanathan

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Professional Experience

- **Quantitative Developer, Morgan Stanley India, Mumbai** 2013- 2015
  - Implemented **Line Search minimization** methods separating callbacks from the minimization algorithm. Assisted an internship project in implementing Trust Region Strategies. Implementations to be used in Calibration use cases across the bank
  - Refactored proprietary Date Rolling Library - Developed a **Stateless Referentially Transparent Immutable API** while removing the extant **Dependency** on **Singleton** pattern in C++. Extend functionality to Java using **SWIG**
  - Library Support and Maintenance - bug fixes and new additional features for the proprietary legacy Bond Analytics library while conforming to industry standards
  - Integral part of the transition in the development environment of the team. Ensured backward compatibility of the build systems and responsible for setting up and testing of software releases
- **Internship, American Express India, Gurgaon** May - July 2012
  - Leveraged the **Longitudinal Behaviour** of early transactions towards predicting **Short & Long Term Risk** - Model **2 times better risk** indication for early defaulters and **50 bps lower** for good customers than existing methods
  - Developed a system that extracts **risky/credit-worthy behaviour** and flags events across different markets worldwide

Education & Scholastic Achievements

- **Indian Institute of Technology Madras** 2008-2013
  - **Major**: Electrical Engineering **Masters**: VLSI Design and Microelectronics **Minor**: Physics **CGPA: 9.06/10**
  - **Technical Skills**. Prog. Languages - Advanced: C++, Verilog. Basic: Java, Scala, Python
  - Winner of **TAU Contest**(Variation aware timing) 2012-13. Implemented a multi-threaded Statistical Timing Tool for multi-core CPU architecture. *Team Size*: 2
  - Selected to represent IIT Madras in the **Indo-German Winter Academy** conducted in December 2011 by IIT Delhi-FAU Erlangen. Presented a Technical Talk on **Resistive Memory Devices**
  - Selected for the **International Olympiad in Informatics Training Camp**. Ranked in **top 25** at the Indian National Olympiad For Informatics(**INOI**)

Projects

- **Final Year Project** 2012-2013
  - Statistical Static Timing Analysis Model(**SSTA**) based timing algorithms on a GP-GPU - Explored features, methods and drawbacks of different implementations of the algorithm
  - Implemented and Anaylsed the Block Based SSTA algorithm on different MT environments: **multi-core** and in **NVidia GPUs** using CUDA while tackling constraints of CUDA architecture
- **Course Projects** 2010-2012
  - Digital VLSI: A Pipelined and Sliding-Window Canny Edge Detector on FPGA (*CAD For VLSI Design*). Reciprocal and Square Root of Complex Numbers using spline interpolation on FPGA (*DSP Architectures*)

Positions Of Responsibility

- **Core, Web And Mobile Operations, Shaastra** May-October 2011
  - Led a team of 20 coordinators to completely rebuild website for Shaastra, annual technical festival of IIT Madras - in 2 months with **custom backend** - improved ease of use for Event Coordinators and Participants
  - Laid the foundations for an in-house **Enterprise Resource Planning**(ERP) system for the entire team of 300 students
- **Core, Election Engineering Team**
  - Led the Election Engineering team for the Student Body Elections 2011. Implemented a **Secure Web Based Voting** for a 5000-strong electorate across 20 polling stations

Extra Curricular Activities

- Integral part of Morgan Stanley Cricket team in Corporate Leagues.
- Trained in Vocal Carnatic Music. Participated in Solo Vocal competitions held in IIT Madras.