HIGH-VOLTAGE MIXED-SIGNAL IC

UC1601

65x132 STN Controller-Driver

MP Specifications
Datasheet Revision: 1.25

IC Version: s_A
August 11, 2010

ULTRACHIP

The Coolest LCD Driver, Ever!

Table of Content

UC1601

Single-Chip, Ultra-Low Power
65COM by 132SEG
Passive Matrix LCD Controller-Driver

INTRODUCTION

UC1601s is an advanced high-voltage mixed-signal CMOS IC, especially designed for the display needs of ultra-low power hand-held devices.

This chip employs UltraChip's unique DCC (Direct Capacitor Coupling) driver architecture to achieve near crosstalk free images.

In addition to low power column and row drivers, the IC contains all necessary circuits for high-V LCD power supply, bias voltage generation, timing generation and graphics data memory.

Advanced circuit design techniques are employed to minimize external component counts and reduce connector size while achieving extremely low power consumption.

MAIN APPLICATIONS

- Cellular Phones, Smart Phones, PDA, and other battery operated palm top devices or portable Instruments

FEATURE HIGHLIGHTS

- Single chip controller-driver support 65x132 graphics STN LCD panels.
- Support both row ordered and column ordered display buffer RAM access.
- A software-readable ID pin to support configurable vender identification.
- Support both row-ordered and column-ordered display buffer RAM access.
- Support industry standard 8-bit parallel bus (8080 or 6800 mode), 4-wire and 3-wire serial buses (S8 and S9), and 2-wire I^2C serial interface.
- Ultra-low power consumption under all display patterns.
- Fully programmable Mux Rate, partial display, Bias Ratio and Frame Rate allow many flexible power management options.
- Software programmable frame rates at 80 and 100 Hz.
- Four software programmable temperature compensation coefficients.
- 7-x internal charge pump with on-chip pumping capacitor requires only 3 external capacitors to operate.
- On-chip Power-ON Reset and Software RESET commands, make RST pin optional.
- Very low pin count (10-pin) allows exceptional image quality in COG format on conventional ITO glass.
- Flexible data addressing/mapping schemes to support wide ranges of software models and LCD layout placements.
- V_{DD} (digital) range (Typ.): 1.8V ~ 3.3V
  V_{DD} (analog) range(Typ.): 2.5V ~ 3.3V
  LCD V_{OP} range: 4.7V ~ 11.5V
- Available in gold bump dies
- COM/SEG bump information
  Bump pitch: 35.5 μM
  Bump gap: 13 μM
  Bump surface: 2002.5 μM^2

ORDERING INFORMATION

Part Number	MTP	I^2C	Description
UC1601sGAA	No	Yes	Gold Bumped Die

General Notes

APPLICATION INFORMATION

For improved readability, the specification contains many application data points. When application information is given, it is advisory and does not form part of the specification for the device.

USE OF I^2C

The implementation of I^2C is already included and tested in all silicon.

BARE DIE DISCLAIMER

All die are tested and are guaranteed to comply with all data sheet limits up to the point of. There is no post waffle saw/pack testing performed on individual die. Although the latest modern processes are utilized for wafer sawing and die pick-&-place into waffle pack carriers, UltraChip has no control of third party procedures in the handling, packing or assembly of the die. Accordingly, it is the responsibility of the customer to test and qualify their application in which the die is to be used. UltraChip assumes no liability for device functionality or performance of the die or systems after handling, packing or assembly of the die.

LIFE SUPPORT APPLICATIONS

These devices are not designed for use in life support appliances, or systems where malfunction of these products can reasonably be expected to result in personal injuries. Customer using or selling these products for use in such applications do so at their own risk.

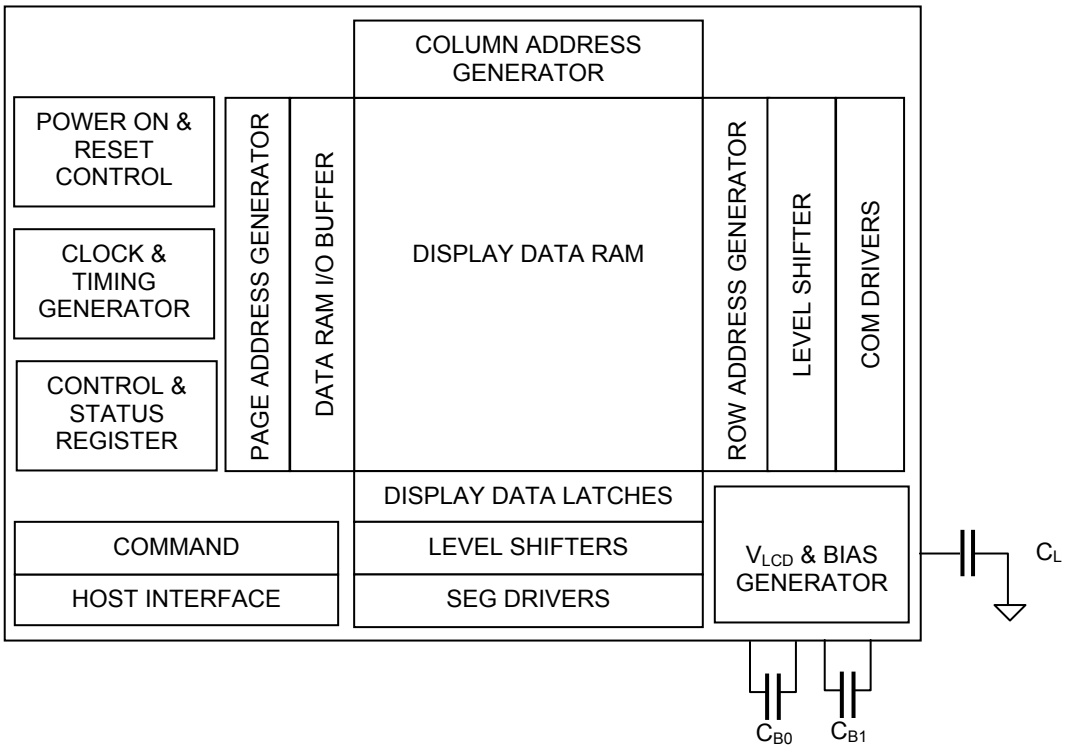
CONTENT DISCLAIMER

CONTACT DETAILS

UltraChip Inc. (Headquarter)
4F, No. 618, Recom Road,
Neihu District, Taipei 114,
Taiwan, R. O. C.

Tel: +886 (2) 8797-8947
Fax: +886 (2) 8797-8910
Sales e-mail: sales@ultrachip.com
Web site: http://www.ultrachip.com

BLOCK DIAGRAM

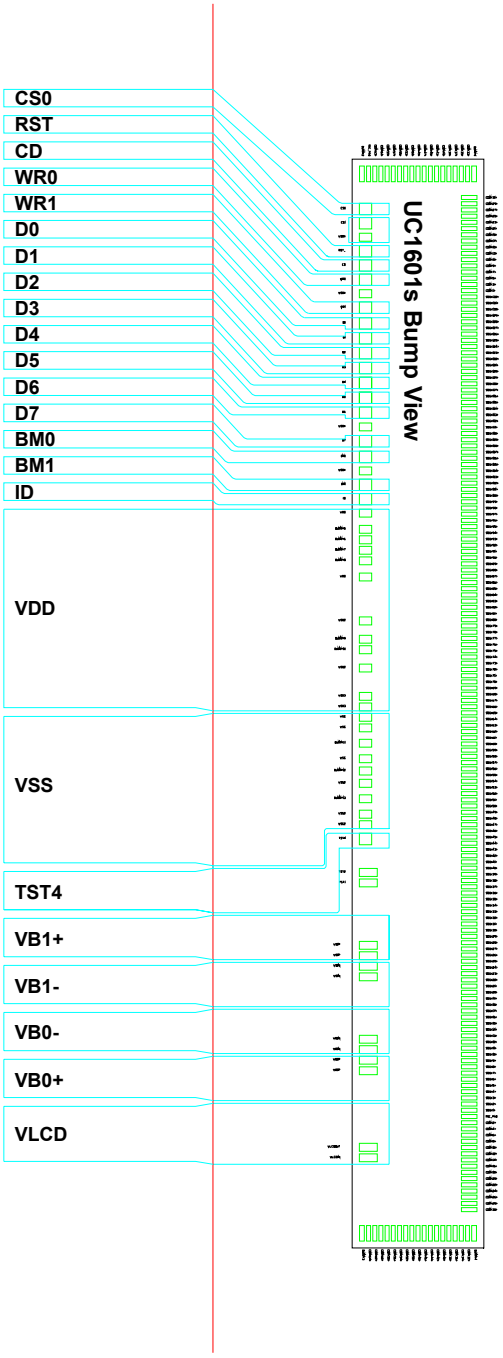


PIN DESCRIPTION

Name	Type	Pins	Description
MAIN POWER SUPPLY			
V_{DD} V_{DD2} V_{DD3}	PWR	3 3 2	V_{DD} supplies for Display Data RAM and digital logic, V_{DD2} supplies for V_{LCD} and V_D generator, V_{DD3} supplies for V_{BIAS} and other analog circuits. V_{DD2}/V_{DD3} should be connected to the same power source. But V_{DD} can be connected to a source voltage no higher than V_{DD2}/V_{DD3}. Please maintain the following relationship: $V_{DD}+1.3V \geqslant V_{DD2/3} \geqslant V_{DD}$ ITO trace resistance needs to be minimized for V_{DD2}/V_{DD3}.
V_{SS} V_{SS2}	GND	4 4	Ground. Connect V_{SS} and V_{SS2} to the shared GND pin. In COG applications, minimize the ITO resistance for both V_{SS} and V_{SS2}.
LCD POWER SUPPLY & VOLTAGE CONTROL			
V_{B1+} V_{B1-} V_{B0+} V_{B0-}	PWR	2 2 2 2	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of C_{BX} value between V_{BX+} and V_{BX-}. In COG application, the resistance of these ITO traces directly affects the SEG driving strength of the resulting LCD module. Minimize these trace resistance is critical in achieving high quality image.
V_{LCDIN} V_{LCDOUT}	PWR	1 1	Main LCD Power Supply. When internal V_{LCD} is used, connect these pins together. When external V_{LCD} source is used, connect external V_{LCD} source to V_{LCDIN} pins and leave V_{LCDOUT} open. By-pass capacitor C_L is optional. It can be connected between V_{LCD} and V_{SS}. When C_L is used, keep the ITO trace resistance around 70 Ω .
NOTE: • Recommended capacitor values: C_B: 2.2μF/5V or 300x(LCD load capacitance), whichever is higher. C_L: 330nF/25V is appropriate for most applications.			
HOST INTERFACE			
BM0 BM1	I	1 1	Bus mode: The interface bus mode is determined by BM[1:0] and {DB7, DB6} by the following relationship: BM[1:0] / {DB7, DB6} / Mode 11 / Data / 6800/8-bit 10 / Data / 8080/8-bit 00 / 10 / 4-wire SPI w/ 8-bit token (S8: conventional) 01 / 10 / 3-wire SPI w/ 9-bit token (S9: conventional) 01 / 11 / 2-wire serial (I^2C)
CS1/A3 CS0/A2	I	1 1	Chip Select. Chip is selected when CS1="H" and CS0 = "L". When the chip is not selected, D[15:0] will be of high impedance. In I^2C mode, these two pins specifies bits 3~2 of UC1601s' device address (A[3:2]).
RST	I	1	When RST="L", all control registers are re-initialized by their default states. Since UC1601s has built-in Power-On Reset and Software Reset command, RST pin is not required for proper chip operation. An RC Filter has been included on-chip. There is no need for external RC noise filter. When RST is not used, connect the pin to V_{DD}.
CD	I	1	Select Control data or Display data for read/write operation. In S9, CD pin is not used. Connect CD to V_{SS} when not used. "L": Control data "H": Display data

<table>
<tr><th>Name</th><th>Type</th><th>Pins</th><th>Description</th></tr>
<tr><td>ID</td><td>I</td><td>1</td><td>ID may be used for production identification.
Connect ID to V_{DD} for “H” or V_{SS} for “L”.</td></tr>
<tr><td>WR0
WR1</td><td>I</td><td>1
1</td><td>WR [1:0] controls the read/write operation of the host interface. See Host Interface section for details.
In parallel mode, the meaning of WR[1:0] depends on which interface it is in, 6800 or 8080 mode. In serial interface modes, these two pins are not used, Connect them to V_{SS}.</td></tr>
<tr><td>D0~D7</td><td>I/O</td><td>8</td><td>Bi-directional bus for both serial and parallel host interfaces.
In serial modes, connect D[0] to SCK, D[3] to SDA.
<table>
<tr><th></th><th>BM=1x
(8-bit)</th><th>BM=00
(S8)</th><th>BM=01
(S9)</th><th>BM=01
(I^2C)</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td><td>SCK</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td>--</td><td>--</td><td>--</td></tr>
<tr><td>D2</td><td>D2</td><td>--</td><td>--</td><td>--</td></tr>
<tr><td>D3</td><td>D3</td><td>SDA</td><td>SDA</td><td>SDA</td></tr>
<tr><td>D4</td><td>D4</td><td>--</td><td>--</td><td>--</td></tr>
<tr><td>D5</td><td>D5</td><td>--</td><td>--</td><td>--</td></tr>
<tr><td>D6</td><td>D6</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>D7</td><td>D7</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Always connect unused pins to either V_{SS} or V_{DD}.</td></tr>
<tr><th colspan="4">HIGH VOLTAGE LCD DRIVER OUTPUT</th></tr>
<tr><td>SEG1 ~
SEG132</td><td>HV</td><td>132</td><td>SEG (column) driver outputs. Support up to 132 pixels.
Leave unused SEG drivers open-circuit.</td></tr>
<tr><td>COM1 ~
COM64</td><td>HV</td><td>64</td><td>COM (row) driver outputs. Support up to 64 rows.
When designing LCM, always start from COM1. If the LCM has N pixel rows and N is less than 64, set CEN to be N-1, and leave COM drivers [N+1 ~ 64] open-circuit.</td></tr>
<tr><td>CIC</td><td>HV</td><td>2</td><td>Icon driver outputs. Leave it open if not used.</td></tr>
<tr><td colspan="4">Note:
Several control registers will specify “0 based index” for COM and SEG electrodes. In those situations, COMX or SEGX will correspond to index X-1, and the value range for those index register will be 0~63 for COM and 0~131 for SEG.</td></tr>
<tr><th colspan="4">MISC. PINS</th></tr>
<tr><td>V_{DDX}</td><td></td><td>1</td><td>Auxiliary V_{DD}. This pin is connected to the main V_{DD} bus within the IC. It’s provided to facilitate chip configurations in COG application.
There’s no need to connect V_{DDX} to main V_{DD} externally and it should NOT be used to provide V_{DD} power to the chip.</td></tr>
<tr><td>TST4</td><td>I</td><td>1</td><td>Test control. There’s an on-chip pull-up resistor for TST4. Connect to GND during normal operation.</td></tr>
<tr><td>TST2
TST1</td><td>I/O</td><td>1
1</td><td>Test I/O pins. Leave these pins open during normal use.</td></tr>
<tr><td>Dummy</td><td></td><td>13</td><td>Dummy pins are NOT connected inside the IC.</td></tr>
</table>

RECOMMENDED COG LAYOUT



NOTES FOR V_{DD} WITH COG:

The operation condition, V_{DD}=1.8V (typical), should be satisfied under all operating conditions. UC1601s' peak current (I_{DD}) can be up to ~15mA during high speed data-write to UC1601s' on-chip SRAM. Such high pulsing current mandates very careful design of V_{DD} and V_{SS} ITO trances in COG modules. When V_{DD} and V_{SS} trace resistance is not low enough, the pulsing I_{DD} current can cause the actual on-chip V_{DD} to drop to below 1.65V and cause the IC to malfunction.

CONTROL REGISTERS

UC1601s contains registers, which control the chip operation. The following table is a summary of these control registers, a brief description and the default values. These registers can be modified by commands, which will be described in the next two sections, Command Table and Command Description.

Name: The Symbolic reference of the register. Note that, some symbol name refers to bits (flags) within another register.

Default: Numbers shown in **Bold** font are default values after Power-Up-Reset and System-Reset.

Name	Bits	Default	Description
SL	6	00H	Scroll Line. Scroll the displayed image up by *SL* rows. The valid SL value is between 0 (for no scrolling) and 63. Setting SL outside of this range causes undefined effects on the displayed image. This register does not affect icon output CIC.
CA	8	00H	Column Address of DDRAM (Display Data RAM). Value range is 0~131. (Used in Host to access DDRAM)
PA	4	0H	Page Address of DDRAM. Value range 0~8. (Used in Host to access DDRAM)
BR	2	3H	Bias Ratio. The ratio between V_{LCD} and V_D. 00: 6 01: 7 10: 8 **11: 9**
TC	2	0H	Temperature Compensation (per ^oC). **00: -0.05%** 01: -0.10% 10: -0.15% 11: -0.00%
PM	8	C0H	Electronic Potentiometer to fine tune the value of V_{LCD}
PC	3	6H	Power Control. PC [0]: **0: LCD: ⩽ 15nF** 1: LCD: 15~24nF PC [2:1]: 00: External V_{LCD} **11: Internal V_{LCD} (7x charge pump)**
AC	3	1H	Address Control. AC[0]: WA: automatic column/page Wrap Around (Default **1: ON**) AC[1]: Auto-Increment order **0: Column (CA) first** 1: Page (PA) first AC[2]: PID: PA (page address) auto Increment Direction (**0:+1** 1:-1)
DC	3	0H	Display Control: DC[0]: PXV: Pixels Inverse (bit-wise data inversion. Default **0: OFF**) DC[1]: APO: All Pixels ON (Default **0: OFF**) DC[2]: Display ON/OFF (Default **0: OFF**) When DC[2] is set to 0, the IC will enter Sleep Mode
LC	5	00H	LCD Control: LC[0]: Reserved. LC[1]: MX, Mirror X SEG/Column sequence inversion (Default: **OFF**) LC[2]: MY, Mirror Y COM/Row sequence inversion (Default: **OFF**) LC[3]: Frame Rate **0b: 80 fps** 1b: 100 fps LC[4]: Partial Display control **0b: Disable** Mux-Rate = CEN+1 (DST, DEN not used) 1b: Enabled Mux-Rate = DEN-DST+1

Name	Bits	Default	Description
CEN DST DEN	6 6 6	3FH 00H 3FH	COM-scanning End (last COM with full line cycle, 0-based index) Display Start (first COM with active scan pulse, 0-based index) Display End (last COM with active scan pulse, 0-based index) Please maintain the following relationship: CEN = (the actual number of pixel rows on the LCD) - 1 CEN ⩾ DEN ⩾ DST+ 9 CEN ⩾ 20 If duty between 9 and 20 is used, ensure that Partial Display is enabled (Duty = DEN – DST +1) and CEN ⩾ 20 is set.
APC		N/A	Advanced Program Control. For UltraChip only. Please do not use.
Status Registers			
OM	2	–	Operating Modes (Read only) 00b: Reset 01b: (Not used) 10b: Sleep 11b: Normal
ID	2	PIN	Access the connected status of ID pins.

COMMAND TABLE

The following is a list of host commands supported by UC1601s

C/D: 0: Control, 1: Data W/R: 0: Write Cycle, 1: Read Cycle D7-D0: # Useful Data bits – Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1.	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2.	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3.	Get Status	0	1	ID	MX	MY	WA	DE	0	0	0	Get Status	--
	(double-byte command)	0	1	Prod[3:0]				Ver	0	0	0		
4.	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA [3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA [7:4]	0
5.	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6.	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	110b
7.	Set Adv. Program Control	0	0	0	0	1	1	0	0	0	R	Set R, R = 0, or 1	N/A
	(double byte command)	0	0	#	#	#	#	#	#	#	#	Set APC[R][7:0]	
8.	Set Scroll Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
9.	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
10.	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	C0H
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
11.	Set Partial Display Control	0	0	1	0	0	0	0	1	0	#	Set LC[4]	0b
12.	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
13.	Set Frame Rate	0	0	1	0	1	0	0	0	0	#	Set LC[3]	0b
14.	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
15.	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
16.	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0b
17.	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	0	Set LC[2:1]	00b
18.	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
19.	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
20.	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#	Do not use.	
21.	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 9
22.	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	63
	(double-byte command)	0	0	-	#	#	#	#	#	#	#		
23.	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
	(double-byte command)	0	0	-	#	#	#	#	#	#	#		
24.	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	63
	(double-byte command)	0	0	-	#	#	#	#	#	#	#		
Serial Read Command (Enabled only in S8/S9 mode)													
25.	Get Status	0	0	1	1	1	1	1	1	1	0	Get status till chip disabled	N/A
	(triple-byte command)	0	1	ID	MX	MY	WA	DE	0	0	0		
		0	1	Prod [3:0]				Ver	0	0	0		

* Other than commands listed above, all other bit patterns result in NOP (No Operation).

COMMAND DESCRIPTION

1. Write Data Byte to Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8-bit data-write to SRAM							

2. Read Data Byte from Memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8-bit data-read from SRAM							

Write/Read Data Byte (Command 1,2) access Display Data RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will increase or decrease automatically after each bus cycle, depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of the page, and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches the end of the page, CA will be reset to 0 and PA will increase or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM, PA will be wrapped around to the other end of RAM and continue.

3. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	ID	MX	MY	WA	DE	**0**	**0**	**0**
	0	1	Prod [3:0]				Ver	**0**	**0**	**0**

Status1 definitions:
- ID: Provide access to ID pins connection status.
- MX: Status of register LC[1], mirror X.
- MY: Status of register LC[2], mirror Y.
- WA: Status of register AC[0]. Automatic column/row wrap around.
- DE: Display Enable flag. DE=1 when display is enabled.

Status2 definitions:
- Prod: Production identification. Default: **0110b**.
- Ver: IC Version, Value: **0**~1.

4. Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA value range: **0**~131

5. Set Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.05%/ °C 01b= -0.10%/ °C 10b= -0.15%/ °C 11b= -0.00%/°C

6. Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Power Control PC[2:0]	0	0	**0**	**0**	**1**	**0**	**1**	PC2	PC1	PC0

Set PC[0] according to the capacitance loading of LCD panel.
Panel loading definition: **0b : ≤ 15nF** 1b : 15~24nF

Set PC[2:1] to program the build-in charge pump stages.
00b = External V_{LCD} **11b =** Internal V_{LCD} (x7)

7. Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Adv. Program Control APC[R][7:0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
(Double byte command)	0	0	APC register parameter							

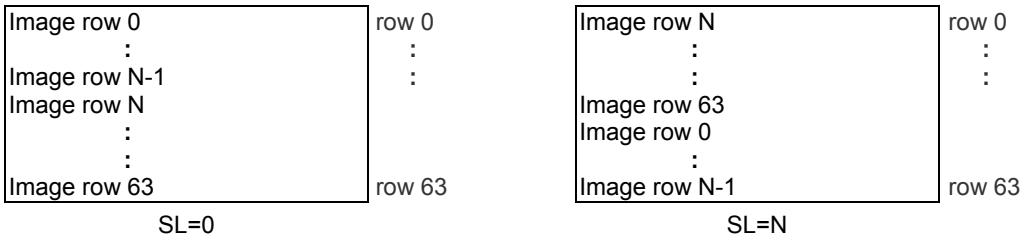
For UltraChip only. Please Do *NOT* use.

8. Set Scroll Line

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Scroll Line SL[5:0]	0	0	**0**	**1**	SL5	SL4	SL3	SL2	SL1	SL0

Set the number of lines to scroll up/down.

Scroll line setting will scroll the displayed image up by *SL* rows. Icon output CIC will not be affected by `Set Scroll Line` command.



9. Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address	0	0	**1**	**0**	**1**	**1**	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface. Each page of SRAM corresponds to 8 COM lines on LCD panel, except for the last page. The last page corresponds to the icon output CIC.

Possible value = 0~8.

10. Set VBIAS Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer PM [7:0] (Double byte command)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section `LCD Voltage Setting` for more detail.

Effective range: 0 ~ 255

11. Set Partial Display Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Partial Display Enable LC [4]	0	0	**1**	**0**	**0**	**0**	**0**	**1**	**0**	LC4

This command is used to enable partial display function.

LC[4] : **0**b: Disable Partial Display, Mux-Rate = CEN+1 (DST, DEN not used.)
1b: Enable Partial Display, Mux-Rate = DEN-DST+1

12. Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control. It controls the auto-increment behavior of CA and PA.

AC[0] – WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and CA or PA will increase by one.

AC[1] – Auto-Increment order
0 : column (CA) increasing (+1) first until CA reach CA boundary, then PA will increase by (+/-1).
1 : page (PA) increasing (+/-1) first until PA reach PA boundary, then CA will increase by (+1).

AC[2] – PID, page address (PA) auto increment direction (0/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether page address will be adjusted by +1 or -1.

13. Set Frame Rate

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Frame Rate LC [3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	**0**	LC3

Program LC [3] for frame rate setting

0b: 80 fps 1b: 100 fps
(fps: frame-per-second)

14. Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel ON DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

15. Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data (bit-wise) stored in display RAM. This function has no effect on the existing data stored in display RAM.

16. Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	DC2

This command is for programming register DC[2]. When DC[2] is set to 1, UC1601s will first exit from sleep mode, restore the power and then turn on COM drivers and SEG drivers.

17. Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Control LC[2:1]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	**0**

Set LC[2:1] for COM (row) mirror (MY), SEG (column) mirror (MX).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 50-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

18. System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset.

Control register values will be reset to their default values. Data store in RAM will not be affected.

19. NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No Operation	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**1**

This command is used for “no operation”.

20. Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT	0	0	**1**	**1**	**1**	**0**	**0**	**1**	**TT**	
(Double byte command)	0	0	Testing parameter							

This command is used for UltraChip production testing. Please do *NOT* use.

21. Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

Bias ratio definition:

00b= 6 01b= 7 10b= 8 **11b= 9**

22. Set COM End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set CEN [6:0]	0	0	1	1	1	1	0	0	0	1
(Double-byte command)	0	0	-	*CEN* register parameter						

This command programs the ending COM electrode. CEN defines the number of used COM electrodes, and it should correspond to the number of pixel-rows in the LCD. When the LCD has less than 64 pixel rows, the LCM designer should set CEN to n-1 (where n is the number of pixel rows) and use COM1 through COMn as COM driver electrodes.

23. Set Partial Display Start

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DST [6:0]	0	0	1	1	1	1	0	0	1	0
(Double-byte command)	0	0	-	*DST* register parameter						

This command programs the starting COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

24. Set Partial Display End

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set DEN [6:0]	0	0	1	1	1	1	0	0	1	1
(Double-byte command)	0	0	-	*DEN* register parameter						

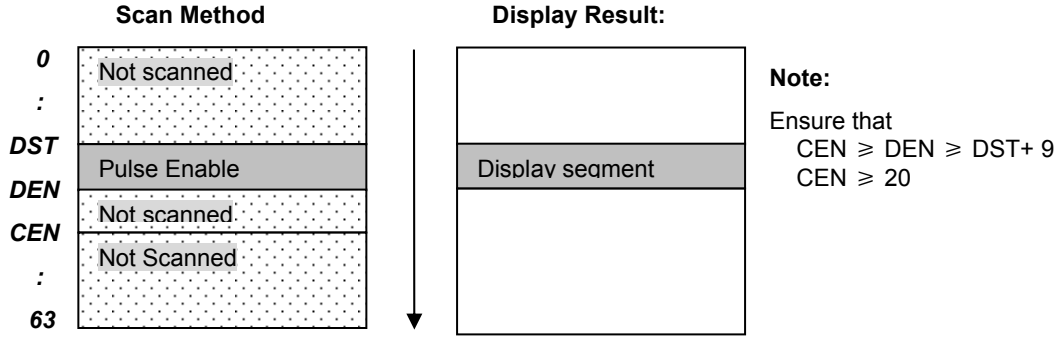
This command programs the ending COM electrode, which has been assigned a full scanning period and will output an active COM scanning pulse.

CEN, DST, and DEN are 0-based index of COM electrodes. They control only the COM electrode activity, and do not affect the mapping of display RAM to each COM electrodes. The image displayed by each pixel row is therefore not affected by the setting of these three registers.

When LC[4]=1b, the Mux-Rate is narrowed down to DEN – DST + 1. When MUX rate is reduced, reduce the frame rate accordingly to reduce power. Changing MUX rate also require BR and V_{LCD} to be reduced.

For minimum power consumption, set LC[4]=1b, set (DST, DEN, CEN) to minimize Mux rate, use slowest frame rate which satisfies the flicker requirement, set PC[0]=0b, and use lowest BR, lowest V_{LCD} which satisfies the contrast requirement. When Mux-Rate is under 16, it is recommended to set BR=6 for optimum power saving.

In either case, DST/DEN defines a small subsection of the display which will remain active while shutting down all the rest of the display to conserve energy.



Note:

Ensure that
CEN ⩾ DEN ⩾ DST+ 9
CEN ⩾ 20

If duty between 9 and 20 is used,
ensure that Partial Display is enabled (Duty = DEN – DST +1) and CEN ⩾ 20 is set.

Serial Read Command (Enable only in S8/S9 mode):

25. Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**
	0	1	ID	MX	MY	WA	DE	**0**	**0**	**0**
	0	1	Prod [3:0]				Ver	**0**	**0**	**0**

See command (3) for more detail.

LCD VOLTAGE SETTING

MULTIPLEX RATES

Multiplex Rate is completely software programmable in UC1601s via registers CEN, DST, DEN, and partial display control flags LC[4].

Combined with low power partial display mode and a low bias ratio of 6, UC1601s can support wide variety of display control options. For example, when a system goes into stand-by mode, a large portion of LCD screen can be turned off to conserve power.

BIAS RATIO SELECTION

Bias Ratio (*BR*) is defined as the ratio between V_{LCD} and V_{BIAS}, i.e.

$$BR = V_{LCD}/V_{BIAS},$$

where $V_{BIAS} = V_{B1+} - V_{B1-} = V_{B0+} - V_{B0-}$.

The theoretical optimum *Bias Ratio* can be estimated by $\sqrt{Mux}+1$. *BR* of value 15~20% lower/higher than the optimum value calculated above will not cause significant visible change in image quality.

UC1601s supports four *BR* as listed below. BR can be selected by software program.

BR	0	1	2	3
Bias Ratio	6	7	8	9

Table 1: Bias Ratios

TEMPERATURE COMPENSATION

Four different temperature compensation coefficients can be selected via software. The four coefficients are given below:

TC	0	1	2	3
% per ^{o}C	–0.05	–0.10	–0.15	–0.00

Table 2: Temperature Compensation

V_{LCD} GENERATION

V_{LCD} may be supplied either by internal charge pump or by external power supply. The source of V_{LCD} is controlled by PC[2:1].

When V_{LCD} is generated internally, the voltage level of V_{LCD} is determined by three control registers: *BR* (Bias Ratio), *PM* (Potentiometer), and *TC* (Temperature Compensation), with the following relationship:

$$V_{LCD} = (C_{V0} + C_{PM} \times PM) \times (1 + (T - 25) \times C_T\%)$$

where

C_{V0} and C_{PM} are two constants, whose value depends on the setting of BR register, as illustrated in the table on the next page,

PM is the numerical value of PM register,

T is the ambient temperature in ^{O}C, and

C_T is the temperature compensation coefficient as selected by TC register.

V_{LCD} FINE TUNING

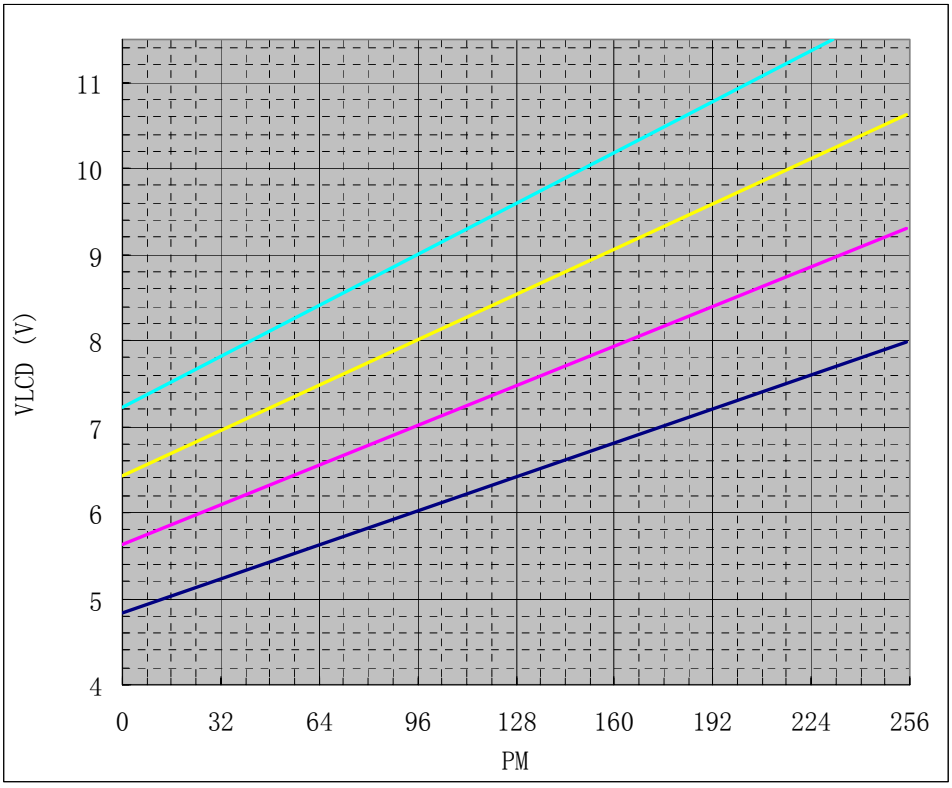
Black-and-white STN LCD is sensitive to even a 1% mismatch between IC driving voltage and the V_{OP} of LCD. However, it is difficult for LCD makers to guarantee such high precision matching of parts from different venders. It is therefore necessary to adjust V_{LCD} to match the actual V_{OP} of the LCD.

For the best result, software based approach for V_{LCD} adjustment is the recommended method for V_{LCD} fine-tuning. System designers should always consider the contrast fine tuning requirement before finalizing on the LEM design

LOAD DRIVING STRENGTH

The power supply circuit of UC1601s is designed to handle LCD panels with loading up to ~24nF using 20-Ω/Sq ITO glass with $V_{DD2/3} \geq 2.4V$. For larger LCD panels, use lower resistance ITO glass packaging.

V_{LCD} QUICK REFERENCE



V_{LCD} Programming Curve.

BR	C_{V0} (V)	C_{PM} (mV)	PM	V_{LCD} Range (V)
6	4.838	12.36	0	4.84
			255	7.99
7	5.636	14.40	0	5.64
			255	9.31
8	6.433	16.45	0	6.43
			255	10.63
9	7.228	18.49	0	7.23
			231	11.50

Note:

1. For good product reliability, keep V_{LCD} under **11.5V** over all temperature.
2. The integer values of BR above are for reference only and may have slight shift.

HI-V GENERATOR AND BIAS REFERENCE CIRCUIT

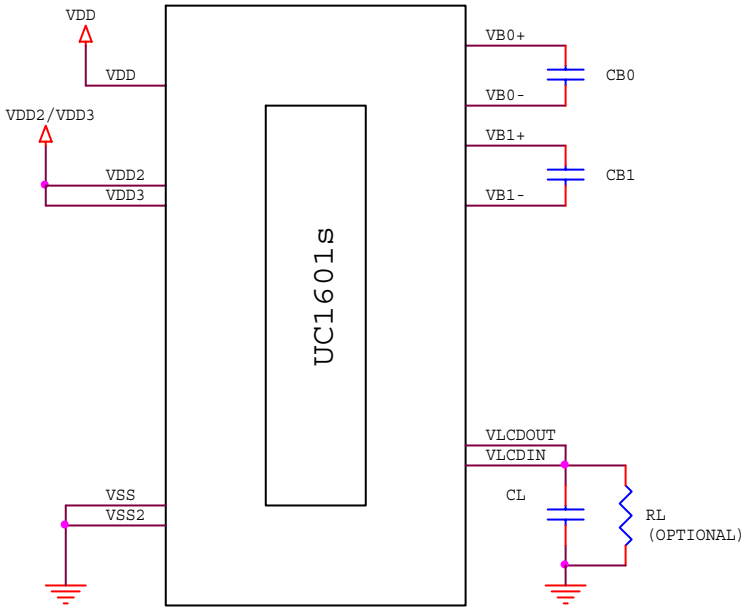


FIGURE 1: Reference circuit using internal Hi-V generator circuit

Note

Sample component values: (The illustrated circuit and component values are for reference only. Please optimize for specific requirements of each application.)

C_{Bx} : 2.2 µF/5V or 300x LCD load capacitance, whichever is higher.

C_L : 330nF(25V) is appropriate for most applications.

R_L: 3.3M~10M Ω to act as a draining circuit when V_{DD} is shut down abruptly.

LCD DISPLAY CONTROLS

CLOCK & TIMING GENERATOR

UC1601s contains a built-in system clock. All required components for the clock oscillator are built-in. No external parts are required.

Two different frame rates are provided for system design flexibility. The frame rate is controlled by register LC[3]. When Mux-Rate is above 34, Frame rate: 80 fps and 100 fps.

When Mux-Rate is lowered to 33, and 16, frame rate will be scaled down automatically by 2 and 4 times to reduce power consumption.

Choose lower frame rate for lower power, and choose higher frame rate to improve LCD contrast and minimize flicker.

DRIVER MODES

COM and SEG drivers can be in either Idle mode or Active mode, controlled by Display Enable flag (DC[2]). When SEG and COM drivers are in idle mode, they will be connected together to ensure zero DC condition on the LCD.

DRIVER ARRANGEMENTS

The naming conventions are: COM*x,* where x = 1~64, refers to the row driver for the x-th row of pixels on the LCD panel.

The mapping of COM(x) to LCD pixel rows is fixed and it is not affected by SL, CEN, DST, DEN, MX or MY settings.

DISPLAY CONTROLS

There are three groups of display control flags in the control register DC: Driver Enable (DE), All-Pixel-ON (APO) and Inverse (PXV). DE has the overriding effect over PXV and APO.

DRIVER ENABLE (DE)

Driver Enable is controlled by the value of DC[2] via *Set Display Enable* command. When DC[2] is set to OFF (logic "0"), both COM and SEG drivers will become idle and UC1601s will put itself into Sleep Mode to conserve power.

When DC[2] is set to ON, the DE flag will become "1",and UC1601s will first exit from Sleep Mode, restore the power (V_{LCD}, V_D etc.) and then turn on COM and SEG drivers.

ALL PIXELS ON (APO)

When set, this flag will force all SEG drivers to output ON signals, disregarding the data stored in the display buffer.

This flag has no effect when Display Enable is OFF and it has no effect on data stored in RAM.

INVERSE (PXV)

When this flag set to ON, SEG drivers will output the inverse of the value it received from the display buffer RAM (bit-wise inversion). This flag has no impact on data stored in RAM.

PARTIAL DISPLAY

UC1601s provides flexible control of Mux Rate and active display area. Please refer to commands `Set COM End`, `Set Partial Display Start`, and `Set Partial Display End` for more detail.

ITO LAYOUT AND LC SELECTION

Since COM scanning pulses of UC1601s can be as short as 153µS, it is critical to control the RC delay of COM and SEG signal to minimize crosstalk and maintain good mass production consistency.

COM TRACES

Excessive COM scanning pulse RC decay can cause fluctuation of contrast and increase COM direction crosstalk.

Please limit the worst case of COM signals RC delay (RC_{MAX}) as calculated below

$$(R_{ROW} / 2.7 + R_{COM}) \times C_{ROW} < 9.23\mu S$$

where

C_{ROW}: LCD loading capacitance of one row of pixels. It can be calculated by C_{LCD}/Mux-Rate, where C_{LCD} is the LCD panel capacitance.

R_{ROW}: ITO resistance over one row of pixels within the active area

R_{COM}: COM routing resistance from IC to the active area + COM driver output impedance.

In addition, please limit the min-max spread of RC decay to be:

$$| RC_{MAX} - RC_{MIN} | < 2.76\mu S$$

so that the COM distortions on the top of the screen to the bottom of the screen are uniform.

(Use worst case values for all calculations)

SEG TRACES

Excessive SEG signal RC decay can cause image dependent changes of medium gray shades and sharply increase the crosstalk of SEG direction.

For good image quality, please minimize SEG ITO trace resistance and limit the worst case of SEG signal RC delay as calculated below.

$$(R_{COL} / 2.7 + R_{SEG}) \times C_{COL} < 6.30\mu S$$

where

C_{COL}: LCD loading capacitance of one pixel column. It can be calculated by C_{LCD} / (# of column), where C_{LCD} is the LCD panel capacitance.

R_{COL}: ITO resistance over one column of pixels within the active area

R_{SEG}: SEG routing resistance from IC to the active area + SEG driver output impedance.

(Use worst case values for all calculations)

SELECTING LIQUID CRYSTAL

The selection of LC material is crucial to achieve the optimum image quality of finished LCM.

When $(V_{90}-V_{10})/V_{10}$ is too large, image contrast will deteriorate, and images will look murky and dull.

When $(V_{90}-V_{10})/V_{10}$ is too small, image contrast will become too strong, and crosstalk will increase.

For the best result, it is recommended the LC material has the following characteristics:

$$(V_{90}-V_{10})/V_{10} = (V_{ON}-V_{OFF})/V_{OFF} \times 0.72\sim0.80$$

where V_{90} and V_{10} are the LC characteristics, and V_{ON} and V_{OFF} are the ON and OFF V_{RMS} voltage produced by LCD driver IC at the specific Mux-rate.

Two examples are provided below:

Duty	Bias	V_{ON}/V_{OFF} -1	x0.80	x0.72
1/65	1/9	10.6%	9.6%	7.5%
1/65	1/8	10.5%	9.5%	7.4%

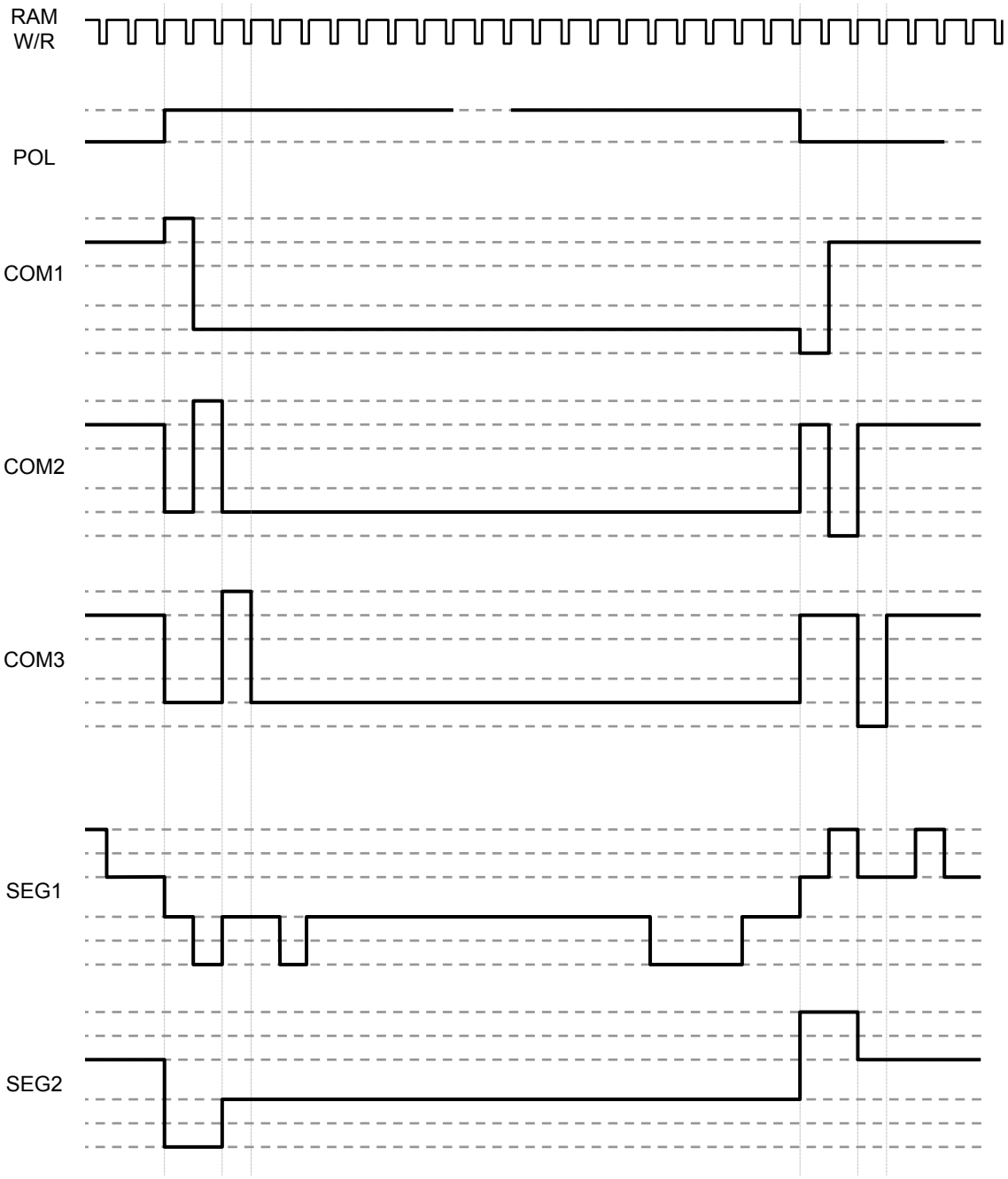


FIGURE 2: COM and SEG Electrode Driving Waveform

HOST INTERFACE

As summarized in the table below, UC1601s supports two (2) 8-bit parallel bus protocols and three (3) serial bus protocols. Designers can choose either the 8-bit parallel bus to achieve high data transfer rate, or use the serial bus to create compact LCD modules and minimize connector pins.

Bus Type		8080	6800	S8(4wr)	S9(3wr)	I^2C(2wr)
Width		8-bit	8-bit	Serial		
Access		Read / Write		Read (status) / Write		R / W
Control & Data Pins	BM[1:0]	10	11	00	01	01
	{DB[7], DB[6]}	Data	Data	10	10	11
	CS[1:0]	Chip Select				A[3:2]
	CD	Control/Data			0	
	WR0	$\overline{WR}$	R/$\overline{W}$	0		
	WR1	$\overline{RD}$	EN	0		
	DB[1,2,4,5,6,7]	Data		-		
	DB[0:3]	Data		DB[0]=SCK, DB[3]=SDA		

* Connect unused control pins and data bus pins to V_{DD} or V_{SS}

	CS Disable Bus Interface	CS Init. Bus State	RESET Init. Bus State
8-bit	✓	–	✓
S8 or S9	✓	✓	✓
I^2C	–	–	✓

- CS disable bus interface – CS can be used to disable Bus Interface Write / Read Access.
- RESET can be pin reset / soft reset / power on reset.

Table 3: Host interfaces Summary

PARALLEL INTERFACE

The timing relationship between UC1601s internal control signal RD, WR and their associated bus actions are shown in the figure below.

The Display RAM read interface is implemented as a two-stage pipeline. This architecture requires that, every time memory address is modified, either in parallel mode or serial mode, by either `Set CA` or `Set PA` command, a dummy read cycle need to be performed before the actual data can propagate through the pipeline and be read from data port D[7:0].

There is no pipeline in write interface of Display RAM. Data are transferred directly from bus buffer to internal RAM on the rising edges of write pulses.

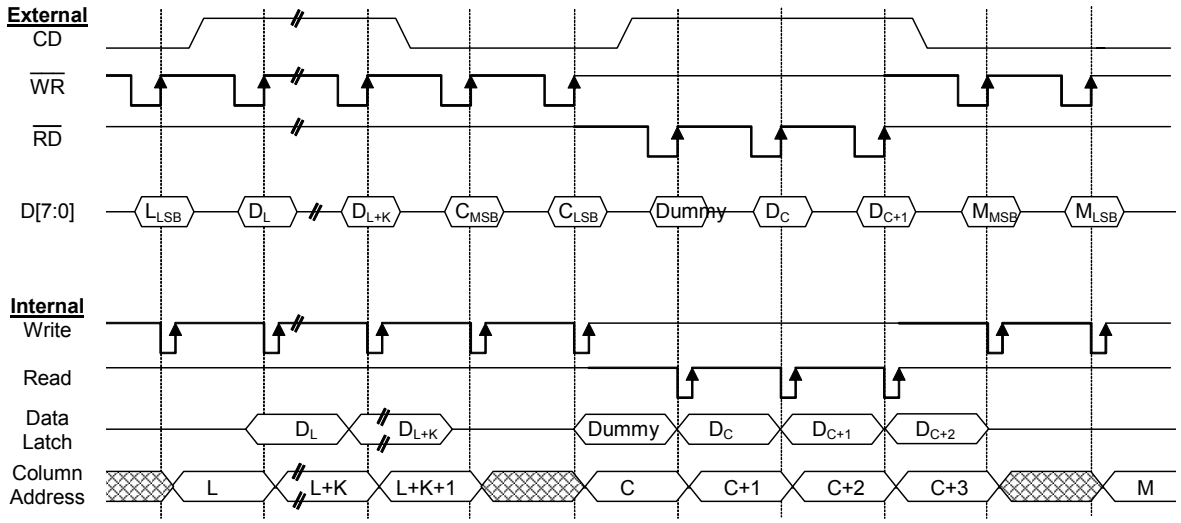


Figure 3: Parallel Interface & Related Internal Signals

SERIAL INTERFACE

UC1601s supports three (3) serial modes, one 4-wire SPI mode (S8), one 3-wire SPI mode (S9) and one 2-wire SPI mode (I^2C). Bus interface mode is determined by the wiring of the BM[1:0] and DB[7:6]. See table in last page for more detail.

S8 (4-WIRE) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. Pin CD is used to determine the content of the data been transferred. During each write cycle, 8 bits of data, MSB first, are latched on eight rising SCK edges into an 8-bit data holder.

If CD=0, the data byte will be decoded as command. If CD=1, these 8 bits will be treated as data and transferred to proper address in the Display Data RAM on the rising edge of the last SCK pulse. Pin CD is examined when SCK is pulled low for the LSB (D0) of each token.

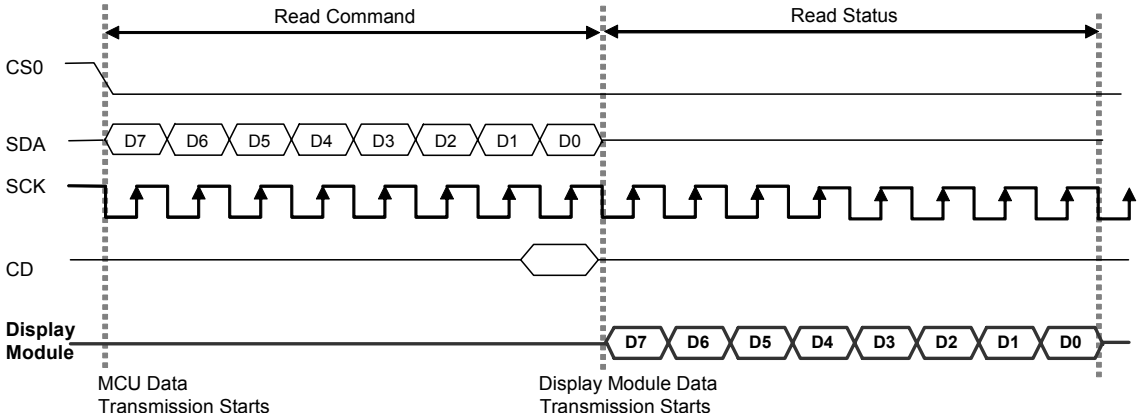


FIGURE 4.a: 4-wire Serial Interface (S8) – Read

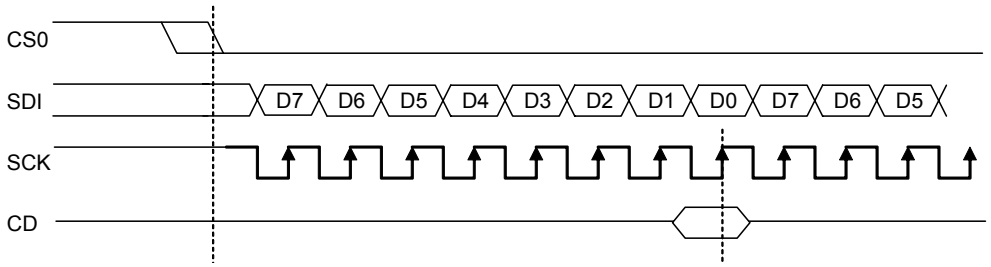


Figure 4.b: 4-wire Serial Interface (S8) – Write

S9 (3-WIER) INTERFACE

Pins CS[1:0] are used for chip select and bus cycle reset. On each write cycle, the first bit is CD, which determines the content of the following 8 bits of data, MSB first. These 8 command or data bits are latched on rising SCK edges into an 8-bit data holder. If CD=0, the data byte will be decoded as command. If CD=1, this 8-bit will be treated as data and transferred to proper address in the Display Data RAM at the rising edge of the last SCK pulse.

By sending CD information explicitly in the bit stream, control pin CD is not used, and should be connected to either V_{DD} or V_{SS}. The toggle of CS0 (or CS1) for each byte of data/command is recommended but optional.

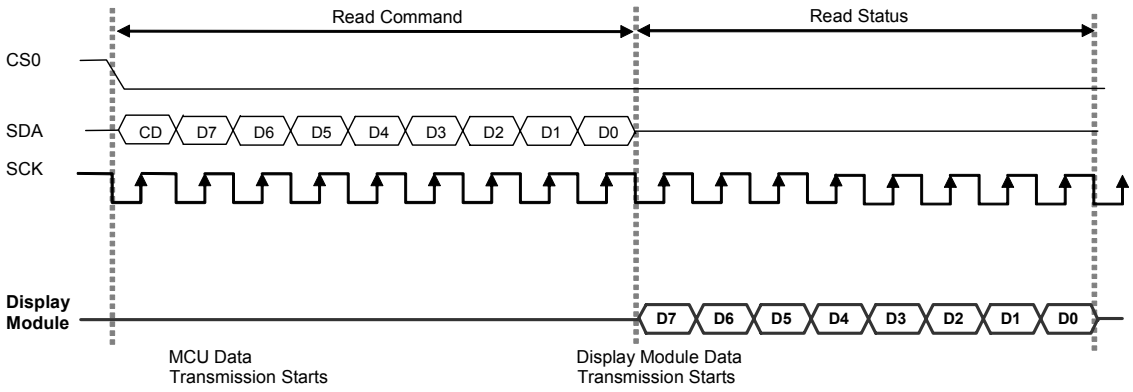


Figure 5.a: 3-wire Serial Interface (S9) – Read

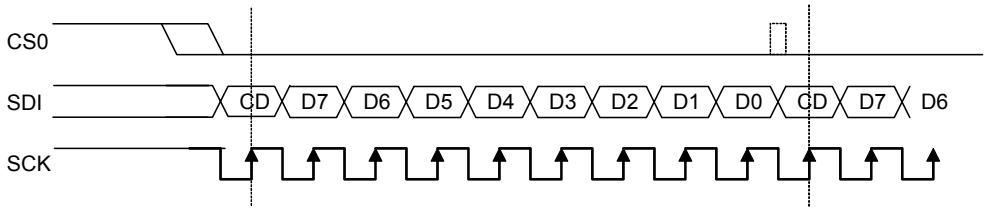
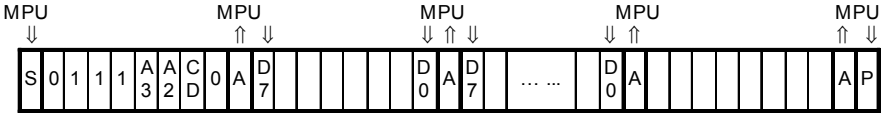


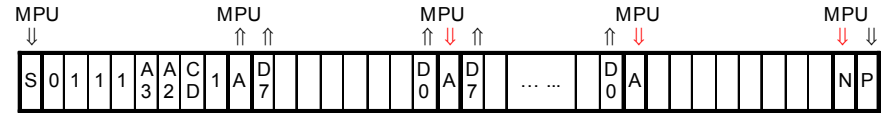
Figure 5.b: 3-wire Serial Interface (S9) – Write

I²C (2-WIRE) INTERFACE

Write Mode



Read Mode



When BM[1:0] is set to "LH" and D[7:6] is set to "HH", UC1601s is configured as an I²C bus signaling protocol compliant slave device. Please refer to I²C standard for details of the bus signaling protocol, and AC Characteristic section for timing parameters of UltraChip implementation.

In this mode, pins CS[1:0] become A[3:2] and is used to configure UC1601s' device address. Proper wiring to V_{DD} or V_{SS} is required for the IC to operate properly for I²C mode.

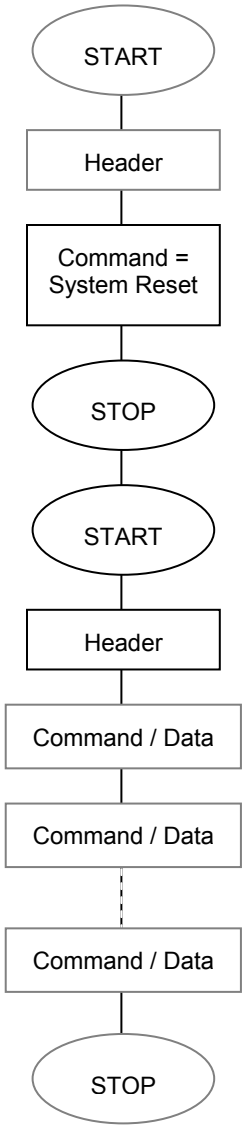
Each UC1601s I²C interface sequence starts with a "S" (Start) from the bus master, followed by a sequence header, containing a device address, the mode of transfer (CD, 0:Control, 1:Data), and the direction of the transfer (RW, 0:Write, 1:Read).

Since both WR and CD are expressed explicitly in the header byte, the control pins WR[1:0] and CD are not used in I²C mode and should be connected to V_{SS}. The direction (read or write) and content type (command or data) of the data bytes following each header byte are fixed for the sequence. To change the direction (R⇔W) or the content type (C⇔D), start a new sequence with a START (S) flag, followed by a new header.

After receiving the header, the UC1601s will send out a "A" (Acknowledge signal). Then, depends on the setting of the header, the transmitting device (either the bus master or UC1601s) will start placing data bits on SDA, MSB to LSB, and the sequence will repeat until a STOP signal (P, in WRITE mode), or an N (Not Acknowledged, in READ mode) is sent by the bus master.

When using I²C serial mode, if command `System Reset` is to be written, the writing sequence must be finished (STOP) before succeeding data or commands start. The flow chart on the right shows a writing sequence with a "System Reset" command.

Note that, for data read (CD=1), the first byte of data transmitted will be dummy.



HOST INTERFACE REFERENCE CIRCUIT

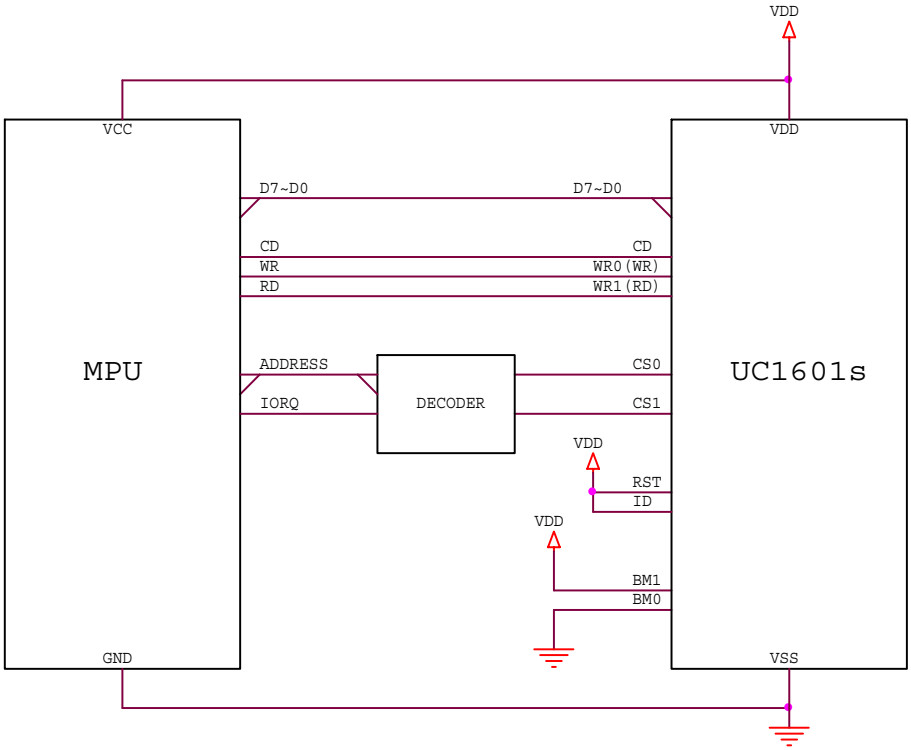


FIGURE 6: 8080/8bit parallel mode reference circuit

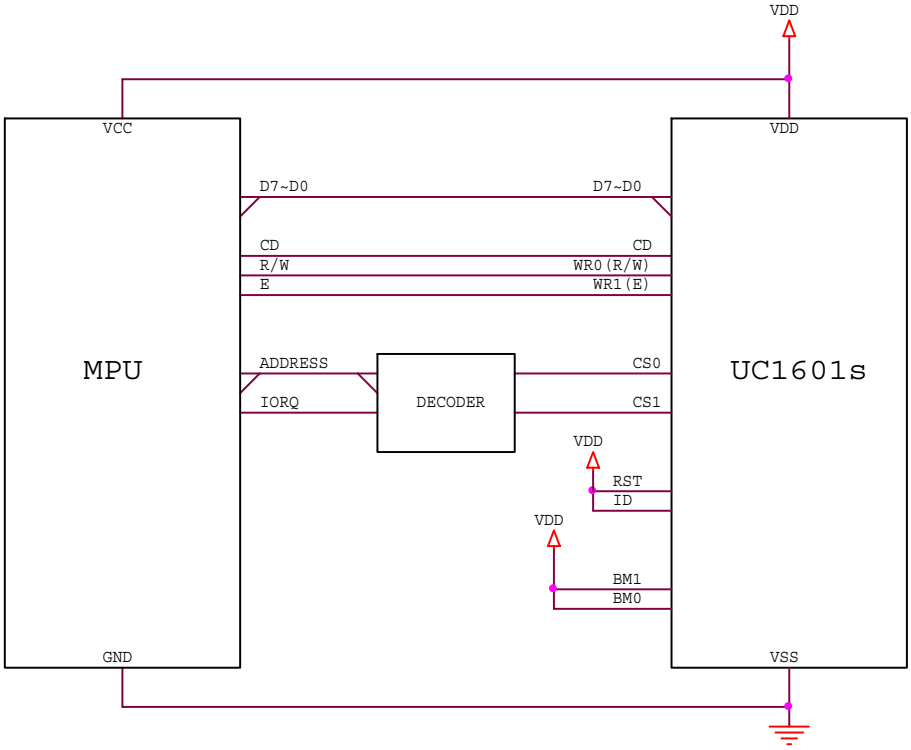


FIGURE 7: 6800/8bit parallel mode reference circuit

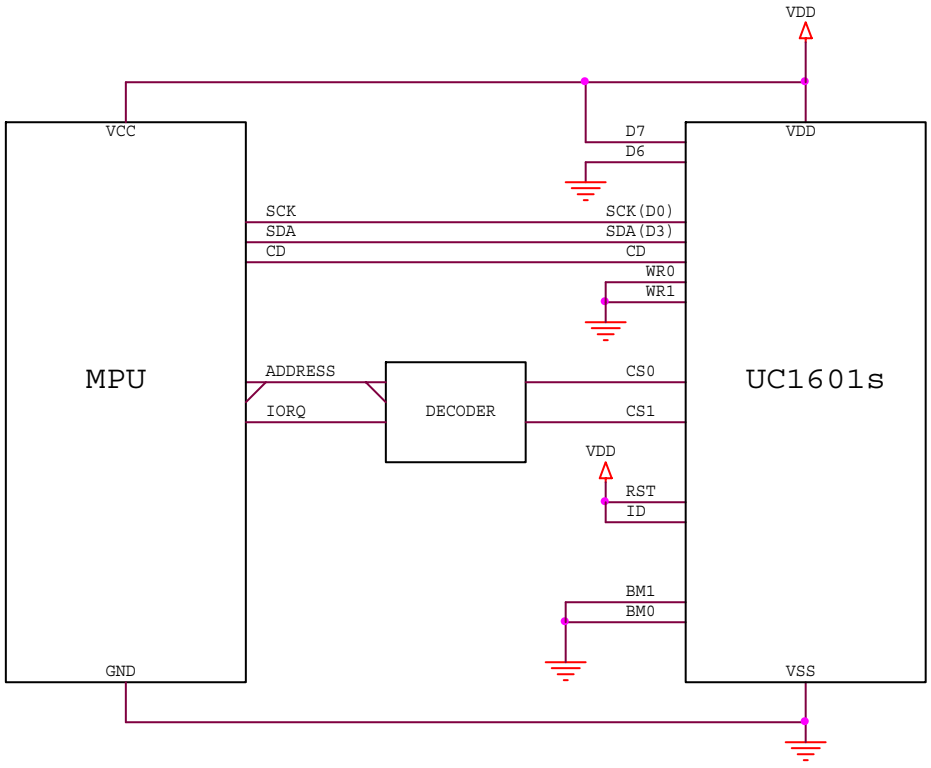


FIGURE 8: Serial-8 serial mode reference circuit

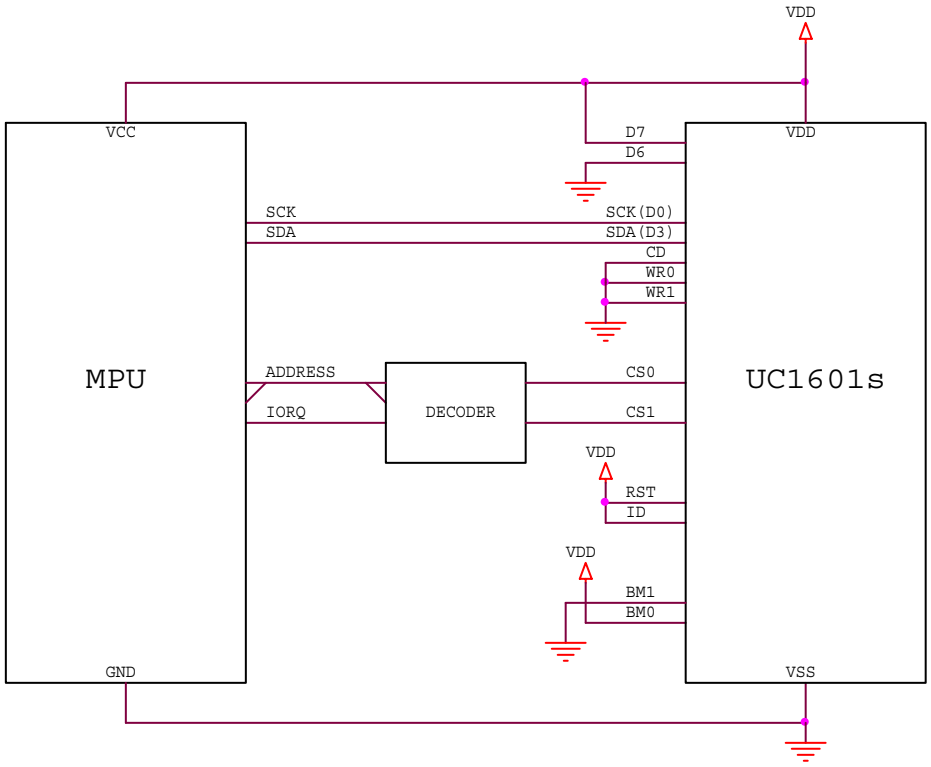


FIGURE 9: Serial-9 serial mode reference circuit

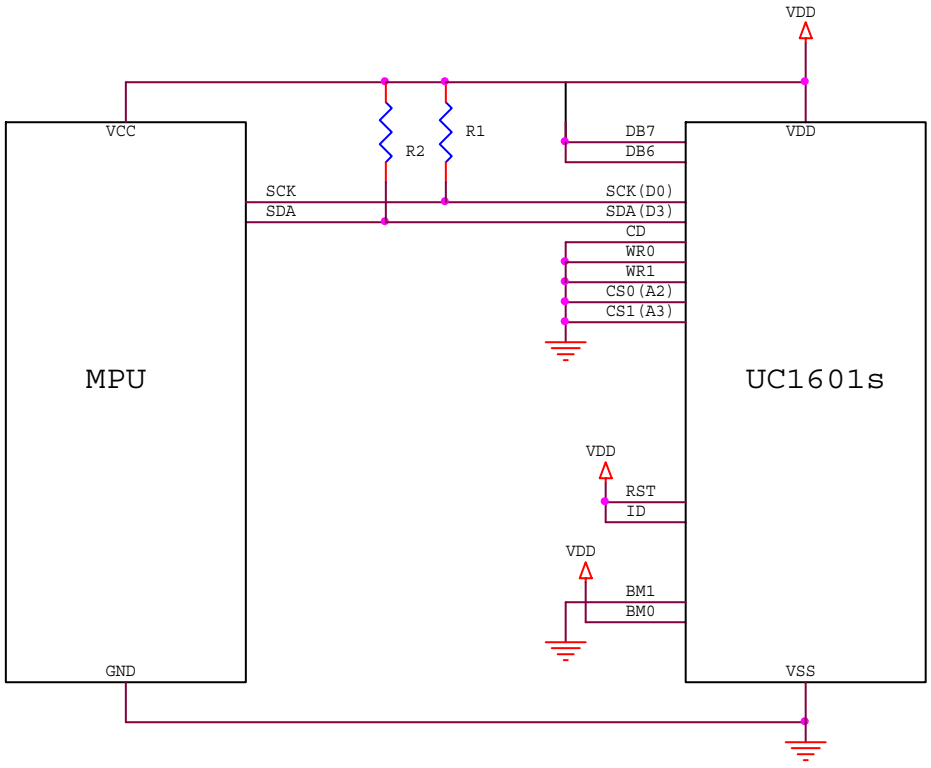


FIGURE 10: I^2C serial mode reference circuit

Note

- The ID pins are for production control. The connection will affect the content of D[7] of the 1st byte of the `Get Status` command. Connect to V_{DD} for "H" or V_{SS} for "L".
- RST pin is optional. When the RST pin is not used, connect it to V_{DD}.
- When using I^2C serial mode, CS1/0 are user configurable and affect A[3:2] of device address.
- R1, R2: 2k ~ 10k Ω, use lower resistor for bus speed up to 3.6MHz, use higher resistor for lower power.

DISPLAY DATA RAM (DDRAM)

DATA ORGANIZATION

The input display data are stored to a dual port static DDRAM (DDRAM, for Display Data RAM) organized as 65x132.

After setting CA and RA, the subsequent data write cycle will store the data for the specified pixel to the proper memory location.

Please refer to the map in the following page between the relation of COM, SEG, SRAM, and various memory control registers.

DISPLAY DATA RAM ACCESS

The Display RAM is a special purpose dual port RAM which allows asynchronous access to both its column and row data. Thus, RAM can be independently accessed both for Host Interface and for display operations.

DISPLAY DATA RAM ADDRESSING

A Host Interface (HI) memory access operation starts with specifying Row Address (RA) and Column Address (CA) by issuing *Set Row Address* and *Set Column Address* commands.

If wrap-around (WA, AC[0]) is OFF (0), CA will stop increasing after reaching the end of row (131), and system programmers need to set the values of PA and CA explicitly.

If WA is ON (1), when CA reaches end of page, CA will be reset to 0 and PA will increase or decrease, depending on the setting of row Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 7), PA will be wrapped around to the other end of RAM and continue.

MX IMPLEMENTATION

Column Mirroring (MX) is implemented by selecting either (CA) or (131–CA) as the RAM column address. Changing MX affects the data written to the RAM.

Since MX has no effect of the data already stored in RAM, changing MX does not have immediate effect on the displayed pattern. To refresh the display, refresh the data stored in RAM after setting MX.

ROW MAPPING

COM electrode scanning orders are not affected by Start Line (SL), Fixed Line (FLT & FLB) or Mirror Y (MY, LC[3]). Visually, register SL having a non-zero value is equivalent to scrolling the LCD display up or down (depends on MY) by *SL* rows.

RAM ADDRESS GENERATION

The mapping of the data stored in the display SRAM and the scanning electrodes can be obtained by combining the fixed R*m* scanning sequence and the following RAM address generation formula.

During the display operation, the RAM line address generation can be mathematically represented as following:

For the 1st line period of each field
Line = *SL*
Otherwise
Line = Mod(*Line*+1, 64)

Where Mod is the modular operator, and *Line* is the bit slice line address of RAM to be outputted to column drivers. Line 0 corresponds to the first bit-slice of data in RAM.

The above *Line* generation formula produce the “loop around” effect as it effectively resets *Line* to 0 when *Line+1* reaches *64*.

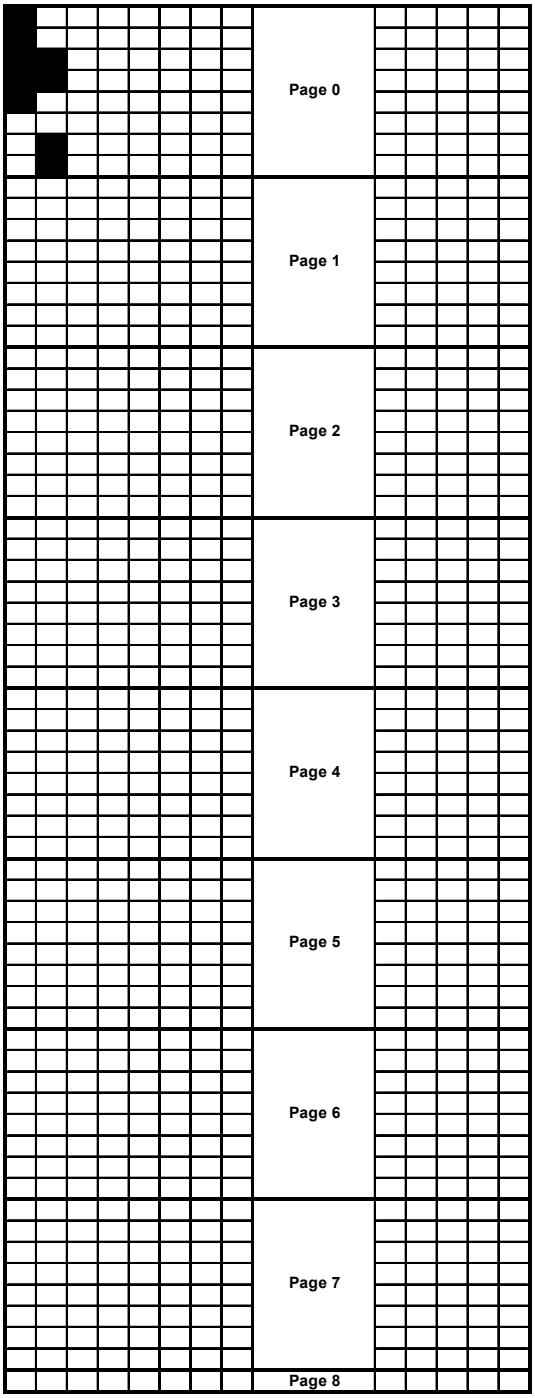
MY IMPLEMENTATION

Row Mirroring (MY) is implemented by reversing the mapping order between row electrodes and RAM, i.e. the mathematical address generation formula becomes:

For the 1st line period of each field
Line = Mod(*SL* + *MR -1*, *64*)
Otherwise
Line = Mod(*Line-1* , *64*)

Visually, the effect of MY is equivalent to flipping the display upside down. The data stored in display RAM is not affected by MY.

PA[3:0]	0	Line AddeCss
0000	D0	00H
	D1	01H
	D2	02H
	D3	03H
	D4	04H
	D5	05H
	D6	06H
	D7	07H
0001	D0	08H
	D1	09H
	D2	0AH
	D3	0BH
	D4	0CH
	D5	0DH
	D6	0EH
	D7	0FH
0010	D0	10H
	D1	11H
	D2	12H
	D3	13H
	D4	14H
	D5	15H
	D6	16H
	D7	17H
0011	D0	18H
	D1	19H
	D2	1AH
	D3	1BH
	D4	1CH
	D5	1DH
	D6	1EH
	D7	1FH
0100	D0	20H
	D1	21H
	D2	22H
	D3	23H
	D4	24H
	D5	25H
	D6	26H
	D7	27H
0101	D0	28H
	D1	29H
	D2	2AH
	D3	2BH
	D4	2CH
	D5	2DH
	D6	2EH
	D7	2FH
0110	D0	30H
	D1	31H
	D2	32H
	D3	33H
	D4	34H
	D5	35H
	D6	36H
	D7	37H
0111	D0	38H
	D1	39H
	D2	3AH
	D3	3BH
	D4	3CH
	D5	3DH
	D6	3EH
	D7	3FH
1000	D0	40H



MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=0	MY=1 SL=25	MY=1 SL=25
C1	C49	C64	C48	C25	C9
C2	C50	C63	C47	C24	C8
C3	C51	C62	C46	C23	C7
C4	C52	C61	C45	C22	C6
C5	C53	C60	C44	C21	C5
C6	C54	C59	C43	C20	C4
C7	C55	C58	C42	C19	C3
C8	C56	C57	C41	C18	C2
C9	C57	C56	C40	C17	C1
C10	C58	C55	C39	C16	---
C11	C59	C54	C38	C15	---
C12	C60	C53	C37	C14	---
C13	C61	C52	C36	C13	---
C14	C62	C51	C35	C12	---
C15	C63	C50	C34	C11	---
C16	C64	C49	C33	C10	---
C17	C1	C48	C32	C9	---
C18	C2	C47	C31	C8	---
C19	C3	C46	C30	C7	---
C20	C4	C45	C29	C6	---
C21	C5	C44	C28	C5	---
C22	C6	C43	C27	C4	---
C23	C7	C42	C26	C3	---
C24	C8	C41	C25	C2	---
C25	C9	C40	C24	C1	---
C26	C10	C39	C23	C64	C48*
C27	C11	C38	C22	C63	C47
C28	C12	C37	C21	C62	C46
C29	C13	C36	C20	C61	C45
C30	C14	C35	C19	C60	C44
C31	C15	C34	C18	C59	C43
C32	C16	C33	C17	C58	C42
C33	C17	C32	C16	C57	C41
C34	C18	C31	C15	C56	C40
C35	C19	C30	C14	C55	C39
C36	C20	C29	C13	C54	C38
C37	C21	C28	C12	C53	C37
C38	C22	C27	C11	C52	C36
C39	C23	C26	C10	C51	C35
C40	C24	C25	C9	C50	C34
C41	C25	C24	C8	C49	C33
C42	C26	C23	C7	C48	C32
C43	C27	C22	C6	C47	C31
C44	C28	C21	C5	C46	C30
C45	C29	C20	C4	C45	C29
C46	C30	C19	C3	C44	C28
C47	C31	C18	C2	C43	C27
C48	C32	C17	C1	C42	C26
C49	C33	C16	---	C41	C25
C50	C34	C15	---	C40	C24
C51	C35	C14	---	C39	C23
C52	C36	C13	---	C38	C22
C53	C37	C12	---	C37	C21
C54	C38	C11	---	C36	C20
C55	C39	C10	---	C35	C19
C56	C40	C9	---	C34	C18
C57	C41	C8	---	C33	C17
C58	C42	C7	---	C32	C16
C59	C43	C6	---	C31	C15
C60	C44	C5	---	C30	C14
C61	C45	C4	---	C29	C13
C62	C46	C3	---	C28	C12
C63	C47	C2	---	C27	C11
C64	C48	C1	---	C26	C10
CIC	CIC	CIC	CIC	CIC	CIC
		65	49	65	49

MUX

MX															
0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG128	SEG129	SEG130	SEG131	SEG132
1	SEG132	SEG131	SEG130	SEG129	SEG128	SEG127	SEG126	SEG125		SEG5	SEG4	SEG3	SEG2	SEG1

Example for memory mapping: let MX = 0, MY = 0, SL = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1 (D7-D0) : 0001 1111b
⇒ Page 0 SEG 2 (D7-D0) : 1100 1100b

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1601s has two different types of Reset:

Power-ON-Reset and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1601s enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1601s has three operating modes (OM):
Reset, Sleep, Normal.

For each mode, the related statuses are as below:

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions:

Set Display Enable, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep mode.

OM changes are synchronized with the edges of UC1601s' internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` or `System Reset` command.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1601s consumes very little energy in Sleep mode (typically under 2µA).

EXITING SLEEP MODE

UC1601s contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1601s internal voltage sources are restored to their proper values.

Power-Up Sequence

UC1601s power-up sequence is simplified by built-in "Power Ready" flags and by the automatic invocation of *System-Reset* command after *Power-ON-Reset*.

System programmer is required to wait for only 5 ~ 10 mS before starting to issue commands to UC1601s. No additional commands or waits are required between enabling of the charge pump, turning on the display drivers, writing to RAM or any other commands.

There's no delay needed while turning on V_{DD} and $V_{DD2/3}$, and either one can be turned on first.

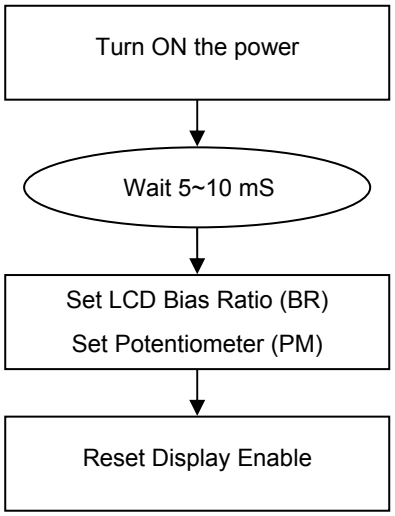


FIGURE 11: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitor C_L causing abnoraml residue horizontal line on display when V_{DD} is switched off, use Reset mode to enable the built-in charge draining circuit to discharge these external capacitors.

When internal V_{LCD} is not used, UC1601s will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

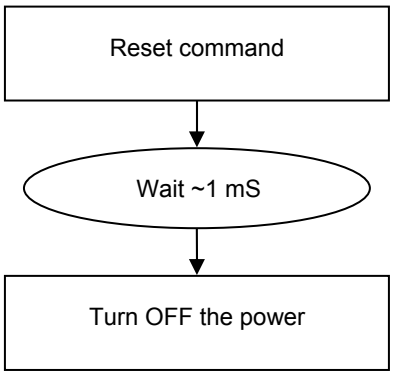


FIGURE 12: Reference Power-Down Sequence

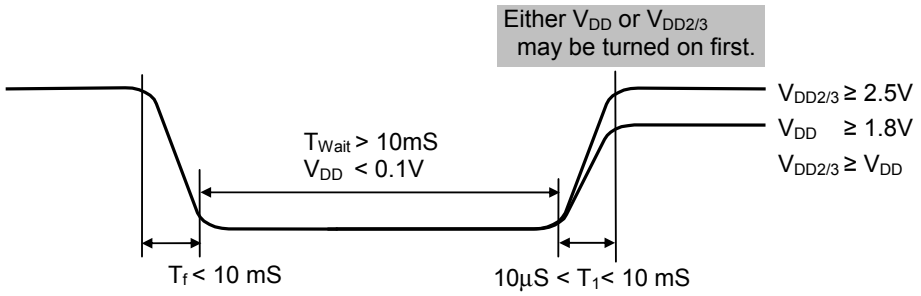


Figure 13: Power Off-On Sequence

SAMPLE COMMAND SEQUENCES FOR POWER MANAGEMENT

The following tables are examples of command sequence for power-up, power-down and display ON/OFF operations. These are only to demonstrate some "*typical, generic*" scenarios. Designers are encouraged to study related sections of the datasheet and find out what the best parameters and control sequences are for their specific design needs.

Type
Required: These items are required
Customized: These items are not necessary if customer parameters are the same as default
Advanced: We recommend new users to skip these commands and use default values.
Optional: These commands depend on what users want to do.

C/D The type of the interface cycle. It can be either Command (0) or Data (1)

W/R The direction of data flow of the cycle. It can be either Write (0) or Read (1).

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON Reset.	Wait ~5mS after V_{DD} is ON
C	0	0	0	0	1	0	0	1	#	#	Set Temp. Compensation	Set up LCD format specific parameters, MX, MY, etc.
C	0	0	1	1	0	0	0	#	#	#	Set LCD Mapping Control	
A	0	0	1	0	1	0	0	0	0	#	Set Frame Rate	Fine tune for power, flicker, contrast.
C	0	0	1	1	1	0	1	0	#	#	Set LCD Bias Ratio	LCD specific operating voltage setting
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	Set V_{BIAS} Potentiometer	
O	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

POWER-DOWN

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	1	1	0	0	0	1	0	System Reset	
R	–	–	–	–	–	–	–	–	–	–	Draining capacitor	Wait ~3mS before V_{DD} OFF

DISPLAY-OFF

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	0	0	1	0	1	0	1	1	1	0	Set Display Disable	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image (Image update is optional. Data in the RAM is retained through the SLEEP state.)
R	0	0	1	0	1	0	1	1	1	1	Set Display Enable	

ESD CONSIDERATION

UC1600 series products usually are provided in bare die format to customers. This makes the product particularly sensitive to ESD damage during handling and manufacturing process. It is, therefore, highly recommended that LCM makers strictly follow the "JESD 625-A Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices" when manufacturing LCM.

The following pins in UC1601s require special "ESD Sensitivity" consideration in particular:

Pins \ Test Mode		Machine Mode		Human Body Mode	
		V_{DD}	V_{SS}	V_{DD}	V_{SS}
LCD Driver		225V	250V	3.0KV	3.0KV
LCM Digital Interface		300V	300V	3.0KV	3.0KV
LCM HV Interface	TST1/2/4	300V	300V	3.0KV	3.0KV
	C_B pins	300V	300V	3.0KV	3.0KV
	V_{LCDIN}	300V	300V	3.0KV	3.0KV
	V_{LCDOUT}	300V	300V	3.0KV	3.0KV
PWR/GND		--	300V	--	3.0KV

According to UltraChip's Mass Production experiences, the ESD tolerance conditions are believed to be very stable and can produce high yield in multiple customer sites. However, special care is still required during handling and manufacturing process to avoid unnecessary yield loss due to ESD damages.

ABSOLUTE MAXIMUM RATINGS

In accordance with IEC134 - notes 1, 2 and 3.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Logic Supply voltage	-0.3	+4.0	V
V_{DD2}	LCD Generator Supply voltage	-0.3	+4.0	V
V_{DD3}	Analog Circuit Supply voltage	-0.3	+4.0	V
$V_{DD2/3}$-V_{DD}	Voltage difference between V_{DD} and $V_{DD2/3}$	--	1.2	V
V_{LCD}	LCD Generated voltage	-0.3	+13.2	V
V_{IN} / V_{OUT}	Any input/output	-0.4	V_{DD} + 0.3	V
T_{OPR}	Operating temperature range	-30	+85	°C
T_{STR}	Storage temperature	-55	+125	°C

Notes

1. V_{DD} is based on V_{SS} = 0V
2. Stress values listed above may cause permanent damages to the device.

SPECIFICATIONS

DC CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply for digital circuit		1.65		3.465	V
$V_{DD2/3}$	Supply for bias & pump		2.4		3.465	V
V_{LCD}	Charge pump output	$V_{DD2/3} \geqslant$ 2.4V, 25^{O}C			11.5	V
V_D	LCD data voltage	$V_{DD2/3} \geqslant$ 2.4V, 25^{O}C	0.80		1.32	V
V_{IL}	Input logic LOW				$0.2V_{DD}$	V
V_{IH}	Input logic HIGH		$0.8V_{DD}$			V
V_{IL}	Input logic LOW	For I^{2}C only			$0.15V_{DD}$	V
V_{IH}	Input logic HIGH	For I^{2}C only	$0.85V_{DD}$			V
V_{OL}	Output logic LOW				$0.2V_{DD}$	V
V_{OH}	Output logic HIGH		$0.8V_{DD}$			V
I_{IL}	Input leakage current				1.5	µA
I_{SB}	Standby current	$V_{DD} = V_{DD2/3}$ = 3.3V, Temp = 85^{o}C			50	µA
C_{IN}	Input capacitance			5	10	PF
C_{OUT}	Output capacitance			5	10	PF
$R_{0(SEG)}$	SEG output impedance	V_{LCD} = 11V		2000	3000	Ω
$R_{0(COM)}$	COM output impedance	V_{LCD} = 11V		2000	3000	Ω
F_{FR}	Average Frame Rate	LC[3] = 0b	-10%	80	+10%	Hz

POWER CONSUMPTION

V_{DD} = 2.7V, Bias Ratio = 11b, PM =192,
V_{LCD} = 10.73 V Frame Rate = 0b, Panel Loading (PC[0]) ⩽ 0 b,
Mux Rate = 65, Bus mode = 6800, C_L =330 nF,
C_B = 2.2 µF Temperature = 25^{o}C, All outputs are open circuit.

Display Pattern	Conditions	Typ.	Max.	Unit
All-OFF	Bus = idle	223	335	µA
2-pixel checker	Bus = idle	249	373	µA
-	Bus = idle (standby current)	-	5	µA

AC CHARACTERISTICS

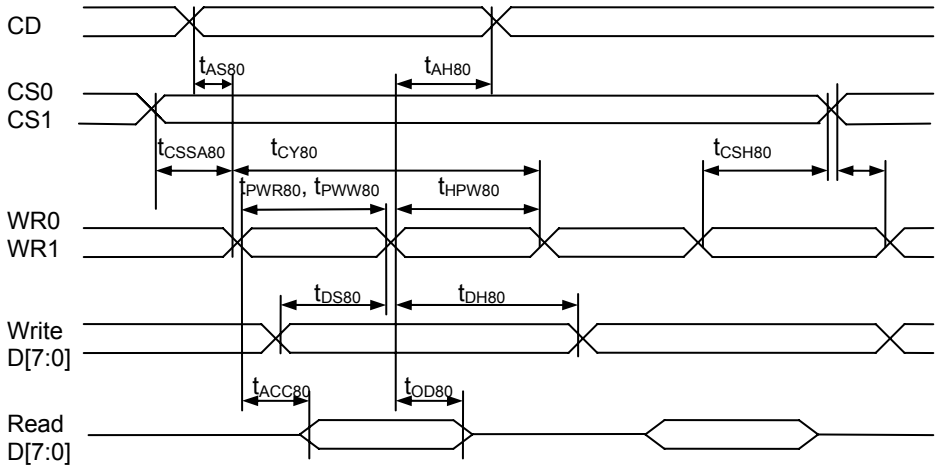


FIGURE 14: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Addresssetup time Address hold time		0 5	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip selectsetup time Chip select hold time		5 5	–	nS
t_{CY80} t_{PWR80} / t_{PWW80} t_{HPW80}	WR1 / WR0	Cycle time Pulse width High pulse width		150 / 110 60 / 40 60 / 40	–	nS
t_{DS80} t_{DH80}	D0~D7 (Write)	Data setup time Data hold time		/ 30 / 0	–	nS
t_{ACC80} t_{OD80}	D0~D7 (Read)	Read access time Output disable time	C_L = 100pF	– / 15 /	60 30	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY80} t_{PWR80} / t_{PWW80} t_{HPW80}	WR1 / WR0	Cycle time Pulse width High pulse width		270 / 190 120 / 80 120 / 80	–	nS
t_{DS80} t_{DH80}	D0~D7 (Write)	Data setup time Data hold time		/ 60 / 0	–	nS
t_{ACC80} t_{OD80}	D0~D7 (Read)	Read access time Output disable time	C_L = 100pF	– / 15 /	60 30	nS

Note: The rising time and the falling time are stipulated to be equal to or less than 15nS each.

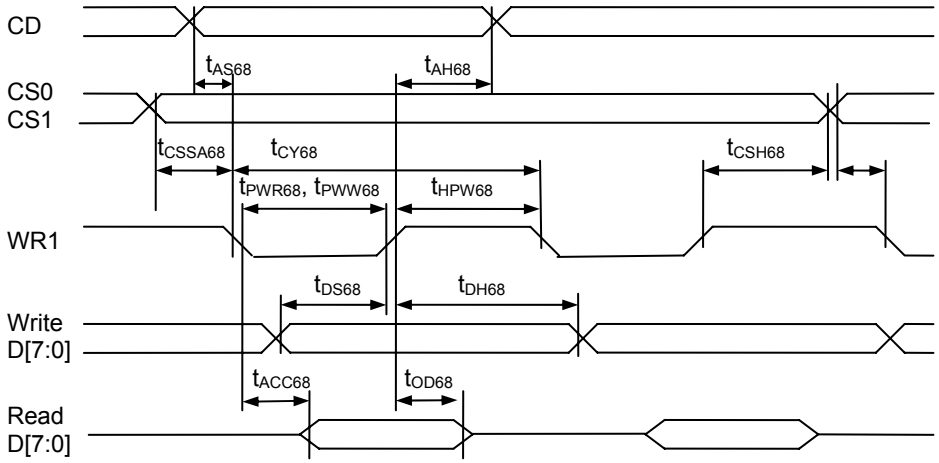


FIGURE 15: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CY68} t_{PWR68} / t_{PWW68} t_{HPW68}	WR1	Cycle time Pulse width High pulse width		150 / 110 60 / 40 60 / 40	–	nS
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Data hold time		/ 30 / 0	–	nS
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– / 15 /	60 30	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS
t_{CY68} t_{PWR68} / t_{PWW68} t_{HPW68}	WR1	Cycle time Pulse width High pulse width		270 / 190 120 / 80 120 / 80	–	nS
t_{DS68} t_{DH68}	D7~D0 (Write)	Data setup time Datahold time		/ 60 / 0	–	nS
t_{ACC68} t_{OD68}	D7~D0 (Read)	Read access time Output disable time	C_L = 100pF	– / 15 /	60 30	nS

Note: The rising time and the falling time are stipulated to be equal to or less than 15nS each.

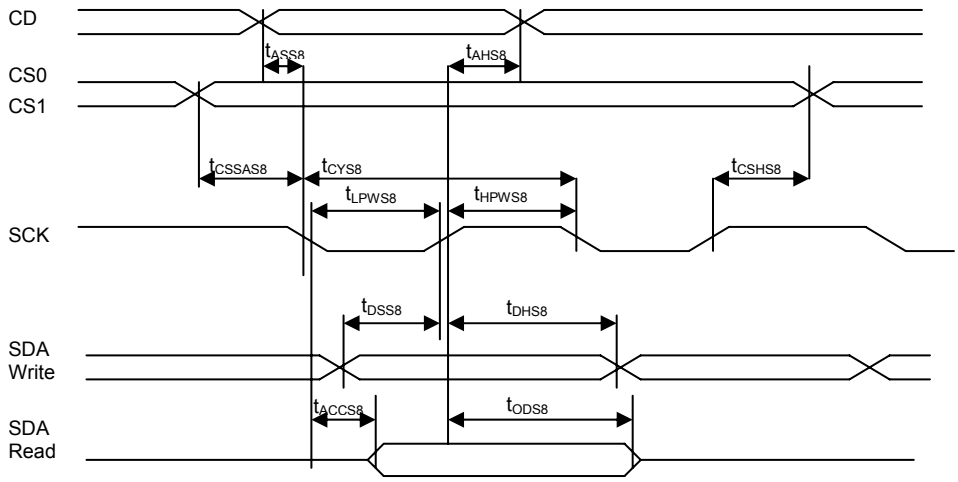


FIGURE 16: Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	Cycle time Low pulse width High pulse width		130 / 60 50 / 15 50 / 15	–	nS
t_{DSS8} t_{DHS8}	SDA (Write)	Data setup time Data hold time		/ 12 / 0	–	nS
t_{ACCS8} t_{ODS8}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / 30 /	50 –	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{ASS8} t_{AHS8}	CD	Address setup time Address hold time		0 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		10 10	–	nS
t_{CYS8} t_{LPWS8} t_{HPWS8}	SCK	Cycle time Low pulse width High pulse width		160 / 90 65 / 30 65 / 30	–	nS
t_{DSS8} t_{DHS8}	SDA (Write)	Data setup time Data hold time		/ 24 / 0	–	nS
t_{ACCS8} t_{ODS8}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / 60 /	90 –	nS

Note: The rising time and the falling time are stipulated to be equal to or less than 15nS each.

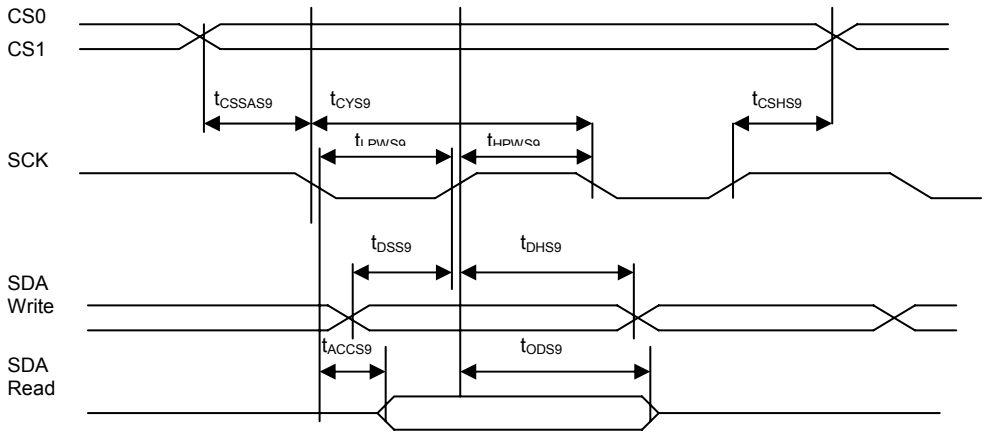


FIGURE 17: Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time Chip select hold time		5 5	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	Cycle time Low pulse width High pulse width		130 / 60 50 / 15 50 / 15	–	nS
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		/ 12 / 0	–	nS
t_{ACCS9} t_{ODS9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / 30 /	50 –	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{CSSAS9} t_{CSHS9}	CS1/CS0	Chip select setup time Chip select hold time		10 10	–	nS
t_{CYS9} t_{LPWS9} t_{HPWS9}	SCK	Cycle time Low pulse width High pulse width		160 / 90 65 / 30 65 / 30	–	nS
t_{DSS9} t_{DHS9}	SDA (Write)	Data setup time Data hold time		/ 24 / 0	–	nS
t_{ACCS9} t_{ODS9}	SDA (Read)	Read access time Output disable time	C_L = 100pF	– / 60 /	90 –	nS

Note: The rising time and the falling time are stipulated to be equal to or less than 15nS each.

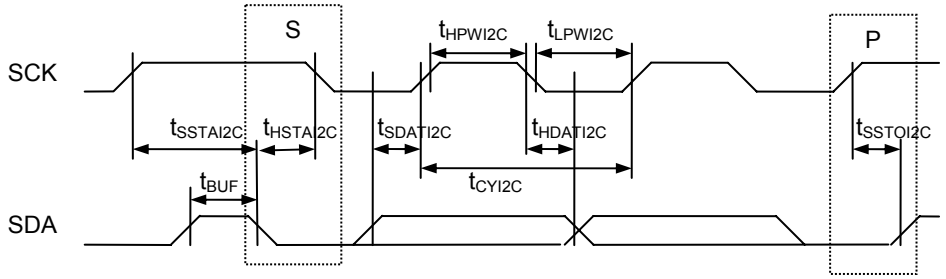


FIGURE 18: Serial bus timing characteristics (for I^2C)

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(2.5V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)				(Read / Write)		
t_{CYI2C} t_{LPWI2C} t_{HPWI2C}	SCK	SCK cycle time Low pulse width High pulse width		610 / 305 290 / 165 290 / 110	–	nS
$t_{SSDAI2C}$ t_{HDAI2C}	SCK SDA	Data setup time Data hold time		28 11	–	nS
$t_{SSTAI2C}$ $t_{HSTAI2C}$		START setup time START hold time		28 55	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
t_{BUF}		Bus free time between STOP and START condition		165	–	nS
(1.65V ≤ V_{DD} < 2.5V, Ta= –30 to +85°C)				(Read / Write)		
t_{CYI2C} t_{LPWI2C} t_{HPWI2C}	SCK	SCK cycle time Low pulse width High pulse width		780 / 360 375 / 200 375 / 130	–	nS
$t_{SSDAI2C}$ t_{HDAI2C}	SCK SDA	Data setup time Data hold time		55 11	–	nS
$t_{SSTAI2C}$ $t_{HSTAI2C}$		START setup time START hold time		28 65	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
t_{BUF}		Bus free Time between STOP and START condition		220		nS

Note: The rising time and the falling time are stipulated to be equal to or less than 15nS each.

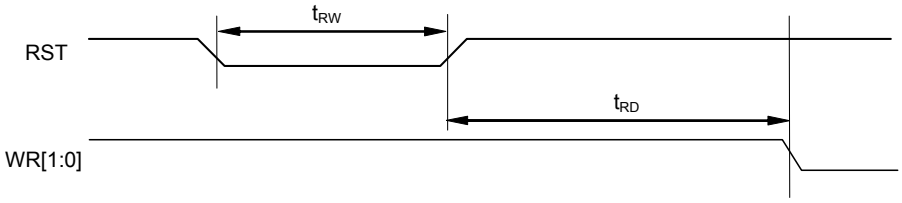


FIGURE 19: Reset Characteristics

Symbol	Signal	Description	Condition	Min.	Max.	Unit
(1.65V ⩽ V_{DD} < 3.3V, Ta= –30 to +85°C)						
t_{RW}	RST	Reset low pulse width		3	–	µS
t_{RD}	RST, WR	Reset to WR pulse delay		6	–	mS

Note:

For each mode, the signal's rising time and falling time (tf, tr) are stipulated to be equal to or less than 15nS each.

PHYSICAL DIMENSIONS

DIE SIZE:
6225 µM x 755 µM ±40 µM

DIE THICKNESS:
400 µM ± 20 µM or
300 µM ± 20 µM

$D_{MAX} - D_{MIN} \leqslant 2$ µM

BUMP HEIGHT:
15µM ±3 µM
($H_{MAX} - H_{MIN}$) within die ⩽ 2 µM

BUMP SIZE:
SEG/COM: 22.5 µM x 89 µM (Typ.)

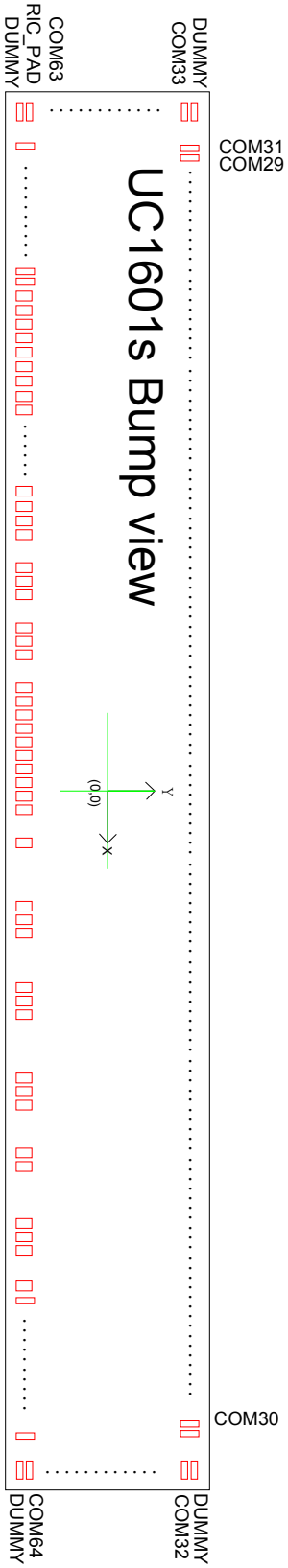
BUMP PITCH:
SEG/COM: 35.5 µM

BUMP GAP:
13 µM

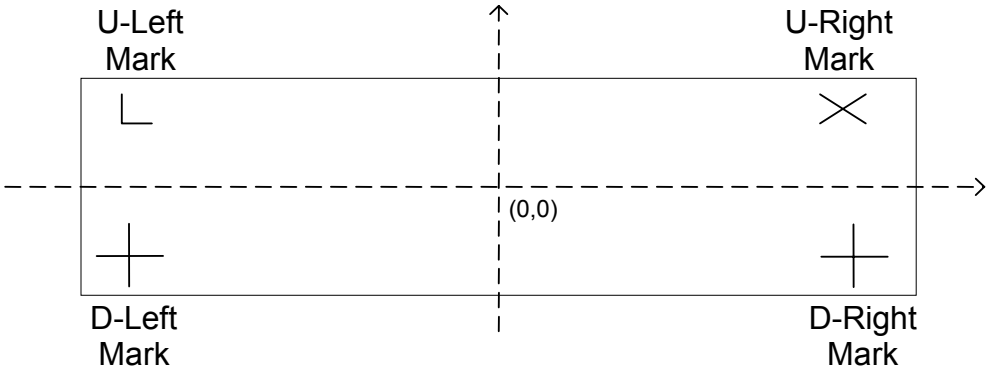
COORDINATE ORIGIN:
Chip center

PAD REFERENCE:
Pad center

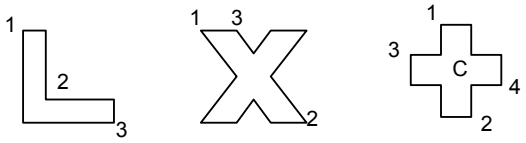
(Drawing and coordinates are for the Circuit/Bump view.)



ALIGNMENT MARK INFORMATION



SHAPE OF THE ALIGNMENT MARK:



NOTE:

Alignment mark is on Metal3 under Passivation.

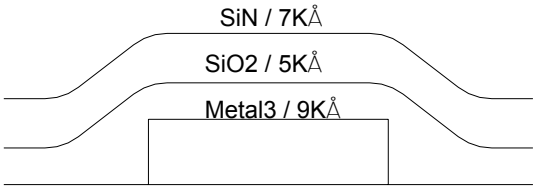
The "x" and "+" marks are symmetric both horizontally and vertically.

COORDINATES:

	U-Left Mark (L)		U-Right Mark (X)	
	X	Y	X	Y
1	-2966.6	306.75	2946.6	306.75
2	-2958.6	294.75	2966.6	286.75
3	-2946.6	286.75	2951.6	306.75

	D-Left Mark (+)		D-Right Mark (+)	
	X	Y	X	Y
1	-2935.5	-254	2820.575	-254
2	-2915.5	-329	2840.575	-329
3	-2963	-281.5	2793.075	-281.5
4	-2888	-301.5	2868.075	-301.5
C	-2925.5	-291.5	2830.575	-291.5

TOP METAL AND PASSIVATION:



FOR PROCESS CROSS-SECTION

PAD COORDINATES

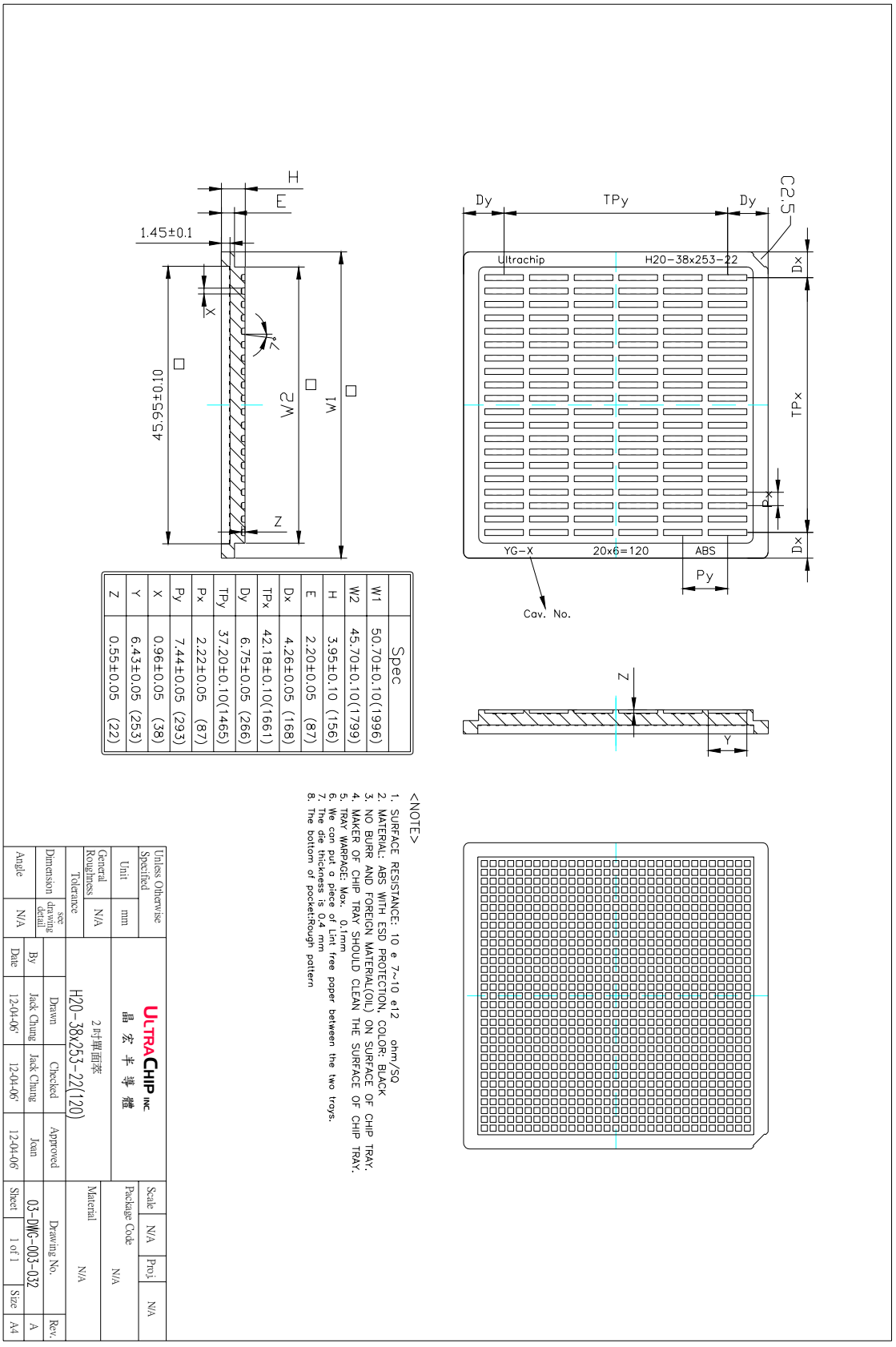
#	Pad	X	Y	W	H
1	DUMMY	-3028.5	322.125	89	27.75
2	COM33	-3028.5	284	89	22.5
3	COM35	-3028.5	248.5	89	22.5
4	COM37	-3028.5	213	89	22.5
5	COM39	-3028.5	177.5	89	22.5
6	COM41	-3028.5	142	89	22.5
7	COM43	-3028.5	106.5	89	22.5
8	COM45	-3028.5	71	89	22.5
9	COM47	-3028.5	35.5	89	22.5
10	COM49	-3028.5	0	89	22.5
11	COM51	-3028.5	-35.5	89	22.5
12	COM53	-3028.5	-71	89	22.5
13	COM55	-3028.5	-106.5	89	22.5
14	COM57	-3028.5	-142	89	22.5
15	COM59	-3028.5	-177.5	89	22.5
16	COM61	-3028.5	-213	89	22.5
17	COM63	-3028.5	-248.5	89	22.5
18	CIC	-3028.5	-284	89	22.5
19	DUMMY	-3028.5	-322.125	89	27.5
20	CS0	-2827.7	-301.275	65	71.45
21	CS1	-2746.1	-301.275	65	71.45
22	VDDX	-2666.3	-301.275	45	71.45
23	RST_	-2586.5	-301.275	65	71.45
24	CD	-2504.9	-301.275	65	71.45
25	WR0	-2423.3	-301.275	65	71.45
26	VDDX	-2343.5	-301.275	45	71.45
27	WR1	-2263.7	-301.275	65	71.45
28	D0	-2173.75	-301.275	65	71.45
29	D1	-2088.65	-301.275	65	71.45
30	D2	-2003.55	-301.275	65	71.45
31	D3	-1918.45	-301.275	65	71.45
32	D4	-1833.35	-301.275	65	71.45
33	D5	-1748.25	-301.275	65	71.45
34	D6	-1663.15	-301.275	65	71.45
35	VDDX	-1581.6	-301.275	45	71.45
36	D7	-1500.05	-301.275	65	71.45
37	BM0	-1410.1	-301.275	65	71.45
38	VDDX	-1330.3	-301.275	45	71.45
39	BM1	-1250.5	-301.275	65	71.45
40	ID	-1168.9	-301.275	65	71.45
41	VDD	-1089.1	-301.275	45	71.45
42	DUMMY	-996.35	-301.275	45	71.45
43	DUMMY	-936.35	-301.275	45	71.45
44	DUMMY	-876.35	-301.275	45	71.45
45	DUMMY	-816.35	-301.275	45	71.45
46	VDD	-723.6	-301.275	45	71.45
47	VDD2	-472.6	-301.275	45	71.45
48	DUMMY	-368	-301.275	45	71.45
49	DUMMY	-308	-301.275	45	71.45
50	VDD2	-203.5	-301.275	45	71.45
51	VDD3	-41.4	-301.275	45	71.45
52	VDD3	18.6	-301.275	45	71.45
53	VSS	78.6	-301.275	45	71.45
54	VSS	138.6	-301.275	45	71.45
55	DUMMY	226.95	-301.275	45	71.45
56	VSS	315.3	-301.275	45	71.45
57	DUMMY	385.45	-301.275	45	71.45
58	VSS2	455.6	-301.275	45	71.45
59	DUMMY	543.95	-301.275	45	71.45
60	VSS2	632.3	-301.275	45	71.45
61	VSS2	692.3	-301.275	45	71.45
62	TST4	774.1	-301.275	65	71.45
63	TST2	965.425	-285.5	45	103
64	TST1	1025.425	-285.5	45	103
65	VB1+	1381.925	-285.5	45	103
66	VB1+	1441.925	-285.5	45	103
67	VB1-	1501.925	-285.5	45	103
68	VB1-	1561.925	-285.5	45	103
69	VB0-	1918.925	-285.5	45	103
70	VB0-	1978.925	-285.5	45	103
71	VB0+	2038.925	-285.5	45	103
72	VB0+	2098.925	-285.5	45	103
73	VLCDOUT	2536.925	-285.5	45	103
74	VLCDIN	2596.925	-285.5	45	103
75	DUMMY	3028.5	-322.125	89	27.75
76	COM64	3028.5	-284	89	22.5
77	COM62	3028.5	-248.5	89	22.5
78	COM60	3028.5	-213	89	22.5
79	COM58	3028.5	-177.5	89	22.5
80	COM56	3028.5	-142	89	22.5
81	COM54	3028.5	-106.5	89	22.5
82	COM52	3028.5	-71	89	22.5
83	COM50	3028.5	-35.5	89	22.5
84	COM48	3028.5	0	89	22.5
85	COM46	3028.5	35.5	89	22.5
86	COM44	3028.5	71	89	22.5
87	COM42	3028.5	106.5	89	22.5
88	COM40	3028.5	142	89	22.5
89	COM38	3028.5	177.5	89	22.5
90	COM36	3028.5	213	89	22.5
91	COM34	3028.5	248.5	89	22.5
92	COM32	3028.5	284	89	22.5
93	DUMMY	3028.5	322.125	89	27.75
94	COM30	2893.25	293.5	22.5	89
95	COM28	2857.75	293.5	22.5	89
96	COM26	2822.25	293.5	22.5	89
97	COM24	2786.75	293.5	22.5	89
98	COM22	2751.25	293.5	22.5	89
99	COM20	2715.75	293.5	22.5	89
100	COM18	2680.25	293.5	22.5	89
101	COM16	2644.75	293.5	22.5	89
102	COM14	2609.25	293.5	22.5	89
103	COM12	2573.75	293.5	22.5	89
104	COM10	2538.25	293.5	22.5	89
105	COM8	2502.75	293.5	22.5	89
106	COM6	2467.25	293.5	22.5	89
107	COM4	2431.75	293.5	22.5	89
108	COM2	2396.25	293.5	22.5	89
109	CIC	2360.75	293.5	22.5	89
110	SEG1	2325.25	293.5	22.5	89
111	SEG2	2289.75	293.5	22.5	89
112	SEG3	2254.25	293.5	22.5	89
113	SEG4	2218.75	293.5	22.5	89
114	SEG5	2183.25	293.5	22.5	89
115	SEG6	2147.75	293.5	22.5	89
116	SEG7	2112.25	293.5	22.5	89
117	SEG8	2076.75	293.5	22.5	89
118	SEG9	2041.25	293.5	22.5	89

#	Pad	X	Y	W	H
119	SEG10	2005.75	293.5	22.5	89
120	SEG11	1970.25	293.5	22.5	89
121	SEG12	1934.75	293.5	22.5	89
122	SEG13	1899.25	293.5	22.5	89
123	SEG14	1863.75	293.5	22.5	89
124	SEG15	1828.25	293.5	22.5	89
125	SEG16	1792.75	293.5	22.5	89
126	SEG17	1757.25	293.5	22.5	89
127	SEG18	1721.75	293.5	22.5	89
128	SEG19	1686.25	293.5	22.5	89
129	SEG20	1650.75	293.5	22.5	89
130	SEG21	1615.25	293.5	22.5	89
131	SEG22	1579.75	293.5	22.5	89
132	SEG23	1544.25	293.5	22.5	89
133	SEG24	1508.75	293.5	22.5	89
134	SEG25	1473.25	293.5	22.5	89
135	SEG26	1437.75	293.5	22.5	89
136	SEG27	1402.25	293.5	22.5	89
137	SEG28	1366.75	293.5	22.5	89
138	SEG29	1331.25	293.5	22.5	89
139	SEG30	1295.75	293.5	22.5	89
140	SEG31	1260.25	293.5	22.5	89
141	SEG32	1224.75	293.5	22.5	89
142	SEG33	1189.25	293.5	22.5	89
143	SEG34	1153.75	293.5	22.5	89
144	SEG35	1118.25	293.5	22.5	89
145	SEG36	1082.75	293.5	22.5	89
146	SEG37	1047.25	293.5	22.5	89
147	SEG38	1011.75	293.5	22.5	89
148	SEG39	976.25	293.5	22.5	89
149	SEG40	940.75	293.5	22.5	89
150	SEG41	905.25	293.5	22.5	89
151	SEG42	869.75	293.5	22.5	89
152	SEG43	834.25	293.5	22.5	89
153	SEG44	798.75	293.5	22.5	89
154	SEG45	763.25	293.5	22.5	89
155	SEG46	727.75	293.5	22.5	89
156	SEG47	692.25	293.5	22.5	89
157	SEG48	656.75	293.5	22.5	89
158	SEG49	621.25	293.5	22.5	89
159	SEG50	585.75	293.5	22.5	89
160	SEG51	550.25	293.5	22.5	89
161	SEG52	514.75	293.5	22.5	89
162	SEG53	479.25	293.5	22.5	89
163	SEG54	443.75	293.5	22.5	89
164	SEG55	408.25	293.5	22.5	89
165	SEG56	372.75	293.5	22.5	89
166	SEG57	337.25	293.5	22.5	89
167	SEG58	301.75	293.5	22.5	89
168	SEG59	266.25	293.5	22.5	89
169	SEG60	230.75	293.5	22.5	89
170	SEG61	195.25	293.5	22.5	89
171	SEG62	159.75	293.5	22.5	89
172	SEG63	124.25	293.5	22.5	89
173	SEG64	88.75	293.5	22.5	89
174	SEG65	53.25	293.5	22.5	89
175	SEG66	17.75	293.5	22.5	89
176	SEG67	-17.75	293.5	22.5	89
177	SEG68	-53.25	293.5	22.5	89
178	SEG69	-88.75	293.5	22.5	89
179	SEG70	-124.25	293.5	22.5	89

#	Pad	X	Y	W	H
180	SEG71	-159.75	293.5	22.5	89
181	SEG72	-195.25	293.5	22.5	89
182	SEG73	-230.75	293.5	22.5	89
183	SEG74	-266.25	293.5	22.5	89
184	SEG75	-301.75	293.5	22.5	89
185	SEG76	-337.25	293.5	22.5	89
186	SEG77	-372.75	293.5	22.5	89
187	SEG78	-408.25	293.5	22.5	89
188	SEG79	-443.75	293.5	22.5	89
189	SEG80	-479.25	293.5	22.5	89
190	SEG81	-514.75	293.5	22.5	89
191	SEG82	-550.25	293.5	22.5	89
192	SEG83	-585.75	293.5	22.5	89
193	SEG84	-621.25	293.5	22.5	89
194	SEG85	-656.75	293.5	22.5	89
195	SEG86	-692.25	293.5	22.5	89
196	SEG87	-727.75	293.5	22.5	89
197	SEG88	-763.25	293.5	22.5	89
198	SEG89	-798.75	293.5	22.5	89
199	SEG90	-834.25	293.5	22.5	89
200	SEG91	-869.75	293.5	22.5	89
201	SEG92	-905.25	293.5	22.5	89
202	SEG93	-940.75	293.5	22.5	89
203	SEG94	-976.25	293.5	22.5	89
204	SEG95	-1011.75	293.5	22.5	89
205	SEG96	-1047.25	293.5	22.5	89
206	SEG97	-1082.75	293.5	22.5	89
207	SEG98	-1118.25	293.5	22.5	89
208	SEG99	-1153.75	293.5	22.5	89
209	SEG100	-1189.25	293.5	22.5	89
210	SEG101	-1224.75	293.5	22.5	89
211	SEG102	-1260.25	293.5	22.5	89
212	SEG103	-1295.75	293.5	22.5	89
213	SEG104	-1331.25	293.5	22.5	89
214	SEG105	-1366.75	293.5	22.5	89
215	SEG106	-1402.25	293.5	22.5	89
216	SEG107	-1437.75	293.5	22.5	89
217	SEG108	-1473.25	293.5	22.5	89
218	SEG109	-1508.75	293.5	22.5	89
219	SEG110	-1544.25	293.5	22.5	89
220	SEG111	-1579.75	293.5	22.5	89
221	SEG112	-1615.25	293.5	22.5	89
222	SEG113	-1650.75	293.5	22.5	89
223	SEG114	-1686.25	293.5	22.5	89
224	SEG115	-1721.75	293.5	22.5	89
225	SEG116	-1757.25	293.5	22.5	89
226	SEG117	-1792.75	293.5	22.5	89
227	SEG118	-1828.25	293.5	22.5	89
228	SEG119	-1863.75	293.5	22.5	89
229	SEG120	-1899.25	293.5	22.5	89
230	SEG121	-1934.75	293.5	22.5	89
231	SEG122	-1970.25	293.5	22.5	89
232	SEG123	-2005.75	293.5	22.5	89
233	SEG124	-2041.25	293.5	22.5	89
234	SEG125	-2076.75	293.5	22.5	89
235	SEG126	-2112.25	293.5	22.5	89
236	SEG127	-2147.75	293.5	22.5	89
237	SEG128	-2183.25	293.5	22.5	89
238	SEG129	-2218.75	293.5	22.5	89
239	SEG130	-2254.25	293.5	22.5	89
240	SEG131	-2289.75	293.5	22.5	89

#	Pad	X	Y	W	H
241	SEG132	-2325.25	293.5	22.5	89
242	COM1	-2360.75	293.5	22.5	89
243	COM3	-2396.25	293.5	22.5	89
244	COM5	-2431.75	293.5	22.5	89
245	COM7	-2467.25	293.5	22.5	89
246	COM9	-2502.75	293.5	22.5	89
247	COM11	-2538.25	293.5	22.5	89
248	COM13	-2573.75	293.5	22.5	89
249	COM15	-2609.25	293.5	22.5	89
250	COM17	-2644.75	293.5	22.5	89
251	COM19	-2680.25	293.5	22.5	89
252	COM21	-2715.75	293.5	22.5	89
253	COM23	-2751.25	293.5	22.5	89
254	COM25	-2786.75	293.5	22.5	89
255	COM27	-2822.25	293.5	22.5	89
256	COM29	-2857.75	293.5	22.5	89
257	COM31	-2893.25	293.5	22.5	89

TRAY INFORMATION



	Spec
W1	50.70±0.10(1996)
W2	45.70±0.10(1799)
H	3.95±0.10 (156)
E	2.20±0.05 (87)
Dx	4.26±0.05 (168)
TPx	42.18±0.10(1661)
Dy	6.75±0.05 (266)
TPy	37.20±0.10(1465)
Px	2.22±0.05 (87)
Py	7.44±0.05 (293)
X	0.96±0.05 (38)
Y	6.43±0.05 (253)
Z	0.55±0.05 (22)

Unless Otherwise Specified		ULTRACHIP INC 晶宏半導體									
Unit	mm	2吋單面萊 H20-38x253-22(120)									
General Roughness Tolerance	N/A										
Dimension see drawing detail	N/A										
Angle	N/A		By	Drawn	Checked	Approved	Material	N/A	Package Code	N/A	Scale N/A
		Date	Jack Chung	Jack Chung	Joan						Proj. N/A
		12-04-06'	12-04-06'	12-04-06'	12-04-06				Drawing No.	03-DWG-003-032	Rev. A
									Sheet	1 of 1	Size A4

REVISION HISTORY

Revision	Contents	Date
0.1	Origin: UC1601(D) v1.1	Nov. 10, '06
0.6	First release	Jan. 30, '07
0.7	(1) Description for dummy pins is added. (Section "Pin Description", page 6)	Mar. 1, '07
0.8	(1) The Read command for S8/S9 mode is removed. (Section "Command Table" – (24) Read Data, page 10)	Apr. 27, '07
	(2) V_{LCD} formula is updated. (Section "V_{LCD} Quick Reference", page 18)	
	(3) In the second table, the "CD Init. Bus State" & "RESET Init. Color Mapping" columns, and related notes are removed. (Section "Host Interface", page 23)	
	(4) The drawings are updated by adding the ID pin. (Section "Host Interface Reference Circuit", Pp 28~30)	
	(5) The example data beneath the Display Data RAM table are corrected. (Section "Display Data RAM", page 32)	
	(6) V_{IL} and V_{IH}, Input Logic Low/High, for I^2C mode are added. (Section "Specifications" – DC Characteristics, page 38)	
	(7) The maximum value of power consumption present. (Section "Specifications" – Power Consumption, page 38)	
	(8) Some AC timings and the drawings for S8 & S9 are updated. (Section "AC Characteristics", Pp 39~43)	
1.0	(No specification is changed.)	May 3, '07
1.1	(1) V_{DD} (Maximum) and $V_{DD2/3}$ (Maximum) are adjusted: 3.3V → 3.465V (Section "Specifications" – DC Characteristics, page 40)	May 17, '07
1.11	(1) Command "Get Status" under S8/S9 mode, is corrected. (Section "Command Table" – (25), page 12; "Command Description" – (25), page 18)	Apr. 3, '08
	(2) The description of sub-section "Power Down Sequence" is updated. (Section "Reset and Power Management", page 36)	
1.12	(1) Some legacy words are removed. (Section "Command Description" – (2) Read Data, page 13)	Apr. 11, '08
	(2) The illustration is corrected, # of COM : 95 → 63 (Section "Command Description" - (24) Set Partial Display End, p. 17)	
1.13	(1) The description on draining circuit in Sleep mode is updated. (Section "Reset & Power Management", page 35)	May 1, '08
1.14	(1) The notes on I^2C license are removed. (Section "General Notes", page 4)	May 30, '08
	(2) Figures 4a / 5a are inserted to illustrate Read in S8 / S9 modes. (Section "Host Interfaces", Pp 27~28)	
1.15	(1) Pad RIC_PAD is renamed to CIC. (Section "Pad Coordinates", page 50)	Jul. 17, '08
1.16	(1) The example under the RAM table is corrected. (Section "Display Data RAM", page 35)	Aug. 7, '08
1.2	(1) One more die thickness, 300μM, is added. (Section "Physical Dimension", page 48)	Sep. 17, '08
1.21	(1) The relationship among CEN, DST and DEN is updated. (pages 11, 17)	Aug. 25, '09
1.22	Rising time (tr) and falling time (tf), 15nS each, are added into System Cycle Time. (Pp 43~48)	Nov. 19, '09
1.23	(1) Correct the inequations for CEN, DST and DEN.	Jan. 14, '10
	(2) The timing of SCK for the S9 mode is corrected.	
1.24	(1) Bump Height: 15uM → 12uM	Apr. 13, '10

Revision	Contents	Date
1.25	(1) Bump Height: 12uM → 15uM	Aug. 11, 2010