VIT

Reg. No. :

Final Assessment Test (FAT) - November/December 2023

Programme	B.Tech.	Semester	FALL SEMESTER 2023 - 24
Course Title	COMPUTER ARCHITECTURE AND ORGANIZATION	Course Code	BCSE205L
Faculty Name	Prof. A. K Ilavarasi	Slot	F2+TF2
		Class Nbr	CH2023240101204
Time	3 Hours	Max. Marks	100

PART - A (10 X 10 Marks)

Answer all questions

01. i. Discuss how the stored program concept works for the following instructions which adhere to *Opcode source, destination* format. . Explain the operational steps involved with a suitable diagram. (5 marks) **[10]**

LOAD (R12), R6

DIV R6, R0, R8

ii. Comment on the speed of operation in processors that use Von-Neumann architecture and Harvard architecture. Draw suitable diagrams to justify your inference. [5 marks]

02. i. Perform multiplication $(-21)_{10}$ X $(9)_{10}$ using modified booth algorithm. (7 marks) **[10]**

ii. If the least significant bit of Q register is 0 in every iteration, the algorithm yields a best case outcome. Prove if this statement is true or not. (3 marks)

03. Perform the following Floating point operation on the numbers $(357.65)_{10}$ and $(222.75)_{10}$. **[10]**

i. Convert the above numbers into normalized notation of binary format. (5 marks)

ii. Perform addition operation for the given numbers and write the normalized result in IEEE-754 double precision format.(5 marks)

04. Illustrate the architectural design of Single Cycle Data Path to fetch and execute the following instructions. **[10]**

MOV #20, AX

MUL (R2), AX

MOV AX, R1

i. Write down the micro routine control sequence steps involved with respect to the given instructions which adhere to Opcode source, destination format. (8 marks)

ii. What is the significance of WMFC signal? (2 marks)

05. Consider a cache of 4 lines of 16 bytes each. Main memory is divided into blocks of 16 bytes each. That is, block 0 has bytes with addresses 0 through 15, and so on. Now consider a program that accesses memory in the following sequence of addresses: **[10]**

Repeat 2 times: 63 through 70

Once: 15 through 32; 80 through 95

a. Suppose the cache is organized as direct mapped. Memory blocks 0, 4, and so on are assigned to line 0; blocks 1, 5, and so on to line 1; and so on. Compute the hit ratio.(5 marks)

b. Suppose the cache is organized as fully associative(Assume flexible block assignment). Compute the hit ratio using the least recently used replacement scheme.(5 marks)

06. i. Discuss the principle of synchronous bus operation using a clock diagram for burst mode data transfer. How does a high frequency clock impact the communicating devices? (5 marks) [10]
ii. Differentiate strobe control and handshake protocol ?(5 marks)

07. Let us assume that 00110010 is the code word that is sent, and that 00100010 is received. The receiver has to search for appropriate parities to ascertain whether the code is correct because it has no idea what was communicated. [10]
a) If even parity is employed, identify transmission errors using Hamming code algorithm.(8 marks)
b) Discuss in detail how the bit errors are corrected as per the above algorithm.(2 marks)

08. Consider the following sequence of instructions organized in a 4-stage pipeline: [10]
Add #20, R0, R1
Mul #3, R2, R3
And R1, R2, R4
Add R0, R4, R5
(Note: In all the instructions, the destination operand is given last)
i. Identify the specific type of data dependences observed in the pipelined execution with appropriate 4- stage pipeline diagram.(5 marks)
ii. Discuss the methods to eliminate the hazards with a suitable diagram.(5 marks)

09. i. An E-commerce application like Flipkart demands zero down time and maintains payment-based sensitive data. How will you ensure reliability, availability and redundancy of data if the server crashes out. Suggest a nested RAID level suitable for this application with appropriate diagram. (5 marks) [10]
ii. A small -scale industry is looking for a cost-effective storage design. The response time is vital for the day to day operations of this industry and requires both read and write operations to be fast. Discuss a suitable RAID level architecture that will meet with the requirements.(5 marks)

10. Consider that the processor is executing instructions in a sequence by fetching data from the memory. Simultaneously the processor receives interrupt requests from five devices. [10]
Programmed I/O is consuming more time when issuing commands for data transfer and holds the processor in data transfer while the data processing is neglected.
i. Address this issue and suggest how to improve the processor performance when high speed peripherals require bulk transfer of data (7 Marks)
ii. Discuss the interrupt driven I/O process with a suitable example.(3 Marks)

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