Course code	Computer Architecture And Organization	L	T	P	J	C
CSE2001		3	0	0	0	3
Pre-requisite	-	Syllabus version				
		v. xx.xx				

Course Objectives:

The objective of this course is

- To provide basic concepts of computer architecture and organization.
- To impart the knowledge of implementation of arithmetic operations in the computer.
- To develop a deeper understanding of the hardware environment upon which all processing are carried out.
- To provide knowledge about internals of memory system, interfacing techniques and subsystem devices.

Expected Course Outcome:

CO 1: Differentiate Von Neumann, Harvard, and CISC and RISC architectures. Analyze the performance of machines with different capabilities.
CO 2: Illustrate binary format for numerical and characters. Validate efficient algorithm for arithmetic operations.
CO 3: Construct machine level program for given expression on n-address machine. Analyze and calculate memory traffic for a program execution. Design an efficient data path for an instruction format for a given architecture.
CO 4: Explain the importance of hierarchical memory organization. Able to construct larger memories. Analyze and suggest efficient cache mapping technique and replacement algorithms for given design requirements. Demonstrate hamming code for error detection and correction.
CO 5: Understand the need for an interface. Compare and contrast memory mapping and IO mapping techniques. Describe and Differentiate different modes of data transfer. Appraise the synchronous and asynchronous bus for performance and arbitration.
CO 6: Understand the structure and read write mechanisms for different storage systems. Illustrate and suggest appropriate use of RAID levels. Assess the performance of IO and external storage systems.
CO 7: classify parallel machine models. Illustrate typical 6-stage pipeline for overlapped execution. Analyze the hazards and solutions.

Student Learning Outcomes (SLO):	1,2,5

Module:1	INTRODUCTION AND OVERVIEW OF COMPUTER ARCHITECTURE	3 hours	SLO: 2

Introduction to computer systems – Overview of Organization and Architecture – Functional Components of a computer – Registers and register files – Interconnection of components – Organization of the von Neumann machine and Harvard architecture – Performance of Processor.

Module:2	Data Representation And Computer Arithmetic	6 hours	SLO: 1, 2

Fixed point representation of numbers-algorithms for arithmetic operations: multiplication (Booth's, Modified Booth's) - division (restoring and non-restoring)- Floating point representation with IEEE standards and algorithms for common arithmetic operations- Representation of non-numeric data (character codes**).**

Module:3	Fundamentals of Computer Architecture	11 hours	SLO: 1,2

Introduction to ISA (Instruction Set Architecture)-Instruction formats- Instruction types and addressing modes-Instruction execution (Phases of instruction cycle)- Assembly language programming-Subroutine call and return mechanisms-Single cycle Data path design-Introduction to multi cycle data path-Multi cycle Instruction execution.

Module:4	Memory System Organization & Architecture	9 hours	SLO: 1,2,5

Memory systems hierarchy-Main memory organization-Types of Main memory-memory interleaving and its characteristics and performance- Cache memories: address mapping-line size-replacement and policies- coherence-Virtual memory systems- TLB- Reliability of memory systems- error detecting and error correcting systems.			
Module:5	**Interfacing and Communication**	**7 hours**	**SLO: 2,5**
I/O fundamentals: handshaking, buffering-I/O techniques: programmed, I/O, interrupt-drive I/O, DMA – Interrupt structures: vectored and prioritized-interrupt overhead – Buses: Synchronous and asynchronous – Arbitration.			
Module:6	**Device Subsystems**	**4 hours**	**SLO: 2,5**
External storage systems-organization and structure of disk drives: Electronic- magnetic and optical technologies- RAID Levels- I/O Performance			
Module:7	**Performance Enhancements**	**4 hours**	**SLO: 2,5**
Classification of models – Flynn's taxonomy of parallel machine models (SISD, SIMD, MISD, MIMD) – Introduction to Pipelining – Pipelined data path – Introduction to hazards.			
Module:8	**Recent Trends**	1	**SLO: x,x**
Multiprocessor architecture: Overview of Shared Memory Architecture Distributed Architecture			
	Total Lecture hours:	**45 hours**	

Text Book(s)	
1.	David A. Patterson and . John L. Hennessy "Computer Organization and Design-The Hardware/Software Interface" 5th edition, Morgan Kaufmann, 2011.
2.	Carl Hamacher, Zvonko Vranesic, Safwat Zaky, Computer organization, Mc Graw Hill, Fifth edition ,Reprint 2011.
Reference Books	
1.	W. Stallings, Computer organization and architecture, Prentice-Hall, 8th edition, 2009
	Authors, book title, year of publication, edition number, press, place

Mode of Evaluation:			
Mode of evaluation:			
Recommended by Board of Studies	DD-MM-YYYY		
Approved by Academic Council	No. xx	Date	DD-MM-YYYY

CO-PO MAPPING:

	PO 1 **SLO 1**	**PO 2** **SLO 2**	**PO 3** **SLO 5**	**PO 9**	**PO 10**	**PO 11**	**PO 12**	**PO 13**	**PO 15**	**PO 16**	**PO 18**	**PO 20**
CO1		*										
CO2	*	*										
CO3	*	*										

CO4	*	*	*									
CO5		*	*									
CO6		*	*									
CO7		*	*									

Knowledge areas that contain topics and learning outcomes covered in the course

Knowledge Area	**Total Hours of Coverage**
CS: AR(Architecture) / CE: CAO(Computer Architecture and Organization)	45

Body of Knowledge coverage

KA	**Knowledge Unit**	**Topics Covered**	**Hours**
CS: AR CE:CAO	**AR/Digital Logic and Digital Systems** **AR/Assembly Level Machine Organization**	• Indicate some reasons for studying computer architecture and organization • Indicate some important topic areas such as system organization and architecture, memory, interfacing, microprocessors, and performance • Contrast the meanings of between computer organization and computer architecture • Indicate the importance of doing binary arithmetic with computers • Mention memory as a crucial component to the design of a computer • Illustrate the importance of interfacing with computer components and peripherals • Mention a typical CPU and sketch its organization • Indicate why performance leads to alternate architectures • Mention some of the strategies used in architecture such as CISC and RISC approaches.	**3**

		• Functional units of a computer • Registers and register files • Organization of the von Neumann machine • Harvard architecture • Differences between von Neumann & Harvard architecture • Measuring performance	
CS: AR CE:CAO	**AR/Machine Level Representation of Data**	• Bits, bytes, and words • Representation of integers (positive and negative numbers) • Representation of non-numeric data (character codes) • Algorithms for common arithmetic operations (multiplication, division) • Representation of real numbers (IEEE standards for floating-point representation) • Significance of range, precision, and accuracy in computer arithmetic for carrying out common floating-point operations • Algorithms floating-point operations	6
CS: AR CE:CAO	**AR/Assembly Level Machine Organization** **AR/Functional Organization(Elective)**	• Instruction formats • Instruction types and addressing modes • Assembly/machine language programming • Subroutine call and return mechanisms • Programming in assembly language • Single cycle Data path design • Introduction to multi cycle data path • Multi cycle Instruction execution.(Five step Instruction execution)	11
CS: AR CE:CAO	**AR/Memory System Organization and Architecture**	• Storage systems and their technology • Memory technologies systems such as DRAM, EPROM, and FLASH • Memory hierarchy: importance of temporal and spatial locality • Main memory organization and operations	9

		• Memory interleaving • Cache memories (address mapping, block size, replacement and store policy) • cache consistency • Virtual memory (page table, TLB) • Error detection and error correction: Hamming Error detection and error correction	
CS: AR CE:CAO	**AR/Interfacing and Communication**	• I/O fundamentals: handshaking, buffering, • I/O techniques: programmed I/O, interrupt-driven I/O, DMA • Interrupt structures: vectored and prioritized, interrupt overhead • Buses: Synchronous and asynchronous, bus arbitration	7
CS: AR CE:CAO	**AR/Interfacing and Communication**	• External storage systems; organization and structure of disk drives and optical memory (three tier and pyramid structure**)** • Basic I/O controllers such as a keyboard and a mouse • RAID levels • I/O Performance	4
CS: AR CE:CAO	**AR/Assembly Level Machine Organization** **AR/Functional Organization(Elective)**	• Classification of models: parallel machine models (SISD, SIMD, MISD, MIMD) Flynn's taxonomy • Introduction to Pipelining • Pipelined data path • Introduction to hazards	4
CS: AR CE:CAO	**AR/Multiprocessing and Alternative Architectures**	• Multiprocessor architecture – Overview of Shared Memory architecture, Distributed architecture	1
		Total hours	**45**

Where does the course fit in the curriculum?

This course is a

- Program core Course.
- Suitable from 3rd semester onwards.
- Knowledge of Fundamental Digital logic is preferred.

What is covered in the course?

This course is designed to cover basic principles of computer organization, operation and performance. The first two modules give an overview of the computer hardware and computer arithmetic. Numeric and non-numeric data representation, algorithms for various arithmetic operations are covered in the second module.

Fundamentals of computer architecture like various instruction types, formats, addressing modes, subroutine call and return implementations, single cycle data path, introduction to multi-cycle data path are covered in the module 3. Introduction and sufficient coverage of assembly level language programming s also dealt in this module.

Various memory technologies, organization are covered in the 4th module. Memory hierarchy, Caches, multi-module memory systems, memory interleaving, and performance metrics are also covered in this module.

The basics of I/O organization, data transfer, and synchronization are coved in the fifth module. This module also covers different interfacing techniques, interrupts, and bus arbitration techniques.

The next module discusses about the Device Subsystems, External Storage Devices including Hard Disks, RAID, etc.

The last module is intended for covering the enhancements for improving the performance. Pipelining, Advances in computer architecture like multi-processor architectures are also dealt in the last module

What is the format of the course?

This Course is designed with 150 minutes of in-classroom sessions per week. Generally this course should have the combination of lectures, in-class discussion, case studies, guest-lectures, mandatory off-class reading material.

How are students assessed?

- Students are assessed based on group activities, classroom discussion, assignments (design problems, performance analysis and evaluation), continuous assessment test, and final assessment test.
- Students can earn additional weightage based on certificate of completion of a related MOOC course.

Other comments

Designing of single cycle data path, need for multi cycle data path, insights into pipelining are added to increase the understanding level of the subject. This also equips the students with better insights.

Session wise plan

Sl.No	Class Hour	Lab Hour	Topic Covered	levels of mastery	Reference Book	Remarks
1	1		Introduction to computer systems, Overview of Organization and Architecture	Familiarity	2	
2	1		Functional components of a computer, Registers and register files, Interconnection of components; Organization of the von Neumann machine, Harvard architecture	Familiarity	2	
3	1		Performance	assessment	1	
4	1		Data Representation, Fixed point and	Usage	1,2	

			Floating point representation of numbers			
5	1		algorithms for multiplication,	Usage	1,2	
6	1		algorithms for Division	Usage	1,2	
7	1		Algorithms for floating point addition	Usage	1,2	
8	1		algorithms for Floating point multiplication and division	Usage	1,2	
9	1		Representation of non-numeric data,	Familiarity	2	
10	1		ISA, Instruction formats.	Familiarity	1,2	
11	2		Instruction types and addressing modes	Familiarity	1,2,3	
12	1		Assembly language programming	Familiarity	1	
13	1		Subroutine call and return mechanisms	Familiarity	2	
14	3		Single cycle Data path design;	Usage	1	
15	2		Introduction to multi cycle data path; Multi cycle Instruction execution.	Familiarity	1	
16	1		Memory systems hierarchy Main memory	Familiarity	2,3	

			organization,			
17	1		Types of Main memories, characteristics and performance and interleaving	Familiarity	1,2,3	
18	1		Cache memories (Introduction, line size, write policies);	assessment	1,2,3	
19	1		Cache mapping techniques	Usage	1,2,3	
20	1		Replacement policies	Familiarity	1,2,3	
21	2		Virtual Memory	Familiarity	1,2,3	
22	2		error detection and error correcting systems	Usage	3	
23	1		I/O fundamentals: handshaking, buffering	Familiarity	2	
24	1		I/O techniques: programmed I/O	Familiarity	2	
25	1		Interrupt-driven I/O	Familiarity	2	
26	1		DMA	Familiarity	2	
27	1		Interrupt structures: vectored and prioritized.	Familiarity	2	

28	1		Interrupts	Familiarity	2	
29	1		Buses: Synchronous and asynchronous, Local and geographic arbitration	Familiarity	2	
30	1		External storage systems organization and structure of disk drives	Familiarity	1,2	
31	1		organization and structure of Optical Disk Electronic, magnetic tapes	Familiarity	1,2	
32	1		RAID **architectures**;	Familiarity	2,3	
33	1		I/O Performance,	Usage	1,2	
34	2		Introduction to Pipelining, Pipelining data path	Familiarity	1,2	
35	1		Multiprocessor architecture, Shared Memory architecture,	Familiarity	3	
36	1		Distributed architecture	Familiarity	3	
37	1		Parallel Machine Models.	Familiarity	3	