Reg. No.: [redacted]

Name :

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test II - October, 2023

Programme	:	B. Tech. CSE	Semester	:	Fall 2023-24
Course	:	Computer Architecture and Organization	Code	:	BCSE205L
Faculty	:	Dr. A. K Ilavarasi Dr. Vaidehi Vijayakumar Dr. B V A N S S Prabhakar Rao	Class Nbr(s)	:	CH2023240101204 CH2023240100884 CH2023240100883
			Slot(s)	:	F2+TF2
Time	:	1½ Hours	Max. Marks	:	50

Answer ALL the Questions

Q. No.	Question Text	Marks
1.	i) Consider a one addressed machine with the following memory address of the word and its corresponding accumulator value. (5 marks)	10

Address	Content
20	70
30	60
40	50
50	40
60	30
70	20

What values do the following instructions load into the accumulator after execution?

a. Load IMMEDIATE 30
b. Load DIRECT 20
c. Load INDIRECT 20
d. Load IMMEDIATE 40
e. Load INDIRECT 30

ii) Write the sequence of control signals required for executing any two of the above instructions based on your choice in single bus organization. (5 marks)

2	Given the expression R1 + =20 i. Write the instruction to implement the given expression and give the control sequence for single cycle and multi cycle data path. (7 marks) ii. How many clock cycles are reduced with multi cycle data path and justify your answer. (3 marks)	10
3.	A computer has to be interfaced with a memory module that consists of a 1 M x 32 RAM. i. Construct this memory module using 512 K x 8 RAM chips. Discuss with appropriate diagram. (6 marks) ii. How will the address bits be decoded for each memory module of this organization? (4 marks)	10

4.	Consider a machine with a byte addressable main memory of 216 bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. i. How is a 16-bit memory address divided into tag, line number, and byte number? (3 marks) ii. Into what line would bytes with each of the following addresses be stored? (4 marks) 0001 0001 0001 1011 1100 0011 0011 0100 1101 0000 0001 1101 1010 1010 1010 1010 iii. Suppose the byte with address 0001 1010 0001 1010 is stored in the cache. What are the addresses of the other bytes stored along with it? (2 marks) iv. Calculate the total bytes of memory that can be stored in the cache? (1 mark)	10
5.	The following steps represent an algorithm: Step 1: In this step, the corresponding registers will be initialized, i.e., register A contains value 0, register M has the Divisor, register Q has the Dividend, and N is used to specify the number of bits in dividend. Step 2: In this step, register A and register Q will be treated as a single unit, and the value of both the registers will be shifted left. Step 3: After that, the value of register M will be subtracted from register A. The result of subtraction will be stored in register A. Step 4: Now, check the most significant bit of register A. If this bit of register A is 0, then the least significant bit of register Q will be set with a value 1. If the most significant bit of A is 1, then the least significant bit of register Q will be set to with value 0, and restore the value of A that means it will restore the value of register A before subtraction with M. Step 5: After that, the value of N will be decremented. Here n is used as a counter. Step 6: Now, if the value of N is 0, we will break the loop. Otherwise, we have to again go to step 2. Step 7: This is the last step. In this step, the quotient is contained in the register Q, and the remainder is contained in register A. Use the knowledge of Computer Instruction Sets and try to develop a precise of assemble language program code as per the requirement pertaining to each and every step represented above. Also justify the need for each of the instruction.	10