VIT
Vellore Institute of Technology

Reg. No. : 21BPS5364

Final Assessment Test (FAT) – November/December 2022

Programme	B.Tech.	Semester	Fall Semester 2022-23
Course Title	COMPUTER ARCHITECTURE AND ORGANIZATION	Course Code	BCSE205L
Faculty Name	Prof. A. K Ilavarasi	Slot	B2+TB2
		Class Nbr	CH2022231001515
Time	3 Hours	Max. Marks	100

Part A (10 X 10 Marks)
Answer All questions

1. At memory location 2021, Mul A, (R52), #23 instruction is residing. How will the processor fetch the instruction and execute the instruction based on various registers in the CPU, discuss the complete flow in detail using RISC architecture? For the given scenario, draw an architectural diagram as well. [10]

2. (i) In a hardware designing company, a manager assigned his team to perform Binary Floating-Point addition using IEEE 754 single precision format on the following numbers $(198.31)_{10}$ and $(87.346)_{10}$. Your task is to help the team to compute the various intermediate steps to perform the addition operation to produce the result. (7 Marks) [10]
(ii) Represent the final result in single precision floating point format for the problem mentioned in Question 2. section (i). (3 Marks)

3. Multiply $(-23)_{10}$ x $(-7)_{10}$ using Booth's Algorithm. [10]
i) Determine the value of the Accumulator at the end of the second step? (3 Marks)
ii) Write down all the steps needed for computation in each iteration and determine the value in the Accumulator and Q register in the final step? (7 Marks)

4. Write the sequence of control steps required to execute each of the instructions given below using a single bus structure. [10]
(i) Add R1, #6. (3 marks)
(ii) Mul R1, (2090). (3 marks)
(iii) Move the contents of the memory location whose address is at memory location NUM to register R1. (4 marks)

5. Consider that two processors are implemented on the same instruction set architecture. The instructions are divided into four classes according to their CPI namely class A, B, C, and D. Processor P1 has a clock rate of 2.5 GHz with the CPI values of 1, 2, 3, and 3 for different classes of instructions, and Processor P2 has a clock rate of 3 GHz with the CPI values of 2, 2, 2, and 2 for different classes of instructions. Given a program with a dynamic instruction count of 1 million instructions which are divided into four classes namely 10% of class A, 20% of class B, 50% of class C, and 20% of class D. Compute the following: [10]
(i) Which processor implementation is faster? (2 Marks)
(ii) What is the global CPI for each implementation? (4 Marks)
(iii) Find the clock cycles required in both cases. (4 Marks)

6. Consider a computer with the following characteristics: Main memory consists of 1Mbyte; Word size is of 1 byte; Block size is of 16 bytes; The cache size is of 64 Kbytes. [10]

(i) For the main memory addresses of F0010, 01234, and CABBE, give the corresponding tag, cache line address, and word offsets for a direct-mapped cache. (3 Marks)

(ii) Give any two main memory addresses with different tags that map to the same cache slot for a direct-mapped cache. (2 Marks)

(iii) For the main memory addresses of F0010 and CABBE, give the corresponding tag and offset values for a fully-associative cache. (2 Marks)

(iv) For the main memory addresses of F0010 and CABBE, give the corresponding tag, cache set, and offset values for a two-way set-associative cache. (3 Marks)

7. (i) A Processor needs to transfer a file from a peripheral storage to the memory. During the I/O operation, the processor, main memory and I/O share a common bus. Suggest a suitable I/O technique for the above operation and explain its working in detail. (6 Marks) **[10]**

(ii) With a neat sketch, identify and explain the methodology for connecting multiple devices that can receive acknowledgments in a serial manner. (4 Marks)

8. You want to store the following data $(1735)_{10}$ in a 12-bit binary format at the address location 1345H in the memory. Ensure that data is stored and retrieved correctly. Determine the code generated for the given data and store it in the specified location. When the stored data is accessed from the same location after some time it is read as $(1223)_{10}$. **[10]**

a) Draw the diagram of error correcting code function and discuss those results in detail. (3 Marks)

b) Draw the layout of data bits and check bits. (3 Marks)

c) Using SEC code, show the steps involved in error detection and correction for the above scenario. (4 Marks)

9. Infy operational data center requires a solution to recover their critical data disks from abrupt failures and disasters. **[10]**

(i) Suggest at least three generalized solutions to this problem and justify that it increases the reliability of the system too. (4 marks)

(ii) If Infy focuses on providing highest level of fault tolerance to a single disk drive, then which level of the above technique would you recommend? (3 marks)

(iii) Which level of the above technique does Infy follow if they want to strip data at a block level across several drives with parity stored on one drive? (3 marks)

10. (i) Consider the following Assembly language code: **[10]**

I1 : ADD R5, R2, R3

I2 : SUB R4, R5, R2

When the above assembly language program is executed in a pipelined processor, Identify which type of dependency exists and also discuss the hazards encountered and provide solutions to overcome the hazard. (7 Marks)

(ii) Assume a 5-stage instruction cycle. Find out the speedup achieved if a set of 25 instructions is run on a processor without pipelining. (3 Marks)

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