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VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test II – October 2022

Programme	:	**B.Tech (CSE, AI/ML, CPS, AIR)**	Semester	:	**Fall 2022-23**
Course Code	:	**BCSE 205L**	Class Number	:	**CH2022231001507, CH2022231001510, CH2022231001511, CH2022231001512, CH2022231001513, CH2022231001514, CH2022231001515**
Course Title	:	**Computer Architecture and Organization**	Slot	:	**B2+TB2**
Faculty	:	**Dr.Rama Prabha , Dr. Aswiga, Prof.Nivedita, Dr. Bhanu Chander Balusa, Dr.Anushiya Rachel, Dr. Sambasivarao, Dr A.K. Ilavarasi**			
Time	:	**1½ Hours**	Max. Marks	:	**50**

Answer ALL Questions

Q. No.	Question Text	Marks
1.	For a 64-bit machine describe how the processor fetches the instruction Add R1, R2 from the memory location 2044 (which is represented in hexadecimal) and executes it. Explain the role of different registers and buses involved during the instruction fetch and execution cycle and write down the values of MAR, MDR, IR and PC while the instruction is being fetched and executed considering each instruction is 64-bit long. Also draw the architectural diagram for the above scenario.	**10**
2.	Consider the following expression below and write the assembly language code by listing out all the possible sequence using 2 - address, 1-address and 0 -address instruction formats. $$Y = \frac{A + (B \times C)}{D - E + F}$$	**10**
3.	i) In order to implement the instruction given below, you are asked to design a single bus data path architecture and describe the sequence of steps needed to perform the operation. Also indicate the control signals required for the micro operations at each timing signal or clock cycle for the given instruction. (Note: 2000 is the effective address of the operand.)(5 Marks) Instruction : SUB R1, 2000	**10**

	ii) In order to implement the instruction given below, you are asked to design a Multi bus data path architecture and describe the sequence of steps needed to perform the operation. Also indicate the control signals required for the micro operations at each timing signal or clock cycle for the given instruction. (5 Marks) Instruction : DIV R1, (R2)	
4.	The series of address references given as addresses are 6, 2, 2, 6, 8, 8, 2, 4, 2, 4, 6, 8, 6, and 4. Label each reference in the list as a hit or a miss and show the final contents of the cache for a. A direct mapped cache that is initially empty (3 Marks) b. Fully associative cache that is initially empty. (4 Marks) c. Four way set associative cache that is initially empty. (3 Marks) Assume that all these cache memories have eight one-word cache lines	**10**
5.	Assume that processor in your PC generates a 32 bit address for each request. The capacity of the cache memory is 8KB of data and the block size is of 8 words. Assume one word is equal to 4 bytes. a) Find the number of bits required to represent cache line index and tag for the given 32-bit address using directed mapping. (3 Marks) b) Find the number of bits required to represent tag for the given 32-bit address using fully associative mapping. (4 Marks) c) Find the number of bits required to represent tag for the given 32-bit address using 2 way set associative mapping.(3 Marks)	**10**