VIT Reg. No. :

**Final Assessment Test (FAT) – November/December 2022**

| Programme | B.Tech. | Semester | Fall Semester 2022-23 |
|---|---|---|---|
| Course Title | COMPUTER ARCHITECTURE AND ORGANIZATION | Course Code | BCSE205L |
| Faculty Name | Prof. Punitha K | Slot | C1+TC1 |
| | | Class Nbr | CH2022231001232 |
| Time | 3 Hours | Max. Marks | 100 |

**section 1 (10 X 10 Marks)**
**Answer All questions**

1. i) Compare the features of CISC and RISC architectures in terms of the instruction set, instruction formats and lengths, and addressing modes. [5 Marks] [10]
   ii) While implementing a business application architecture how well you can solve the problems in recent trends using the benefits of CISC and RISC architectures? [ 5 Marks]
2. i. Perform the Non-Restoring Division Method and illustrate the step-by-step process for dividing $(22)_{10}$ by $(8)_{10}$, using the Non-Restoring Division Method. [7 Marks] [10]
   ii. Find the decimal equivalent of the content of the accumulator at the end of the third iteration. [3 Marks]
3. Use *IEEE - 754* standard floating point representation to convert: [10]
   i. $(-15.5625)_{10}$ into double precision floating point format [5 marks]
   ii. Half precision floating point $(1101111101000000)_2$ into decimal equivalent [5 marks]
4. Consider the memory details given below : [10]

| Address | Value |
|---|---|
| 4000 | 1000 |
| 4100 | 1100 |
| 4200 | 4000 |
| 4220 | 2500 |
| 4300 | 3000 |
| 4500 | 4200 |
| 4600 | 4220 |

Compute the effective address and operand value for the following instructions.

i) LDA #4000
ii) LDA 4100
iii) LDA (4200)
iv) MOV R1, 50[PC]
v) LDA (R1)

Assume that the initial values of the register R1= 4100, R2=3000, PC=4250.

5. i. Elucidate the step-wise execution of the following instructions in the Single Cycle Data Path architectural design **[5 marks]** **[10]**

**LDA (R2)**
**MUL R1**
**STA R2**

ii. Write down the micro routine control sequence steps involved in the architecture with respect to the given instructions in 5. (i). **[5 marks]**

6. A cache contains a total of 12 blocks. The main memory block requests are as follows: **[10]**

129, 55, 8, 4, 13, 8, 132, 129, 212, 129, 64, 8, 48, 32, 8, 92

Calculate the number of misses and the miss ratio if Least Recently Used (LRU) is used to replace the cache in case of a miss for the following cache mapping techniques:

i. 4-way set associative cache mapping **[5 marks]**

ii. Direct mapping **[5 marks]**

7. The CPU speed of a microprocessor works at 4MIPS. The data transfer from the peripheral devices to the main memory in this microprocessor happens at a rate of $3\times10^3$ bits per second. **[10]**

i. Suggest a suitable I/O technique for bulk data transfer with the minor intervention of the processor and explain in detail with a neat timing diagram. **[5 marks]**

ii. Identify the technique and the steps involved in the given scenario where the CPU gets back control of the bus after each word is transferred. **[5 marks]**

8. i. Consider a hamming code with 12-bits 100110010111. Validate this code, and justify your answer with a proper explanation. **[5 Marks]** **[10]**

ii. Suppose, if the hamming code has 7-bits and the parity value for the data value 0010 is 101. Please identify a code word that has the complementary parity value of 010. **[5 Marks]**

9. i. If you can combine two or more standard RAID levels to ensure better performance and redundancy, which RAID levels will you prefer to design a hybrid RAID level? Why? Illustrate this hybrid RAID levels implementation and explain its advantages in detail. **[8 Marks]** **[10]**

ii. Explain how Hybrid RAID is named after the RAID levels are incorporated. **[2 Marks]**

10. i. A clustering algorithm running on Amazon Data Centre consists of 80% inherently parallel computation. Identify the minimum number of processors that Amazon should procure to achieve a speed-up of 2.5. What is the maximum speed-up that can be attained by this system? **[5 marks]** **[10]**

ii. Consider the following sequence of instructions executed in a processor using pipeline architecture

[1]:ADD R13, R11, R17

[2]:OR R12, R13, (R19)

Identify the specific type of data hazard with proper justification. Mention all the steps available to eliminate this hazard. **[5 marks]**