VIT

Reg. No. :

Final Assessment Test (FAT) - APRIL/MAY 2023

Programme	**B.Tech**	Semester	**Winter Semester 2022-23**
Course Title	**COMPILER DESIGN**	Course Code	**BCSE307L**
Faculty Name	**Prof. Mercy Rajaselvi Beaulah P**	Slot	C1+TC1
		Class Nbr	**CH2022235000216**
Time	**3 Hours**	Max. Marks	**100**

Section 1 (7 X 10 Marks)

Answer All questions

01. Assume that you are involved in designing different phases of a compiler for a language that has the following specifications: [10]

Tokens:

Keywords → float, print, if, else, input, range

Operator → arithmetic (+,-,*,/) Relational (<=, <, >, >=, ==, !=)

Constants → Integer, float, string

Variables → starting with uppercase alphabet followed by one or more numbers or lowercase alphabets

Punctuation symbols → comma(,), colon(:), parathesis ((,)), brackets ([,])

Write a regular expression to represent all the token formats supported by the language.

02. Draw deterministic finite automata to recognize the keywords and variables of the language given in Question 01. Show simulation for the strings, "print" and "A3r". [10]

03. Write a Context Free Grammar to represent the following syntax: [10]

```
while varname in range (init, final, [step]):
 {
  print("Welcome");
  Block;
 }
```

Note:

- While, in, range, print are keywords
- Block is having only arithmetic expressions
- Varname, init, final, step are variables

04. Construct an LL(1) parsing table for the given grammar [10]

S → transaction "EOF"

transaction → deposit | withdrawal | transfer

deposit → "DEPOSIT" amount

withdrawal → "WITHDRAW" amount

transfer → "TRANSFER" amount "TO" account

amount → "$" digits "." digits

account → digits

digits → digit | digit digits

digit → "0" | "1" | "2" | "3" | "4" | "5" | "6" | "7" | "8" | "9"

05. Assume that You are designing a compiler for a new programming language called "VITLang" Your compiler will generate machine code for a hypothetical processor architecture which supports parallelism called "VITArch". You have completed the front-end of the compiler (lexical analysis, syntax analysis, and semantic analysis), and now you are working on the code generation phase. Describe the steps you would take to generate machine code for the "VITLang" programming language on the "VITArch" processor architecture. Discuss the challenges you may encounter during the code generation phase and how you would overcome them. **[10]**

06. You are required to design a code generator for a programming language that generates assembly code for a hypothetical target machine. Discuss the following aspects of your code generator design: **[10]**

(i)Explain the importance of considering the target machine architecture during code generation and describe some of the major design decisions you made with regard to the target machine in your code generator. (3 marks)

(ii)Discuss the use of next-use information in register allocation and assignment and explain how it helps to improve the efficiency of the generated code. Provide an example to illustrate your explanation. (3 marks)

(iii)Explain the concept of runtime organization and the role of activation records in managing the runtime environment. Describe the layout and contents of an activation record and discuss how it is used during function calls and returns. (4 marks) **[10]**

07. Consider the following grammar G:

$S \rightarrow A \mid B$

$A \rightarrow aAb \mid C$

$B \rightarrow bBb \mid C$

$C \rightarrow pqrW$

$W \rightarrow d$

(i) Construct SLR(1) parsing table for G. (8 marks)

(ii) Show the stack status, input and shift/reduce action used for parsing the string "apqrdb" (2 marks)

Section 2 (2 X 15 Marks)
Answer All questions

08. (i) Convert the following piece of code into three address codes. Construct basic blocks. flowgraph for the code written by you. (10 marks) **[15]**

```
for (i = 0;i < k; i++)
    {
     for (j = 0 ;j < k; j++)
       {
        b[i][j] = 0;
        if(i != 0 && j != c)
         {
          b[m][n] = a[i][j];
         }
       }
    }
```