VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

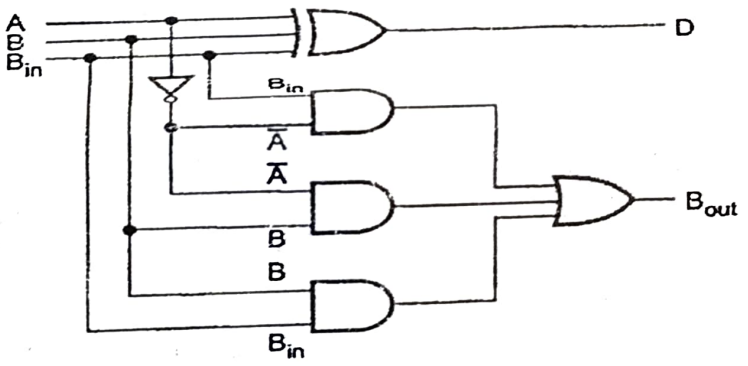
Continuous Assessment Test I – September 2023

Programme	:	**B.Tech.(ECE/ECM)**	Semester	:	**FALL 2023-24**
Course	:	**DIGITAL SYSTEM DESIGN**	Code	:	**BECE102L**
			Class Nbr	:	**CH2023240100538, CH2023240100368, CH2023240100369, CH2023240100535 CH2023240100365**
Faculty	:	**Dr Gargi Raina, Dr K Chitra, Dr B Lakshmi, Dr A Prathiba, Dr Jenifer**	Slot	:	**B1+TB1**
Time	:	**90 Minutes**	Max. Marks	:	**50**

Answer ALL the questions

Q. No.	Sub. Sec.	Question Description	Marks
1	a)	Simplify the Boolean expression $\overline{\overline{A\bar{B} + ABC + A(B + A\bar{B})}}$	[4]
	b)	Using K-map, simplify the following Boolean function and obtain i) minimal SOP and (ii) minimal POS expressions: $F = \sum_m(0, 2, 3, 6, 7) + \sum_d(8, 10, 11, 15)$	[6]
2	a)	The output of a circuit is 1 if a majority (more than half) of its inputs are equal to 1, and the output is 0 otherwise. Construct a truth table for a three-input majority circuit and design the circuit with NOR gates only	[6]
	b)	Construct the following logic expression using CMOS logic. $F = \overline{(A + B + C).D}$	[4]
3	a)	Specify the number of registers and the number of bits per register in the following statement: reg [0:7] name [0:4];	[1]

	b)	Find the output of the test bench shown
		
		`//dataflow half_adder test bench module`
		`half_adder_df_tb;`
		`reg a, b;`
		`wire sum, cout;`
		`initial`
		`$monitor ("ab = %b, sum = %b, cout = %b", {a, b}, sum, cout);`
		`initial`
		`begin`
		`#10 a = 1'b0;`
		`b = 1'b0;`
		`#10 a = 1'b0;`
		`b = 1'b1;`
		`#10 a = 1'b1;`
		`b = 1'b0;`
		`#10 a = 1'b1;`
		`b = 1'b1;`
		`#10 $stop;`
		`end`
		`half_adder_df inst1 ( .a(a), .b(b), .sum(sum), .cout(cout) );`
		`endmodule`
			[5]

	c)	Write a Verilog HDL code for the schematic shown  	[4]
4	a)	Assume that the exclusive-OR gate has a propagation delay of 10 ns and that the AND/OR gates have a propagation delay of 5 ns. What is the total propagation delay time for the full adder circuit? Draw the circuit used for calculation	[3]
	b)	Draw the logic diagram of a 2-to-4-line decoder using universal NAND gates. Include an enable input.	[2]
	c)	Implement the following Boolean function with a 4 X 1 multiplexer and external gates. F1 (A, B, C, D) = $\sum$ (1, 3, 4, 11, 12, 13, 14, 15)	[5]
5.		Design a 4-input priority encoder and simulate the same using Verilog code with gate primitives. Assume that input D3 has the highest priority	[10]
			Total [50]