Reg. No.:

Name :

VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

**Continuous Assessment Test (CAT-2) – May 2023**

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| Programme | : | **B.Tech (CSE)** | Semester | : | **Winter 2022-2023** |
| | | | Code | : | **BECE102L** |
| Course | : | **Digital System Design** | Class Nbr | : | **CH2022232300522 CH2022232300543 CH2022232300532 CH2022232300556 CH2022232300195 CH2022232300524** |
| Faculty | : | **Dr.Nithya Venkatesan, Dr.B.Sri Revathi, Dr.G.Kanimozhi, Dr.S.Angalaeswari, Dr.Ravi Tiwari, Prof. Mohammed Aneesh** | Slot | : | **B2+TB2** |
| Time | : | **90 minutes** | Max. Marks | : | **50** |

Answer **ALL** the Questions

| S.No. | Question Description | Marks |
|---|---|---|
| 1. | Perform multiplication of (20) x (-19) using Booth's Multiplication algorithm. Also find out the number of additions, number of subtractions and number of arithmetic shifts required. | [10] |
| 2. | Perform multiplication of $(1010)_2$ x $(101)_2$ using unsigned array multiplier and draw equivalent logic diagram of 4 x 3 Multiplier. | [10] |
| 3. | Consider a simple human counter system for an elevator overload indication in which the number of persons entering the elevator is detected by an IR sensor. By default, it must display value '0' and increment the number on the display by one each time a human enters the elevator. Assume the maximum capacity of the elevator is 9 persons and if it exceeds the count of 9, there will be an alarm sound to indicate the overload condition and reset the counter. Draw state diagram and design an appropriate control circuit which performs increment operation using T-Flip flop and explain each state in detail. | [10] |
| 4. | Design a synchronous counter which can count the random state sequence as 001,100,011,101,111,110,010,001... using JK flip flops.<br>a) Draw the state diagram. (2 marks)<br>b) Draw the state table and excitation table. (2 marks)<br>c) Draw the required K Maps and find the expression. (4 marks)<br>d) Draw the logic diagram of the given counter. (2 marks) | [10] |

5. A sequential circuit has three D flip-flops with outputs as A, B, and C and one input, $x$. It is described by the following flip-flop input functions: [10]

$$D_A = (BC' + B'C)x + (BC + B'C')x'$$

$$D_B = A$$

$$D_c = B$$

(a) Draw the logic diagram of the above function. (3 marks)

(b) Derive the state table for the circuit. (3 marks)

(c) Draw two state diagrams: one for $x = 0$ and the other for $x = 1$. (4 marks)

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