VIT
Vellore Institute of Technology

Reg. No. : 21BPS1279

Final Assessment Test (FAT) – November/December 2022

Programme	B.Tech.	Semester	Fall Semester 2022-23
Course Title	DIGITAL SYSTEMS DESIGN	Course Code	BECE102L
Faculty Name	Prof. Vipul Dixit	Slot	E2+TE2
		Class Nbr	CH2022231001878
Time	3 Hours	Max. Marks	100

Section I (4 X 15 Marks)
Answer All questions

1. A) A bank vault has three locks with a key for each lock. Key A is owned by the bank manager. Key B is owned by the senior bank teller. Key C is owned by the trainee bank teller. In order to open the vault door at least two people must insert their keys into the assigned locks at the same time. The trainee bank teller can open the vault only if the bank manager is also involved in opening the vault. [15]
   i) Determine the truth table.
   ii) Find the simplified expression using K-Map.
   iii) Obtain the logic circuit using AND-OR gate.
   iv) Convert the obtained circuit to its NAND equivalent gates. (10 marks)
   B) (i) Simplify the Boolean function to minimum number of literals.
   xy+x(wz+wz') (2.5 Marks)
   (ii) Find the complement of xy'+x'y (2.5 Marks)
2. (i) Discuss any four lexical conventions of a Verilog module. (3) [15]
   (ii) Write the Verilog code for 2:4 decoder in data flow modeling and behavioral modeling (6)
   (iii) Write the test bench program for the code written in (ii). (3)
   (iv) Discuss the difference between data-flow and behavioral of modeling (3)
3. A) Design a 3-bit X 2-bit unsigned multiplier and write the Verilog code to realize it using structural modeling.(10 Marks) [15]
   B) Discuss the concept of an adder whose carry propagation delays are eliminated. Draw its block diagram. (5 Marks)
4. A) Design a synchronous counter which counts the state sequence as 000, 001, 010,101,111, using J K flip-flops. [15]
   i) How many flip-flops are required for designing this counter? (1 Marks)
   ii) Draw the state diagram. (1 Marks)
   iii) Draw the state table. (1Marks)
   iv) Write the excitation inputs for the JK flip flops. (2 Marks)
   v) Draw the required K-maps. (2 Marks)
   vi) Draw the circuit diagram of the given counter. (3)
   B) The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 011100. What is the content of the register after each shift? Draw the circuit diagram of the 4-bit shift register. (5 Marks)

Section II (1 X 20 Marks)
Answer All questions

5. A) Implement a full adder using two 4:1 Mux (5 marks) [20]

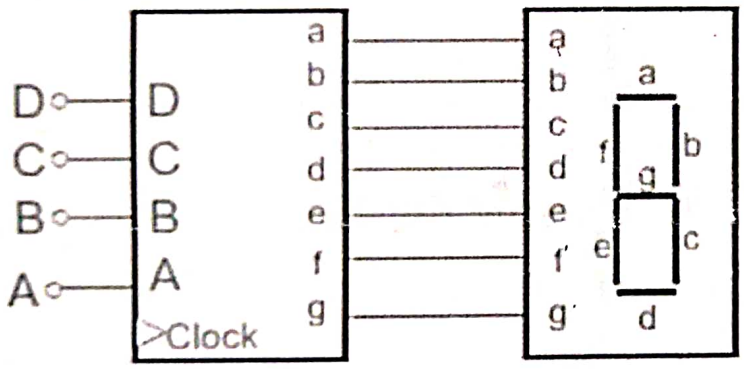
B) A customized priority encoder is defined in the table below: show the simplified NAND-NAND circuit corresponding to such a priority encoder. (10 marks)

Inputs				Outputs		
EN	RI_2	RI_1	RI_0	Y_1	Y_0	RO
0	X	X	X	0	0	0
1	1	X	X	1	0	1
1	0	1	X	0	1	1
1	0	0	1	1	1	1
1	0	0	0	0	0	0

C) A. BCD to seven-segment decoder has four input lines (A, B, C, and D) and 7 output lines (a, b, c, d, e, f, and g). This output is given to seven segment LED display which displays the decimal number depending upon inputs. A segment glows if it is supplied with logic '1'.

Write a Verilog code for BCD to 7-segment decoder using behavioural modeling (hint:use case statement).

The figures below are given for your understanding. (5 marks)



BCD to 7 Segment Decoder

7- Segment LED Display

(a) Segment designation

(b) Numerical designation for display

Section III (2 X 10 Marks)
Answer All questions

6. A sequence detector accepts as input a string of bits: either 0 or 1. Its output goes to 1 when a target sequence has been detected. Design a serial sequence detector that allows 'no-overlapping' and detects the pattern "0101" . Use D flip-flops for your design. [10]

7. Implement the following Boolean functions using Programmable devices. [10]
   a. $F_1(A,B,C) = \Sigma m(1,2,4,5,7)$ using PLA (5 marks)
   b. $F_2(A,B,C) = \Sigma m(0,1,3,5,7)$ using PAL (5 marks)

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