Reg. No.:

Name :

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Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test (CAT-1) – March 2023

Programme	:	**B.Tech (CSE)**	Semester	:	**Winter 2022-2023**
			Code	:	**BECE102L**
Course	:	**Digital System Design**	Class Nbr	:	**CH2022232300522 CH2022232300543 CH2022232300532, CH2022232300556, CH2022232300195, CH2022232300524**
Faculty	:	**Dr.Nithya Venkatesan, Dr.B.Sri Revathi, Dr.G.Kanimozhi, Dr.S.Angalaeswari, Dr.Ravi Tiwari, Prof. Mohammed Aneesh**	Slot	:	**B2+TB2**
Time	:	**90 minutes**	Max. Marks	:	**50**

Answer **Any 5** of the following Questions

S.No.	Question Description	Marks
1.	An assembly line has 3 fail safe sensors and one emergency shutdown switch. The line should keep moving unless any of the following conditions arise: (i) If the emergency switch is pressed (ii) If the sensor1 and sensor2 are activated at the same time. (iii) If sensor 2 and sensor3 are activated at the same time. (iv) If all the sensors are activated at the same time Draw the truth table and implement a combinational circuit for the above case using only NAND gates. How many minimum number of 2 input NAND gates are required?	[10]
2.	A combinational circuit has 3 inputs A, B, C and output F. F is true for following input combinations A is False, B is True A is False, C is True A, B, C are False A, B, C are True (i) Write the Truth table for F. Use the convention True=1 and False = 0. (ii) Write the simplified expression for F in SOP form.	[10]

(iii) Write the simplified expression for F in POS form.

(iv) Draw logic circuit using minimum number of 2-input NOR gates.

3. Design and implement a full subtractor in Verilog using gate level modeling. Draw necessary truth table and logic diagrams. [10]

4. Implement the function F (A,B,C,D) = Σm(2,3,4,5,6,7) using a decoder without using OR gates. [10]

5. Implement a full adder using two 4×1 multiplexers. Draw the truth table and necessary k-maps. [10]

6. Reduce the following expression using K map both in SOP and POS and implement them using basic gates. Comment which simplification uses the minimum number of gates. [10]
F = Σm(0,1,2,8,9,10,11,13,14,15).