VIT

Vellore Institute of Technology

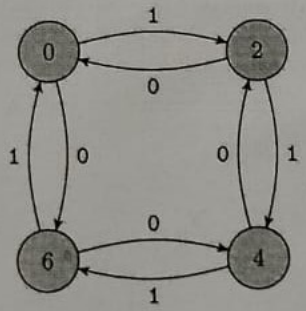
(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test II - May 2023

Programme	:	B.Tech CSE	Semester	:	Winter 2022-23
Course	:	Digital System Design	Code	:	BECE102L
Faculty	:	A. Mohamed Imran	Slot	:	B1+TB1
			Class Number	:	CH2022232300550
Time	:	$1\frac{1}{2}$ Hours	Max. Marks	:	50

Answer ALL Questions

1. Design a sequential circuit using JK Flip Flop that implements the state diagram shown below.
   (a) Using binary assignment for the states, obtain the state table. (6)
   (b) Find combinational circuit required for the inputs of the flip flops using k-maps. (6)
   (c) Draw the sequential circuit. (3)



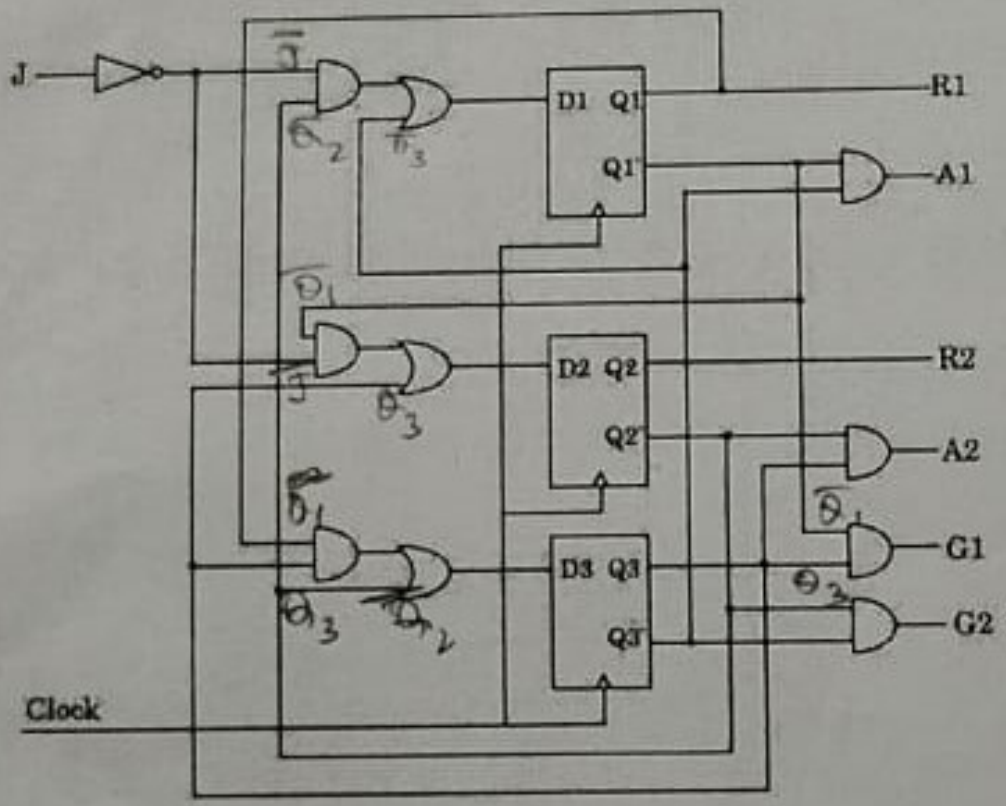
2. Design a asynchronous counter that counts 0,1,2,3 using D Flip Flop.
   (a) Draw the state table and the circuit required to implement the counter. (6)
   (b) Verify the output using a timing diagram. (6)
   (c) If the clock frequency is 64 kHz intially, what will be clock frequency for all other flip flops in the design. (3)

3. A serial input is sensed for a pattern 10011. Draw the state diagram to design a finite state machine using

   (a) Moore Model and Overlapping bit pattern. (5)

   (b) Mealy Model and Non-Overlapping bit pattern. (5)

4. Derive the state table and the state diagram of the sequential circuit shown below, where J is the input and $R_1, R_2, A_1, A_2, G_1, G_2$ are the outputs. Consider only G_1 as the output for building the state table and state diagram. (10)



$$D_1 = (\bar{J} \cdot \bar{Q}_2) + \bar{Q}_3$$

$$D_2 = (\bar{J} \cdot \bar{Q}_1) + Q_3$$

$$D_3 = (Q_1 \cdot Q_3) + \bar{Q}_2$$

$$G_1 = \bar{Q}_1 \cdot Q_3$$