VIT

Reg. No. : 22BPS1081

Final Assessment Test (FAT) - JUNE/JULY 2023

Programme	B.Tech.	Semester	Winter Semester 2022-23
Course Title	DIGITAL SYSTEMS DESIGN	Course Code	BECE102L
Faculty Name	Prof. Mohamed Imran A	Slot	B1+TB1
		Class Nbr	CH2022232300550
Time	3 Hours	Max. Marks	100

Section I (7 X 10 Marks)
Answer All questions

01. For the given Boolean function, [10]

$F(W, X, Y, Z) = X\bar{Y}Z + \bar{X}\bar{Y}Z + \bar{W}XY + W\bar{X}\bar{Y} + WXY$

(a) Obtain the truth table of F and represent the function with minterms.

(b) Use Boolean algebra to simplify the function and realize the circuit using NAND gates

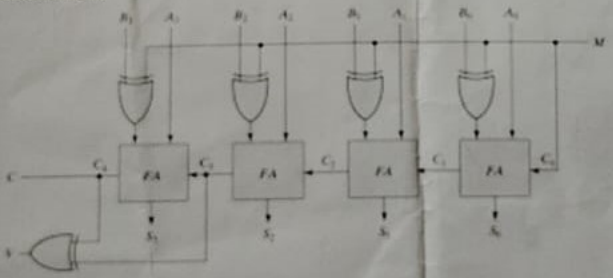
(c) Write a Verilog code to implement the function using structural modelling.

02. Design a combinational circuit to generate EVEN parity and ODD parity. Write the truth table with $(ABCD)$ as inputs and X(Even) , Y (Odd) as outputs. [10]

(a) Implement the output X using 4×1 multiplexer.

(b) Implement the output Y using 3×8 decoder.

03. Comprehend the circuit shown below and find the outputs $(S_3S_2S_1S_0)$, C and V for $M = 0$ and $M = 1$. Assume $A = +6$ and $B = +4$. What does V indicate? Validate your answer with the calculations. [10]



04. (a) The sequence 1011 is applied to the input of a 4bit shift register(SISO) that is initially cleared. What is the state of the shift register after three clock pulses?Explain with timing diagram/table. [10]

(b) Draw the output states of each flipflop for the data signal given below

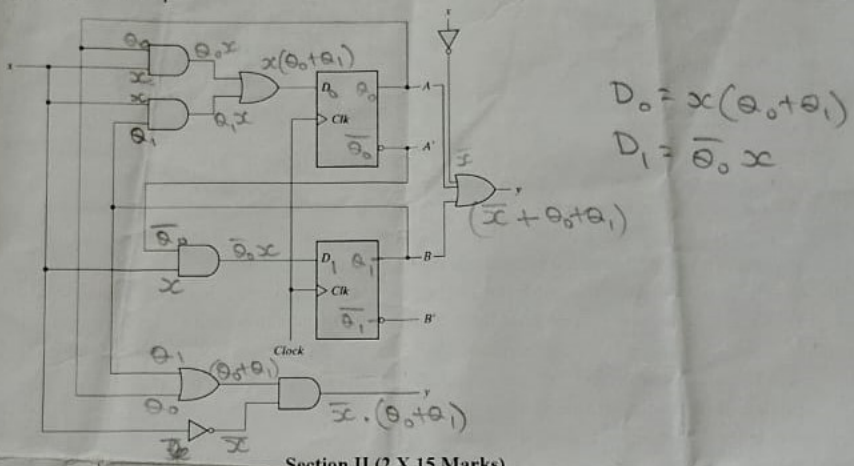
05. Design and draw the state diagram of a FSM to detect two sequences 1010 and 110 for the following cases: [10]

(a) Mealy model with overlapping states

(b) Moore model with non overlapping states.

06. Design an modulo 8 asynchronous counter using negative edge triggered JK Flip Flop [10]
(a) the counter should count with a truncated sequence 2,3,4,5,6.
(b) draw the timing diagram and verify the output.

07. Derive the state table and the state diagram of the sequential circuit shown below, where x is the input and y is the output. [10]



Section II (2 X 15 Marks)
Answer ALL questions

08. The arithmetic operation $C = A * B$ is performed on a digital system. [15]
(a) Tabulate the calculation steps using Booth Algorithm, if $A = +5$ and $B = -4$
(b) Write the Verilog code for implementing the same operation with Array Multiplier using dataflow modelling.

09. Implement the combinational circuit [15]
$F1(W,X,Y,Z) = \sum(2,12,13)$,
$F2(W,X,Y,Z) = \sum(7,8,9,10,11,12,13,14,15)$,
$F3(W,X,Y,Z) = \sum(0,2,3,4,5,6,7,8,10,11,15)$,
$F4(W,X,Y,Z) = \sum(1,2,8,12,13)$
(a) using Programmable Logic Array (PLA).
(b) using Programmable Array Logic (PAL).