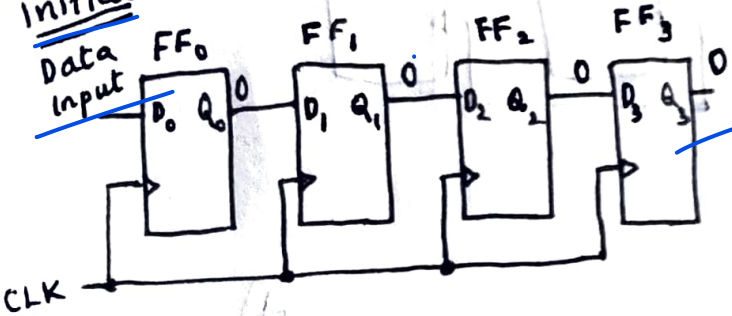
Shift Registers

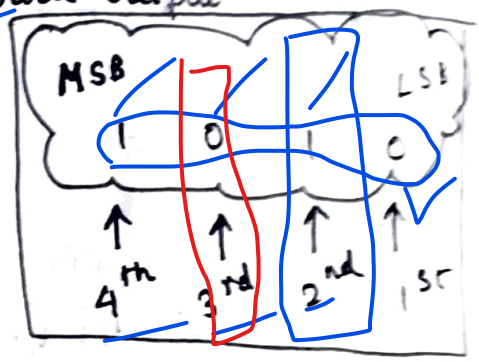
SISO:

Example : If 1010 is applied.

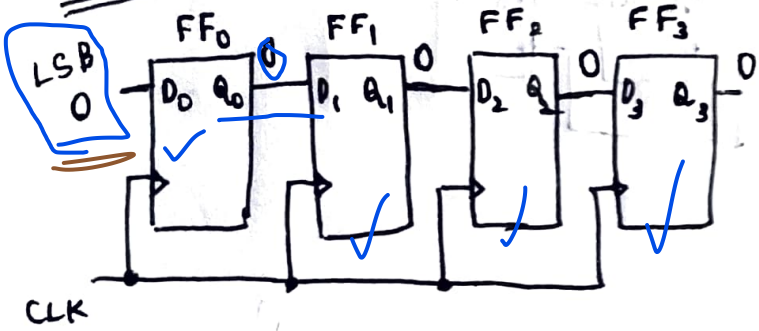
Initial



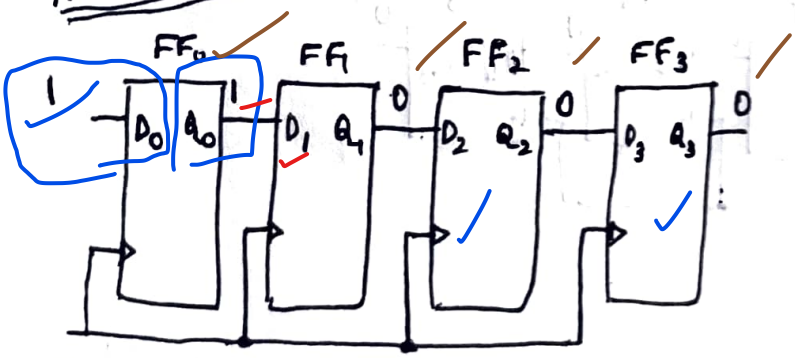
2N-1



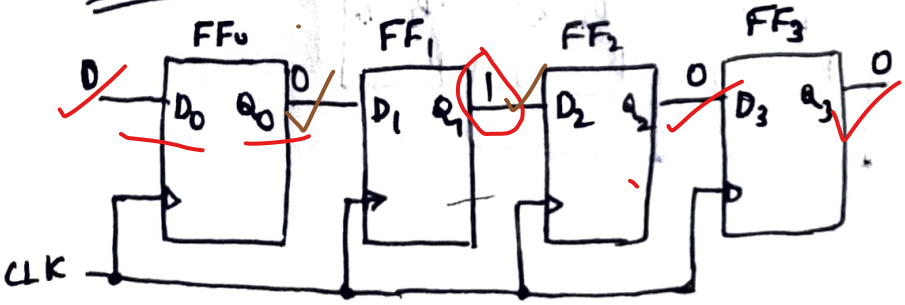
After CLK1



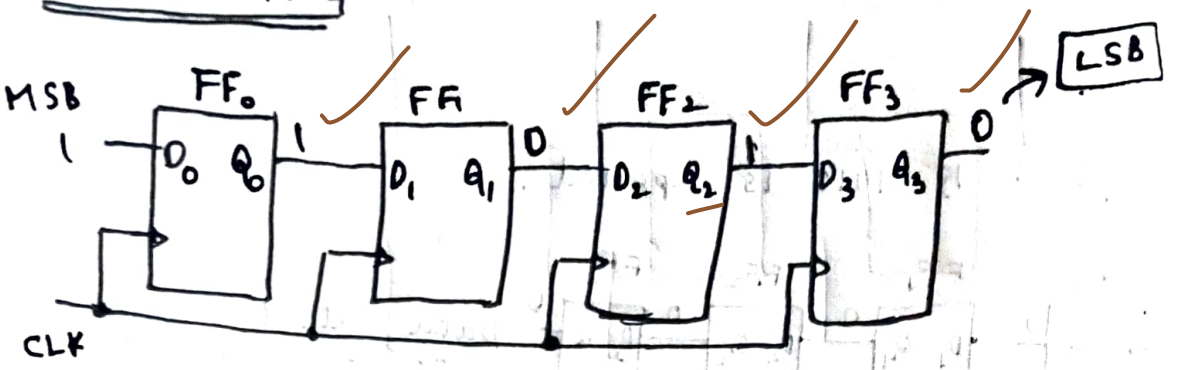
After CLK 2:



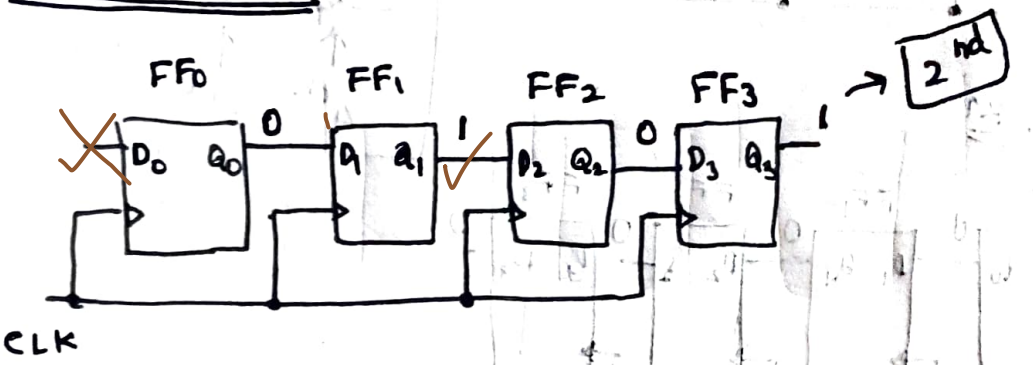
After CLK 3:



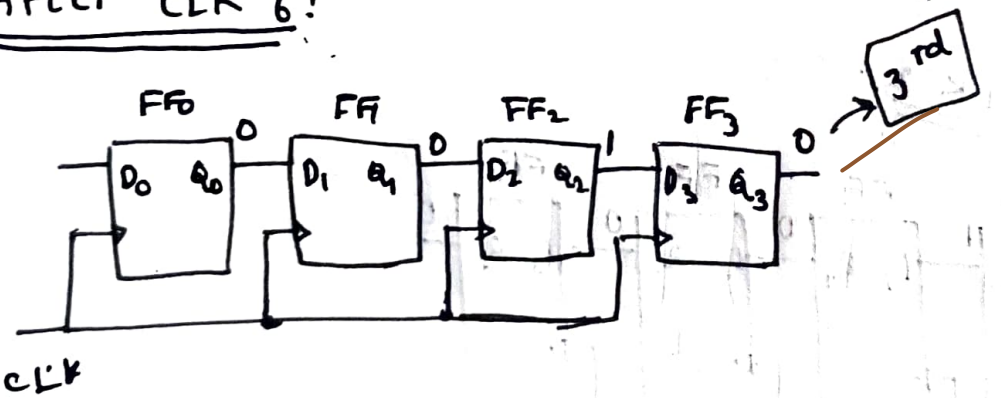
After CLK 4 :



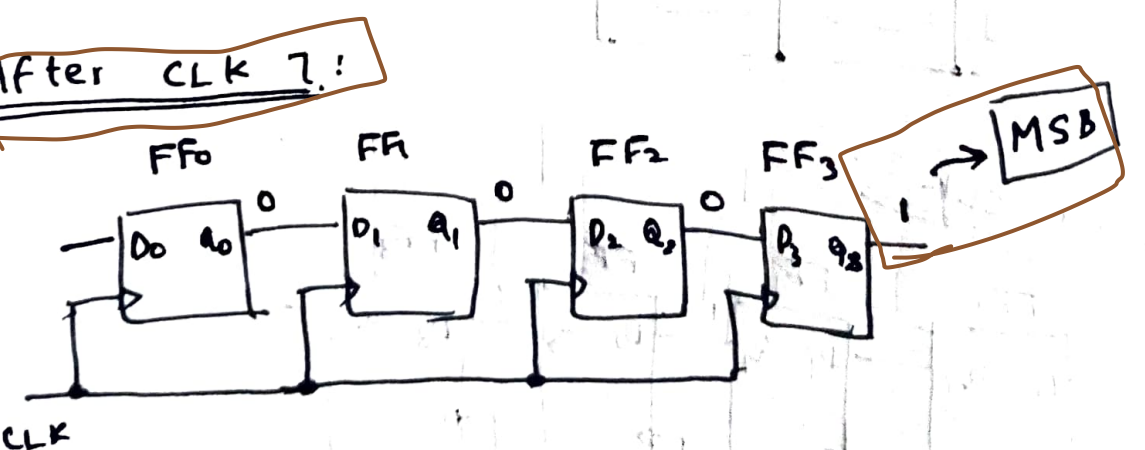
After CLK 5 :



After CLK 6 :



After CLK 7 :



N - bit SISO S.R (shift register) need 2N-1 clock pulse

4 - bit Need 2(4) - 1 = 7 clock pulse.

Table:

No. of positive edge of clock	Serial Input	Q_0	Q_1	Q_2	Q_3
0 (Initial)	-	0	0	0	0
1	D (LSB)	0	0	0	0
2	1	1	0	0	0
3	0	0	1	0	0
4	1 (MSB)	1	0	1	0
5	-	-	1	0	1
6	-	-	-	1	0
7	-	-	-	-	1

input in serial form

0 (LSB), 1, 0, 1 (MSB)

1010

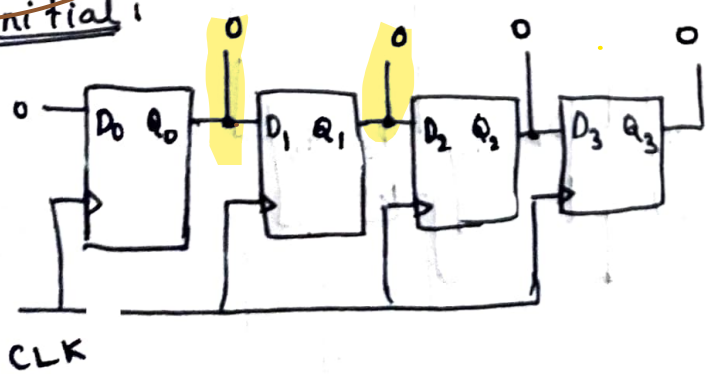
1010

output also in serial form.

SIPO:

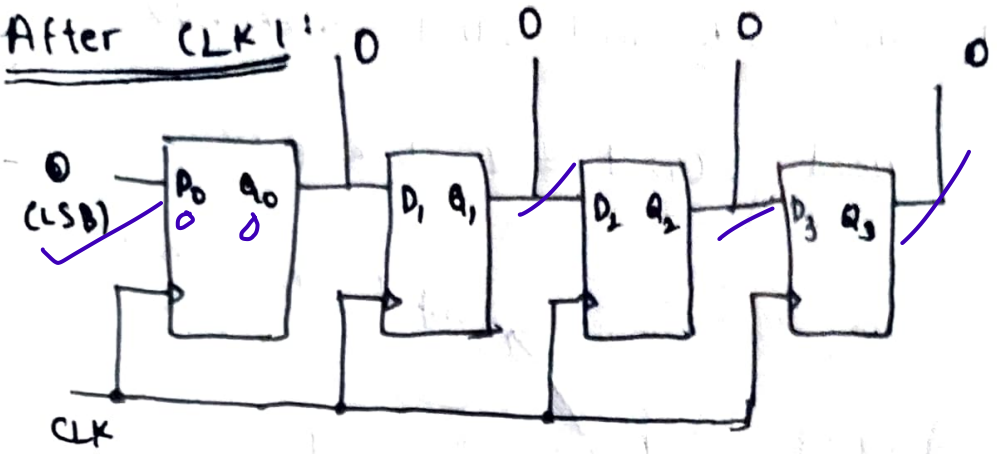
Initial:

- is applied

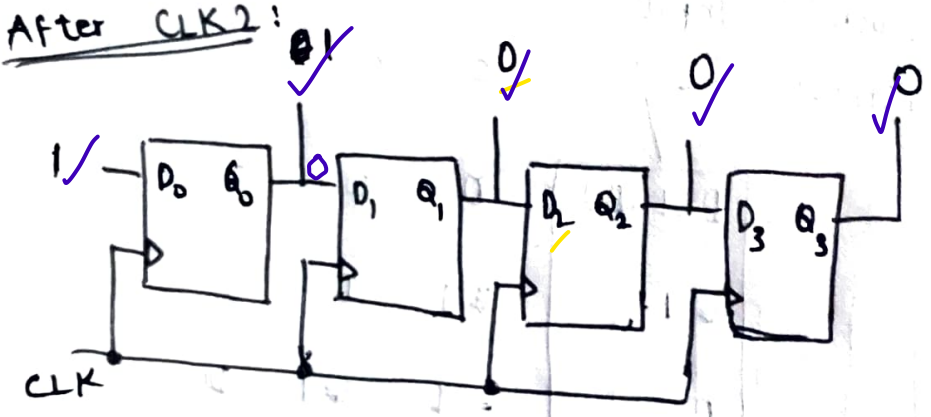


1010

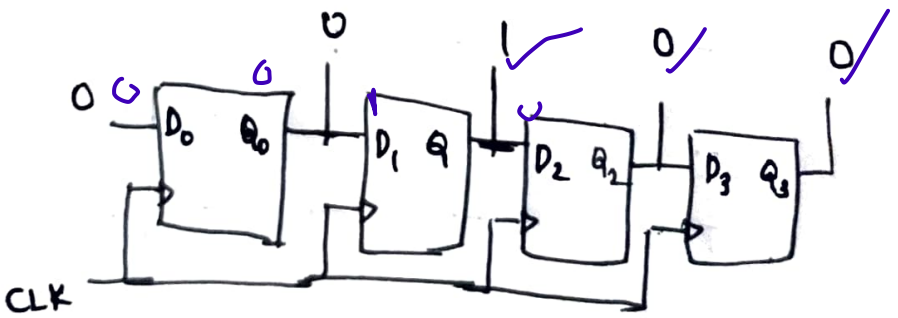
After CLK 1:



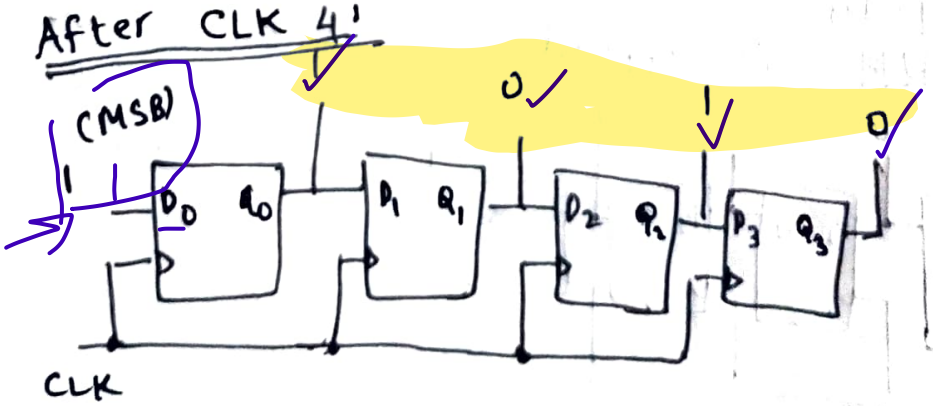
After CLK 2:



After CLK 3:



After CLK 4:



N - bit SIPO S.R need N - clock pulse.

4 - bit SIPO S.R need 4 - clock pulse.

Table:

No. of positive edge of clock	Serial Input	Q_0	Q_1	Q_2	Q_3
0 (Initial)	-	0	0	0	0
1	0 (LSB)	0	0	0	0
2	1	1	0	0	0
3	0	0	1	0	1
4	1 (MSB)	1	0	1	0

↳ input in serial

Output in parallel

PIPO S.R: 1010

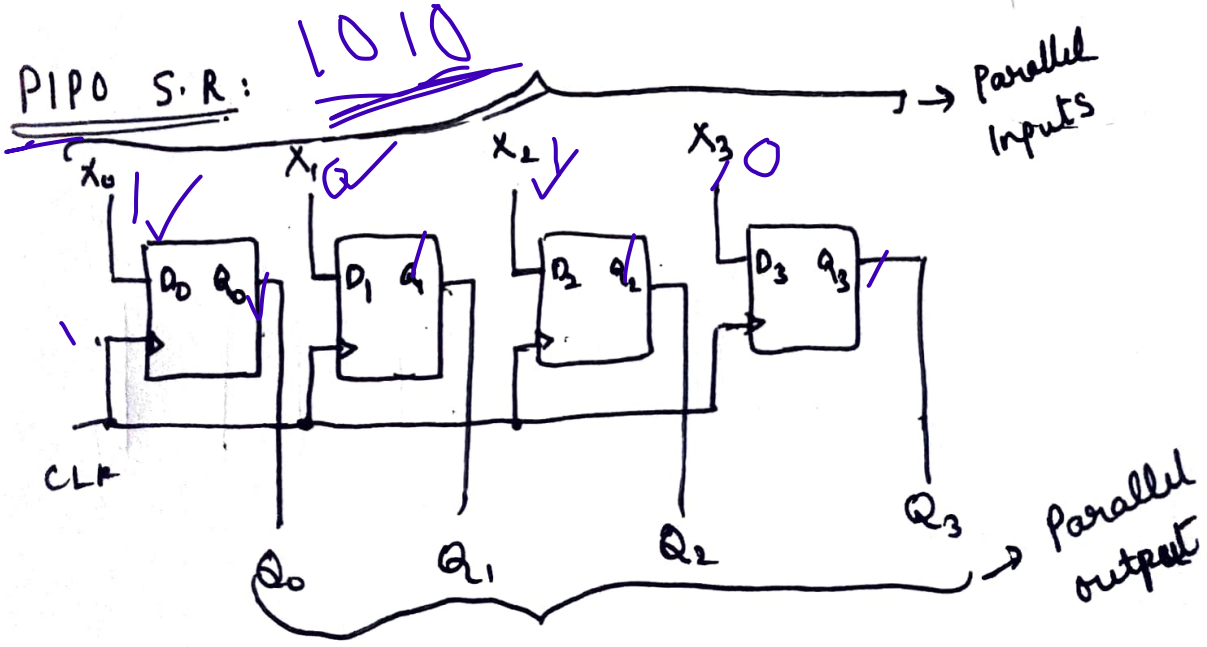
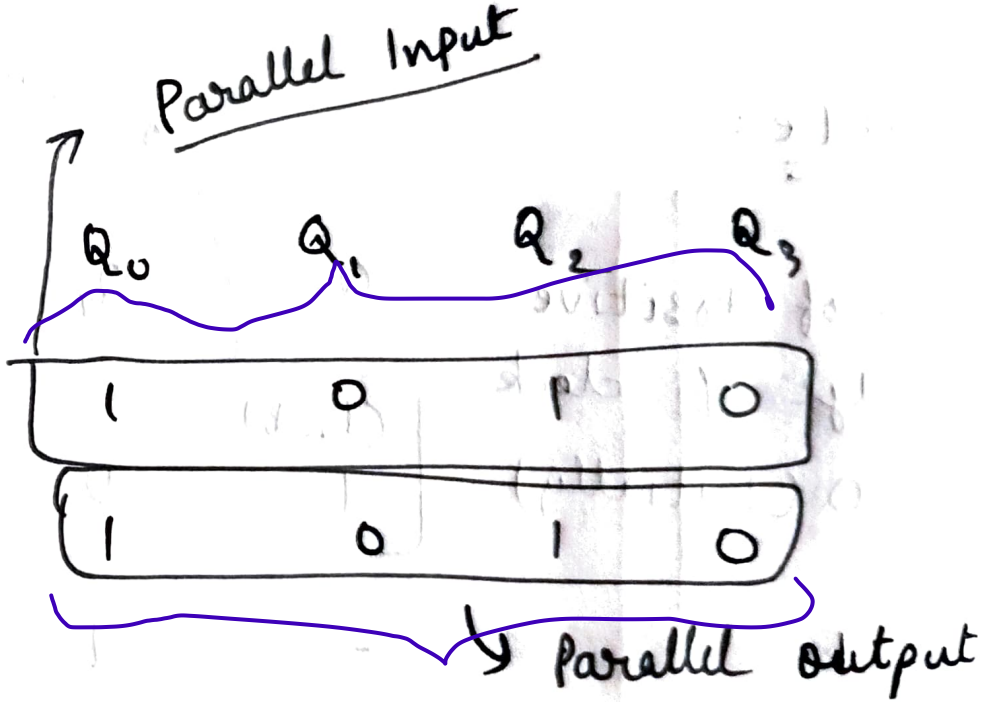
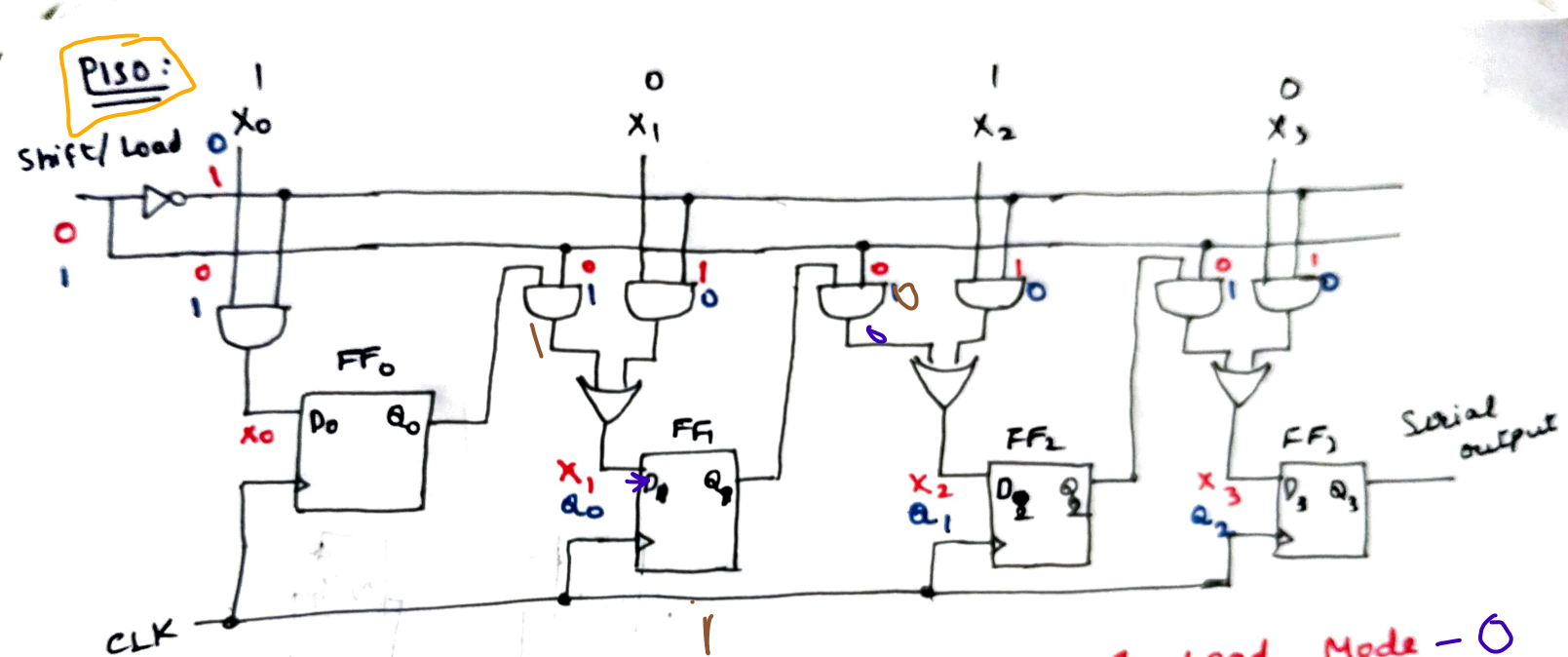


Table:

No. of Positive edge of clock	Q_0	Q_1	Q_2	Q_3
0 (Initial)	1	0	1	0
1	1	0	1	0

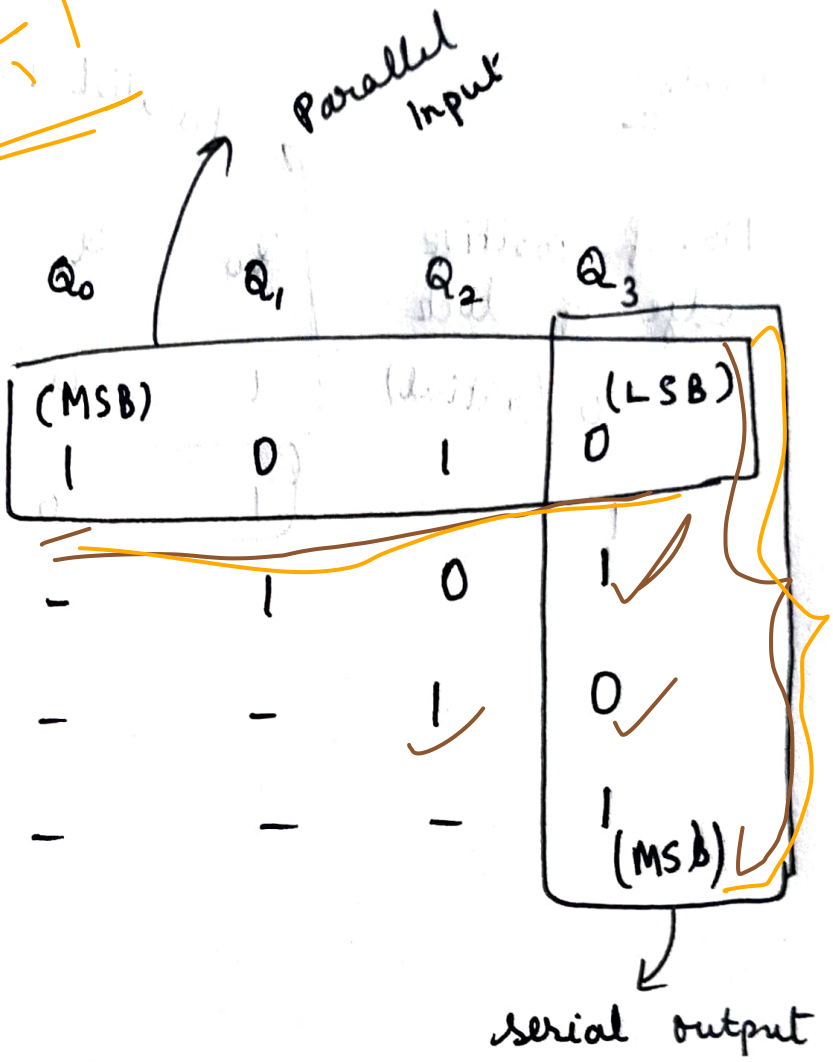




1. Load Mode – 0
2. Shift Mode.

N-1

Table:



No. of Positive edge of clock	Q_0 (MSB)	Q_1	Q_2	Q_3 (LSB)
0 (Initially)	1	0	1	0
1	–	1	0	1
2	–	–	1	0
3	–	–	–	1 (MSB)

N- Bit PISO S.R need N-1 clock pulse.

4- Bit PISO S.R need 3 clock pulse.