Reg. No.:

Name :

VIT

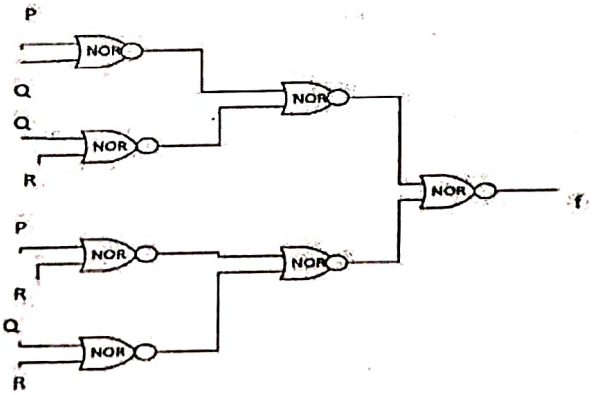
Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test I – August 2022

Programme	:	B. Tech (CSE=AIM), B. Tech(CSE), B. Tech(CSE-CPS) & B. Tech(CSE-AIR)	Semester	:	FS 2022-23
Course	:	Digital System Design	Code	:	BECE102L
			Class Nbr	:	CH2022231001903
Faculty	:	Dr. Sasithradevi. A	Slot	:	F2+TF2
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		Simplify the following function using Boolean Algebra F(A,B,C,D) = (D' + AB' + A'C + AC'D + A'C'D)'	8
2.		Derive the Boolean expression for the output ' f ' of the combinational logic circuit shown in Figure 1.  Figure. 1	5
3.		Simplify the following function using K – Map F(A,B,C,D) = ∑ m(1,5,6,7,11,12,13,15) and realize the minimized expression by NAND gate only.	7

4.		Rewrite the following Verilog code without any errors.
		Module 42code(d,y0,y1);
		input [3:0]d;
		output Y0,y1;
		always @(d)
		begin
		y0 = d[0] & d[1];
		y1 = d[2] | d[3]
		end
		end module
			5

5.		Design a combinational circuit whose input is 4 bit Binary data and outputs are x and y. The outputs produced by x and y are based on the following conditions. x: detects numbers that are divisible by 2 and y: detects numbers which are prime a) Write the truth table for the above design b) Simplify x and y using K-Map and Implement the obtained Boolean Expression using logic gates c) Write a data flow Verilog code for the sub section 5.b.	5+5+5
6.		Explain the step by step procedure to implement full adder using suitable decoder.	10

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