VIT Vellore Institute of Technology

Reg. No. : 21BPS1364

Final Assessment Test (FAT) – November/December 2022

Programme	**B.Tech.**	Semester	**Fall Semester 2022-23**
Course Title	**DIGITAL SYSTEMS DESIGN**	Course Code	**BECE102L**
Faculty Name	**Prof. Sasithradevi A**	Slot	**F2+TF2**
		Class Nbr	**CH2022231001903**
Time	**3 Hours**	Max. Marks	**100**
Answer ALL the Questions			

Section A (1 X 10 Marks)
Answer All questions

1. Perform multiplication of $(1010)_2$ x $(111)_2$ using unsigned array multiplier and draw the equivalent logic diagram for 4x3 Array Multiplier. **[10]**

Section B (6 X 15 Marks)
Answer All questions

2. (a) Simplify the following function F(A, B, C, D) = π (3, 4, 5, 6, 7, 10, 11, 14, 15) using K- Map. Also, implement the simplified expression using NOR gates only. (10 Marks) **[15]**
   (b) Implement the following Boolean function out = (D+A(B+C))' using CMOS logic . (5 Marks)
3. In the given Verilog code, identify and debug the errors . Obtain the truth table and draw the logic diagram for the same. Also, explain the functionality of the design involved. **[15]**

```
module decoder(binary_in, decoder_out, enable)
input [3:0] binary_in;
input enable ;
output [15:0] decoderout
always @ (enable or binary)
begin
 decoder_out = 0
 if (enable) begin
  case (binary_in)
    4'h0 : decoder_out = 16'h0001;   4'h1 : decoder_out = 16'h0002;
    4'h2 : decoder_out = 16'h0004;   4'h3 : decoder_out = 16'h0008;
    4'h4 : decoder_out = 16'h0010;   4'h5 : decoder_out = 16'h0020;
    4'h6 : decoder_out = 16'h0040;   4'h7 : decoder_out = 16'h0080;
    4'h8 : decoder_out = 16'h0100;   4'h9 : decoder_out = 16'h0200;
    4'hA : decoder_out = 16'h0400;   4'hB : decoder_out = 16'h0800;
    4'hC : decoder_out = 16'h1000;   4'hD : decoder_out = 16'h2000;
    4'hE : decoder_out = 16'h4000;   4'hF : decoder_out = 16'h8000;
  end case
 end
end module
```

4. Design a partially simplified Arithmetic Logic Unit (ALU) using basic logic gates which is capable of performing 1-bit arithmetic subtraction with the inclusion of borrow as an additional input. Implement the obtained logical expressions for difference and borrow using a suitable demultiplexer. [15]

5. Consider a smart parking system in a super market which indicates the number of free parking lots , out of which 8 parking lots are indicated as available in the display unit. Whenever the car enters into the super market premises , it will be identified by an IR sensor and the signal is sent to the control unit to decrement the available parking lot by one. Similarly, if any car leaves the supermarket premises, then increment the available parking lot by one. Design an appropriate control circuit which performs increment and decrement operations using T-Flip flop. [15]

6. Design Mealy sequence detector (Non Overlapping) to detect a sequence 1010 using D filpflop. [15]

7. (a) Implement the Boolean expression Y = AB' +BC + AC' using (10 Marks) [15]
   (i) Programmable Logic Array (PLA) and
   (ii) Programmable Array Logic (PAL)
   (b) Discuss about the difference between CPLD and FPGA. (5 Marks)

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