Module 1 Digital Logics

Lec 1.5 Review of Logic families

Review of CMOS & TTL logic families

REVIEW OF LOGIC GATE FAMILIES

INTRODUCTION

- In Digital Electronics, a logic family refers to digital integrated circuit devices which are constructed with a combination of electronic gates.
- There are different families of logic gates. Each family has its own characteristics, limitations and advantages.
- Some families also have common characteristics. Also within each family, there is a range of voltages which may be high level or low level.

REVIEW OF LOGIC GATE FAMILIES

INTRODUCTION

- These families are listed below:
  - Diode Logic (DL)
  - Resistor-Transistor Logic (RTL)
  - Diode-Transistor Logic (DTL)
  - Emitter Coupled Logic (ECL)
  - Transistor-Transistor Logic (TTL) √
  - Complementary Metal Oxide Semiconductor Logic (CMOS) √

REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC

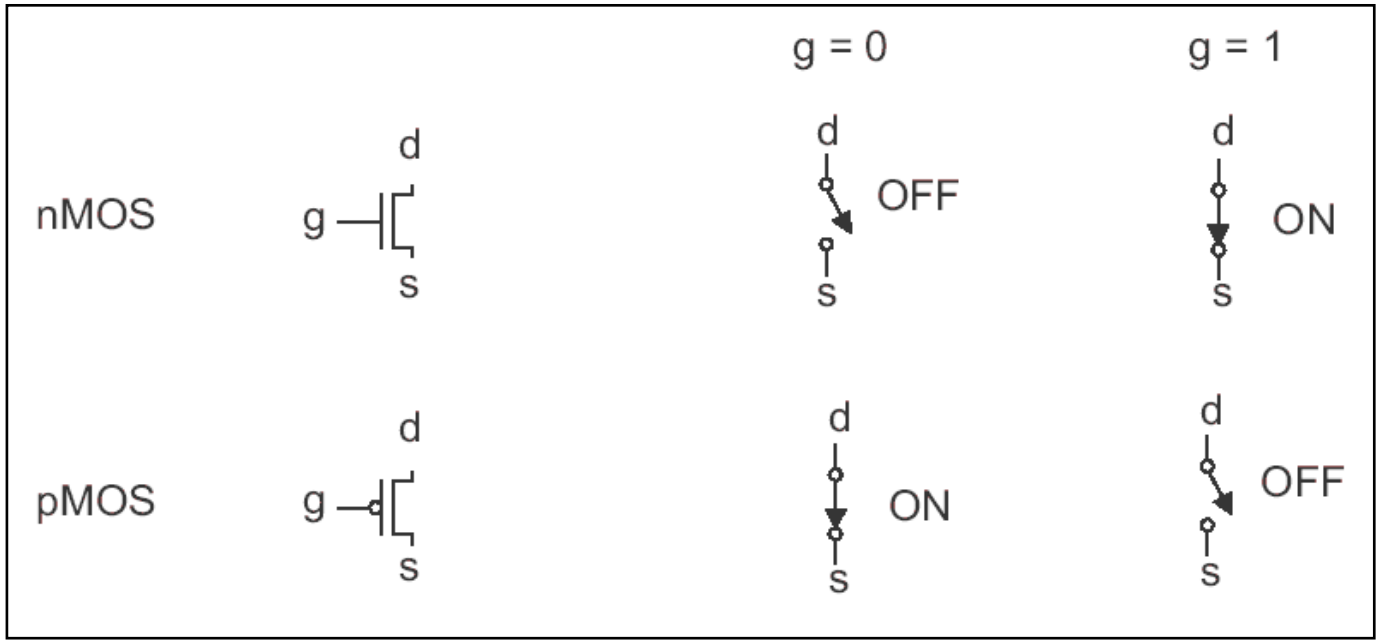
- CMOS is known for its low power consumption and high fan-out. It is also considered to be one of the most reliable logic family today.
- The transistors inside the CMOS are made from an NMOS transistor and PMOS transistor.
- To realize the logical functions, both P-type and N-type transistors are used. It is currently being used in microprocessor technology and Application Specific Integrated Circuits(ASIC).

REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC

- The gate of a MOS transistor controls the flow of the current between the drain and the source

- The MOS transistor can be viewed as a simple ON/OFF switch



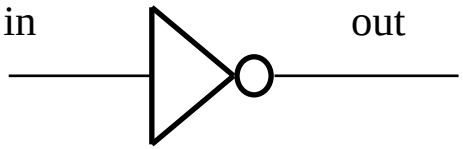
REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC - inverter

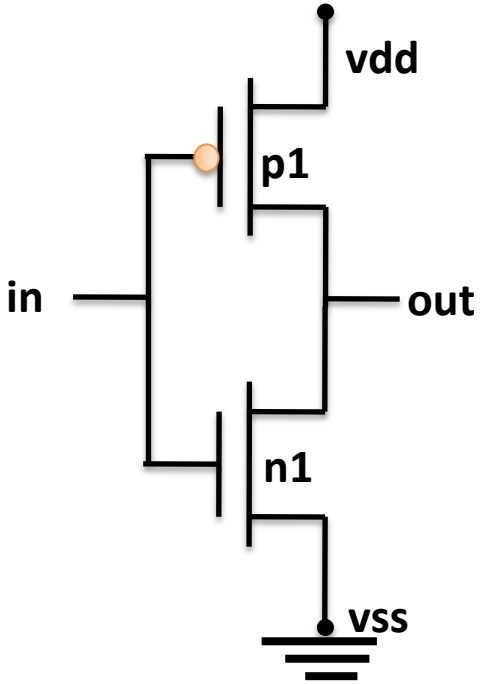
- CMOS gates are built around the technology of the basic CMOS inverter
- Two Transistors are enhancement mode MOSFETs and Transistors come in complementary pairs
- N-Channel with its source grounded & P-Channel with its source connected to +V
- Input: gates connected together & Output: drains connected

REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC - inverter

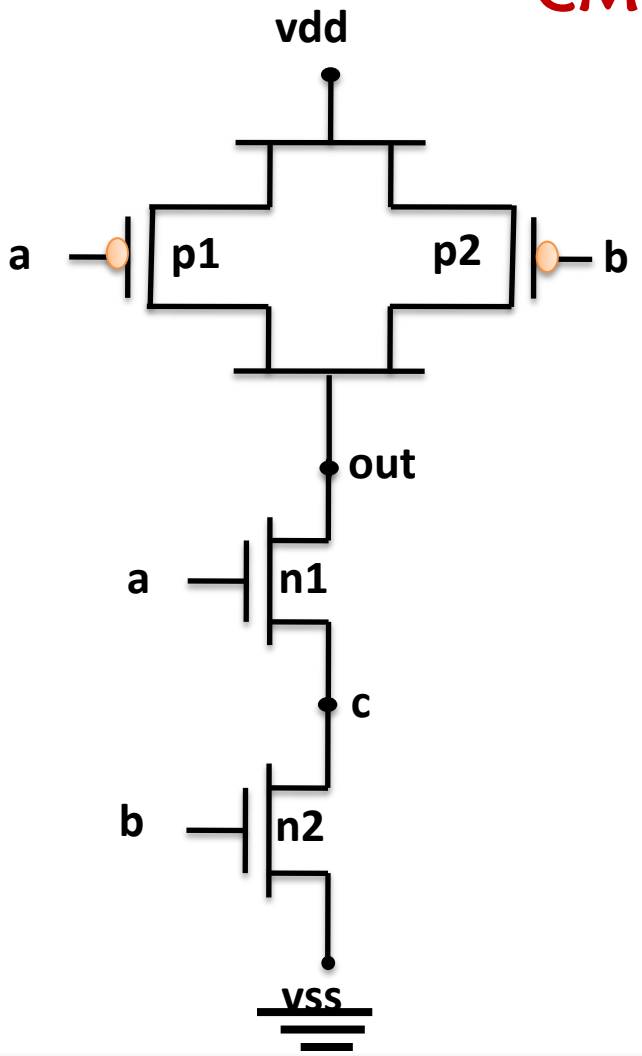


in	p1	n1	out
0	ON	OFF	1
1	OFF	ON	0



REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC - NAND

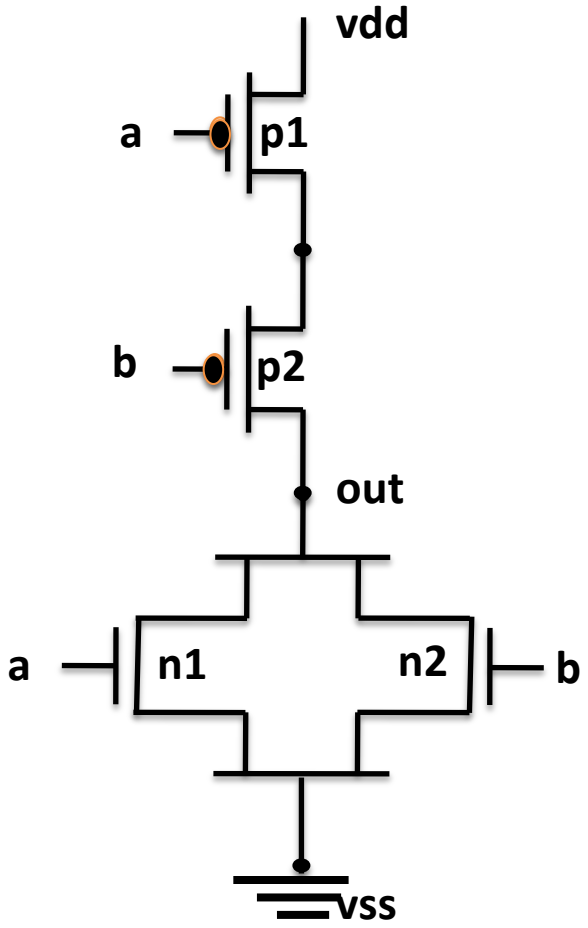


a	b	p1	p2	n1	n2	out
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

REVIEW OF LOGIC GATE FAMILIES

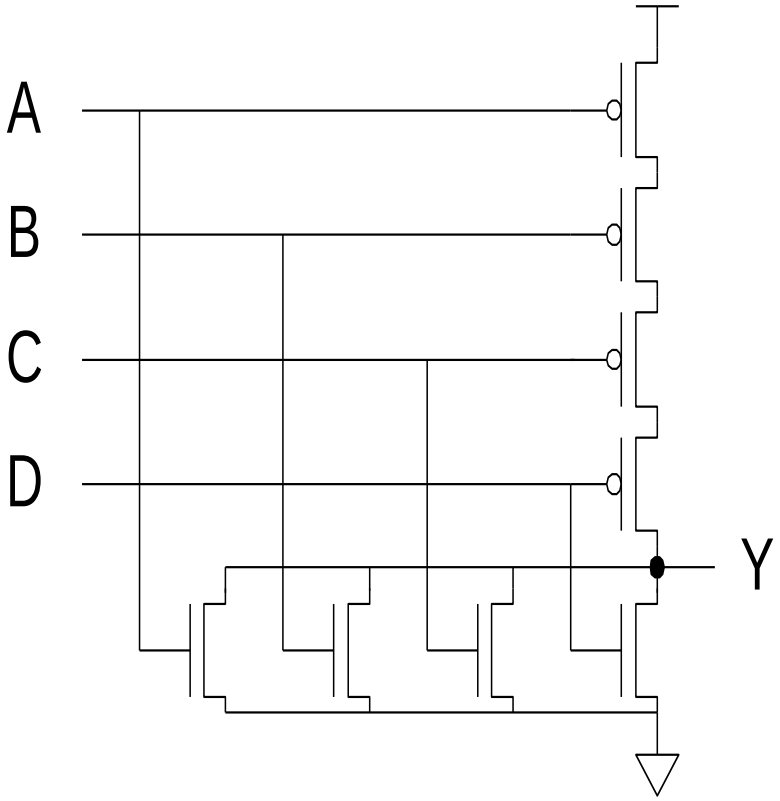
CMOS LOGIC - NOR

a	b	p1	p2	n1	n2	out
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0



REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC - EXAMPLES

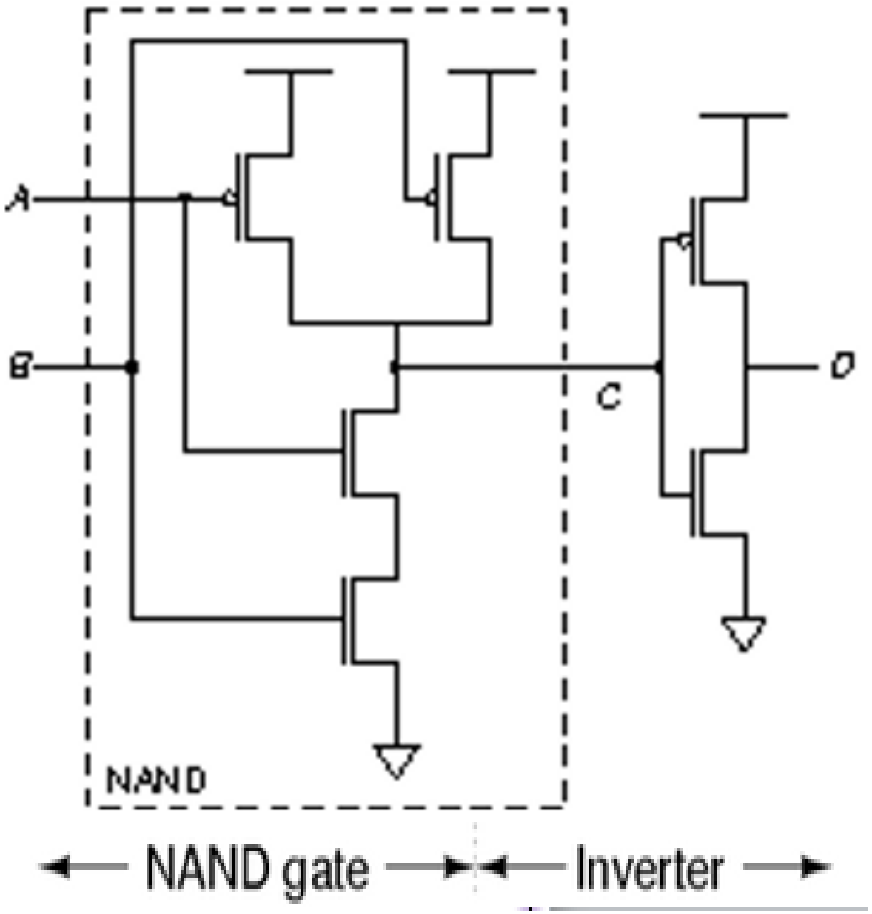


4 INPUT

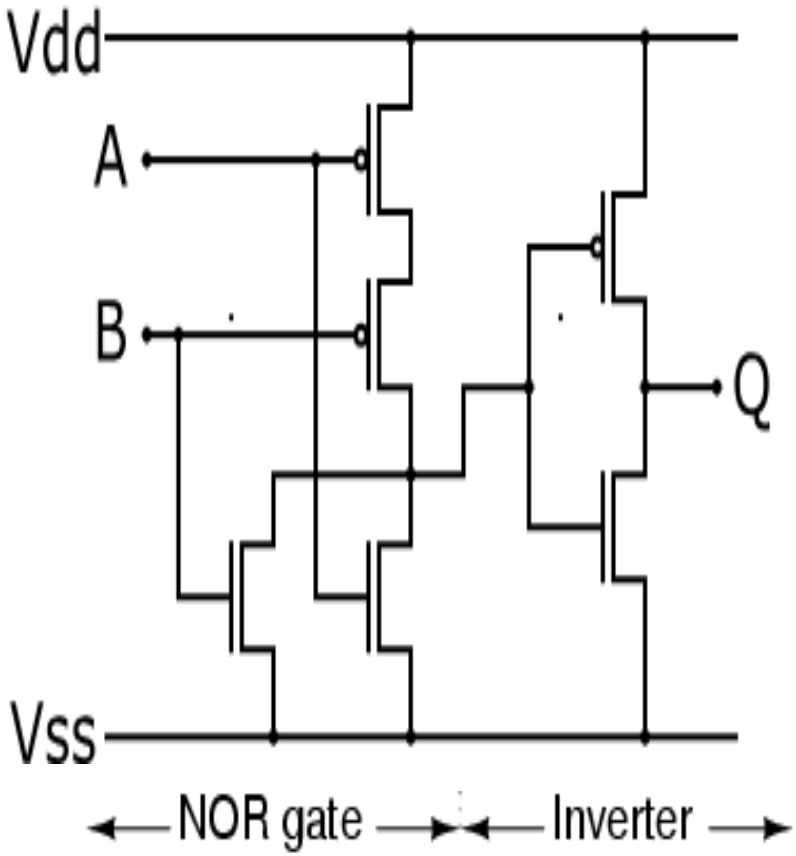
CMOS NOR GATE

REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC - AND



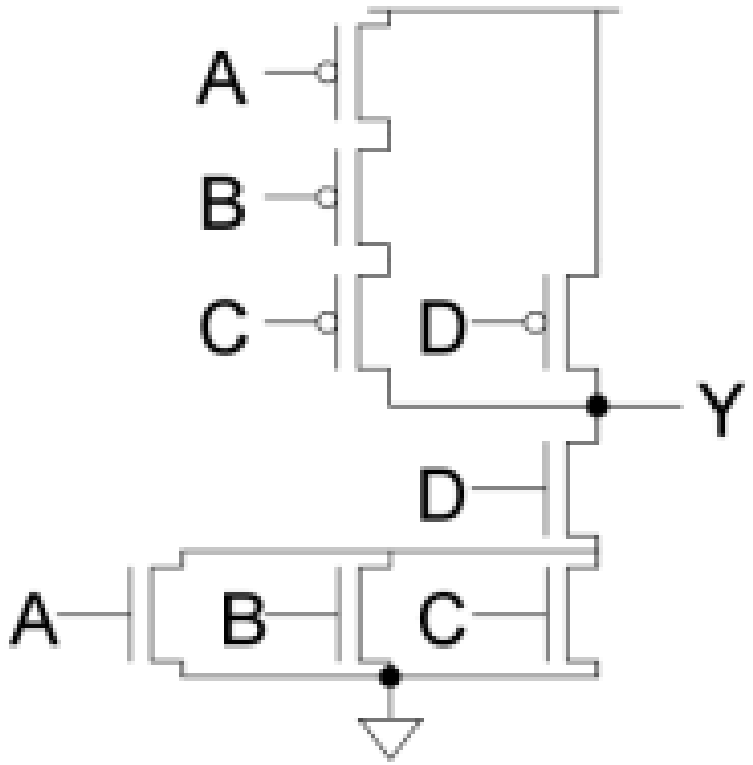
CMOS LOGIC - OR



REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC - EXAMPLES

$$Y = \overline{(A + B + C) \cdot D}$$

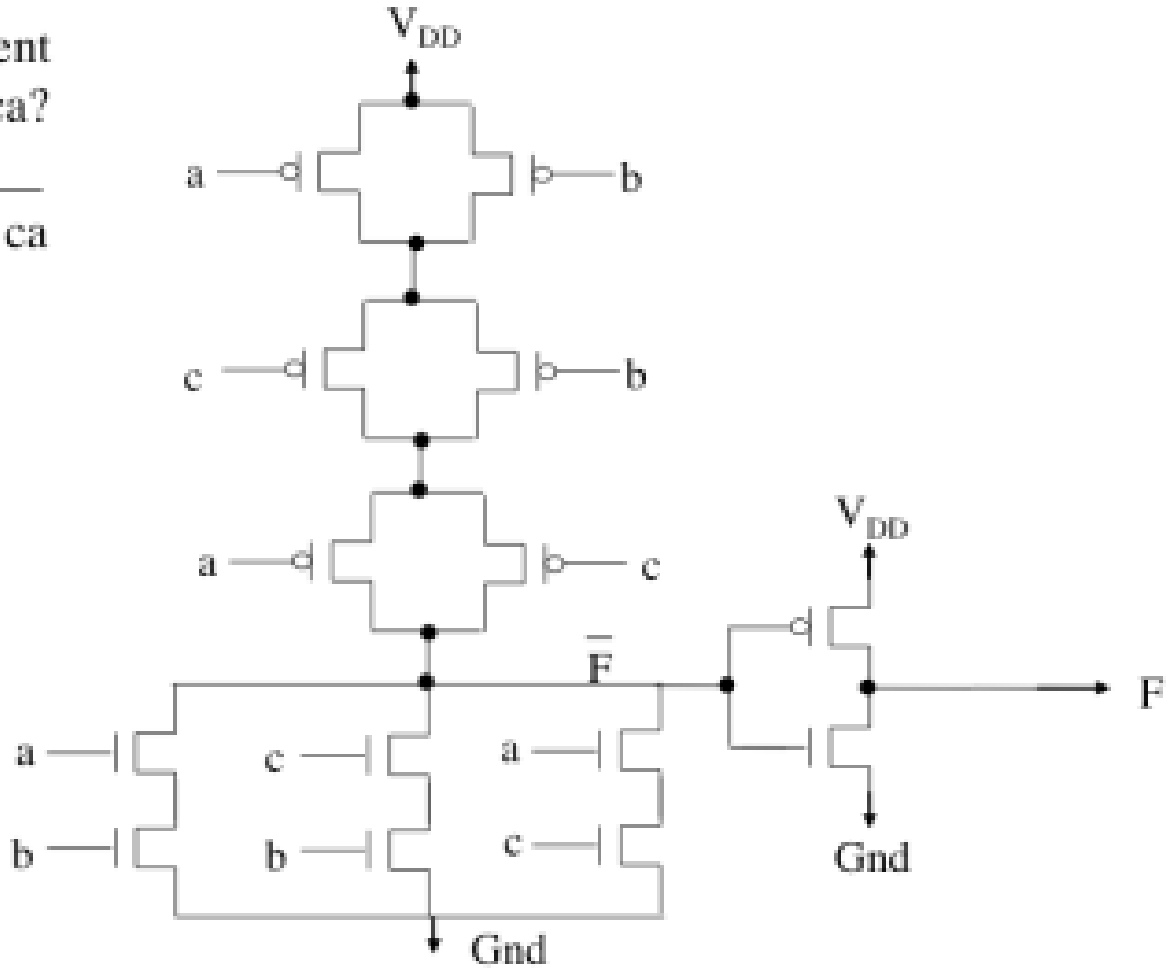


REVIEW OF LOGIC GATE FAMILIES

CMOS LOGIC - EXAMPLES

How to implement
$F = ab + bc + ca$?

- $\overline{F} = \overline{ab + bc + ca}$



REVIEW OF LOGIC GATE FAMILIES

EXERCISE PROBLEMS

Realize following logical expressions using CMOS logic:

1. Y = (AB+C)'
2. Y = AB'+A'B
3. Y = B'C+ ABC'
4. Y = (A(BC+D))'
5. Y = (AB+A(C+D))'
6. Y = (ABC+DE+F)

REVIEW OF LOGIC GATE FAMILIES

TRANSISTOR-TRANSISTOR LOGIC (TTL)

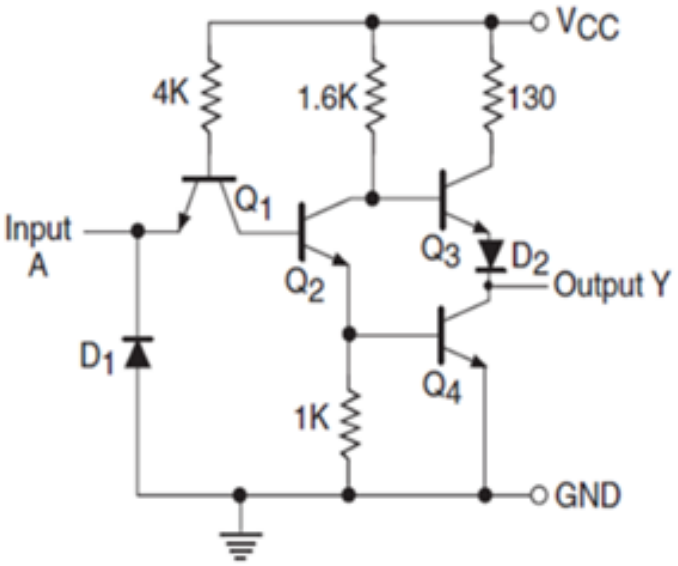
- TTL has become the standard logic circuit in many application for a number of years.
- TTL greatly decreases the manufacturing costs because multiple emitters can be added in the input so no extra space is needed and a multiple input gate can be constructed easily.
- A commercial IC package of TTL includes three three-input gates, four two-input gates, or two four-input gates. The structure of the IC always remains the same.

REVIEW OF LOGIC GATE FAMILIES

TRANSISTOR-TRANSISTOR LOGIC (TTL)

- In transistor-transistor logic, the logic gates are constructed around the transistors.
- TTL uses bipolar transistors to construct its integrated circuits.
- There have been different versions of TTL:
  - Standard TTL.
  - High speed TTL.
  - Low power TTL.
  - Schcottky TTL.

TTL- Transistor Transistor Logic



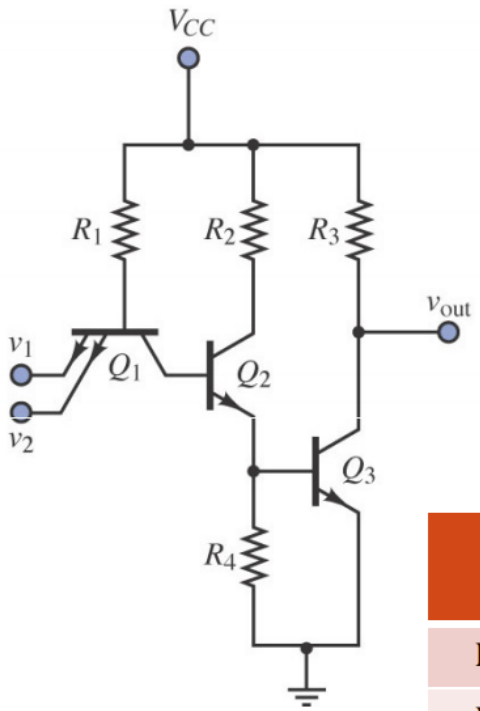
NOT Gate TTL

CASE 1:

- INPUT :LOW
  - corresponding base-emitter junction is forward biased and the base-collector junction is reverse biased.
  - transistor Q2 is cut off and also transistor Q4 is cut off
  - Transistor Q3 goes to saturation and diode D2 starts conducting and output is connected to Vcc and goes to logic high
- INPUT:high

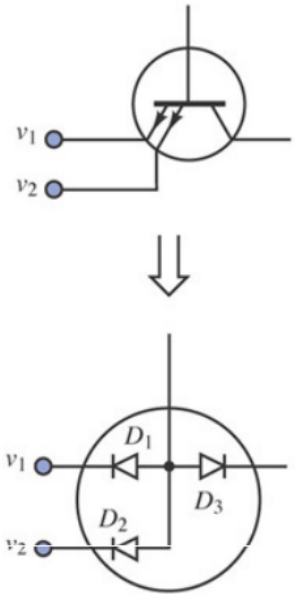
TRANSISTOR-TRANSISTOR LOGIC (TTL)

TTL NAND Gate



LOW = 0V

HIGH = 5V



V_1	V_2	State of Q1	State of Q2	State of Q3	V_{out}
LOW	LOW	ON	OFF	OFF	HIGH
LOW	HIGH	ON	OFF	OFF	HIGH
HIGH	LOW	ON	OFF	OFF	HIGH
HIGH	HIGH	OFF	ON	ON	LOW

Case 1:

Any i/p is logic 0

Q1 : BE-Forward Bias

BC- Reverse Bias

So Q2 and Q3 are off

Vout = Vcc –IcRc logic 1

Case 2:

Any i/p is are 1

Q1 : BE-Reverse Bias

BC- Forward Bias

So Q2 and Q3 are ON

Vout = Vcc –IcRc 0.2 volts Logic 0

REVIEW OF LOGIC GATE FAMILIES

SUMMARY

Logic Parameters	*RTL*	*DTL*	*TTL*	*ECL*	*CMOS*
Basic gates with +ve logic	NOR	NAND	NAND	OR/NOR	NAND/NOR
Maximum fan-in	5	10	8	5	8
Fan out	5	8	10	25	>50
Power dissipation/ gate (in mW)	12	10	10	50	0.01 static at 1 MHz
Propagation delay per gate (nano sec)	20	30	12	4	70
Noise Immunity	Nominal	Good	Very good	Good	Very good
Number of functions	High	Fairly high	Very high	High	Good
Clock rate, MHz	5	12	15	300	5

END