Reg. No.:

Name :

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act 1956)

Continuous Assessment Test II – October 2022

Programme	:	B. Tech (AI & ML), B. Tech(CSE), B. Tech(CPS) & B. Tech(AI & Robotics)	Semester	:	FS 2022-23
Course	:	Digital System Design	Code	:	BECE102L
			Class Nbr	:	CH2022231001903
Faculty	:	Dr. Sasithradevi. A	Slot	:	F2+TF2
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		Construct the truth table of 4-bit parity generator for odd parity and implement its Boolean function using 8:1 multiplexer.	[10]
2.		Perform Multiplication of (15) x (-12) using Booth's Multiplication algorithm. Also find out the number of additions, number of subtractions and number of arithmetic shifts required.	[10]
3.		Consider a control unit for a wheat packing machine to pack wheat of 6kg each. Present weight of the pack is measured and represented in 3-bit binary number and then it is compared with the reference value (6kg). If the wheat pack is less/greater than 6kg control signal generated to add/remove excess wheat into/from the wheat pack. If the wheat pack weight is exactly 6kg then control signal is generated to make a pack. Design an appropriate control circuit for the above mentioned comparison operation using basic logic gates. Also write a Verilog HDL code in dataflow modelling for the same.	[10]
4.		Consider a simple human counter system for an elevator overload indication in which the number of persons entering into the elevator is detected by an IR sensor. By default, it must display value '0' and increment the number on the display by one while each time a human enters into the elevator. Assume the maximum capacity of the elevator is 9 persons and if it exceeds the count of 9, there will be an alarm sound to indicate the overload condition. Design an appropriate control circuit which perform increment operation using T-Flip flop. Also write a Verilog HDL code in sequential modelling for the same.	[20]

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