Additional Practice Problems- Set 2

(To be submitted on 14.10.2022 at 11 am)

1. Implement the function ∑m(1,3,4,11,12,13,14,15) using an 8:1 mux.

2. Implement the function ∑m(1,3,5,7,11,13,15) using a suitable demux

3. Design an odd parity generator using logic gates

4. Write the Verilog code for odd parity generator (with test bench) using data flow modelling