Course Code	Course Title			T	Р	С
BECE102P	Digital Systems Design Lab		0	0	2	1
Pre-requisite	Nil	Syllabus version				
				1.0		

Course Objective

• To apply theoretical knowledge gained in the theory course and get hands-on experience of the topics.

Course Outcome

At the end of the course the student will be able to

- 1. Design, simulate and synthesize combinational logic circuits, data path circuits and sequential logic circuits using Verilog HDL.
- 2. Design and implement FSM on FPGA.
- 3. Design and implement small digital systems on FPGA.

Indicative Experiments								
Characteristics of Digital ICs, Realization of Boolean expressions								
Design and Verilog modeling of Combinational Logic circuits								
Design and Verilog modeling of various data path elements - Adders								
Design and Verilog modeling of various data path elements - Multipliers								
Implementation of combinational circuits – (FPGA / Trainer Kit)								
Implementation of data path circuit - (FPGA / Trainer Kit)								
Design and Verilog modeling of simple sequential circuits like Counters								
and Shift registers								
Design and Verilog modeling of complex sequential circuits								
Implementation of Sequential circuits - (FPGA / Trainer Kit)								
Design and Verilog modeling of FSM based design – Serial Adder								
Design and Verilog modeling of FSM based design – Traffic Light								
Controller / Vending Machine								
Design of ALU								
Total Laboratory Hours								
Mode of Assessment: Continuous Assessment and Final Assessment Test								
Recommended by Board of Studies 14-05-2022								
Approved by Academic Council No. 66 Date 16-06-2022								
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