Course Code	Course Title	L	T	P	C
BECE102P	Digital Systems Design Lab	0	0	2	1
Pre-requisite	Nil	Syllabus version			
		1.0			

Course Objective

- To apply theoretical knowledge gained in the theory course and get hands-on experience of the topics.

Course Outcome

At the end of the course the student will be able to

1. Design, simulate and synthesize combinational logic circuits, data path circuits and sequential logic circuits using Verilog HDL.
2. Design and implement FSM on FPGA.
3. Design and implement small digital systems on FPGA.

Indicative Experiments

1.	Characteristics of Digital ICs, Realization of Boolean expressions	**2 hours**
2.	Design and Verilog modeling of Combinational Logic circuits	**4 hours**
3.	Design and Verilog modeling of various data path elements - Adders	**2 hours**
4.	Design and Verilog modeling of various data path elements - Multipliers	**2 hours**
5.	Implementation of combinational circuits – (FPGA / Trainer Kit)	**2 hours**
6.	Implementation of data path circuit - (FPGA / Trainer Kit)	**2 hours**
7.	Design and Verilog modeling of simple sequential circuits like Counters and Shift registers	**2 hours**
8.	Design and Verilog modeling of complex sequential circuits	**2 hours**
9.	Implementation of Sequential circuits - (FPGA / Trainer Kit)	**2 hours**
10.	Design and Verilog modeling of FSM based design – Serial Adder	**2 hours**
11.	Design and Verilog modeling of FSM based design – Traffic Light Controller / Vending Machine	**4 hours**
12.	Design of ALU	**4 hours**
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	14-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022