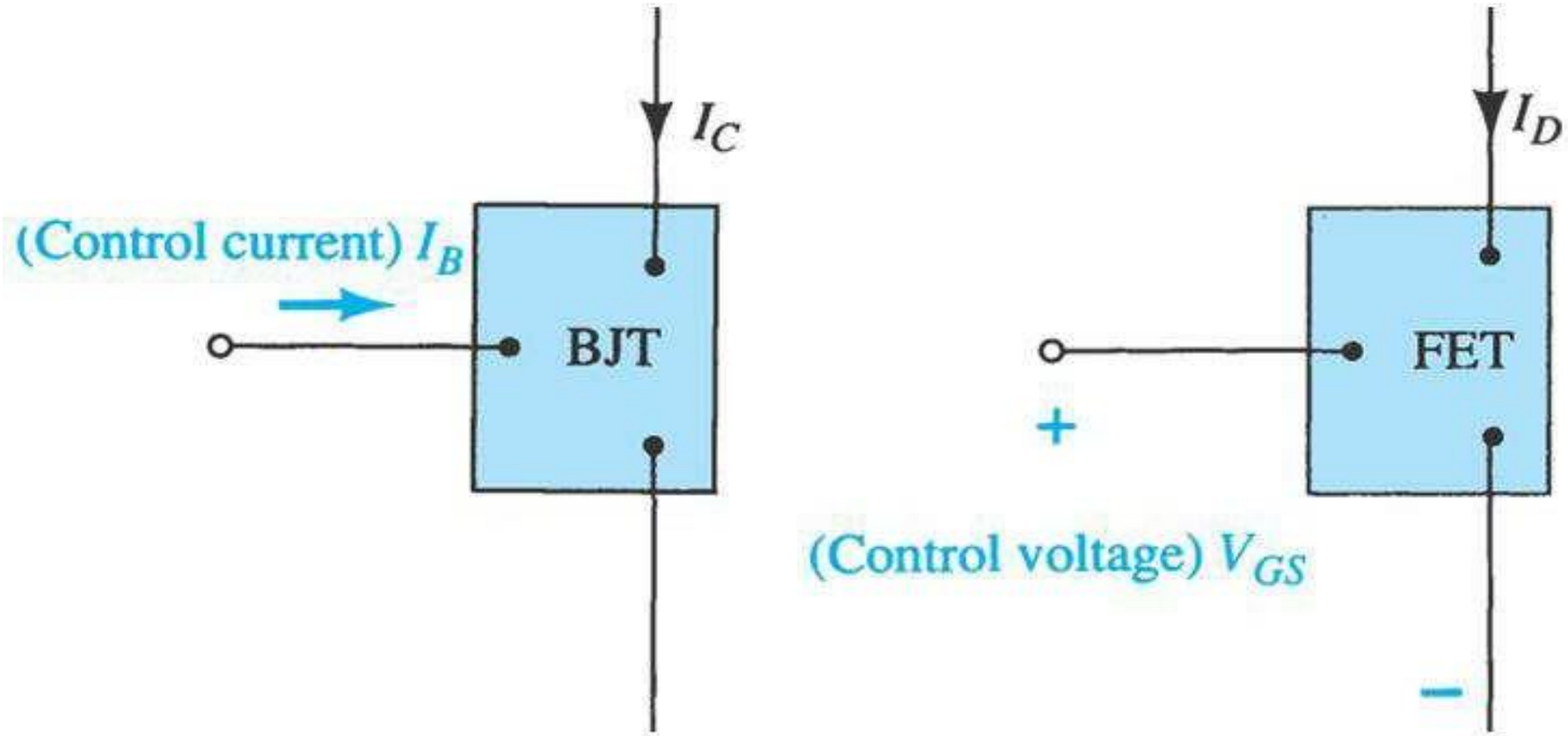
Module 6
JFET & MOSFET

(Field EffectTransistor)

FET'S VS. BJT'S



Similarities:

- Amplifiers
- Switching Device
- Impedance Matching Circuits

DIFFERENCES

FET's	BJT's
✓ Voltage controlled devices	✓ Current controlled devices
✓ Higher input impedance	✓ Lower impedance
✓ Less sensitive to temp. variations	✓ Higher sensitive
✓ Unipolar device	✓ Bipolar device
✓ Smaller/ Easily Integrated Chips	✓ Bigger IC

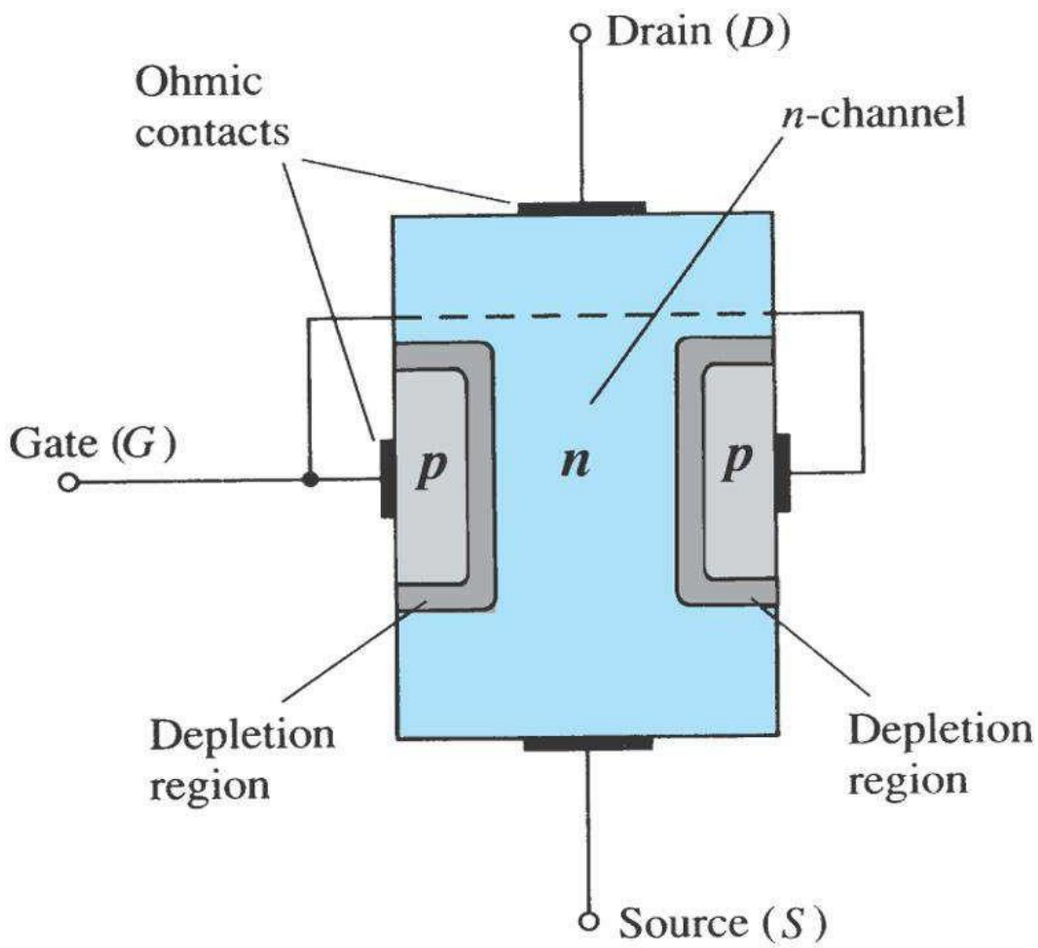
TYPES OF FET

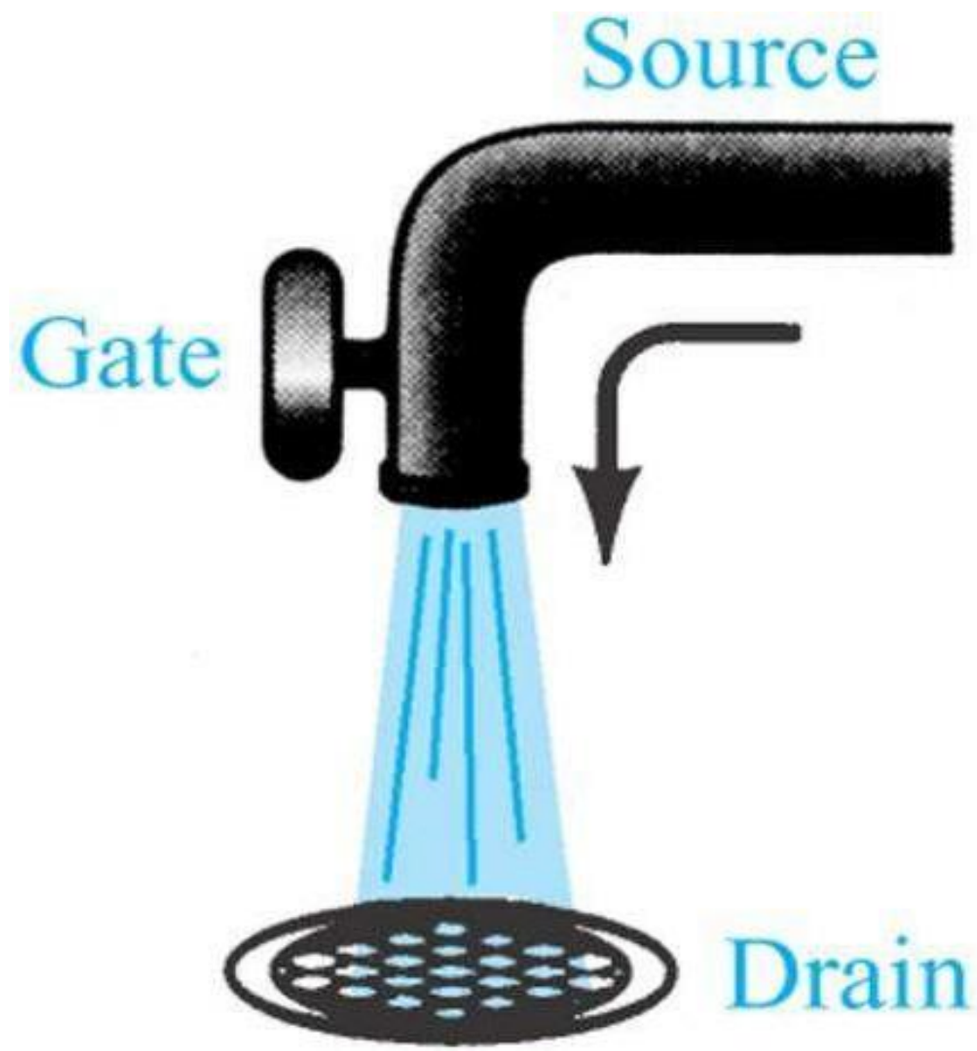
1. JFET (Junction FET)
2. MESFET (metal-semiconductor FET)
3. MOSFET (metal-oxide-semiconductor FET)
   a. D-MOSFET (Depletion)
   b. E-MOSFET (Enhancement)

The FET is a device in which the flow of current through the conducting region is controlled by an electric field. Hence, the name Field Effect Transistor (FET). As current conduction is only by majority carriers, FET is said to be a unipolar device.

Based on the construction, the FET can be classified into two types as *Junction FET(JFET)* and *Metal Oxide Semiconductor FET(MOSFET)* or *Insulated Gate FET (IGFET)* or *Metal Oxide Silicon Transistor(MOST)*.

Depending upon the majority carriers, JFET has been classified into two types, namely, (1) *N-channel JFET* with electrons as the majority carriers, and (2) *P-Channel JFET* with holes as the majority carriers.

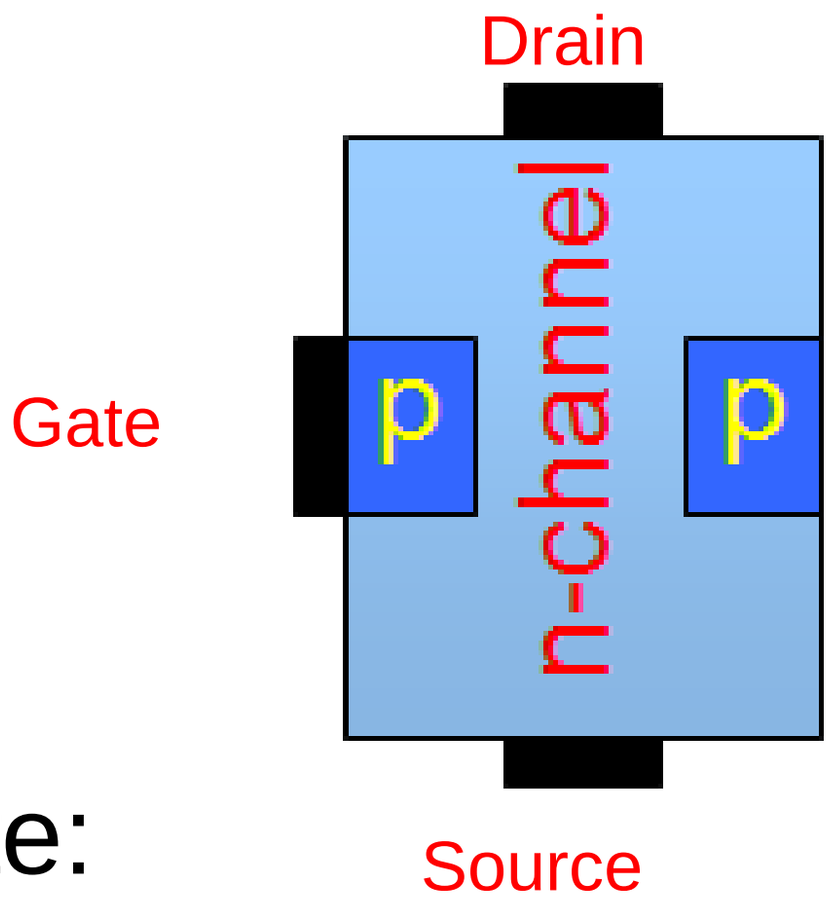


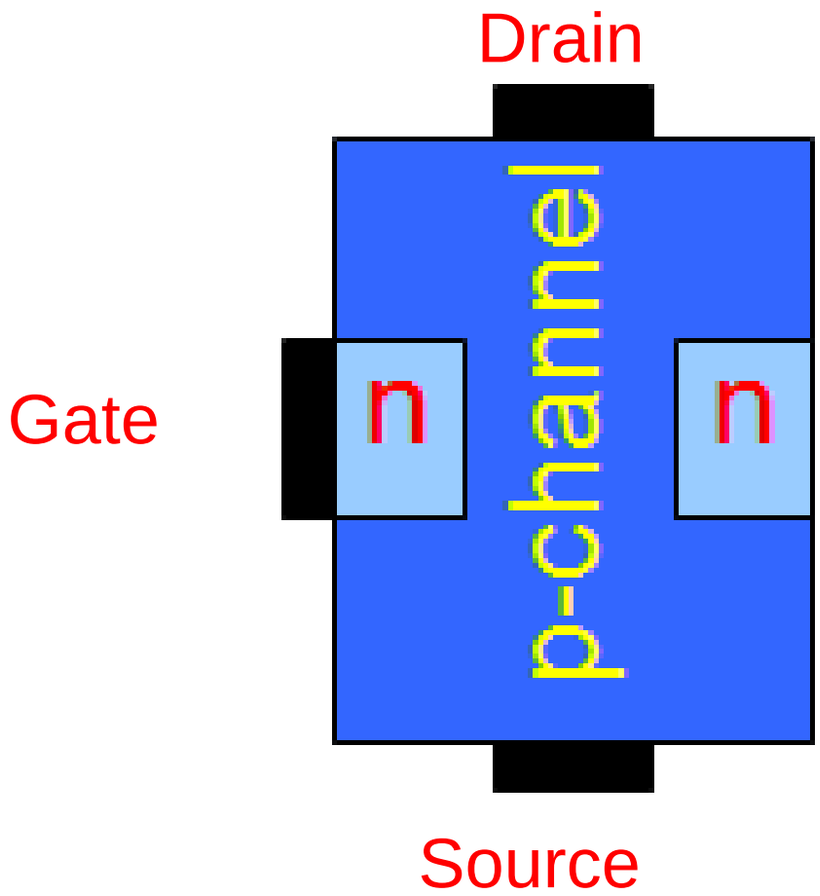


- **Drain (D) and Source (S) are connected to the n-channel**
- **Gate (G) is connected to the p-type material**

Two types of JFET

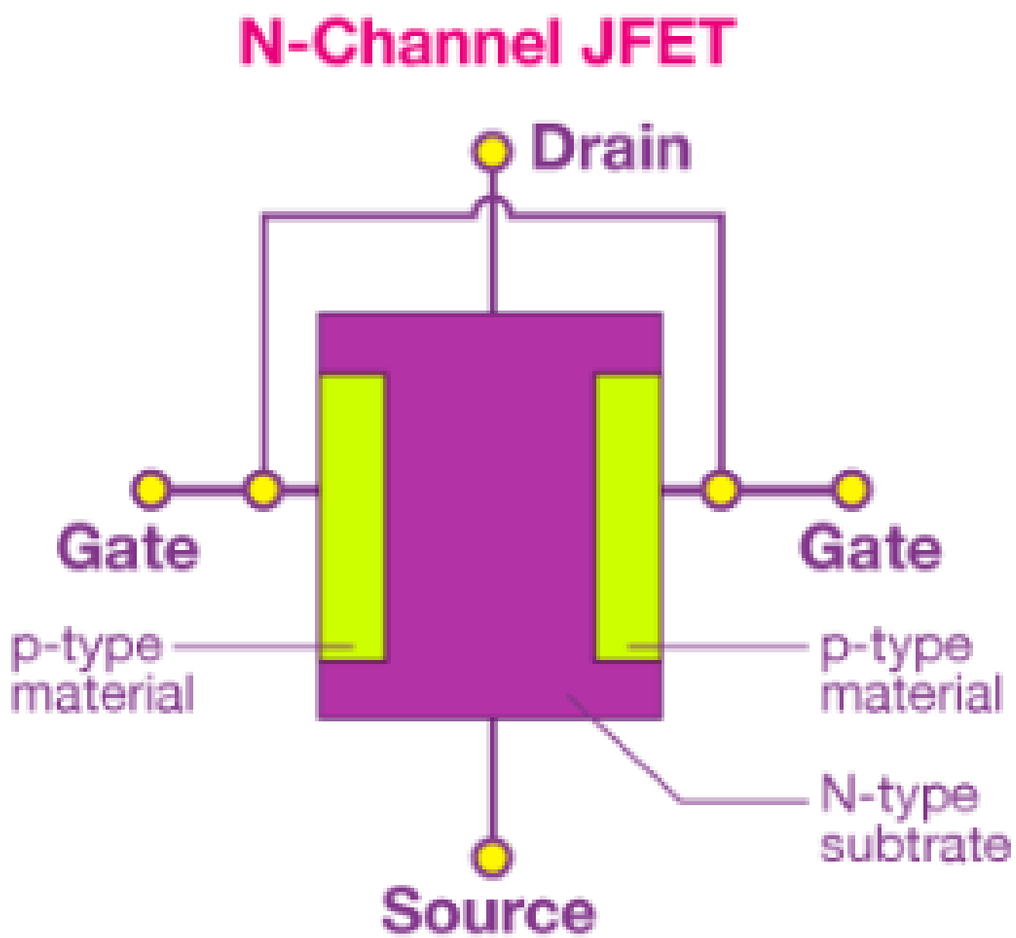
1. n-channel
2. p-channel

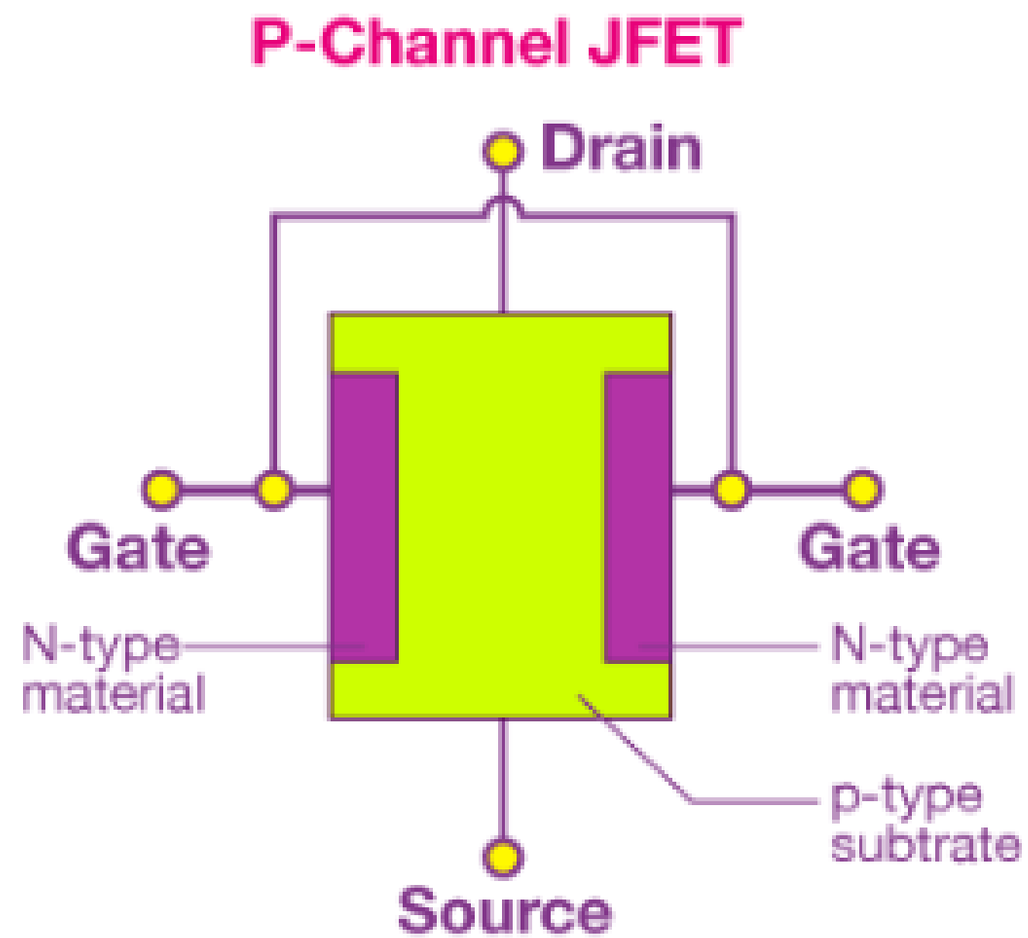


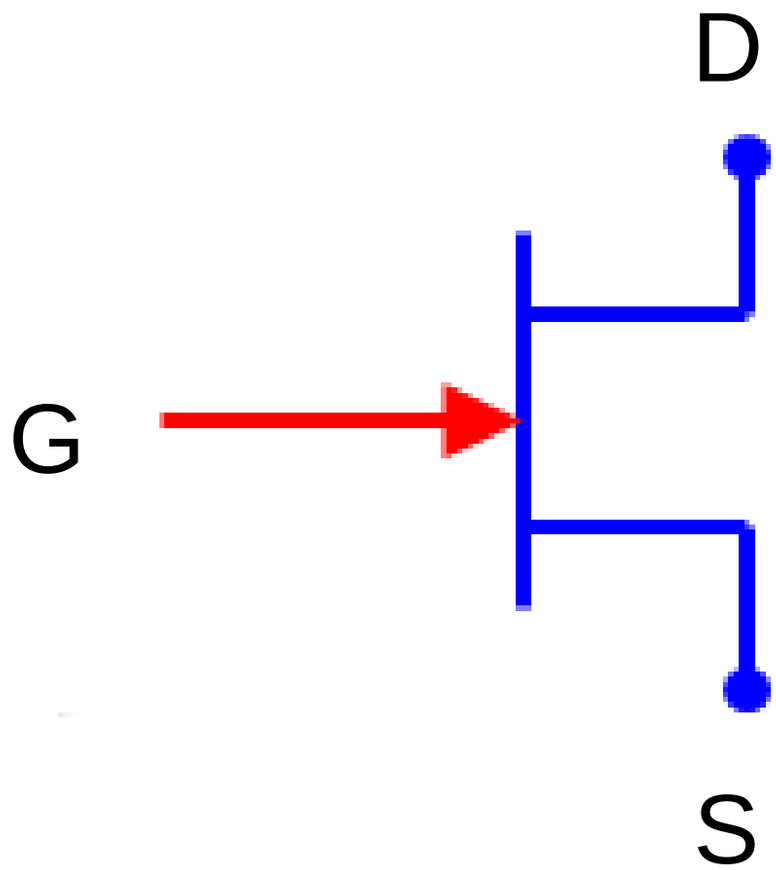


Note:

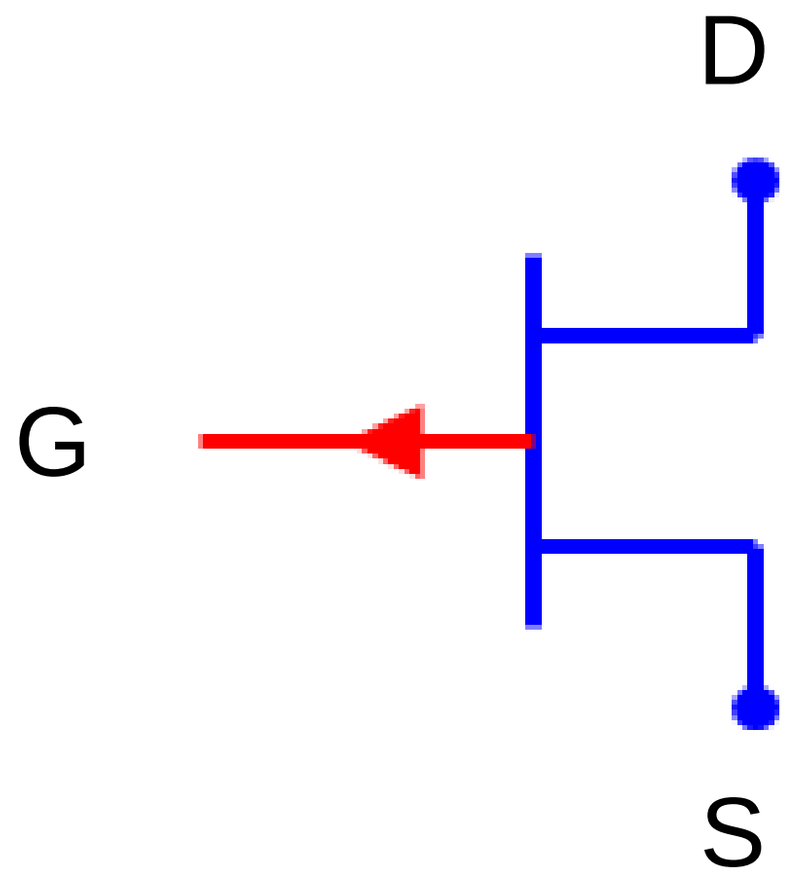
- n-channel is more widely used.


N-Channel JFET
Drain
Gate
Gate
p-type
material
p-type
material
N-type
subtrate
Source


P-Channel JFET
Drain
Gate
Gate
N-type
material
N-type
material
p-type
subtrate
Source



n-channel



p-channel

Dr. Ian Munro Ross & G.C Dacey

Jointly developed an experimental procedure for measuring the characteristics of FET in 1955

CONSTRUCTION OF *N*-CHANNEL JFET

It consists of a *N*-type bar which is made of silicon. Ohmic contacts (terminals), made at the two ends of the bar, are called Source and Drain.

Source (S) This terminal is connected to the negative pole of the battery. Electrons which are the majority carriers in the *N*-type bar enter the bar through this terminal.

Drain (D) This terminal is connected to the positive pole of the battery. The majority carriers leave the bar through this terminal.

Gate (G) Heavily doped *P*-type silicon is diffused on both sides of the *N*-type silicon bar by which *PN* junctions are formed. These layers are joined together and called Gate *G*.

Channel The region of the *N*-type bar between the depletion region is called the channel. Majority carriers move from the source to drain when a potential difference V_{DS} is applied between the source and drain.

- JFET is always operated with the gate- source PN junction **reversed biased**.

- Reverse biasing of the gate source junction with the negative voltage produces a depletion region along the PN junction which extends into the n-channel and thus increases its resistance by restricting the channel width as shown in the preceding figure.

REGIONS OF JFET ACTION

1. Ohmic Region – linear region
   - JFET behaves like an ordinary resistor
2. Pinch Off Region
   - Saturation or Amplifier Region
   - JFET operates as a constant current device because Id is relatively independent of Vds
   - Idss – drain current with gate shorted to source.
3. Breakdown Region
   - If Vds is increased beyond its value corresponding to Va – avalanche breakdown voltage.
   - JFET enters the breakdown region where Id increases to an excessive value.

4. Cut Off Region

- As Vgs is made more and more negative, the gate reverse bias increases which increases the thickness of the depletion region.
- As negative value of Vgs is increased, a stage comes when the 2 depletion regions touch each other.

$V_{gs}(off) = -V_p$

OPERATION OF *N*-CHANNEL JFET

When V_{GS} = o and V_{DS} = o When no voltage is applied between drain and source, and gate and source, the thickness of the depletion regions round the *PN* junction is uniform as shown in Fig.

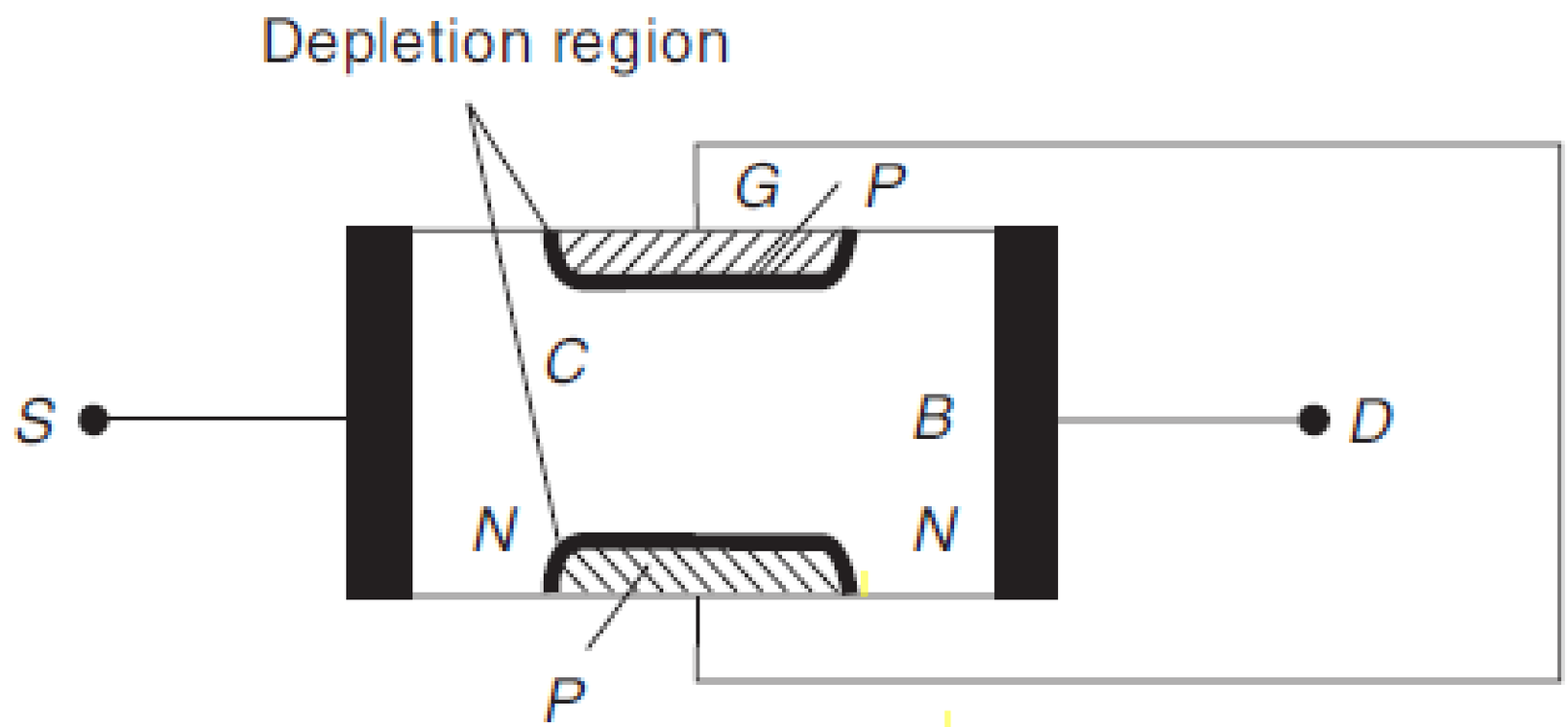


Fig. *JFET construction*

When V_{DS} = o and V_{GS} is decreased from zero In this case, the PN junctions are reverse biased and hence the thickness of the depletion region increases. As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased and hence, the thickness of the depletion region in the channel also increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off. The value of V_{GS} which is required to cut-off the channel is called the cut-off voltage V_C.

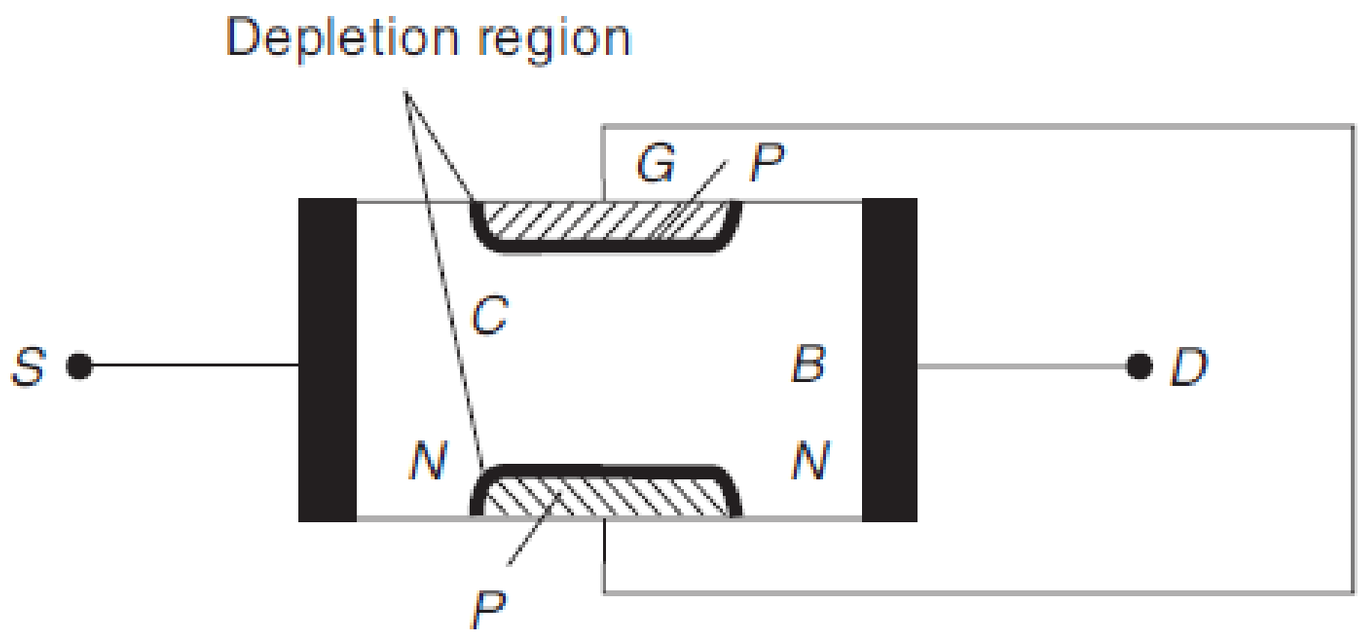


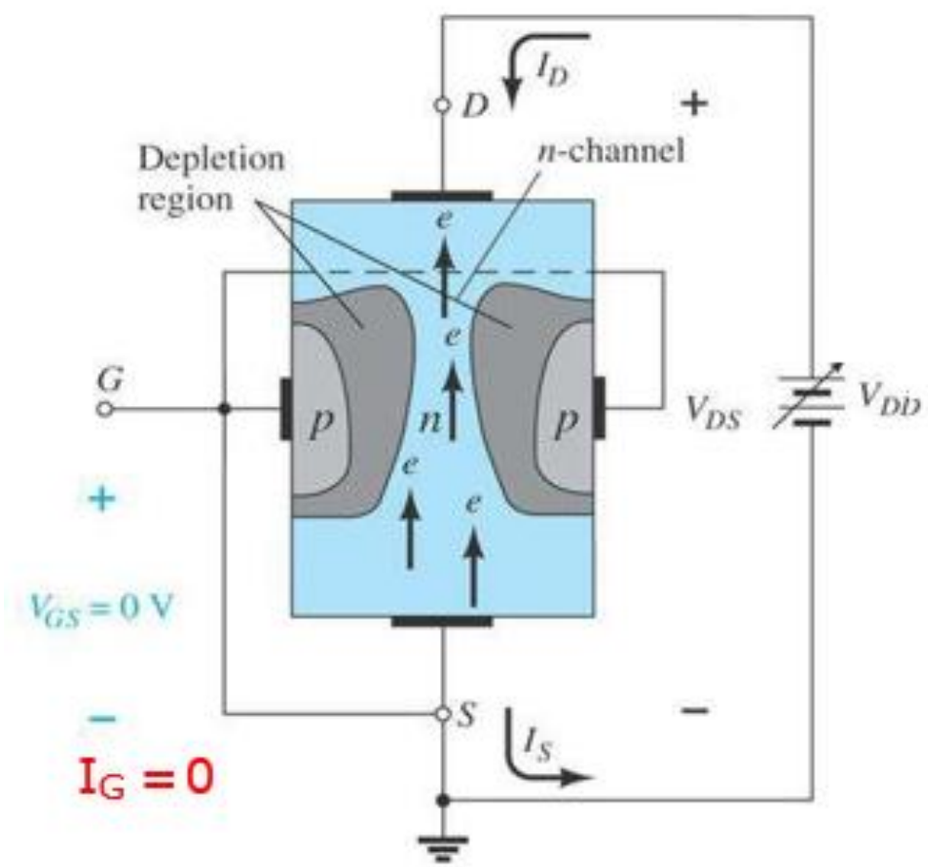
Fig. *JFET construction*

When V_{GS} = o and V_{DS} is increased from zero Drain is positive with respect to the source with $V_{GS} = 0$. Now the majority carriers (electrons) flow through the N-channel from source to drain. Therefore the conventional current I_D flows from drain to source. The magnitude of the current will depend upon the following factors:

1. The number of majority carriers (electrons) available in the channel, i.e., the conductivity of the channel.
2. The length L of the channel.
3. The cross-sectional area A of the channel at B.
4. The magnitude of the applied voltage V_{DS}. Thus the channel acts as a resistor of resistance R given by

$$R = \frac{\rho L}{A}$$

$$I_D = \frac{V_{DS}}{R} = \frac{A V_{DS}}{\rho L}$$



where ρ is the resistivity of the channel. Because of the resistance of the channel and the applied voltage V_{DS}, there is a gradual increase of positive potential along the channel from source to drain. Thus the reverse voltage across the PN junctions increases and hence the thickness of the depletion regions also increases. Therefore, the channel is wedge shaped as shown in Fig. .

As V_{DS} is increased, the cross-sectional area of the channel will be reduced. At a certain value V_P of V_{DS}, the cross-sectional area at B becomes minimum. At this voltage, the channel is said to be pinched off and the drain voltage V_P is called the pinch-off voltage.

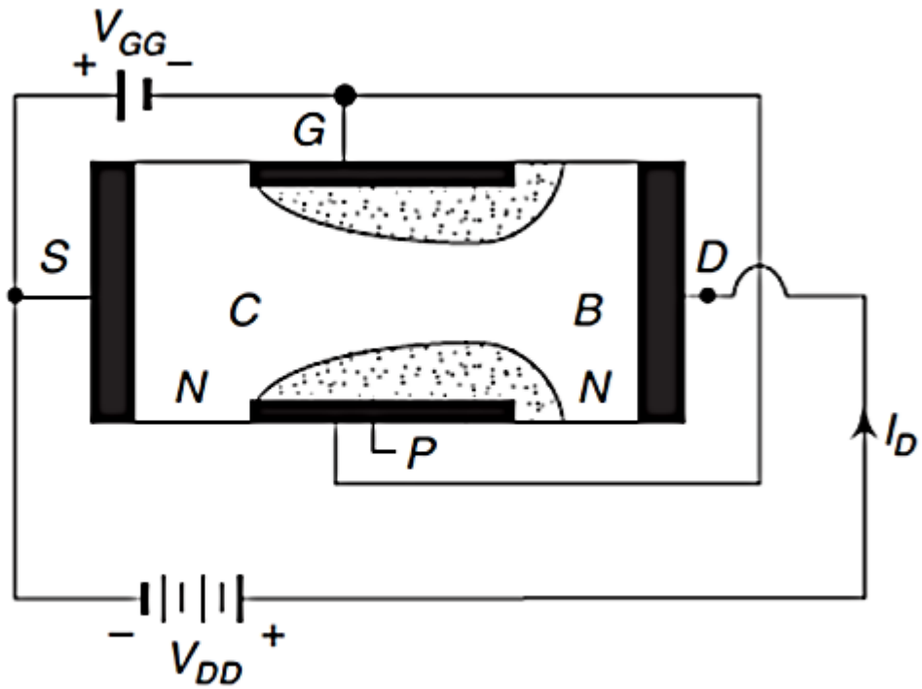


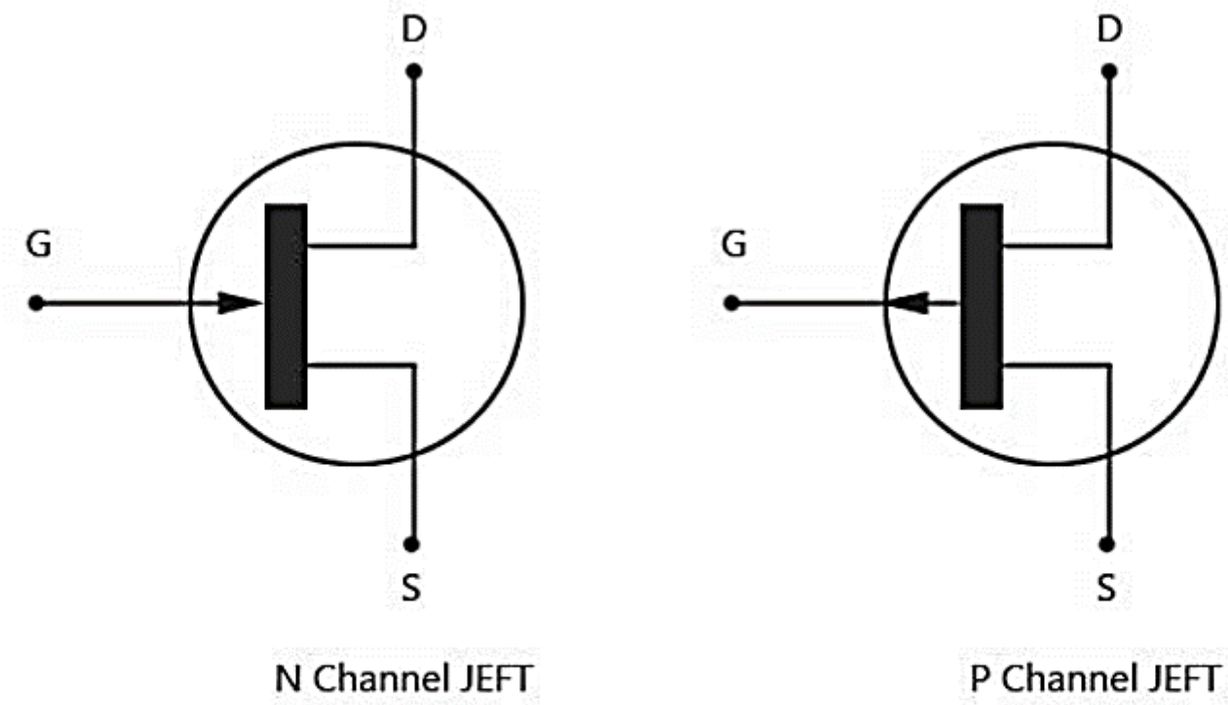
Fig. *JFET under applied bias*

RECAP ON JFET

JFET

JFET is a unipolar-transistor, which acts as a voltage controlled current device and is a device in which current at two electrodes is controlled by the action of an electric field at a p-n junction.

A JFET, or junction field-effect transistor, or JUGFET, is a FET in which the gate is created by reverse-biased junction (as opposed to the MOSFET which creates a junction via a field generated by conductive gate, separated from the gate region by a thin insulator).

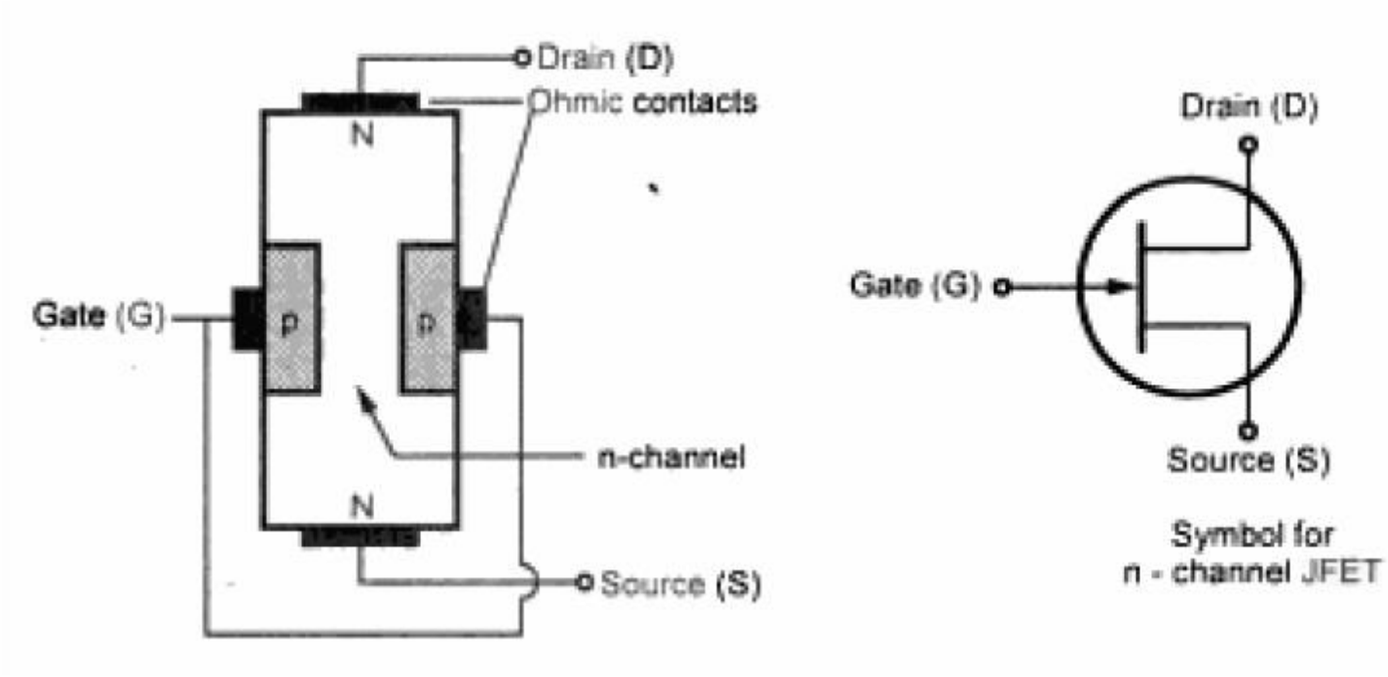


JFET-N-Channel and P-channel Schematic Symbol

Construction

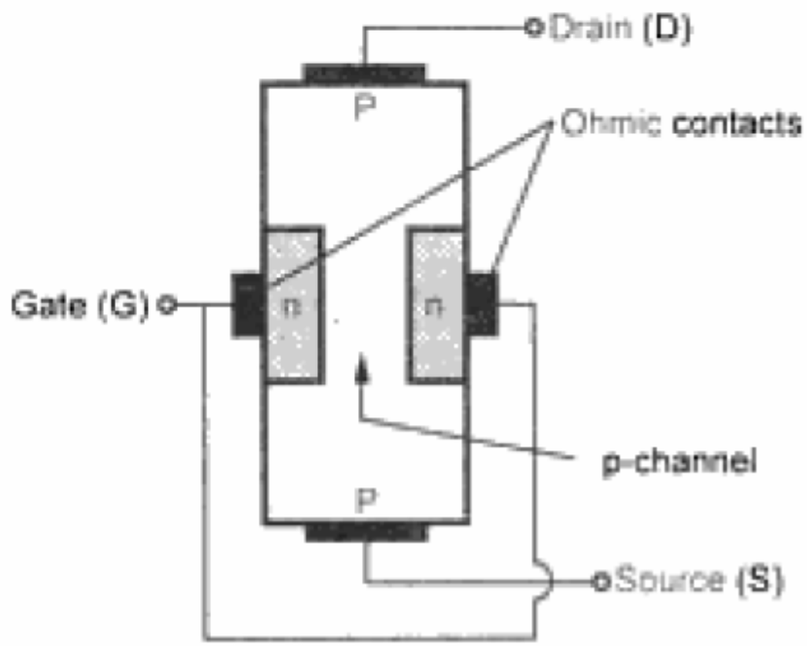
n-channel JFET

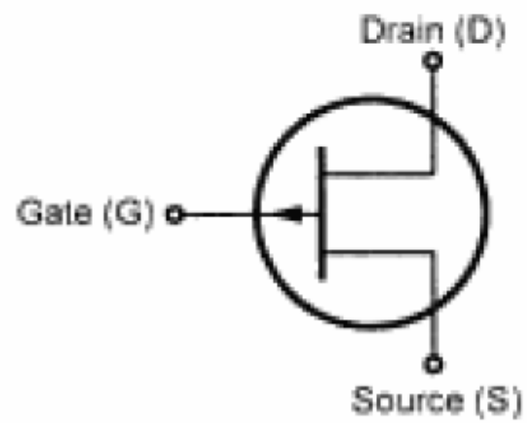
The figure shows construction and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and its two ends, two ohmic contacts are made which is the drain and source terminals of FET. Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the channel. Since this channel is in the n type bar, the FET is known as n-channel JFET.



p-channel JFET

The device could be made of p type bar with two n type gates as shown in the figure. This will be p-channel JFET. The principle of working of n-channel JFET and p-channel JFET are similar. The only difference being that in n-channel JFET the current is carried by electrons while in p-channel JFET, it is carried by holes.



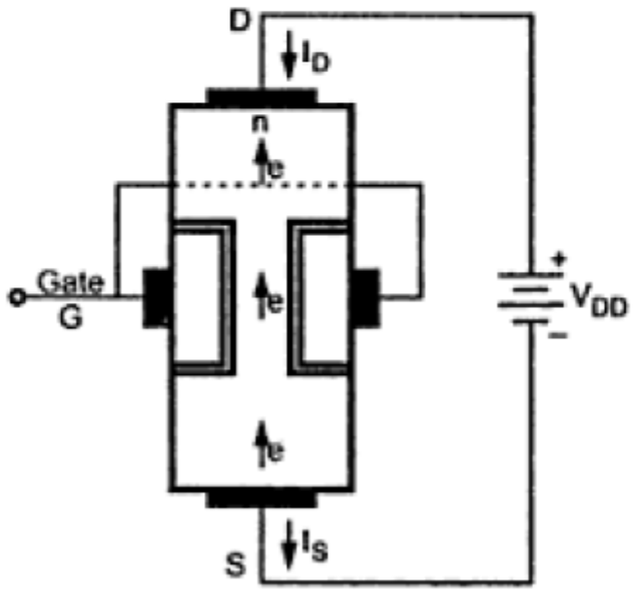


Symbol for p-channel JFET

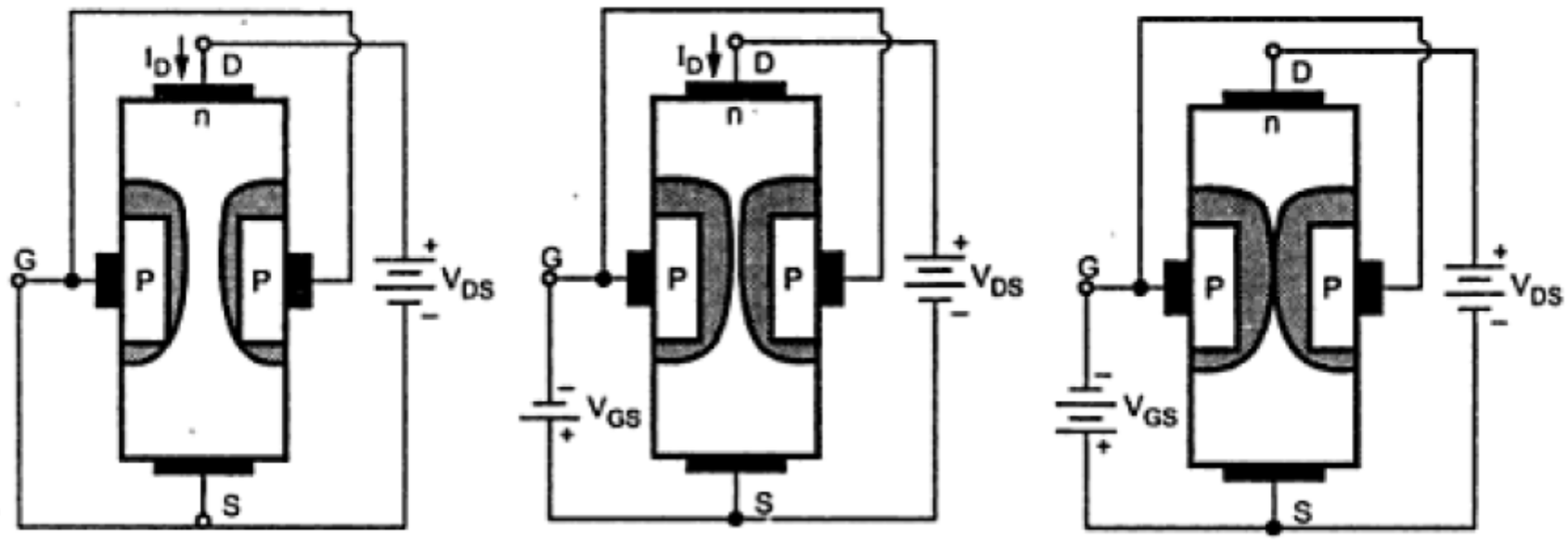
Operation

In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero. The gate current in JFET is often neglected and assumed to be zero.

Let us consider the circuit in the figure, voltage V_{DD} is applied between drain and source. Gate terminal is kept open. The bar is of n-type material. Due to the polarities of applied voltage as shown in the fig, the majority carriers i.e. the electrons start flowing from the source to the drain. The flow of electrons makes the drain current, I_D.



The majority carriers move from source to drain through the space between the gate regions. The space is commonly known as **channel.** The width of this channel can be controlled by varying the gate voltage. To see the effect of gate voltage on channel-width and on drain current I_D, consider the diagram below.



(a) No bias voltage on gates

(b) Small negative gate source bias

(c) Large negative gate source bias

The figure (a) shows that an n-channel JFET with the gate directly connected to the source terminal. When drain voltage V_{DS} is applied, a drain current I_D flows in the direction shown. Since the n-material is resistive, the drain current causes a voltage drop along the channel. This voltage drop reverse biases the pn junctions, and causes the depletion regions to penetrate into the channel. Since gate is heavily doped and the channel is lightly doped the width of the depletion region will mainly be spread in the channel as shown in fig (a). This penetration depends on the reverse bias voltage. From

the fig it can be observed that depletion region width is more at the drain side as compared to source side because near the junction, voltage at drain side is more than the voltage at the source side. This shows that reverse bias is not uniform near the junction as it gradually increases from source side to drain side.

The depletion region does not contain charge carriers. The space between two depletion regions is available for conducting portion of the channel. When reverse bias voltage is applied externally to the gate, the reverse bias will increase and hence increase the penetration of the depletion region which reduces the width of the conducting portion of the channel. When the width of the conducting portion of the channel reduces, the no. of electrons flowing from source to drain reduces and hence the current flowing from drain to source reduces.

When the external reverse bias voltage at the gate is increased as shown in fig (b) & (c) the depletion regions will increase more and at a particular stage the width of the depletion region will be equal to the original width of the depletion regions will increase more and more, and stage will come when the width of the depletion regions will be equal to the original width of the channel, leaving zero width for conducting portion of the channel, as shown in the fig (c). This will prevent any current flow from drain to source and this will cut off the drain current. The gate to source voltage that produces cutoff is known as cutoff voltage ($V_{GS\ (OFF)}$).

When the gate is shorted to source, there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and conducting channel width maximum. In this case maximum drain current flows which is designated by I_{DSS} and this is the possible drain current in JFET. It is clear that the gate to source voltage controls the current flowing through the channel and hence FET is also called **voltage controlled current source.**

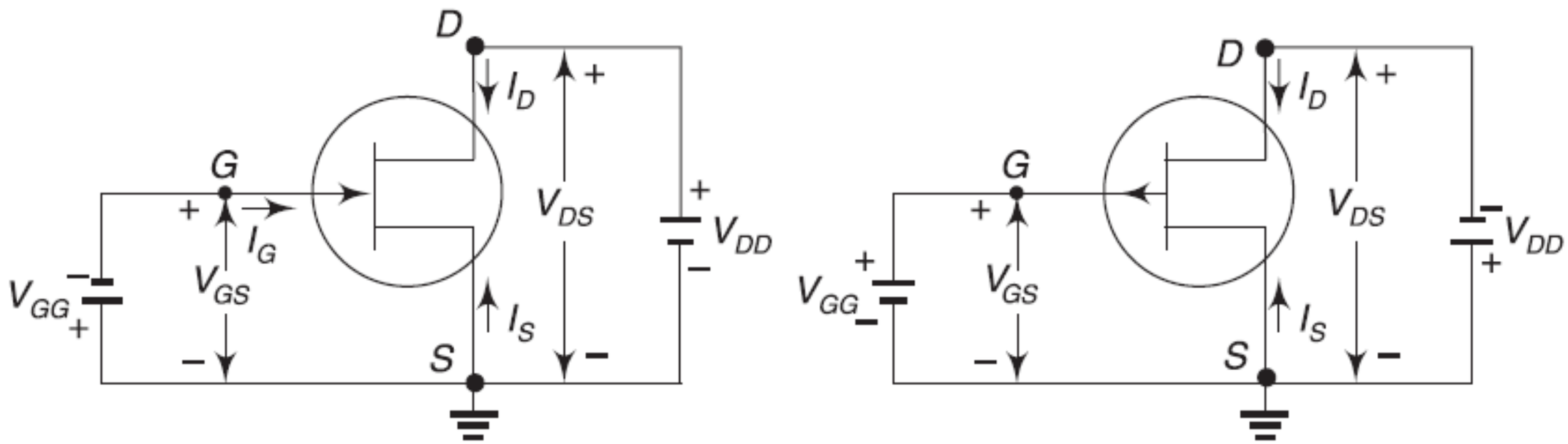


Fig. *Circuit symbols for N- and P-channel JFET*

Characteristics

Drain (or) current voltage characteristics of JFET

The current voltage characteristics of an n-channel JFET is shown in the figure. The drain current (I_D) is plotted with V_{DS} for different values of V_{GS}. This characteristic is also known as drain characteristics of JFET. From the fig, we see that as the voltage increased from 0 to a few volts, the current increases as determined by ohm's law. The straight nature of the curve at low values for V_{DS} reveals that for this region the resistance is essentially constant for a fixed valued of V_{GS}. But the slope of the I_D - V_{DS} curve near the origin is a function of the gate voltage. This region of operation is known as the linear region or ohmic region. As V_{DS} increases and approaches a value V_P (referred to as pinch – off voltage), slope of the curve changes and the channel resistance increases. If V_{DS} increases beyond pinch-off value, characteristics curve becomes more horizontal and I_D maintains a saturation level. For V_{GS} = 0v , the saturated value of I_D is designated as I_{DSS} , which is the drain – to – source current with source – gate short circuit. Thus, I_{DSS} is the maximum drain current for a JFET, obtained under the conditions V_{GS} = 0V and $V_{DS} > |V_P|$. As the V_{DS} increases beyond V_P, the level of I_D remains essentially the same and this region of the characteristics is known as saturation region.

It may also be noted that once $V_{DS} > V_{p,}$ the JFET has the characteristics of a current source. Thus the current – voltage characteristics displayed in fig can be divided into ohmic (linear) and saturation regions with the pinch-off condition as the boundary.

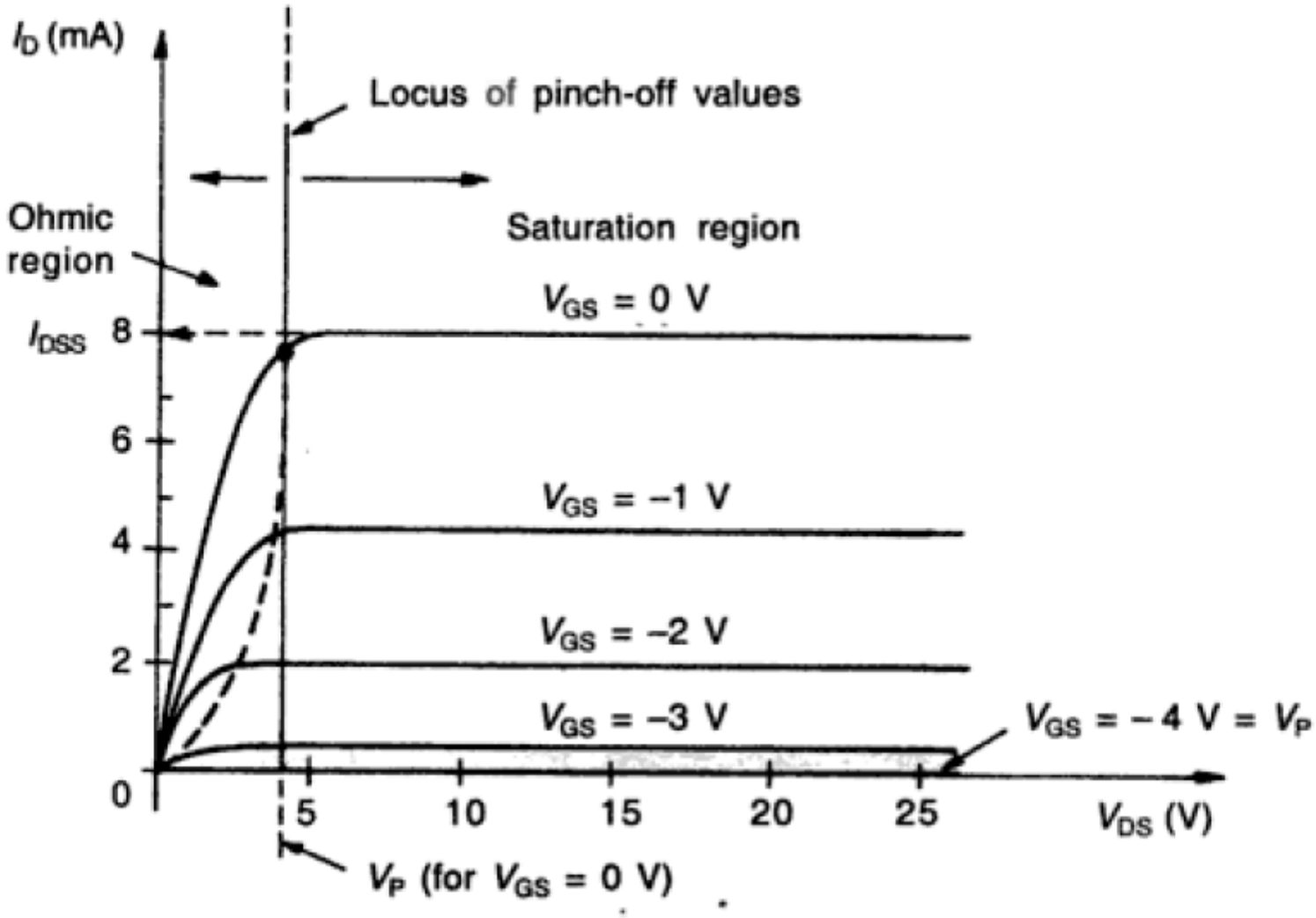


Fig. DRAIN CHARACTERISTICS OF JFET

V_{GS}

② Cutoff Region

As the negative bias of V_{GS} increases, depletion region forms similar to those to those with V_{GS} = 0 V but at a lower level of V_{DS}. Thus, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS}, as shown in the fig. it is seen that $V_{GS} = -V_P$, the saturation level of I_D is essentially 0mA and the devices have been turned off. The region of the right of the pinch-off locus in figure is normally employed in linear amplifiers. The region to the left of the pinch-off locus is referred to as *voltage controlled resistance region*, where the JFET can be used as voltage-controlled resistor. The channel resistance (R_D) increases with increase of V_{GS} values and empirical relation between the two is given by

③ Ohmic Region

Ohmic Region $V \propto I$

$$R_D = \frac{R_0}{[1 - (V_{GS}/V_P)]^2}$$

Where R_0 is the resistance with V_{GS} = 0. For an n-channel JFET with R_0 = 10kΩ at V_{GS} = -2V.

$= -2V$

4 Breakdown Region of JFET :-

The drain currents suddenly rise in an unbounded manner at very high levels of V_{DS}. The vertical rise in current is an indication that breakdown has occurred and the current through the channel is now limited solely by external circuit. In practical applications, the level of V_{DS} is kept less than the breakdown voltages (V_{DSmax}) that are mentioned in specification sheets of JFET.

Transfer characteristics

The transfer characteristics of JFET is a plot of output (drain) current versus input controlling quantity (gate-source voltage) and is used extensively in JFET amplifiers. In contrast to linear input-output relationship of BJT ($I_C = \beta I_B$), the input-output relationship of JFET is not linear. The relationship between I_D and V_{GS} is defined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The squared term on the right-hand side of the equation suggests that the relationship of I_D vs V_{GS} is nonlinear and exponential in nature. The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed. The transfer curve can be obtained using Shockley's equation or from the o/p characteristics.

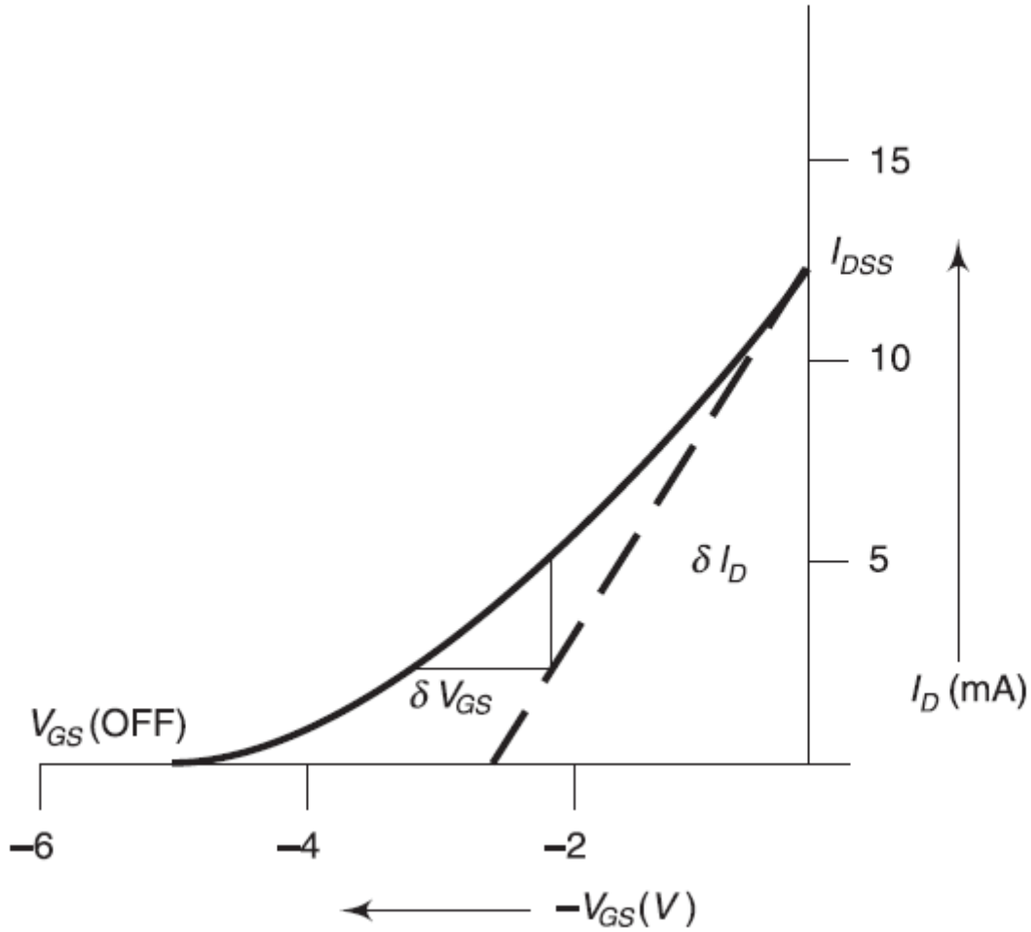


Fig. TRANSFER CHARACTERISTICS OF JFET

For the transfer characteristics, V_{DS} is maintained constant at a suitable value greater than the pinch-off voltage V_P. The gate voltage V_{GS} is decreased from zero till I_D is reduced to zero. The transfer characteristics I_D versus V_{GS} is shown in Fig. . The shape of the transfer characteristic is very nearly a parabola. It is found that the characteristic is approximately represented by the parabola,

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \qquad (1)$$

where I_{DS} is the saturation drain current, I_{DSS} is the value of I_{DS} when $V_{GS} = 0$, and V_P is the pinch-off voltage.

Differentiating Eq. with respect to V_{GS} we can obtain an expression for g_m.

$$\frac{\partial I_{DS}}{\partial V_{GS}} = I_{DSS} \times 2\left(1 - \frac{V_{GS}}{V_P}\right)\left(-\frac{1}{V_P}\right)$$

We know that $g_m = \dfrac{\delta I_{DS}}{\delta V_{GS}}$, V_{DS} is constant.

Therefore, $$g_m = \frac{-2\, I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right) \qquad (2)$$

From (1),

$$\left(1 - \frac{V_{GS}}{V_P}\right) = \sqrt{\frac{I_{DS}}{I_{DSS}}}$$

Substituting this value in Eq (2) , we get

$$g_m = \frac{-2\sqrt{I_{DS}\, I_{DSS}}}{V_P} \qquad (3)$$

Suppose $g_m = g_{mo}$, when $V_{GS} = 0$,

$$g_{mo} = -\frac{2I_{DSS}}{V_P}$$

Therefore, From (2)

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_P}\right) \qquad (4)$$

Equation (3) shows that g_m varies as the square root of the saturation drain current I_{DS}, and Eq. (4) shows that g_m decreases linearly with increase of V_{GS}.

SLOPE OF THE TRANSFER CHARACTERISTIC AT I_{DSS}

From equation (3) we have

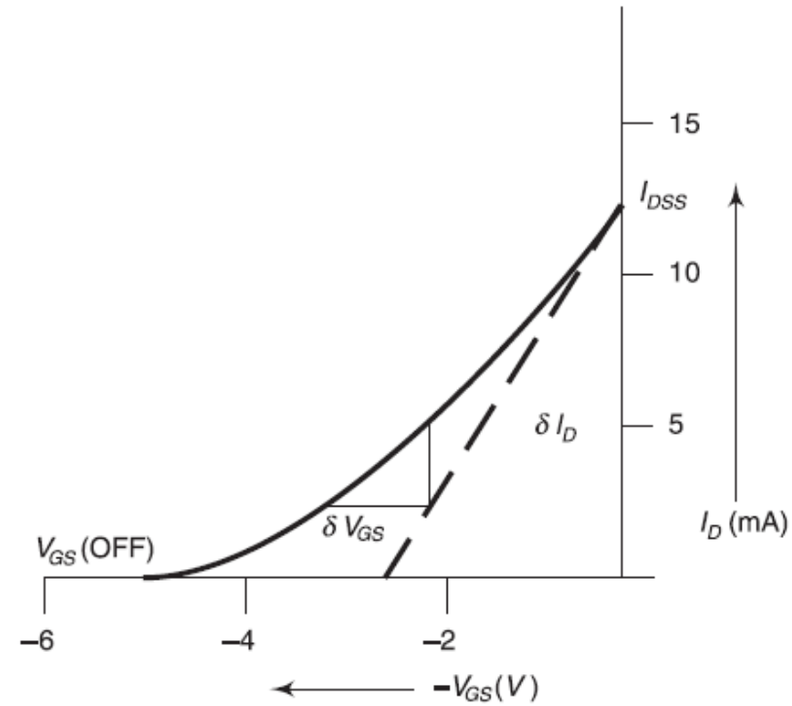
$$g_m = \frac{-2\sqrt{I_{DS}\, I_{DSS}}}{V_P}$$

or

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2\sqrt{I_{DS}\, I_{DSS}}}{V_P}$$

Substituting $I_{DS} = I_{DSS}$,

$$\frac{\partial I_{DS}}{\partial V_{GS}} = -\frac{2I_{DSS}}{V_P} = \frac{I_{DSS}}{\frac{-V_P}{2}}$$



This equation shows that the tangent to the curve at $I_{DS} = I_{DSS}$, $V_{GS} = 0$, will have an intercept at $\frac{-V_P}{2}$ on the axis of V_{GS} as shown in Fig. . Therefore, the value of V_P can be found by drawing the tangent at $I_{DS} = I_{DSS}$, $V_{GS} = 0$.

The gate-source cut off voltage, $V_{GS(off)}$, on the transfer characteristic is equal to the pinch off voltage, V_P, on the drain characteristics, i.e., $V_P = |V_{GS(off)}|$.

Therefore,

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

RECAP ON JFET DRAIN CHARACTERISTICS

FET CHARACTERISTICS

(i) As V_{DS} is increased from zero, I_D increases along OP, and the rate of increase of I_D with V_{DS} decreases as shown in Fig. . The region from $V_{DS} = 0V$ to $V_{DS} = V_P$ is called the ohmic region. In the channel ohmic region, the drain to source resistance $\frac{V_{DS}}{I_D}$ is related to the gate voltage V_{GS}, in an almost linear manner. This is useful as a voltage variable resistor (VVR) or voltage dependent resistor (VDR).

(ii) When $V_{DS} = V_P$, I_D becomes maximum. When V_{DS} is increased beyond V_P, the length of the pinch-off or saturation region increases. Hence, there is no further increase of I_D.

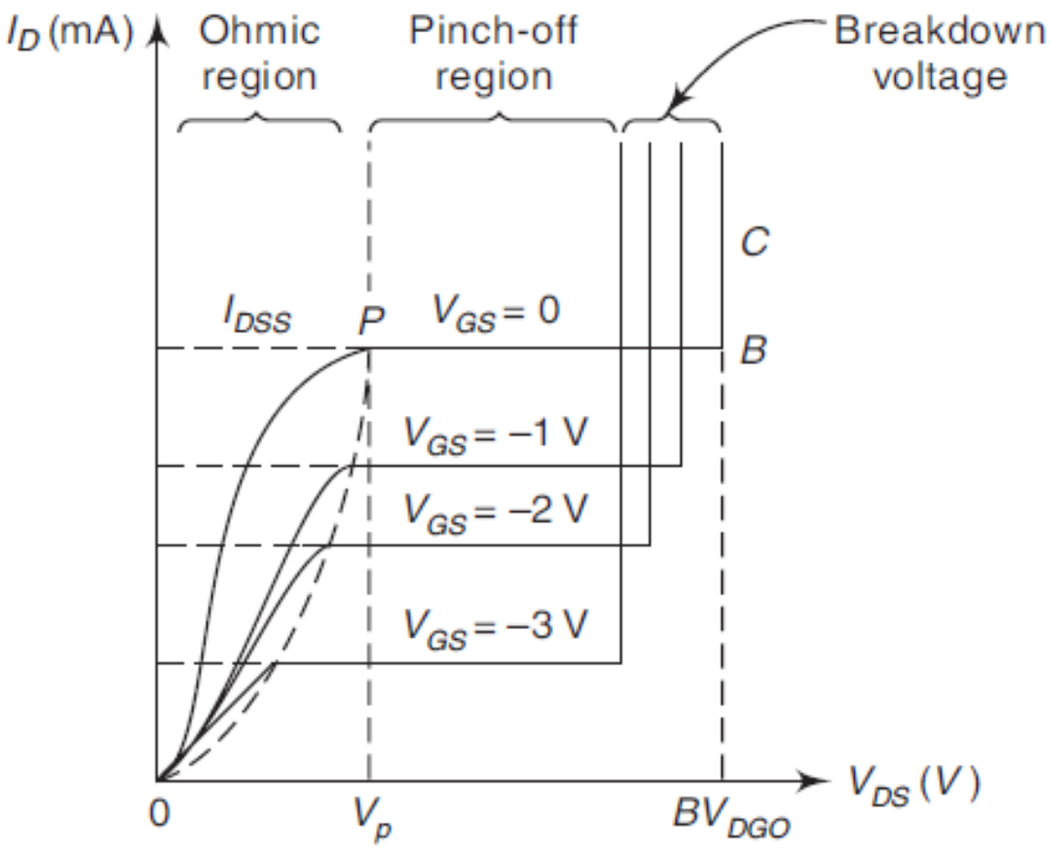


Fig. *Drain characteristics*

(iii) At a certain voltage corresponding to the point B, I_D suddenly increases. This effect is due to the Avalanche multiplication of electrons caused by breaking of covalent bonds of silicon atoms in the depletion region between the gate and the drain. The drain voltage at which the breakdown occurs is denoted by BV_{DGO}. The variation of I_D with V_{DS} when $V_{GS} = 0$ is shown in Fig. by the curve $OPBC$.

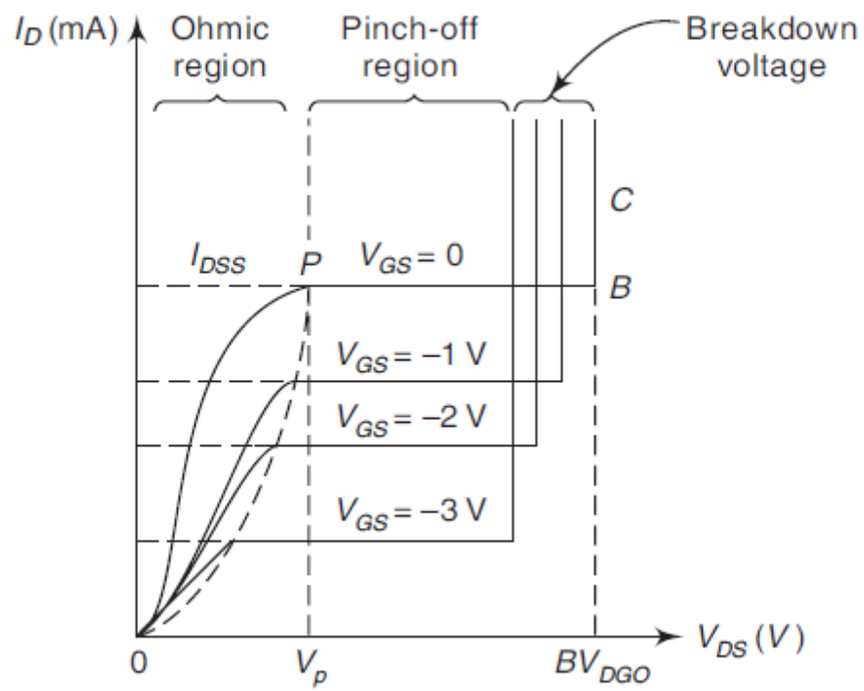


Fig. *Drain characteristics*

When V_{GS} is negative and V_{DS} is increased When the gate is maintained at a negative voltage less than the negative cut-off voltage, the reverse voltage across the junction is further increased. Hence for a negative value of V_{GS}, the curve of I_D versus V_{DS} is similar to that for $V_{GS} = 0$, but the values of V_P and BV_{DGO} are lower, as shown in Fig. 3.3.

From the curves, it is seen that above the pinch-off voltage, at a constant value of V_{DS}, I_D increases with an increase of V_{GS}. Hence, a JFET is suitable for use as a voltage amplifier, similar to a transistor amplifier.

It can be seen from the curve that for voltage $V_{DS} = V_P$, the drain current is not reduced to zero. If the drain current is to be reduced to zero, the ohmic voltage drop along the channel should also be reduced to zero. Further, the reverse biasing to the gate-source *PN* junction essential for pinching off the channel would also be absent.

The drain current I_D is controlled by the electric field that extends into the channel due to reverse biased voltage applied to the gate; hence, this device has been given the name *Field Effect Transistor*.

In a bar of *P*-type semiconductor, the gate is formed due to *N*-type semiconductor. The working of the *P*-channel JFET will be similar to that of *N*-channel JFET with proper alterations in the biasing circuits; in this case holes will be the current carriers instead of electrons. The circuit symbols for *N*-channel and *P*-channel JFETs are shown in Fig. 3.4. It should be noted that the direction of the arrow points in the direction of conventional current which would flow into the gate if the *PN* junction was forward biased.

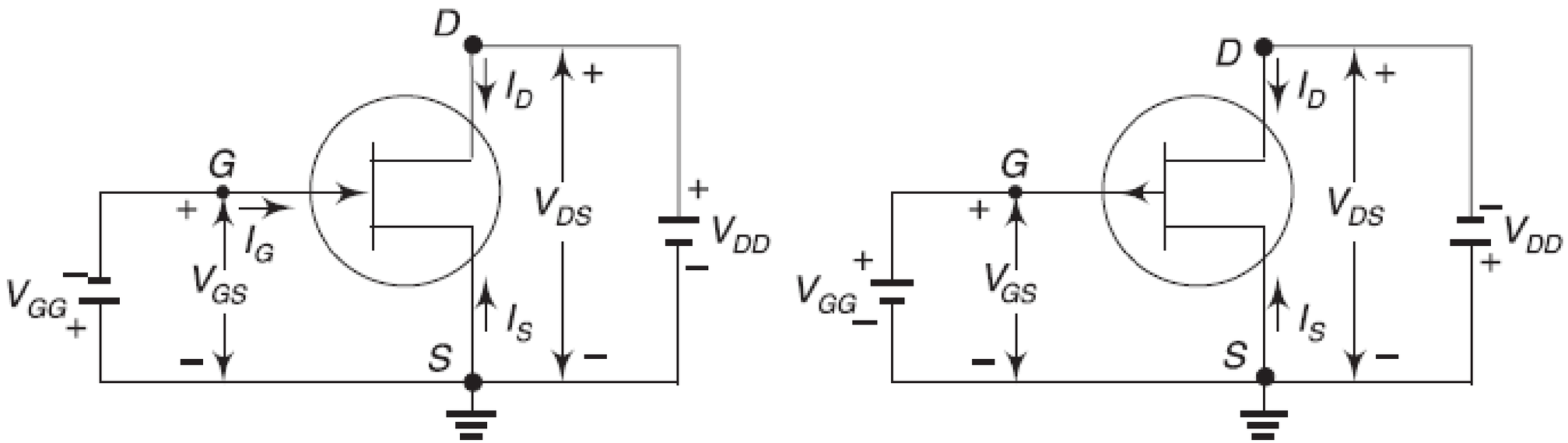


Fig. *Circuit symbols for N- and P-channel JFET*

CHARACTERISTIC PARAMETERS OF THE JFET

In a JFET, the drain current I_D depends upon the drain voltage V_{DS} and the gate voltage V_{GS}. Any one of these variables may be fixed and the relation between the other two are determined. These relations are determined by the three parameters which are defined below.

(1) Mutual conductance or transconductance, g_m It is the slope of the transfer characteristic curves, and is defined by

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} = \frac{\Delta I_D}{\Delta V_{GS}}, \; V_{DS} \text{ held constant.}$$

It is the ratio of a small change in the drain current to the corresponding small change in the gate voltage at a constant drain voltage. The change in I_D and V_{GS} should be taken on the straight part of the transfer characteristics. It has the unit of conductance in mho.

(2) Drain resistance, r_d It is the reciprocal of the slope of the drain characteristics and is defined by

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D}, \; V_{GS} \text{ held constant.}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the drain current at a constant gate voltage. It has the unit of resistance in ohms.

The drain resistance at $V_{GS} = 0$ V, i.e., when the depletion regions of the channel are absent, is called as *drain-source ON resistance,* represented as R_{DS} or $R_{DS(ON)}$.

The reciprocal of r_d is called the drain conductance. It is denoted by g_d or g_{ds}.

(3) Amplification factor, μ It is defined by

$$\mu = \left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} = -\frac{\Delta V_{DS}}{\Delta V_{GS}}, \; I_D \text{ held constant.}$$

It is the ratio of a small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current. Here, the negative sign shows that when V_{GS} is increased, V_{DS} must be decreased for I_D to remain constant.

(4) Relationship among FET parameters As I_D depends on V_{DS} and V_{GS}, the functional equation can be expressed as

$$I_D = f(V_{DS}, V_{GS})$$

If the drain voltage is changed by a small amount from V_{DS} to $(V_{DS} + \Delta V_{DS})$ and the gate voltage is changed by a small amount from V_{GS} to $(V_{GS} + \Delta V_{GS})$, then the corresponding small change in I_D may be obtained by applying Taylor's theorem with neglecting higher order terms. Thus the small change ΔI_D is given by

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS}$$

Dividing both the sides of this equation by ΔV_{GS}, we obtain

$$\frac{\Delta I_D}{\Delta V_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right) + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant, then $\frac{\Delta I_D}{\Delta V_{GS}} = 0$

Therefore, we have

$$0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \left(\frac{\Delta V_{DS}}{\Delta V_{GS}}\right)_{I_D} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

Substituting the values of the partial differential coefficients, we get

$$0 = \left(\frac{1}{r_d}\right)(-\mu) + g_m$$

Hence, $$\mu = g_m r_d$$

Therefore, amplification factor (μ) is the product of transconductance (g_m) and drain resistance (r_d).

(5) Power dissipation, P_D The FET's continuous power dissipation, P_D, is the product of I_D and V_{DS}.

(6) Pinch-off Voltage, V_P

The gate reverse voltage that removes all the free charge from the channel is called the pinch-off voltage V_P.

COMPARISON OF JFET AND BJT

1. FET operation depends only on the flow of majority carriers-holes for *P*-channel FETs and electrons for *N*-channel FETs. Therefore, they are called unipolar devices. Bipolar transistor (BJT) operation depends on both minority and majority current carriers.
2. As FET has no junctions and the conduction is through an *N*-type or *P*-type semiconductor material, FET is less noisy than BJT.
3. As the input circuit of FET is reverse biased, FET exhibits a much higher input impedance (in the order of 100 MΩ) and lower output impedance and there will be a high degree of isolation between input and output. So, FET can act as an excellent buffer amplifier but the BJT has low input impedance because its input circuit is forward biased.
4. FET is a voltage controlled device, i.e., voltage at the input terminal controls the output current, whereas BJT is a current controlled device, i.e., the input current controls the output current.

5. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
6. The performance of BJT is degraded by neutron radiation because of the reduction in minority-carrier lifetime, whereas FET can tolerate a much higher level of radiation since they do not rely on minority carriers for their operation.
7. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature co-efficient at high current levels which leads to thermal breakdown.
8. Since FET does not suffer from minority carrier storage effects, it has higher switching speeds and cut-off frequencies. BJT suffers from minority carrier storage effects and therefore has lower switching speed and cut-off frequencies.
9. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
10. BJTs are cheaper to produce than FETs.

APPLICATIONS OF JFET

1. FET is used as a buffer in measuring instruments, receivers since it has high input impedance and low output impedance.
2. FETs are used in RF amplifiers in FM tuners and in communication equipment for its low noise level.
3. Since the input capacitance is low, FETs are used in cascade amplifiers in measuring and test equipments.
4. Since the device is voltage controlled, it is used as a voltage variable resistor in operational amplifiers and tone controls.
5. FETs are used in mixer circuits in FM and TV receivers, and in communication equipment because inter modulation distortion is low.
6. It is used in oscillator circuits because frequency drift is low.
7. As the coupling capacitor is small, FETs are used in low frequency amplifiers in hearing aids and in inductive transducers.

USE OF JFET AS VOLTAGE-VARIABLE RESISTOR

FET is operated in the constant-current portion of its output characteristics for the linear applications. In the region before pinch-off, where V_{DS} is small, the drain to source resistance r_d can be controlled by the bias voltage V_{GS}. The FET is useful as a *Voltage Variable Resistor* (*VVR*) or *Voltage Dependent Resistor* (*VDR*).

In JFET, the drain-to-source conductance, $g_d = \dfrac{I_D}{V_{DS}}$ for small values of V_{DS}, which may also be expressed as,

$$g_d = g_{do}\left[1 - \left(\frac{V_{GS}}{V_P}\right)^{\frac{1}{2}}\right]$$

where g_{do} is the value of drain conductance when the bias voltage V_{GS} is zero.

The variation of the r_d with V_{GS} can be closely approximated by the empirical expression,

$$r_d = \frac{r_0}{1 - KV_{GS}}$$

where r_0 = drain resistance at zero gate bias, and K = a constant, dependent upon FET type.

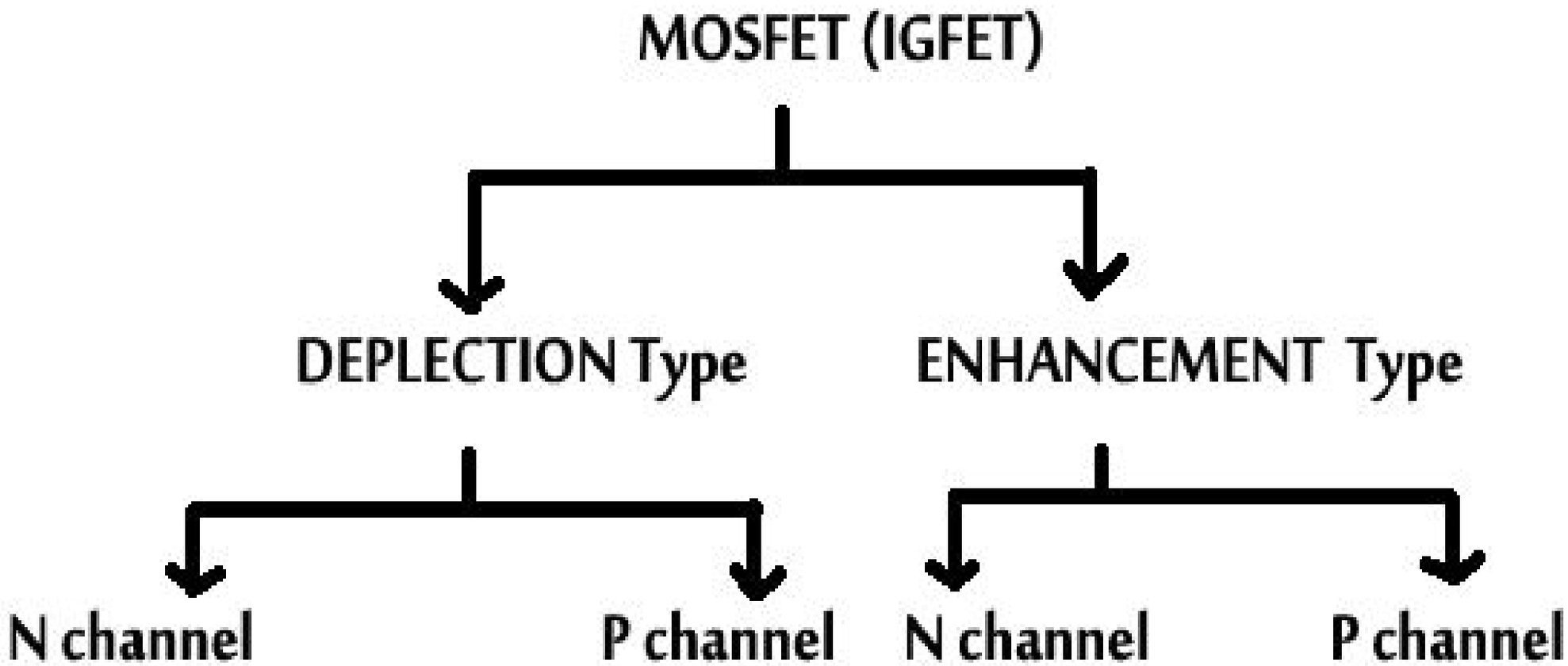
Thus, small signal FET drain resistance r_d varies with applied gate voltage V_{GS} and FET acts like a variable passive resistor.

FET finds wide applications where VVR property is useful. For example, the VVR can be used in Automatic Gain Control (AGC) circuit of a multistage amplifier.

MOSFET

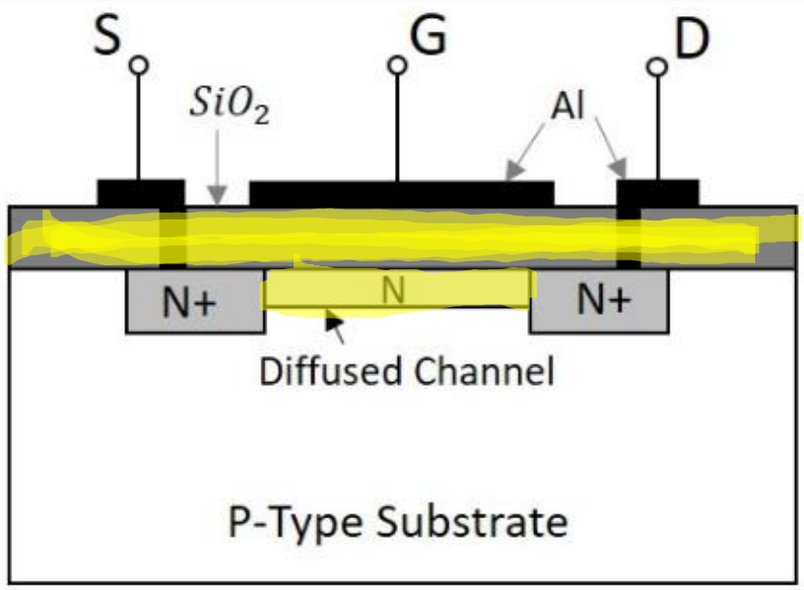
- The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) transistor is a semiconductor device which is widely used for switching and amplifying electronic signals in the electronic devices.
- The MOSFET is a core of integrated circuit and it can be designed and fabricated in a single chip because of these very small sizes.
- The MOSFET works by electronically varying the width of a channel along which charge carriers flow (electrons or holes).
- The charge carriers enter the channel at source and exit via the drain. The width of the channel is controlled by the voltage on an electrode is called gate which is located between source and drain.
- It is insulated from the channel near an extremely thin layer of metal oxide.

MOSFET (or) IGFET Insulated Gate FET


MOSFET (IGFET)
DEPLECTION Type
ENHANCEMENT Type
N channel
P channel
N channel
P channel

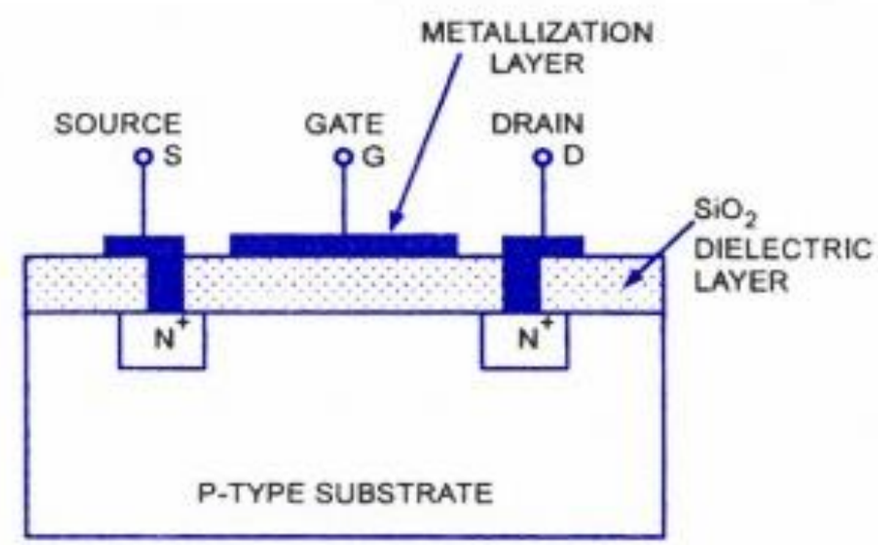
Construction – Depletion type & Enhancement type

Depletion type



Structure of N-channel MOSFET

Enhancement type



N-Channel E-MOSFET Structure

MOSFET Symbol

In Enhancement MOSFET, the channel does not exist initially and is induced i.e the channel is developed by applying a voltage greater than threshold voltage, at the gate terminals.

In depletion MOSFET, the channel is permanently fabricated (by doping) at the time of construction of MOSFET itself.

MOSFET: N-Channel Enhancement Type

MOSFET: P-Channel Enhancement Type

MOSFET: N-Channel Depletion Type

MOSFET: P-Channel Depletion Type

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

MOSFET is the common term for the Insulated Gate Field Effect Transistor (IGFET). There are two basic forms of MOSFET: (i) Enhancement MOSFET and (ii) Depletion MOSFET.

Principle By applying a transverse electric field across an insulator deposited on the semiconducting material, the thickness and hence the resistance of a conducting channel of a semiconducting material can be controlled.

In a depletion MOSFET, the controlling electric field reduces the number of majority carriers available for conduction, whereas in the enhancement MOSFET, application of electric field causes an increase in the majority carrier density in the conducting regions of the transistor.

ENHANCEMENT MOSFET

Construction The construction of an N-channel enhancement MOSFET is shown in Fig. (a) and the circuit symbols for an N-channel and a P-channel enhancement MOSFET are shown in Fig. (b) and (c), respectively. As there is no continuous channel in an enhancement MOSFET, this condition is represented by the broken line in the symbols.

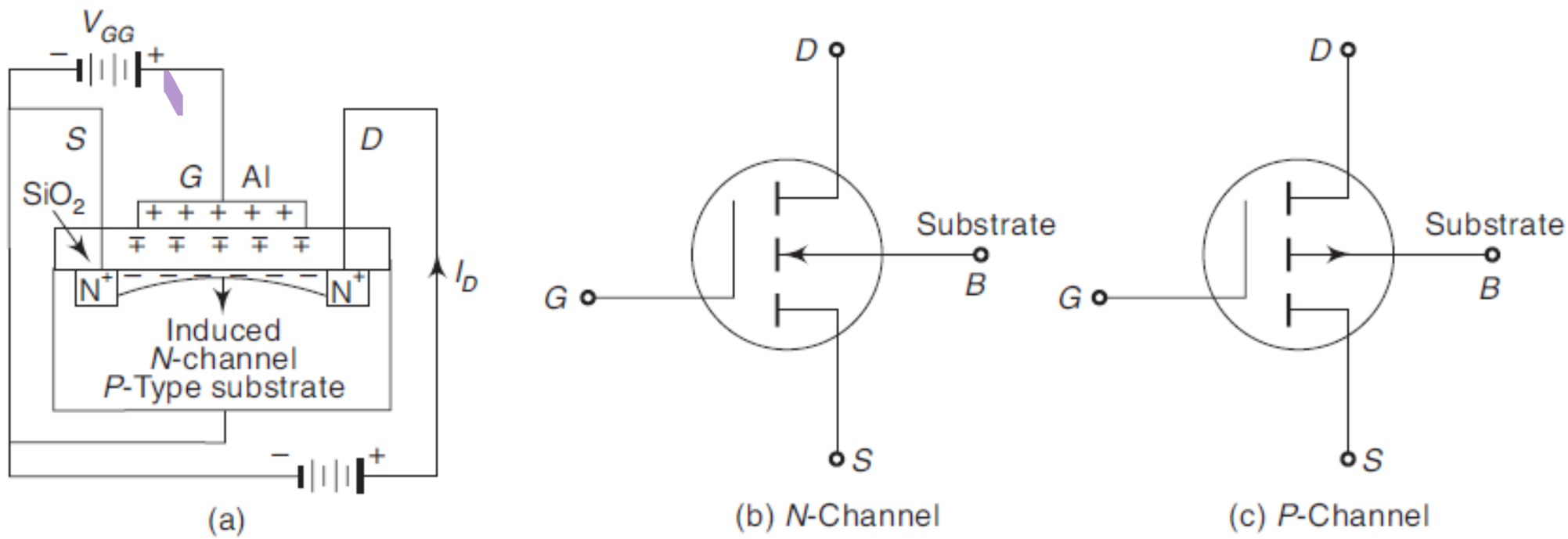


Fig. *(a) N-channel enhancement MOSFET, (b) and (c) Circuit symbols for enhancement MOSFET*

Two highly doped N^+ regions are diffused in a lightly doped substrate of P-type silicon substrate. One N^+ region is called the source S and the other one is called the drain D. They are separated by 1 mil (10^{-3} inch). A thin insulating layer of SiO_2 is grown over the surface of the structure and holes are cut into the oxide layer, allowing contact with source and drain. Then a thin layer of metal aluminium is formed over the layer of SiO_2. This metal layer covers the entire channel region and it forms the gate G.

The metal area of the gate, in conjunction with the insulating oxide layer of SiO_2 and the semiconductor channel forms a parallel plate capacitor. This device is called the insulated gate FET because of the insulating layer of SiO_2. This layer gives an extremely high input impedance for the MOSFET.

Operation If the substrate is grounded and a positive voltage is applied at the gate, the positive charge on *G* induces an equal negative charge on the substrate side between the source and drain regions. Thus, an electric field is produced between the source and drain regions. The direction of the electric field is perpendicular to the plates of the capacitor through the oxide. The negative charge of electrons which are minority carriers in the *P*-type substrate forms an inversion layer. As the positive voltage on the gate increases, the induced negative charge in the semiconductor increases. Hence, the conductivity increases and current flows from source to drain through the induced channel. Thus the drain current is enhanced by the positive gate voltage as shown in Fig.

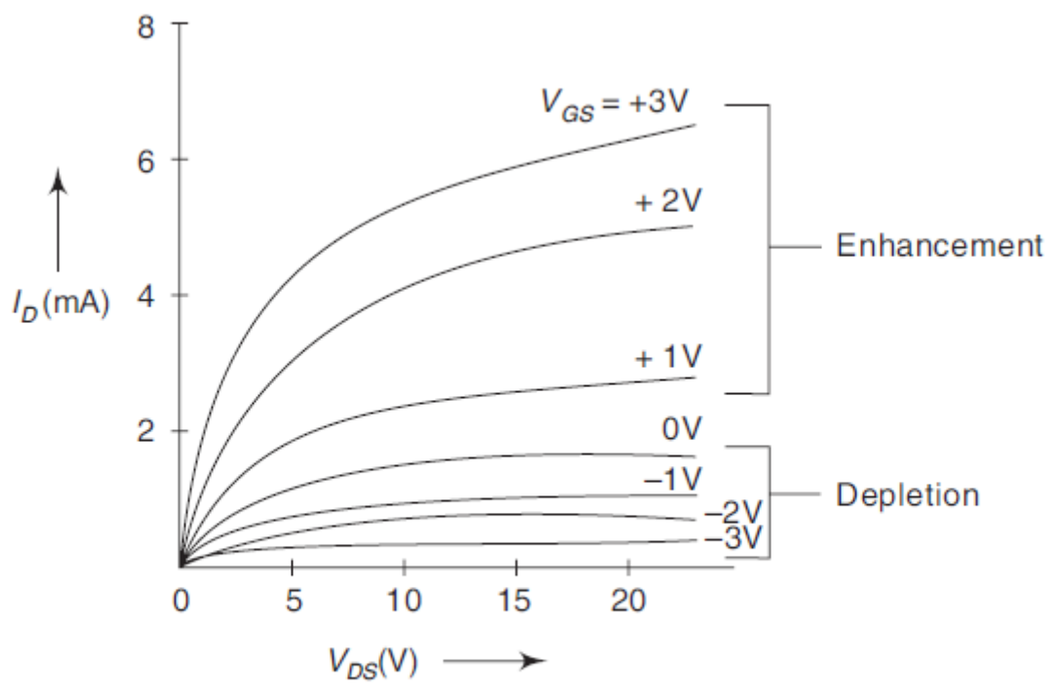


Fig. *Volt-ampere characteristics of MOSFET*

DEPLETION MOSFET

The construction of an N-channel depletion MOSFET is shown in Fig. (a) where an N-channel is diffused between the source and drain to the basic structure of MOSFET. The circuit symbols for an N-channel and a P-channel depletion MOSFET are shown in Figs (b) and (c), respectively.

With $V_{gs} = 0$ and the drain D at a positive potential with respect to the source, the electrons (majority carriers) flow through the N-channel from S to D. Therefore, the conventional current I_D flows through the channel D to S. If the gate voltage is made negative, positive charge consisting of holes is induced in the channel through SiO_2 of the gate-channel capacitor. The introduction of the positive charge causes depletion of mobile electrons in the channel. Thus a depletion region is produced in the channel. The shape of the depletion region depends on V_{GS} and V_{DS}. Hence the channel will be wedge shaped as shown in Fig. . When V_{DS} is increased, I_D increases and it becomes practically constant at a certain value of V_{DS}, called the pinch-off voltage. The drain current I_D almost gets saturated beyond the pinch-off voltage.

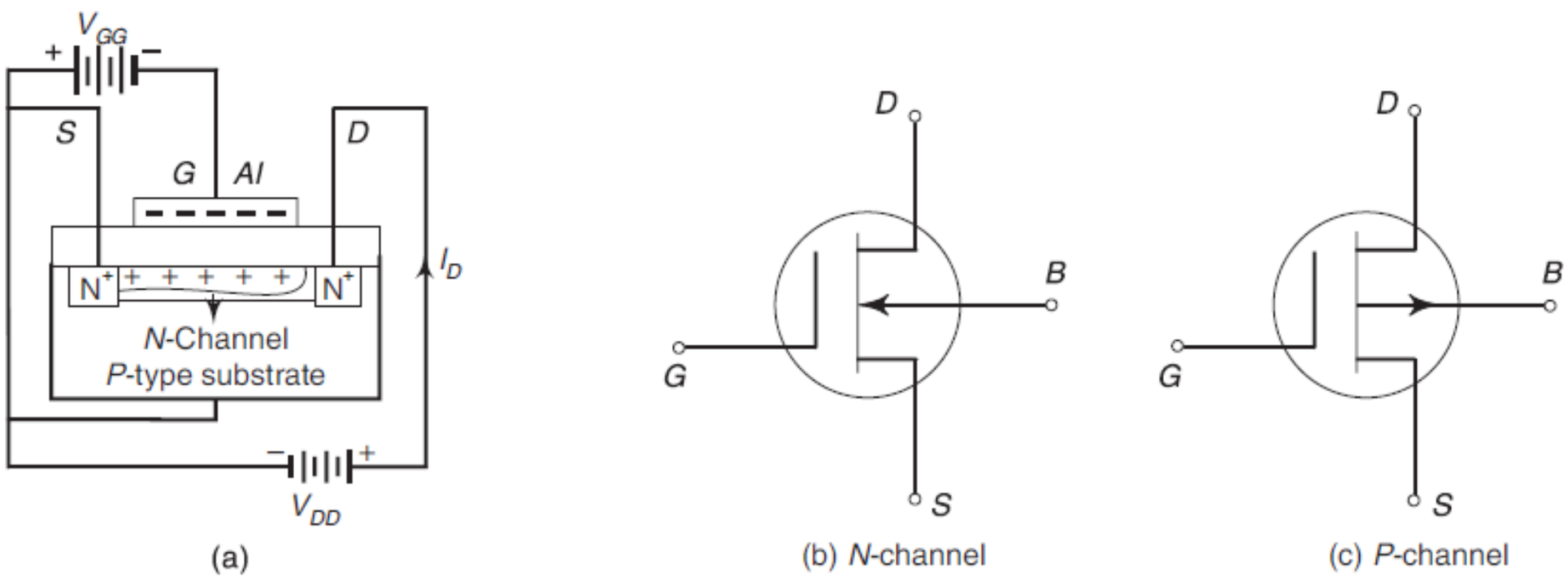


Fig. *(a) N-channel depletion MOSFET, (b) and (c) Circuit symbols for depletion MOSFETs*

Since the current in an FET is due to majority carriers (electrons for an N-type material), the induced positive charges make the channel less conductive, and I_D drops as V_{GS} is made negative.

The depletion MOSFET may also be operated in an enhancement mode. It is only necessary to apply a positive gate voltage so that negative charges are induced into the N-type channel. Hence, the conductivity of the channel increases and I_D increases. As the depletion MOSFET can be operated with bipolar input signals irrespective of doping of the channel, it is also called as *dual mode MOSFET*. The volt-ampere characteristics are indicated in Fig.

The curve of I_D versus V_{GS} for constant V_{DS}, as shown in Fig. is called the transconductance curve for D-MOSFET which is very similar to the curve for JFET. When V_{GS} is negative, $I_D < I_{DSS}$. When $V_{GS} = V_{GS(off)}$, I_D is decreased to approximately 0 mA. When V_{GS} is positive, $I_D > I_{DSS}$. Hence, I_{DSS} is not the maximum possible value for MOSFET.

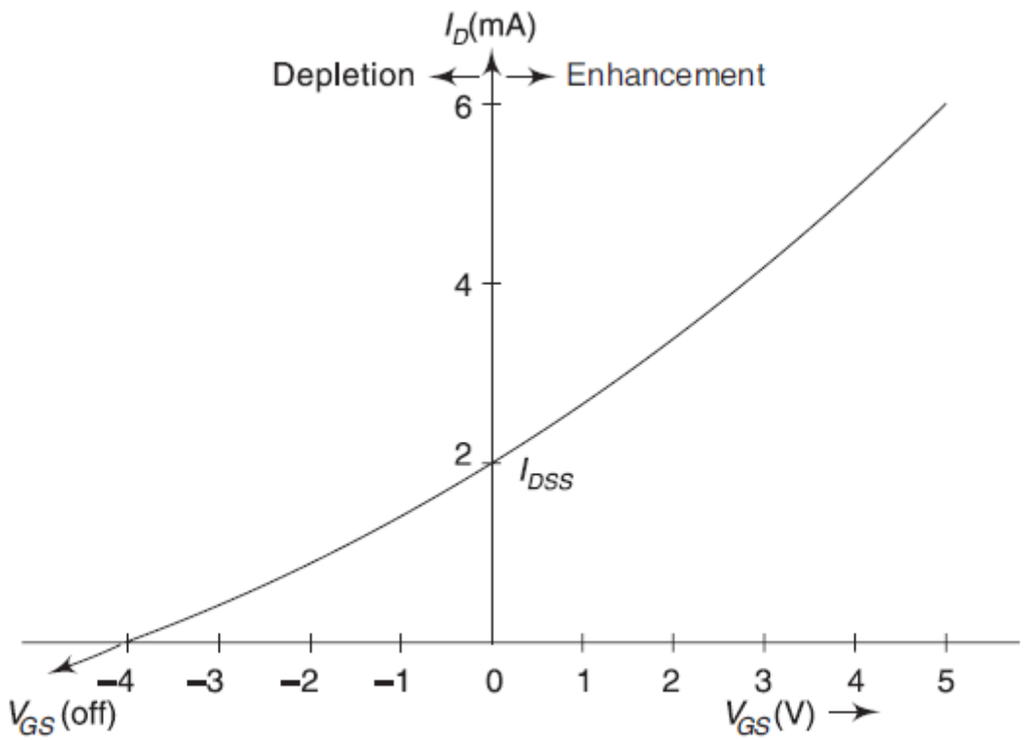


Fig. *Transfer characteristics of MOSFET*

. **Give the current-voltage relationship of the D-MOSFET and E-MOSFET.**

The current-voltage relationship of D-MOSFET is given by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The current-voltage relationship of E-MOSFET is given by

$$I_D = K_N(V_{GS} - V_T)^2$$

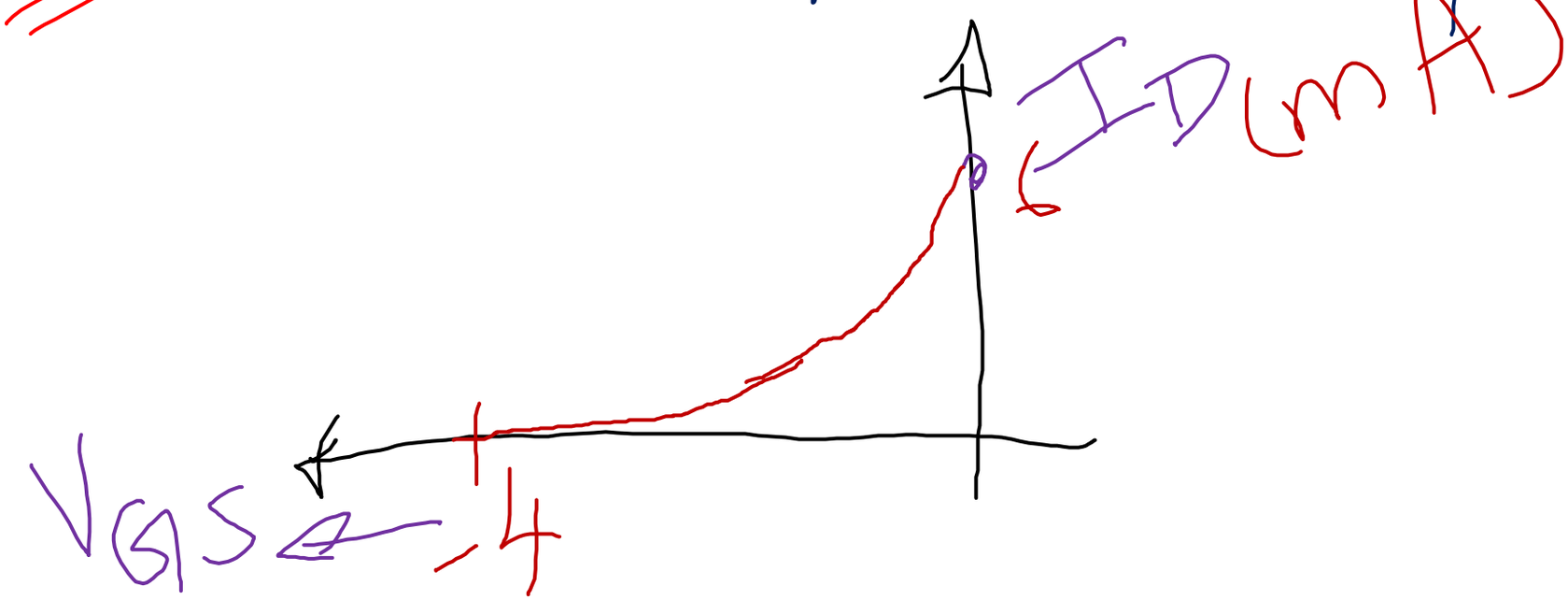
where $K_N = \dfrac{\mu_n \varepsilon W}{2aL}$ and this factor K_N is called a conduction parameter.

Transfer charac curve for p-channel JFET

$I_{DSS} = 6\,mA$, $V_P = 4V$

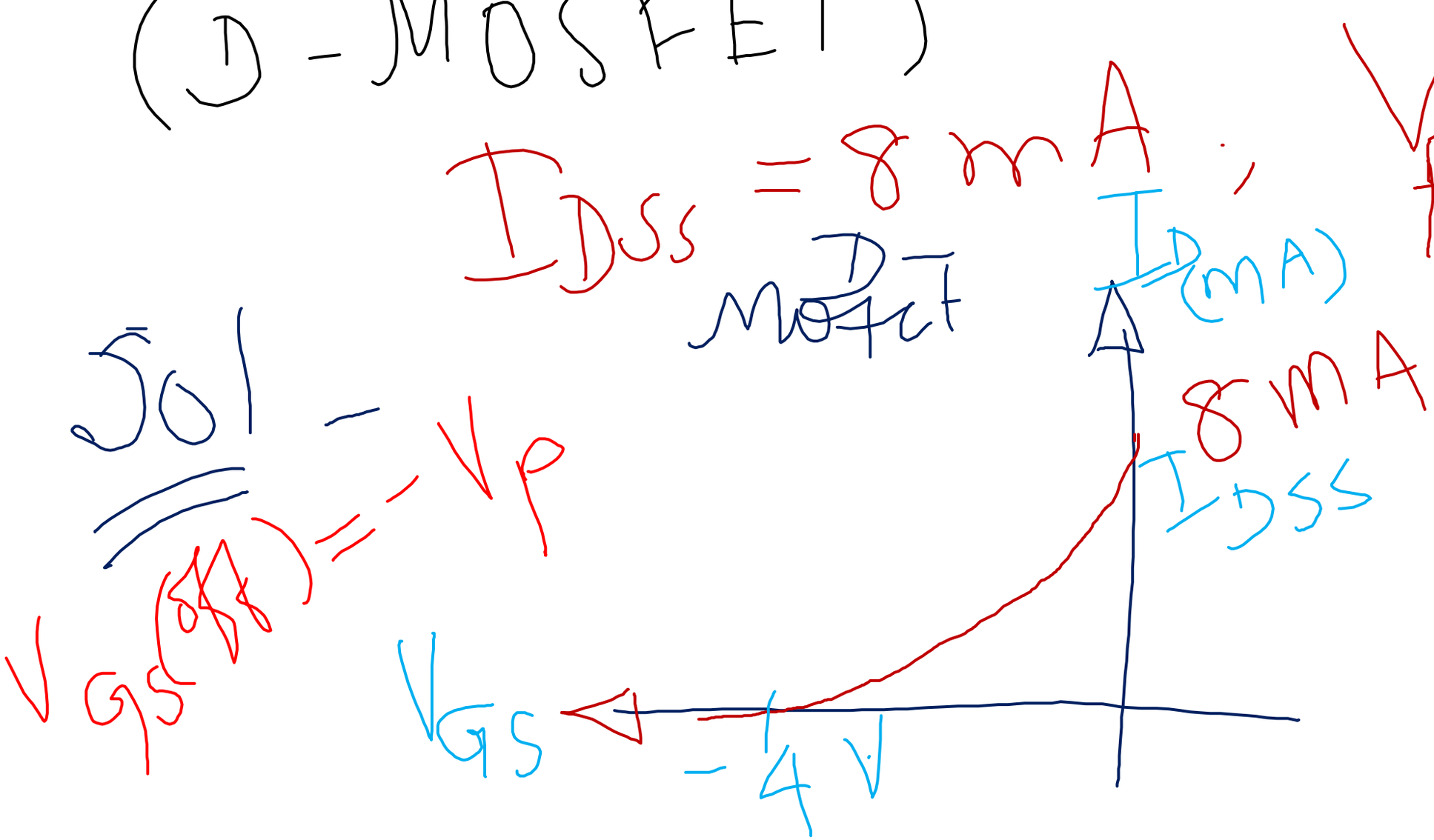
Sol:-

$V_{GS(off)} = -V_P$



Transfer characteristic curve for n-channel depletion MOSFET (D-MOSFET)

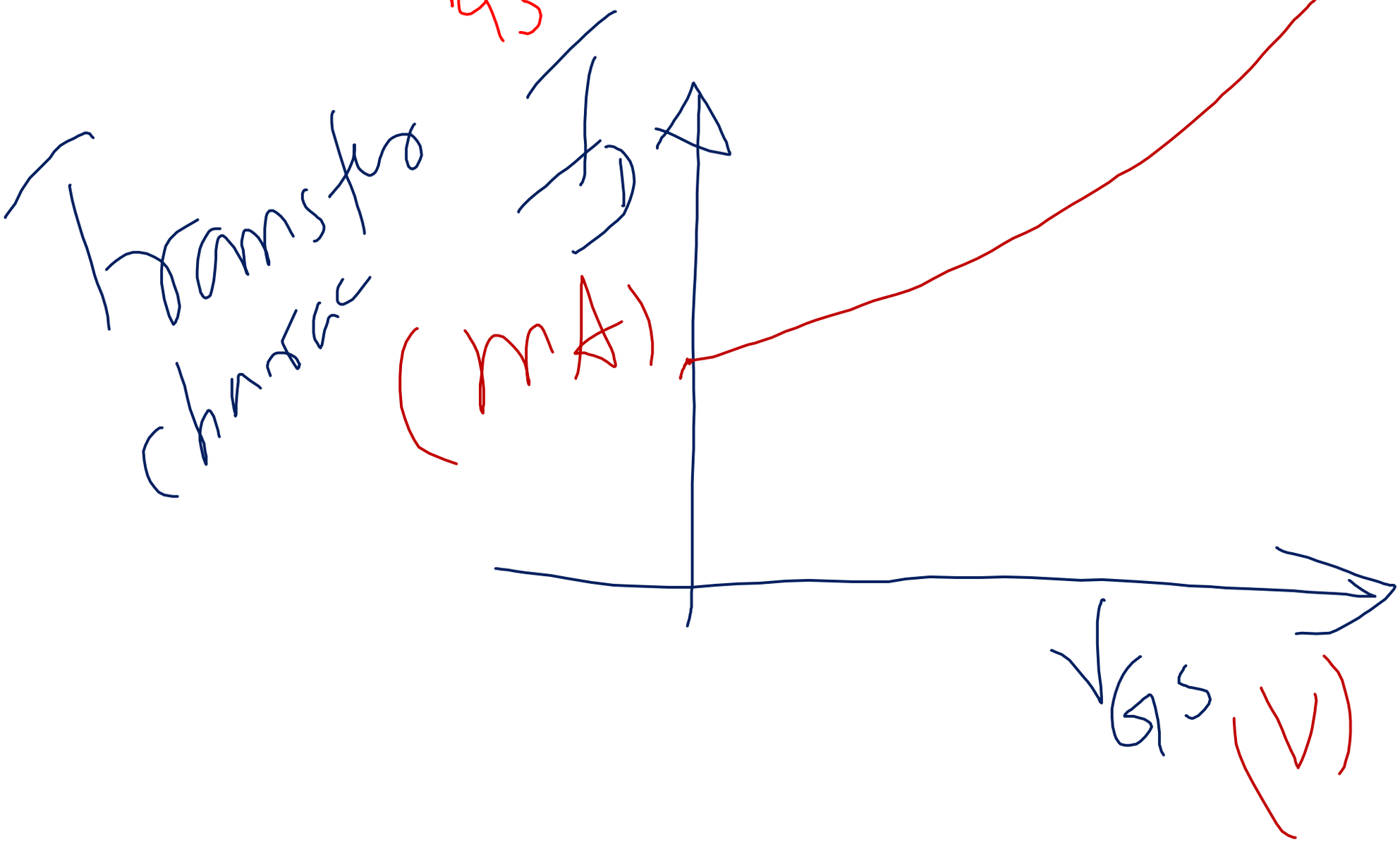
$I_{DSS} = 8\,mA$; $V_P = 4\,V$



Sol

E-MOSFET

V_{GS} → the value



Effect of Channel Length Modulation

In actual MOSFET characteristic as shown in Fig. a non-zero slope exists beyond the saturation point. For the saturation region, i.e., ($V_{DS} > V_{DS}$ (sat)), the effective channel length decreases and this phenomenon is called channel length modulation. For an N-channel device, the slope of the curve in the saturation region can be expressed by using the drain current I_D given by

$$I_D = K_N(V_{GS} - V_{TN})^2 (1 + \lambda V_{DS})$$

where λ is a positive quantity called the channel length modulation parameter or λ^{-1} is analogous to the early voltage in bipolar transistors, K_N is the conduction parameter and V_{TN} is the threshold voltage. The curves are extended so that the intercept at a point $I_D = 0$, $V_{DS} = -V_E$ which means that $V_E = 1/\lambda$.

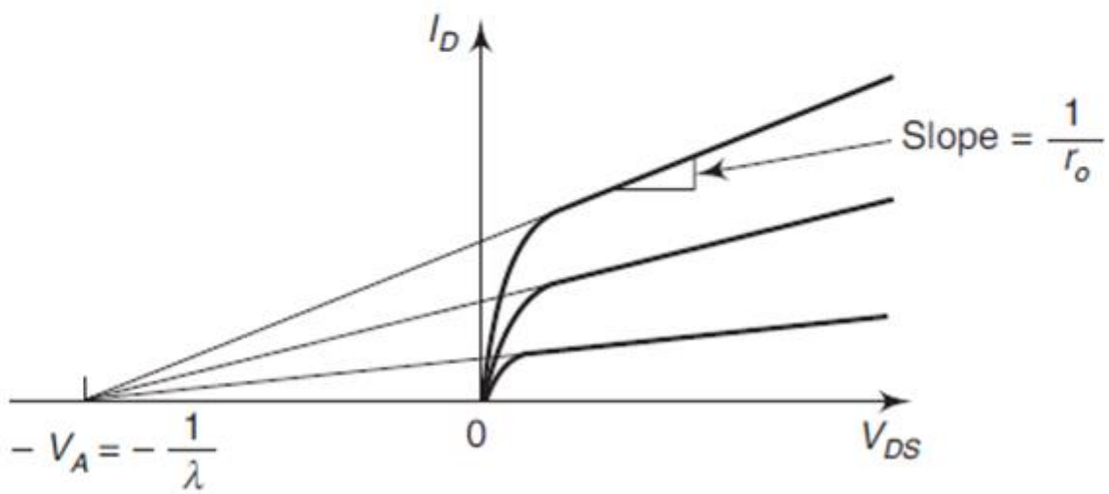


Fig. *Effect of channel length modulation due to the non-zero slope in the saturation region, resulting in a finite output resistance*

The output resistance due to the channel length modulation is expressed by

$$r_0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)\Bigg|_{V_{GS}} = \text{const.}$$

The output resistance can be determined at the Q-point by

$$= \left[\lambda I_{DSS}\left(1 - \frac{V_{GSQ}}{V_P}\right)^2\right]^{-1} = \frac{V_E}{I_{DQ}}$$

The output resistance is an important factor in the analysis of small signal equivalent circuit of MOSFET.

Temperature Effects

The threshold voltage V_{TN} or V_{TP} and conduction parameter K_N or K_P are functions of temperature. The magnitude of threshold voltage decreases with temperature and hence the drain current I_D increases with temperature at a given V_{GS}. The conduction parameter is directly proportional to mobility μ_n or μ_p of the carrier, which increases as the temperature decreases. Here the temperature dependent of mobility is larger than that of the threshold voltage. Hence the net effect of decreasing drain current at a given V_{GS} due to increase in temperature provides a negative feedback condition and hence the stability for a power MOSFET.

$I_{D\,MOSFET} \uparrow \propto$ Temp. $\uparrow$

COMPARISON OF MOSFET WITH JFET

1. In enhancement and depletion types of MOSFET, the transverse electric field induced across an insulating layer deposited on the semiconductor material controls the conductivity of the channel. In the JFET, the transverse electric field across the reverse biased *PN* junction controls the conductivity of the channel.
2. The gate leakage current in a MOSFET is of the order of 10^{-12} A. Hence the input resistance of a MOSFET is very high in the order of 10^{10} to 10^{15} Ω. The gate leakage current of a JFET is of the order of 10^{-9} A and its input resistance is of the order of 10^{8} Ω.
3. The output characteristics of the JFET are flatter than those of the MOSFET and hence, the drain resistance of a JFET (0.1 to 1 MΩ) is much higher than that of a MOSFET (1 to 50 kΩ).
4. JFETs are operated only in the depletion mode. The depletion type MOSFET may be operated in both depletion and enhancement mode.
5. Comparing to JFET, MOSFETs are easier to fabricate.
6. MOSFET is very susceptible to overload voltage and needs special handling during installation. It gets damaged easily if it is not properly handled.
7. MOSFET has zero offset voltage. As it is a symmetrical device, the source and drain can be interchanged. These two properties are very useful in analog signal switching.
8. Special digital CMOS circuits are available which involve near-zero power dissipation and very low voltage and current requirements. This makes them most suitable for portable systems.

COMPARISON OF *N*- WITH *P*-CHANNEL FETs

1. In an *N*-channel JFET the current carriers are electrons, whereas the current carriers are holes in a *P*-channel JFET.
2. Mobility of electrons is large in *N*-channel JFET; mobility of holes is poor in *P*-channel JFET.
3. The input noise in less in *N*-channel JFET than that of *P*-channel JFET.
4. The transconductance is larger in *N*-channel JFET than that of *P*-channel JFET.

PROBLEMS

When a reverse gate voltage of 12 V is applied to JFET, the gate current is 1 nA. Determine the resistance between gate and source.

Solution Given $V_{GS} = 12\text{ V}$ and $I_G = 10^{-9}\text{ A}$.

Therefore, gate-to-source resistance $= \dfrac{V_{GS}}{I_G} = \dfrac{12}{10^{-9}} = 12{,}000\text{ M}\Omega$

When the reverse gate voltage of JFET changes from 4.0 to 3.9 V, the drain current changes from 1.3 to 1.6 mA. Find the value of transconductance.

Solution

$$\Delta V_{GS} = 4.0 - 3.9 = 0.1\text{ V}$$

$$\Delta I_D = 1.6 - 1.3 = 0.3\text{ mA}$$

Therefore, transconductance, $g_m = \dfrac{\Delta I_D}{\Delta V_{GS}} = \dfrac{0.3 \times 10^{-3}}{0.1} = 3\text{ m}\,\Omega^{-1}$

A FET has a drain current of 4 mA. If I_{DSS} = 8 mA and $V_{GS(off)}$ = –6 V. Find the values of V_{GS} and V_P.

Solution The drain current, $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$

$$4 = 8\left[1 + \frac{V_{GS}}{6}\right]^2$$

$$1 + \frac{V_{GS}}{6} = \sqrt{\frac{4}{8}} = \frac{1}{\sqrt{2}} = 0.707$$

Therefore, $V_{GS} = -1.76$ V

$$V_P = |V_{GS(off)}| = 6 \text{ V}$$

An N-channel JFET has I_{DSS} = 8 mA and V_P = – 5 V. Determine the minimum value of V_{DS} for pinch-off region and the drain current I_{DS}, for V_{GS} = – 2 V in the pinch-off region.

Solution The minimum value of V_{DS} for pinch-off to occur for $V_{GS} = -2$ V is

$$V_{DS\,\min} = V_{GS} - V_P = -2 - (-5) = 3 \text{ V}$$

$$I_{DS} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$= 8 \times 10^{-3}\,[1 - (-2)/(-5)]^2 = 2.88 \text{ mA}$$

Determine the pinch-off voltage for an N-channel silicon FET with a channel width of 5.6×10^{-4} cm and a donor concentration of 10^{15} /cm^3. Given, the dielectric constant of Si is 12.

Solution Given $N_D = 10^{15}/\text{cm}^3 = 10^{21}/\text{m}^3$, $\varepsilon = \varepsilon_r\,\varepsilon_o = 12\,\varepsilon_0$ and

$a = 5.6 \times 10^{-4}$ cm $= 5.6 \times 10^{-6}$m

The pinch-off voltage, $|V_P| = \dfrac{qN_D}{2\varepsilon}\,a^2$

where ε = dielectric constant of channel material (Si) = $\varepsilon_r\,\varepsilon_0 = 12\,\varepsilon_0$

q = magnitude of electronic charge

a is in metres and N_D is in electrons/m^3

$$|V_P| = \frac{1.602 \times 10^{-19} \times 10^{21}}{2 \times 12 \times 8.854 \times 10^{-12}} \times (5.6 \times 10^{-6})^2 = 23.6 \text{ V}$$

For a *P*-channel silicon FET, with an effective channel width, $a = 2 \times 10^{-4}$ cm and channel resistively $\rho = 20\ \Omega$-cm, find the pinch-off voltage.

Solution We know that the pinch-off voltage for *P*-channel FET, $V_P = \frac{qN_A}{2\varepsilon} \times a^2$

For silicon, $\varepsilon = 12\ \varepsilon_0$ and $\mu_p = 500\ \text{cm}^2/\text{V-sec}$

$$\sigma = \frac{1}{\rho} = qN_A\mu_p$$

i.e.,

$$qN_A = \frac{1}{\rho\mu_p} = \frac{1}{20 \times 500} = 1 \times 10^{-4}$$

Therefore,

$$V_P = \frac{qN_A}{2\varepsilon} \times a^2 = \frac{1 \times 10^{-4}}{2 \times 12 \times 8.854 \times 10^{-12}} \times (2 \times 10^{-4})^2 = 1.89\ \text{V}$$

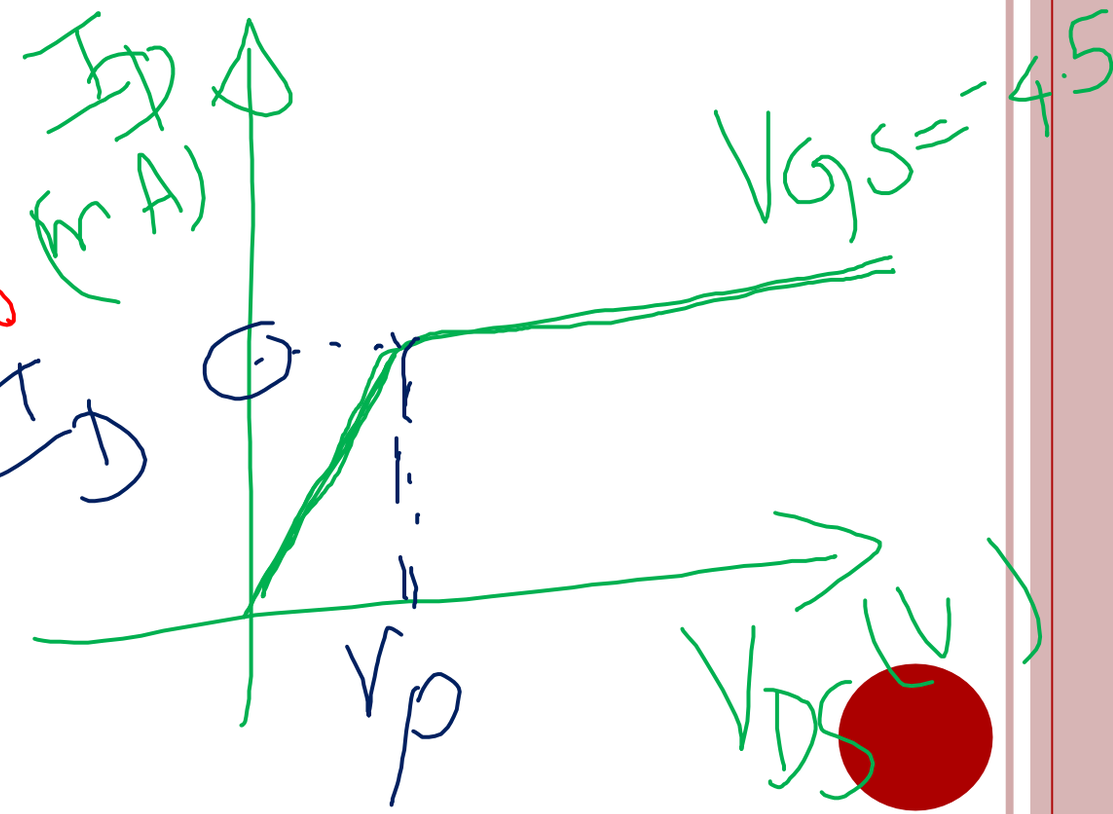
(7) If $I_{DSS} = 16\ mA$

$V_{GS(off)} = -8V$

$V_{GS} = -4.5V$

$V_{GS} = ?$

$I_D = 0$



Sol:

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 6\times10^{-3}\left[1 - \left(\frac{-4.5}{-8}\right)\right]^2$$

$$I_D = 3.09\ mA$$