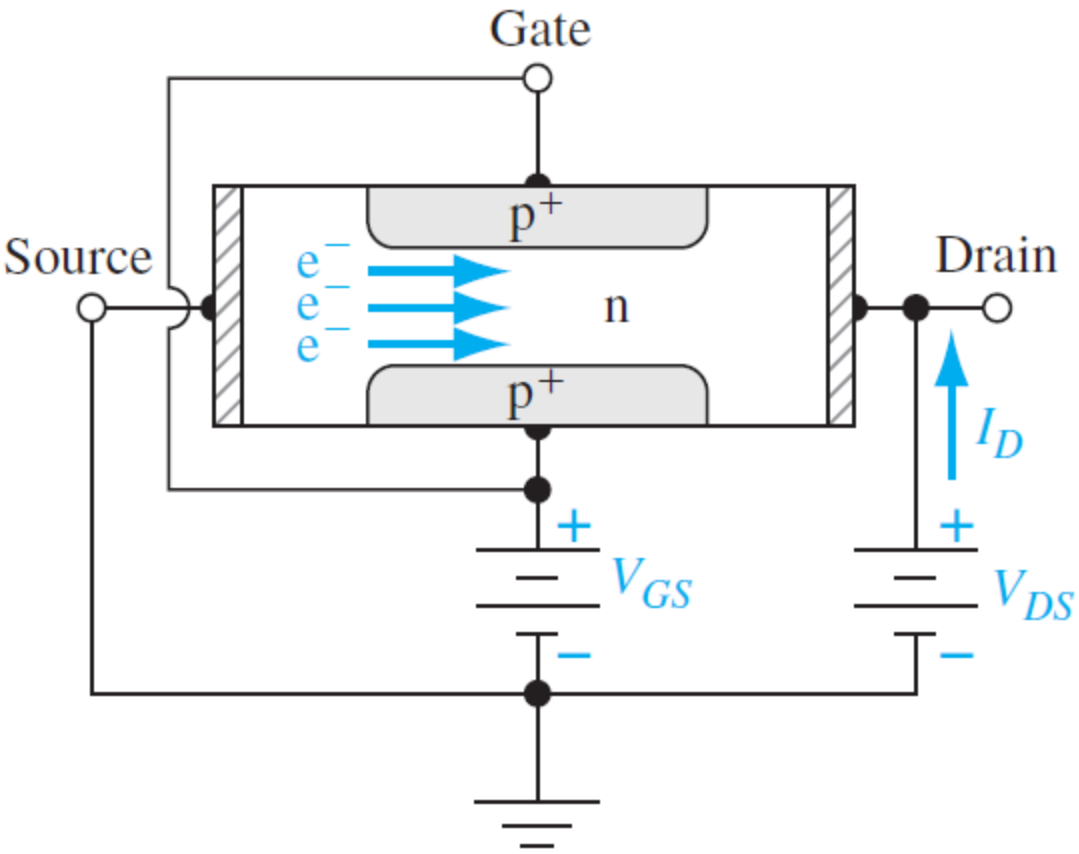
Field Effect Transistor

Basic pn JFET Operation

- The n region between the two p regions is known as the channel and, in this n-channel device, majority carrier electrons flow between the source and drain terminals.
- The source is the terminal from which carriers enter the channel from the external circuit, the drain is the terminal where carriers leave, or are drained from, the device, and the gate is the control terminal.
- The two gate terminals shown in Figure are tied together to form a single gate connection.
- Since majority carrier electrons are primarily involved in the conduction in this n-channel transistor, the JFET is a majority-carrier device.

Basic pn JFET Operation

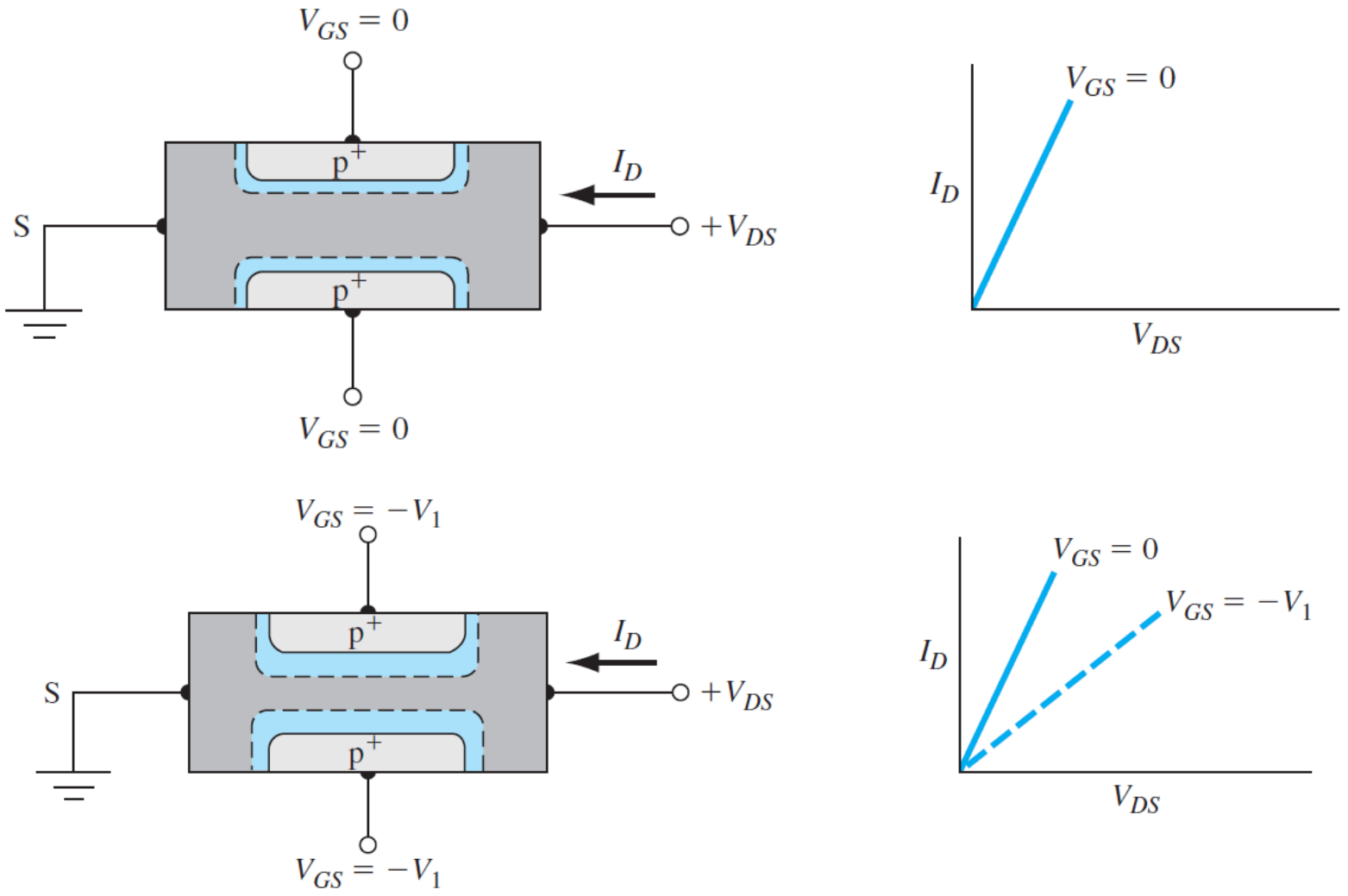


Cross section of a symmetrical n-channel pn junction FET.

Basic pn JFET Operation

- Figure shows an n-channel pn JFET with zero volts applied to the gate.
- If the source is at ground potential, and if a small positive drain voltage is applied, a drain current I_D is produced between the source and drain terminals.
- The n channel is essentially a resistance so the I_D versus V_{DS} characteristic, for small V_{DS} values, is approximately linear, as shown in the figure.
- When we apply a voltage to the gate of a pn JFET with respect to the source and drain, we alter the channel conductance.
- If a negative voltage is applied to the gate of the n-channel pn JFET shown in Figure, the gate-to-channel pn junction becomes reverse biased.
- The space charge region now widens so the channel region becomes narrower and the resistance of the n channel increases.
- The slope of the I_D versus V_{DS} curve, for small V_{DS} , decreases.

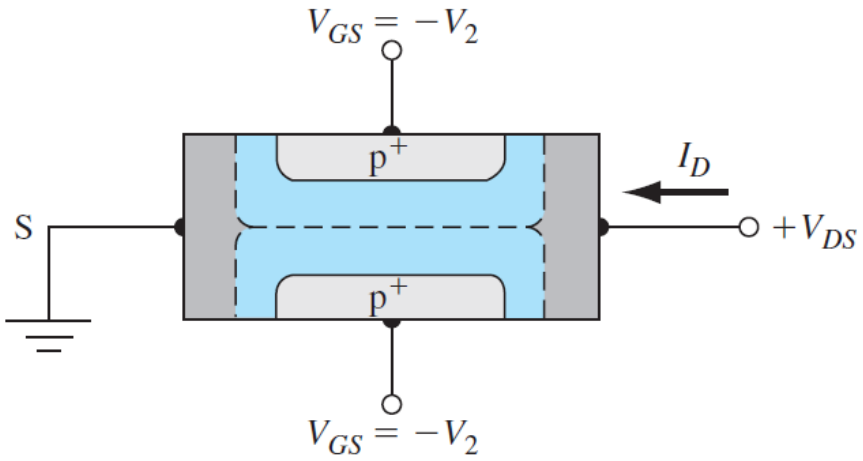
Basic pn JFET Operation

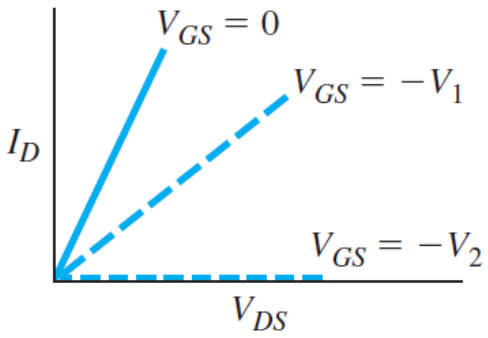


(a) zero gate voltage, (b) small reverse-biased gate voltage

Basic pn JFET Operation

- If a larger negative gate voltage is applied, The reverse-biased gate-to-channel space charge region has completely filled the channel region. This condition is known as pinchoff.
- The drain current at pinchoff is essentially zero, since the depletion region isolates the source and drain terminals.
- The current in the channel is controlled by the gate voltage. The control of the current in one part of the device by a voltage in another part of the device is the basic transistor action. This device is a normally on or *depletion mode* device, which means that a voltage must be applied to the gate terminal to turn the device off.

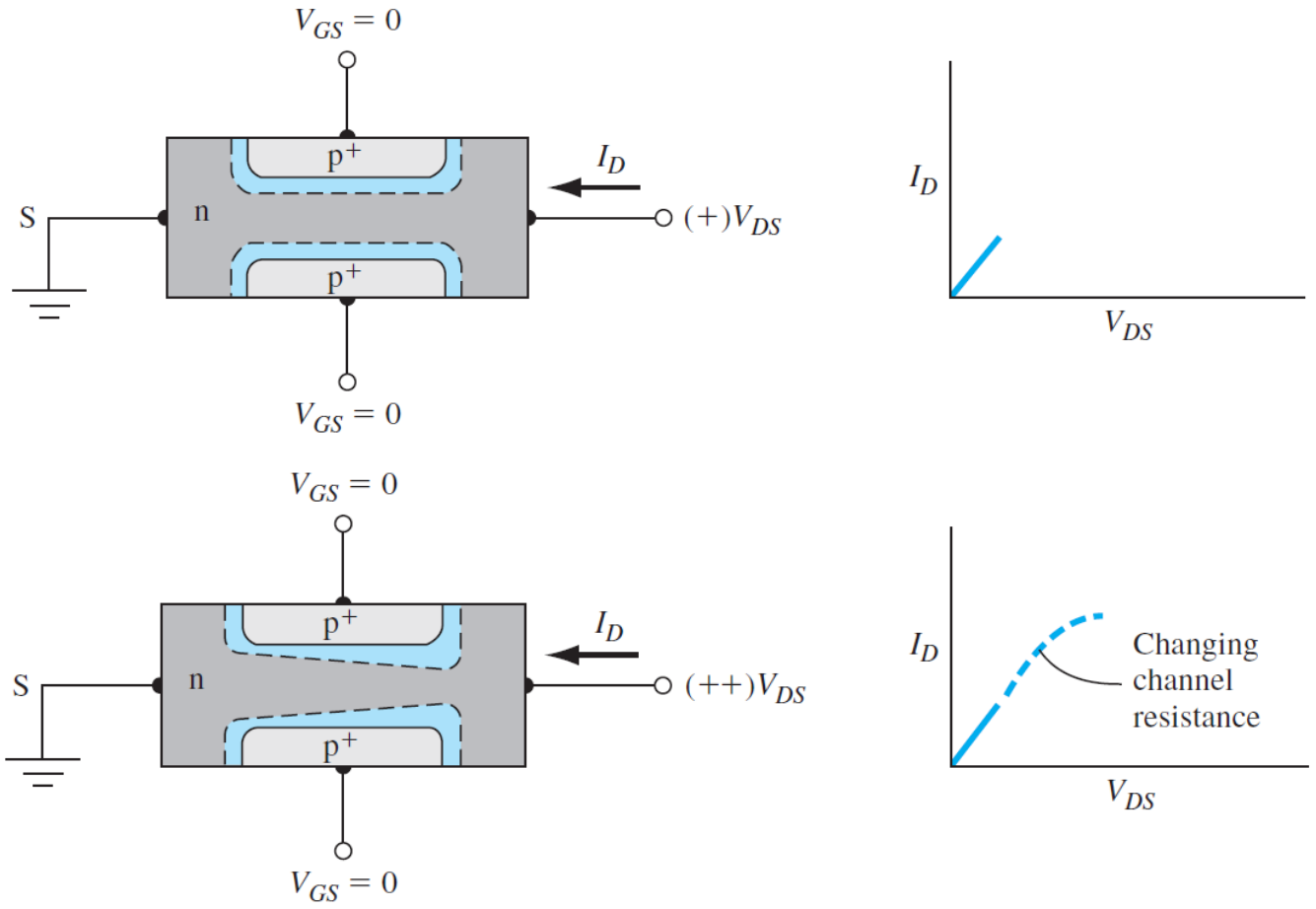




Basic pn JFET Operation

- Now consider the situation in which the gate voltage is held at zero volts, $V_{GS} = 0$, and the drain voltage changes.
- As the drain voltage increases (positive), the gate to- channel pn junction becomes reverse biased near the drain terminal so that the space charge region extends further into the channel.
- The channel is essentially a resistor, and the effective channel resistance increases as the space charge region widens; therefore, the slope of the I_D versus V_{DS} characteristic decreases.
- If the drain voltage increases further, the channel has been pinched off at the drain terminal.
- Any further increase in drain voltage will not cause an increase in drain current.

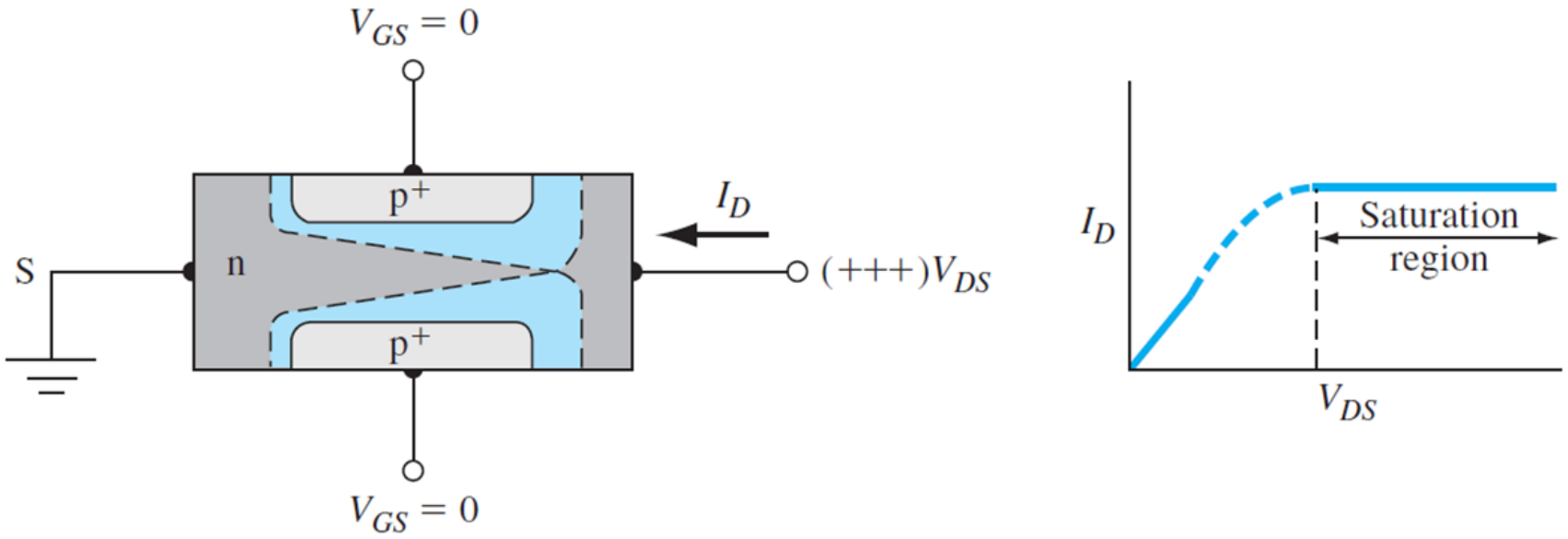
Basic pn JFET Operation



(a) a small drain voltage, (b) a larger drain voltage

Basic pn JFET Operation

- The drain voltage at pinchoff is referred to as $V_{DS(sat)}$.
- For $V_{DS} = V_{DS(sat)}$, the transistor is said to be in the saturation region and the drain current, for this ideal case, is independent of V_D

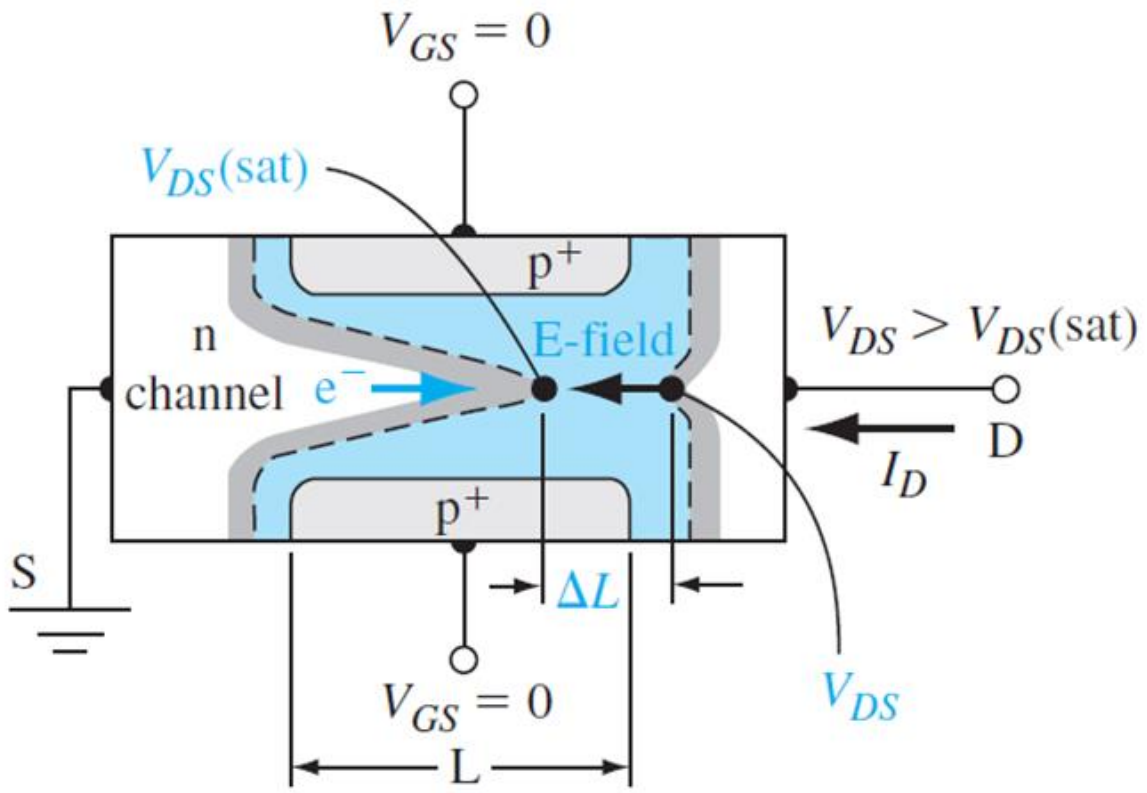


a drain voltage to achieve pinchoff at the drain terminal

Basic pn JFET Operation

- The n channel and drain terminal are now separated by a space charge region which has a length ΔL.
- The electrons move through the n channel from the source and are injected into the space charge region where, subjected to the E-field force, they are swept through into the drain contact area.
- If we assume that $\Delta L << L$, then the electric field in the n-channel region remains unchanged from the $V_{DS(sat)}$ case; the drain current will remain constant as V_{DS} changes.
- Once the carriers are in the drain region, the drain current will be independent of V_{DS}; thus, the device looks like a constant current source.

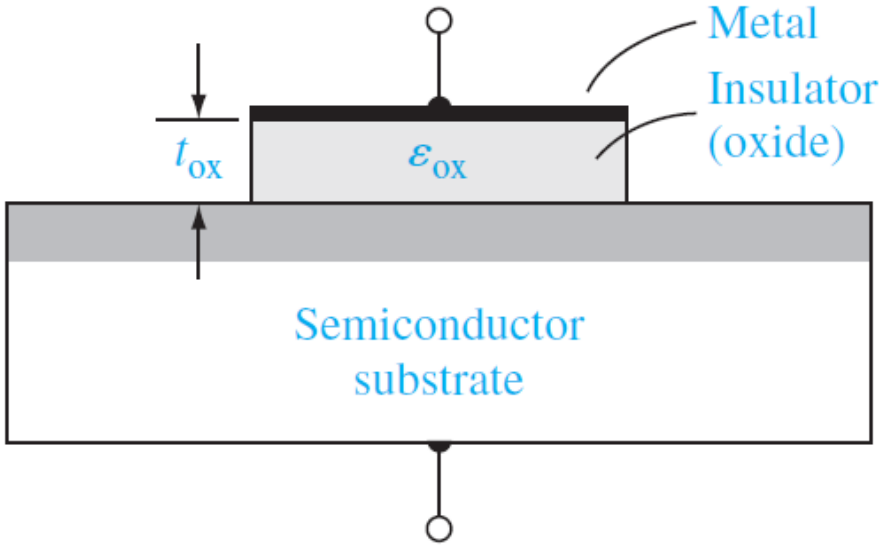
Basic pn JFET Operation



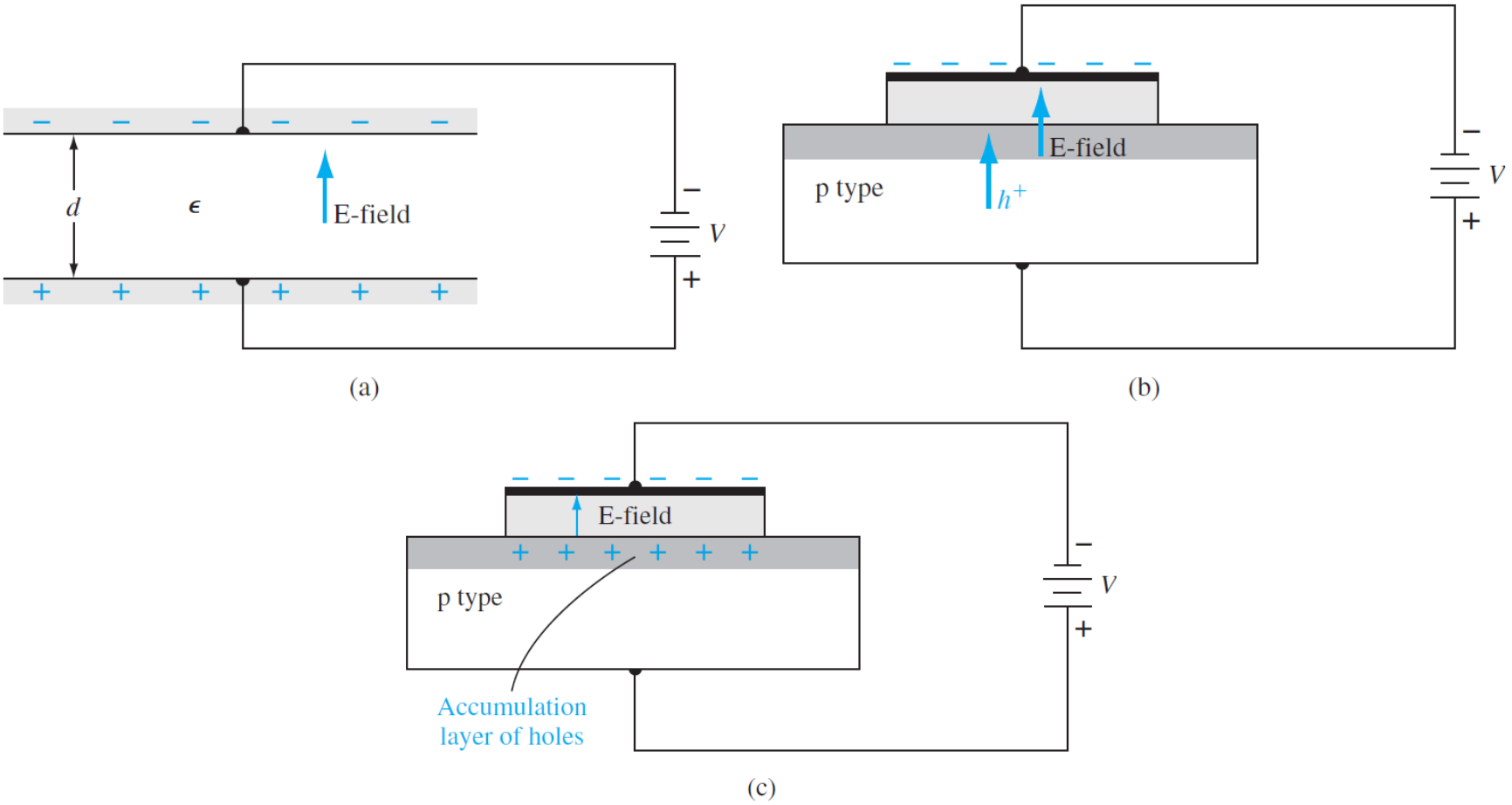
Expanded view of the space charge region in the channel for $V_{DS} > V_{DS(sat)}$.

THE TWO-TERMINAL MOS STRUCTURE (MOS capacitor)

- The heart of the MOSFET is the MOS capacitor shown in Figure.
- The metal may be aluminum or some other type of metal, although in many cases, it is actually a high-conductivity polycrystalline silicon that has been deposited on the oxide; however, the term metal is usually still used.
- The parameter t_{ox} in the figure is the thickness of the oxide and ϵ_{ox} is the permittivity of the oxide.



MOS capacitor



(a) A parallel-plate capacitor showing the electric field and conductor charges.
(b) A corresponding MOS capacitor with a negative gate bias showing the electric field and charge flow.
(c) The MOS capacitor with an accumulation layer of holes.

MOS capacitor

- With this bias, a negative charge exists on the top plate, a positive charge exists on the bottom plate, and an electric field is induced between the two plates.
- The capacitance per unit area for this geometry is

$$C' = \frac{\epsilon}{d}$$

- where $\in$ is the permittivity of the insulator and *d* is the distance between the two plates.
- The magnitude of the charge per unit area on either plate is

$$Q' = C'V$$

- The magnitude of the electric field is

$$\mathrm{E} = \frac{V}{d}$$

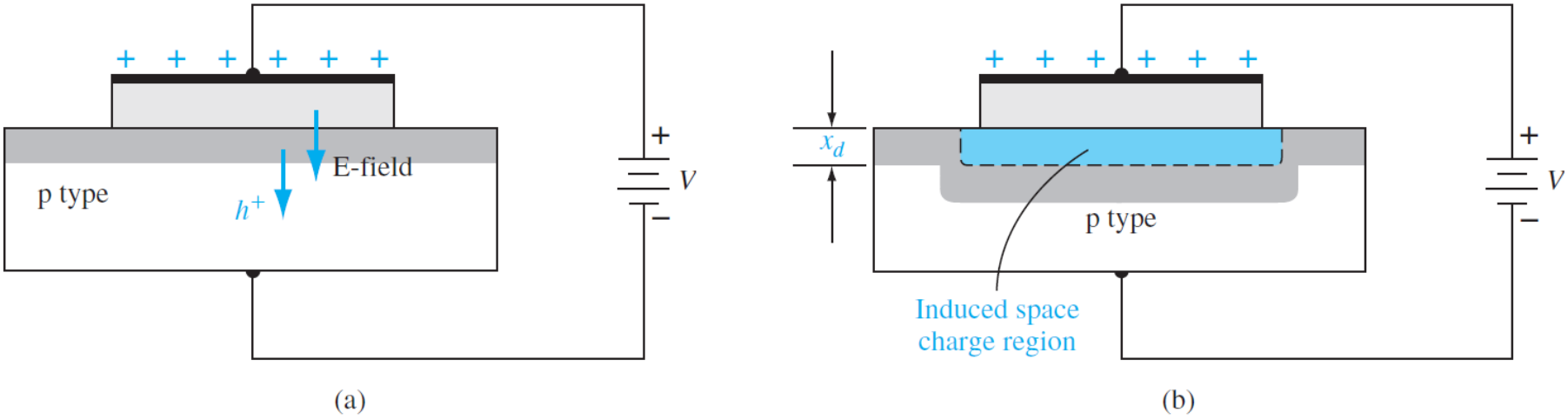
MOS capacitor

- Figure shows a MOS capacitor with a p-type semiconductor substrate.
- The top metal gate is at a negative voltage with respect to the semiconductor substrate
- a negative charge will exist on the top metal plate and an electric field will be induced with the direction shown in the figure.
- If the electric field were to penetrate into the semiconductor, the majority carrier holes would experience a force toward the oxide– semiconductor interface.
- Figure Shows the equilibrium distribution of charge in the MOS capacitor with this particular applied voltage.
- An *accumulation layer* of holes at the oxide–semiconductor junction corresponds to the positive charge on the bottom "plate" of the MOS capacitor.

MOS capacitor

- Figure shows the same MOS capacitor in which the polarity of the applied voltage is reversed.
- A positive charge now exists on the top metal plate and the induced electric field is in the opposite direction as shown.
- If the electric field penetrates the semiconductor in this case, majority carrier holes will experience a force away from the oxide–semiconductor interface.
- As the holes are pushed away from the interface, a negative space charge region is created because of the fixed ionized acceptor atoms.
- The negative charge in the induced depletion region corresponds to
- the negative charge on the bottom “plate” of the MOS capacitor.
- Figure shows the equilibrium distribution of charge in the MOS capacitor with this applied voltage

MOS capacitor

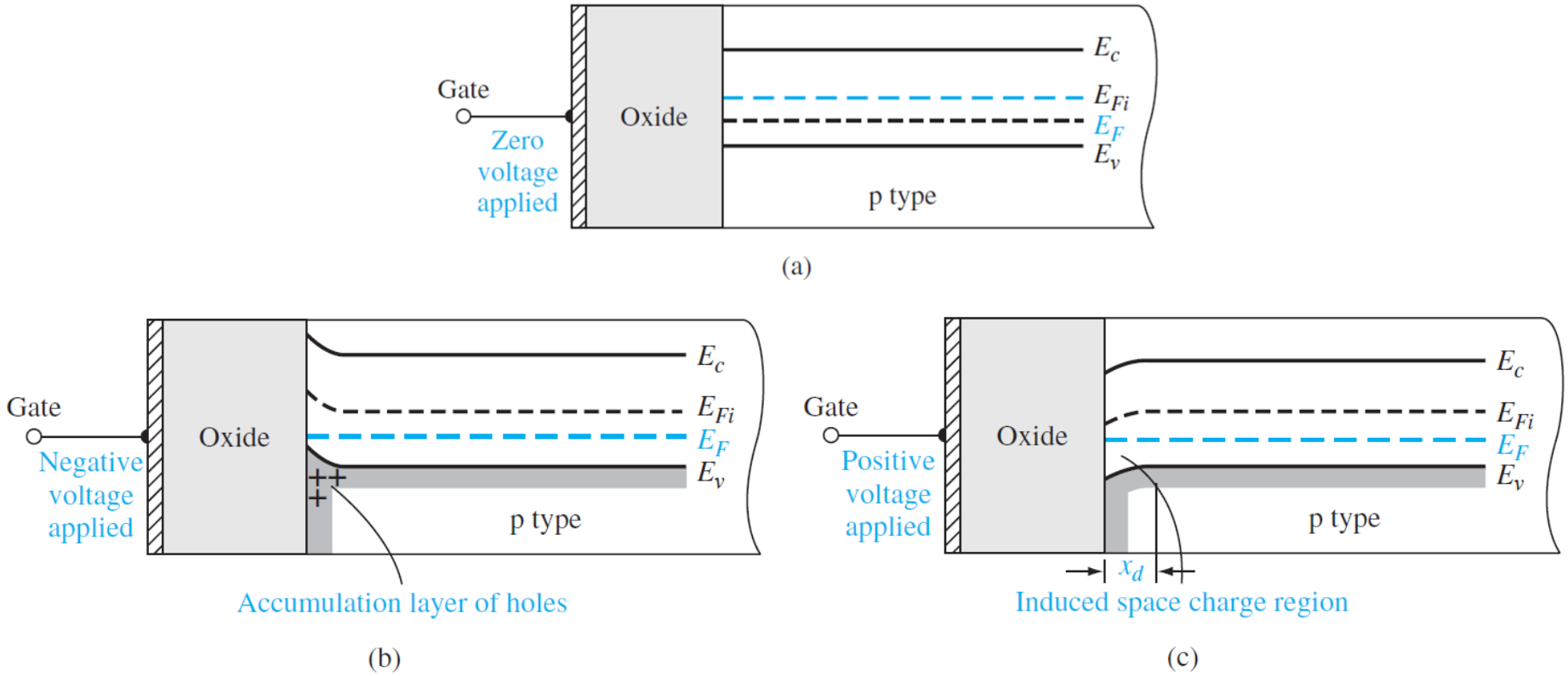


The MOS capacitor with a moderate positive gate bias, showing
(a) the electric field and charge flow and
(b) the induced space charge region

Energy-band diagrams of the MOS capacitor

- Figure shows the ideal case when zero bias is applied across the MOS device.
- The energy bands in the semiconductor are flat indicating no net charge exists in the semiconductor. This condition is known as flat band
- Figure shows the energy-band diagram for the case when a negative bias is applied to the gate. (Remember that positive electron energy is plotted “upward” and positive voltage is plotted “downward.”)
- The valence-band edge is closer to the Fermi level at the oxide–semiconductor interface than in the bulk material, which implies that there is an accumulation of holes.
- The semiconductor surface appears to be more p-type than the bulk material.
- The Fermi level is a constant in the semiconductor since the MOS system is in thermal equilibrium and there is no current through the oxide.

Energy-band diagrams of the MOS capacitor

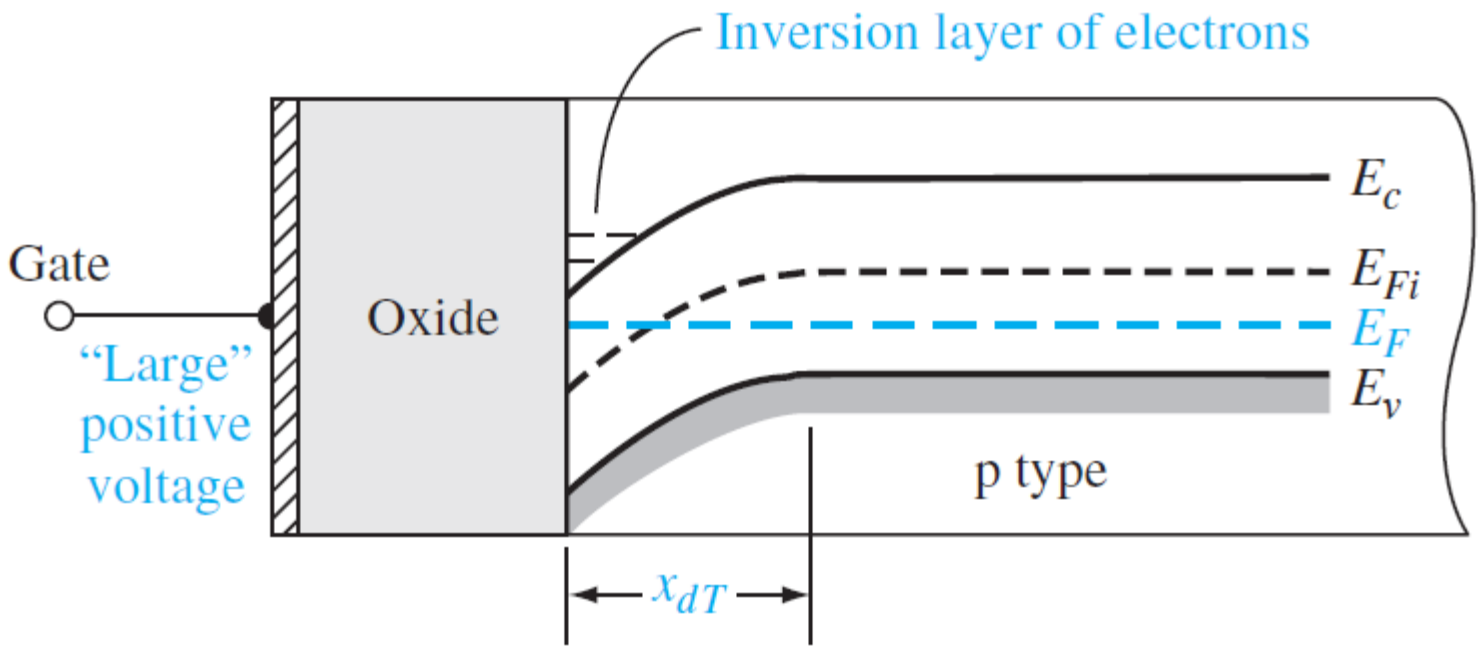


The energy-band diagram of a MOS capacitor with a p-type substrate for (a) a zero applied gate bias showing the ideal case, (b) a negative gate bias, and (c) a moderate positive gate bias

Energy-band diagrams of the MOS capacitor

- Figure shows the energy-band diagram of the MOS system when a positive voltage is applied to the gate.
- The conduction- and valence-band edges bend as shown in the figure, indicating a space charge region similar to that in a pn junction.
- The conduction band and intrinsic Fermi levels move closer to the Fermi level. The induced space charge width is x_d.
- Now consider the case when a still larger positive voltage is applied to the top metal gate of the MOS capacitor. We expect the induced electric field to increase in magnitude and the corresponding positive and negative charges on the MOS capacitor to increase.
- A larger negative charge in the MOS capacitor implies a larger induced space charge region and more band bending.

Energy-band diagrams of the MOS capacitor

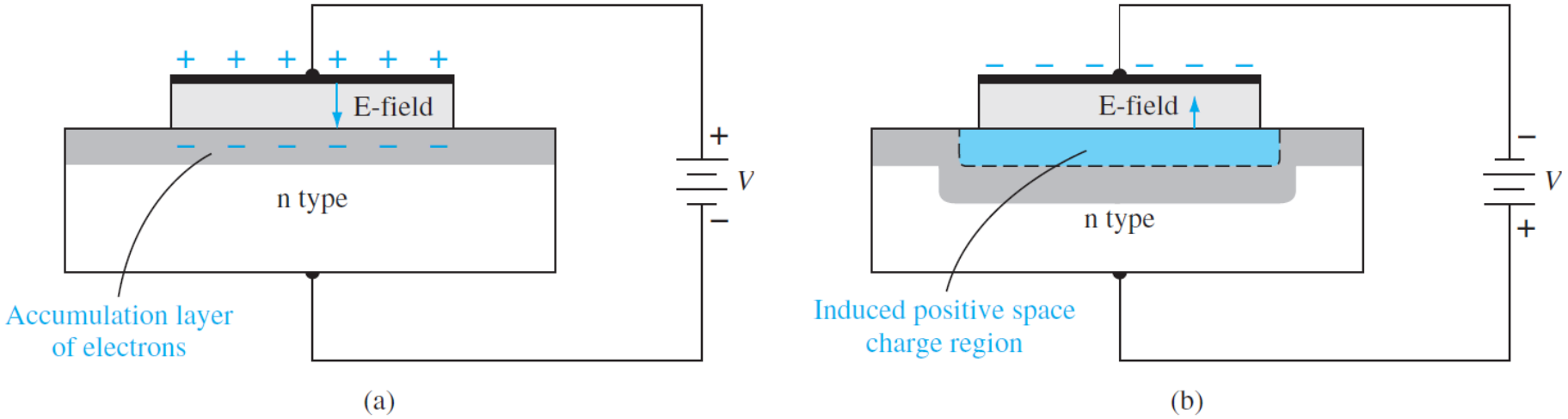


The energy-band diagram of the MOS capacitor with a p-type substrate for a "large" positive gate bias.

Energy-band diagrams of the MOS capacitor

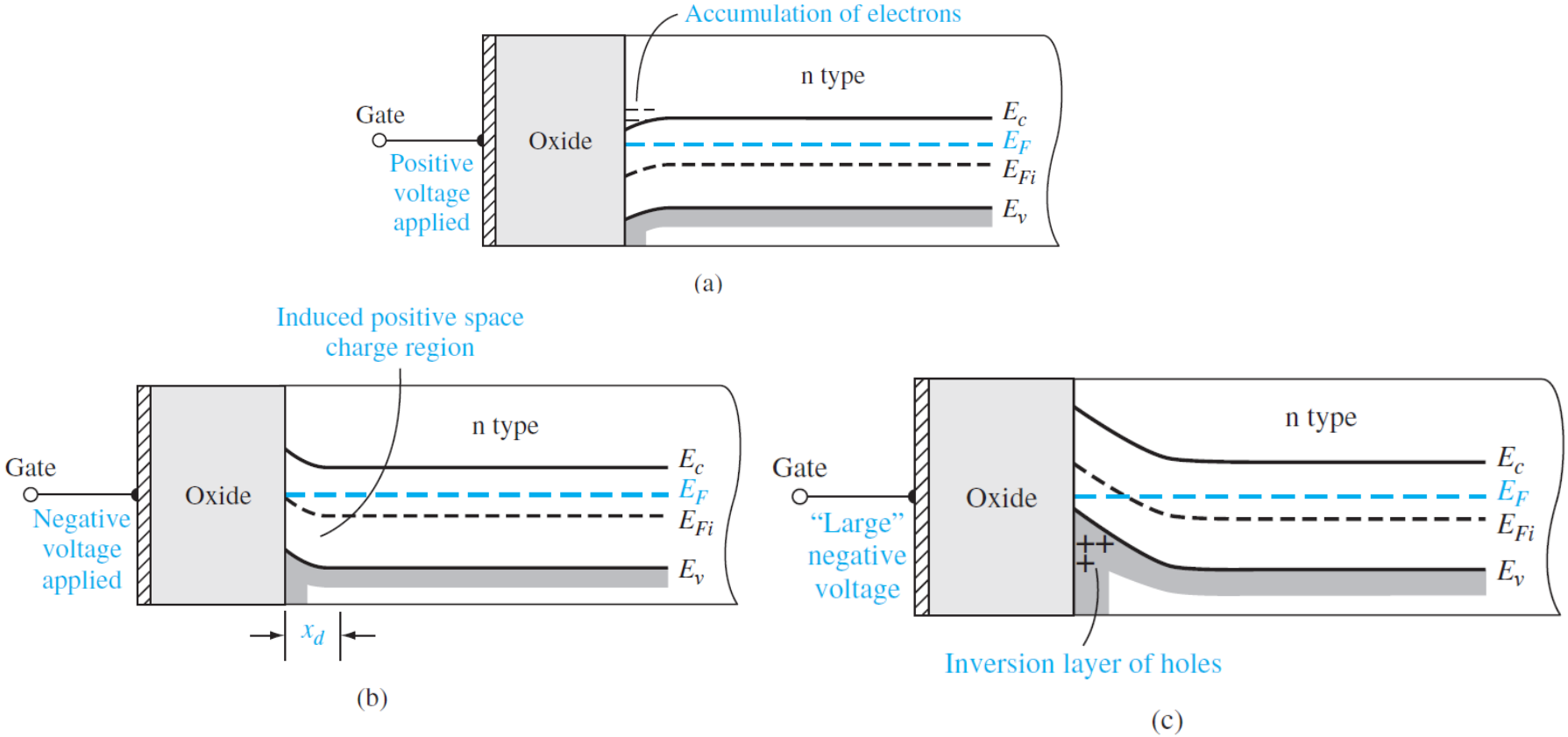
- The intrinsic Fermi level at the surface is now below the Fermi level.
- The conduction band at the surface is now close to the Fermi level, whereas the valence band is close to the Fermi level in the bulk semiconductor.
- This result implies that the surface in the semiconductor adjacent to the oxide–semiconductor interface is n type.
- By applying a sufficiently large positive gate voltage, we have inverted the surface of the semiconductor from a p-type to an n-type semiconductor.
- We have created an **inversion layer** of electrons at the oxide–semiconductor interface.

MOS capacitor (n type)



The MOS capacitor with an n-type substrate for
(a) a positive gate bias and (b) a moderate negative gate bias.

MOS capacitor (n type)



The energy-band diagram of the MOS capacitor with an n-type substrate for (a) a positive gate bias, (b) a moderate negative bias, and (c) a "large" negative gate bias.

Depletion Layer Thickness

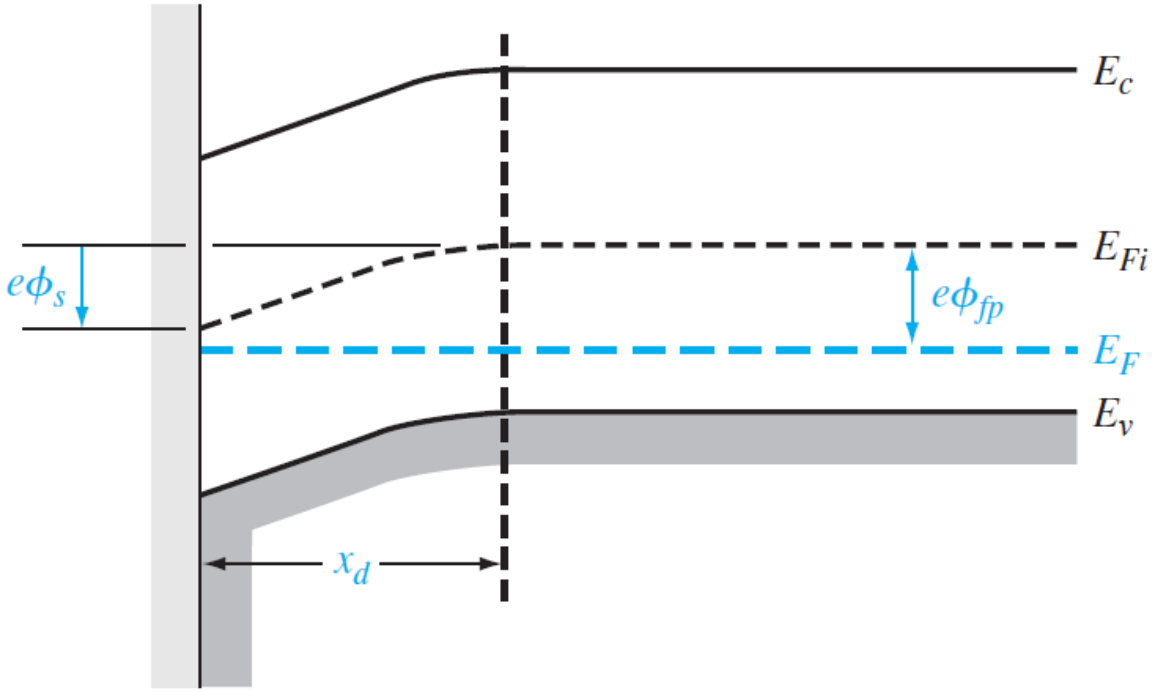
- Figure shows the space charge region in a p type semi conductor substrate.
- The potential Φ_{fp} is the difference (in V) between E_{Fi} and E_F and is given by

$$\phi_{fp} = V_t \ln\left(\frac{N_a}{n_i}\right)$$

- The potential Φ_s is called the surface potential; it is the difference (in V) between E_{Fi} measured in the bulk semiconductor and E_{Fi} measured at the surface.
- The surface potential is the potential difference across the space charge layer.
- The space charge width can now be written in a form similar to that of a one-sided pn junction.
- where ε_s is the permittivity of the semiconductor

$$x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a}\right)^{1/2}$$

Depletion Layer Thickness



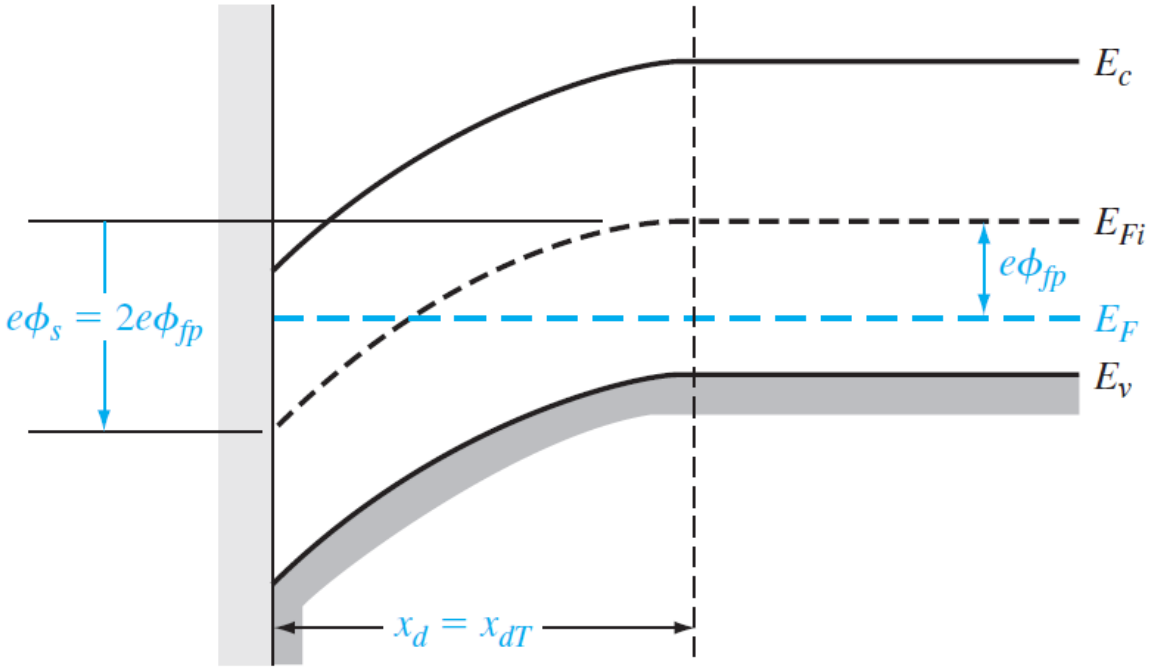
The energy-band diagram in the p-type semiconductor, indicating surface potential

Depletion Layer Thickness

- Figure shows the energy bands for the case in which $\Phi_s = 2\Phi_{fp}$.
- The Fermi level at the surface is as far above the intrinsic level as the Fermi level is below the intrinsic level in the bulk semiconductor.
- The electron concentration at the surface is the same as the hole concentration in the bulk material. This condition is known as the threshold inversion point.
- The applied gate voltage creating this condition is known as the **threshold voltage**.
- If the gate voltage increases above this threshold value, the conduction band will bend slightly closer to the Fermi level, but the change in the conduction band at the surface is now only a slight function of gate voltage.
- The electron concentration at the surface, however, is an exponential function of the surface potential.

Depletion Layer Thickness

- The surface potential may increase by a few (kT/e) volts, which will change the electron concentration by orders of magnitude, but the space charge width changes only slightly.
- In this case, then, the space charge region has essentially reached a maximum width.



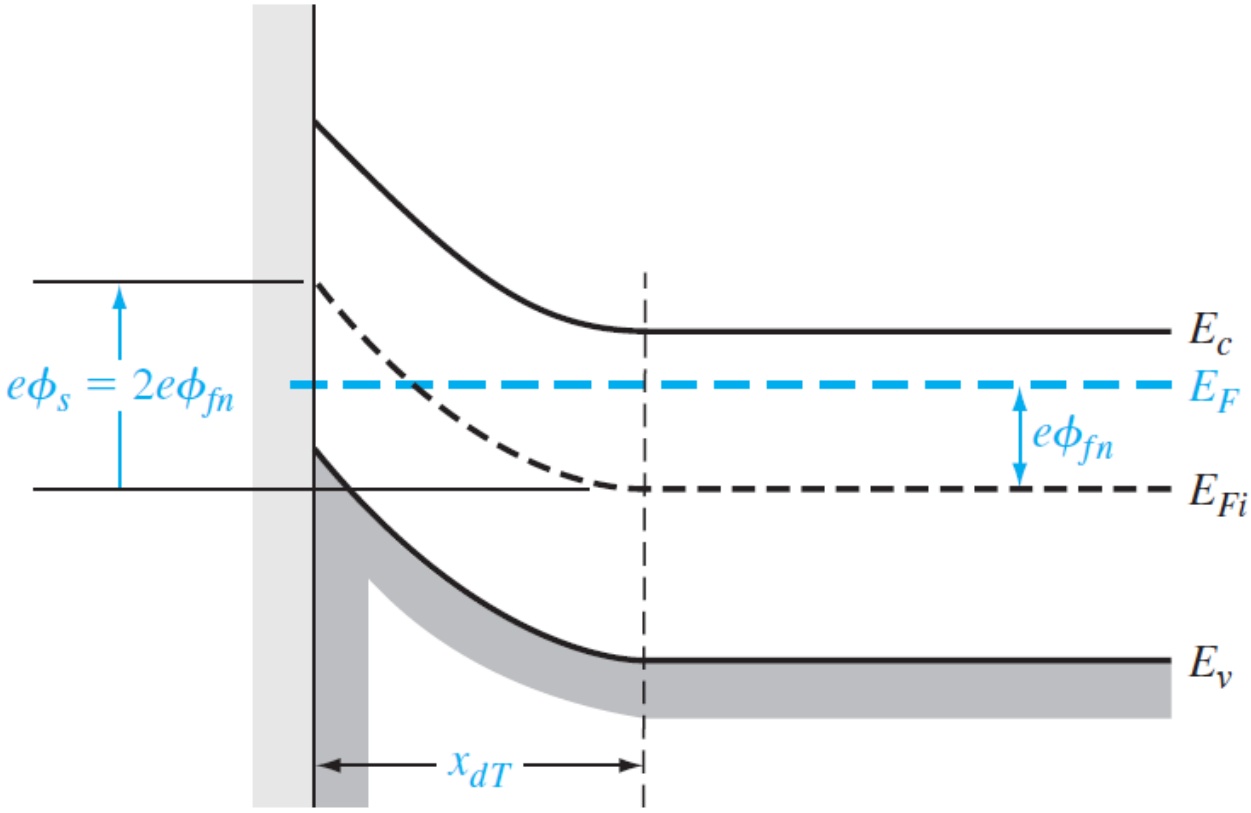
$$\phi_s = 2\phi_{fp}.$$

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a}\right)^{1/2}$$

Depletion Layer Thickness (n type)

$$\phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right)$$

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fn}}{eN_d}\right)^{1/2}$$



The energy-band diagram in the n-type semiconductor at the threshold inversion point.

Surface Charge Density

- the electron concentration in the conduction band

$$n = n_i \exp\left[\frac{E_F - E_{Fi}}{kT}\right]$$

- For a p-type semiconductor substrate, the electron inversion charge density

$$n_s = n_i \exp\left[\frac{e(\phi_{fp} + \Delta\phi_s)}{kT}\right] = n_i \exp\left[\frac{\phi_{fp} + \Delta\phi_s}{V_t}\right]$$

$$n_s = n_i \exp\left(\frac{\phi_{fp}}{V_t}\right) \cdot \exp\left(\frac{\Delta\phi_s}{V_t}\right)$$

- where $\Delta\Phi_s$, is the surface potential greater than $2\Phi_{fp}$.

$$n_{st} = n_i \exp\left(\frac{\phi_{fp}}{V_t}\right)$$

where n_{st} is the surface charge density at the threshold inversion point

$$n_s = n_{st} \exp\left(\frac{\Delta\phi_s}{V_t}\right)$$

Threshold Voltage

- The threshold voltage is defined as the applied gate voltage required to achieve the threshold inversion point.
- The threshold inversion point, in turn, is defined as the condition when the surface potential is $\Phi_s = 2\Phi_{fp}$ for the p-type semiconductor and $\Phi_s = 2\Phi_{fn}$ for the n-type semiconductor.

$$V_{TN} = \left(|Q'_{SD}(\max)| - Q'_{ss}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} + 2\phi_{fp}$$

$$V_{TP} = \left(-|Q'_{SD}(\max)| - Q'_{ss}\right)\left(\frac{t_{ox}}{\epsilon_{ox}}\right) + \phi_{ms} - 2\phi_{fn}$$

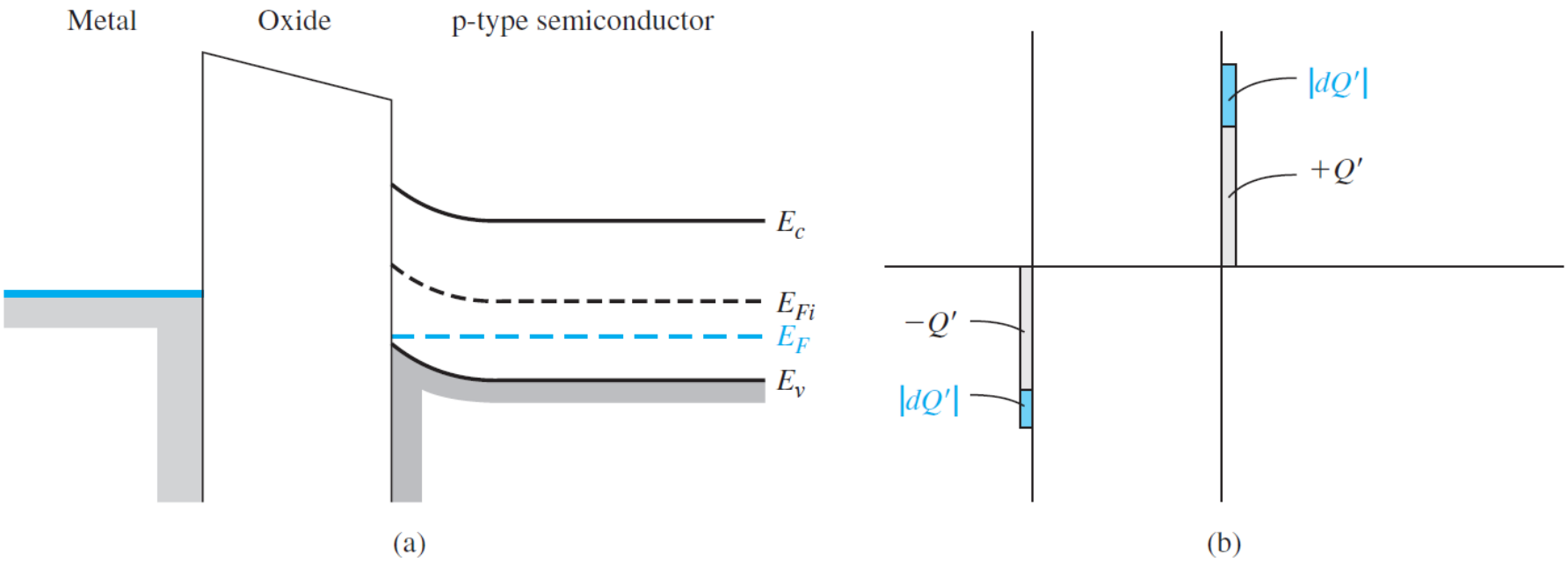
- $Q'_{SD}(max)$ is the magnitude of the maximum space charge density per unit area of the depletion region
- Q'_{SS} oxide charge

CAPACITANCE–VOLTAGE CHARACTERISTICS

- Assume that there is zero charge trapped in the oxide and also that there is no charge trapped at the oxide–semiconductor interface.
- There are three operating conditions of interest in the MOS capacitor: accumulation, depletion, and inversion.
- Figure shows the energy-band diagram of a MOS capacitor with a p-type substrate for the case when a negative voltage is applied to the gate, inducing an accumulation layer of holes in the semiconductor at the oxide–semiconductor interface.
- A small differential change in voltage across the MOS structure will cause a differential change in charge on the metal gate and also in the hole accumulation charge.
- The differential changes in charge density occur at the edges of the oxide, as in a parallel-plate capacitor.
- The capacitance *C′* per unit area of the MOS capacitor for this accumulation mode is just the oxide capacitance

$$C'(\text{acc}) = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

C-V Characteristics of MOS capacitor



(a) Energy-band diagram through a MOS capacitor for the accumulation mode.

(b) Differential charge distribution at accumulation for a differential change in gate voltage.

C-V Characteristics of MOS capacitor

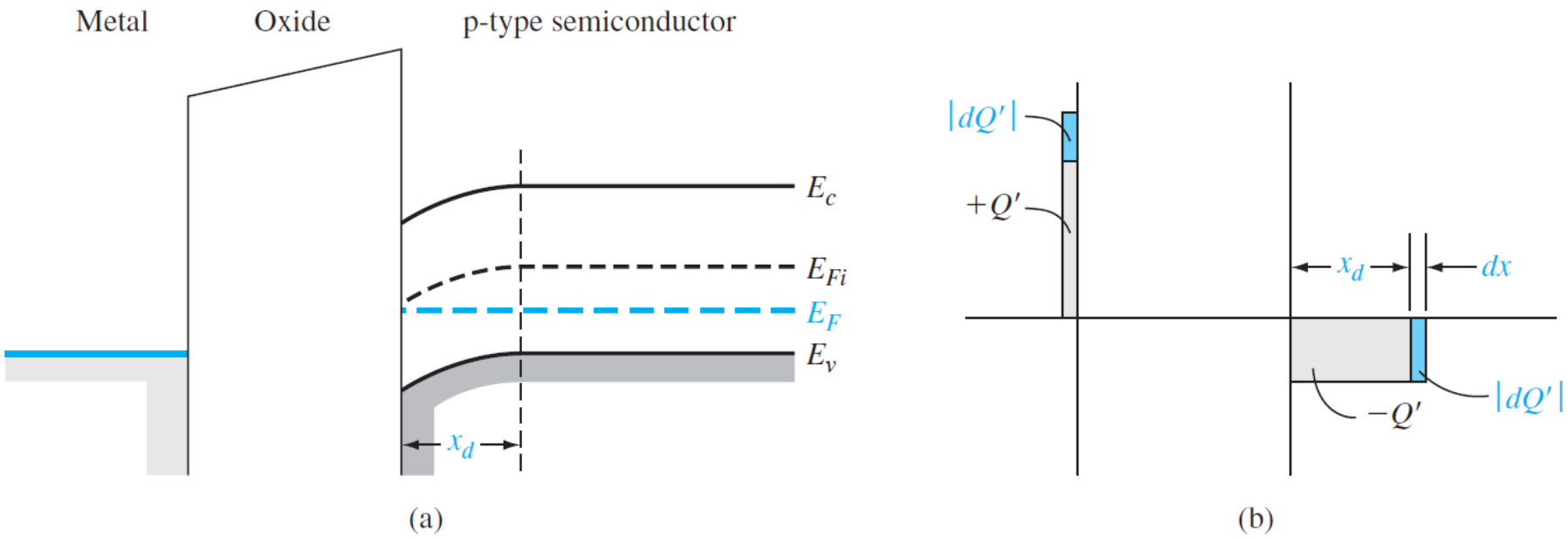
- Figure shows the energy-band diagram of the MOS device when a small positive voltage is applied to the gate, inducing a space charge region in the semiconductor;
- The oxide capacitance and the capacitance of the depletion region are in series.
- A small differential change in voltage across the capacitor will cause a differential change in the space charge width.
- The corresponding differential changes in charge densities are shown in the figure.
- The total capacitance of the series combination is

$$\frac{1}{C'(\text{depl})} = \frac{1}{C_{\text{ox}}} + \frac{1}{C'_{SD}}$$

$$C'(\text{depl}) = \frac{C_{\text{ox}} C'_{SD}}{C_{\text{ox}} + C'_{SD}}$$

$$C_{\text{ox}} = \epsilon_{\text{ox}}/t_{\text{ox}} \text{ and } C'_{SD} = \epsilon_s/x_d$$

C-V Characteristics of MOS capacitor



(a) Energy-band diagram through a MOS capacitor for the depletion mode.

(b) Differential charge distribution at depletion for a differential change in gate voltage.

C-V Characteristics of MOS capacitor

$$C_{ox} = \epsilon_{ox}/t_{ox} \text{ and } C'_{SD} = \epsilon_s/x_d$$

$$C'(\text{depl}) = \frac{C_{ox}}{1 + \dfrac{C_{ox}}{C'_{SD}}} = \frac{\epsilon_{ox}}{t_{ox} + \left(\dfrac{\epsilon_{ox}}{\epsilon_s}\right) x_d}$$

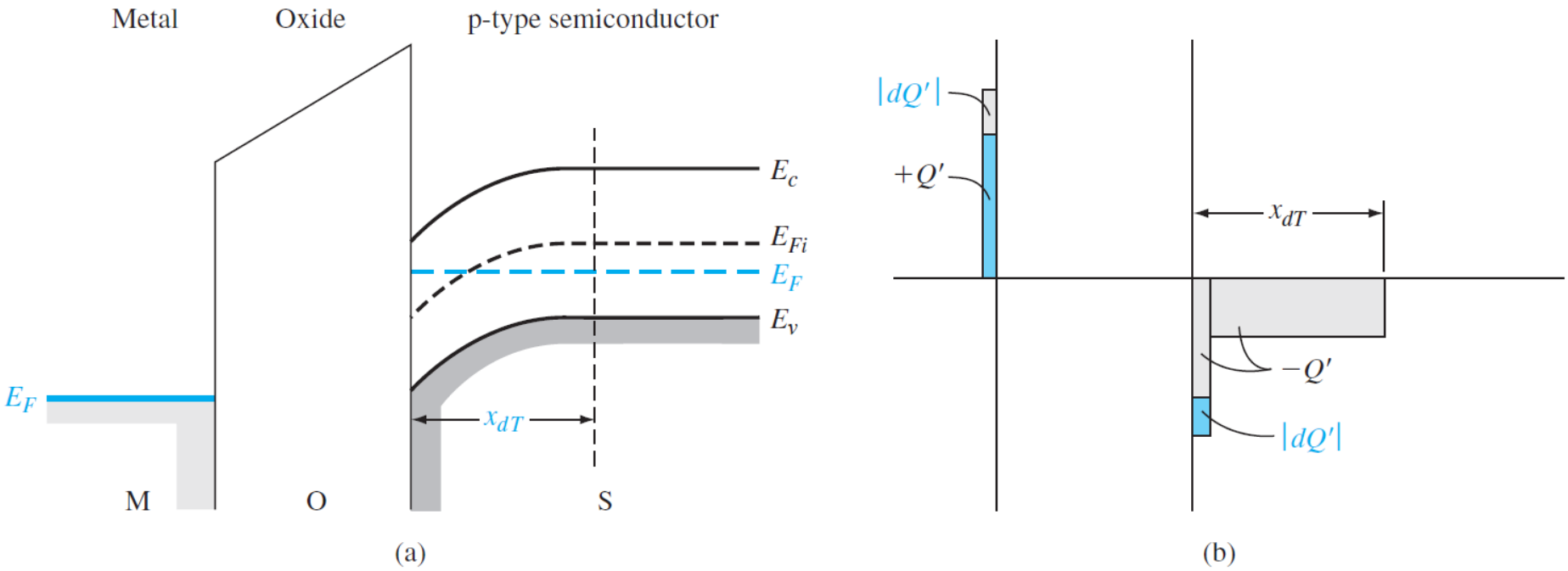
- As the space charge width increases, the total capacitance C'(depl) decreases.
- At zero inversion charge density, minimum capacitance C'_{min}

$$C'_{min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\dfrac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}}$$

- Figure shows the energy-band diagram of this MOS device for the inversion condition.
- If the inversion charge can respond to the change in capacitor voltage, then the capacitance is again just the oxide capacitance

$$C'(\text{inv}) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

C-V Characteristics of MOS capacitor



(a) Energy-band diagram through a MOS capacitor for the inversion mode.

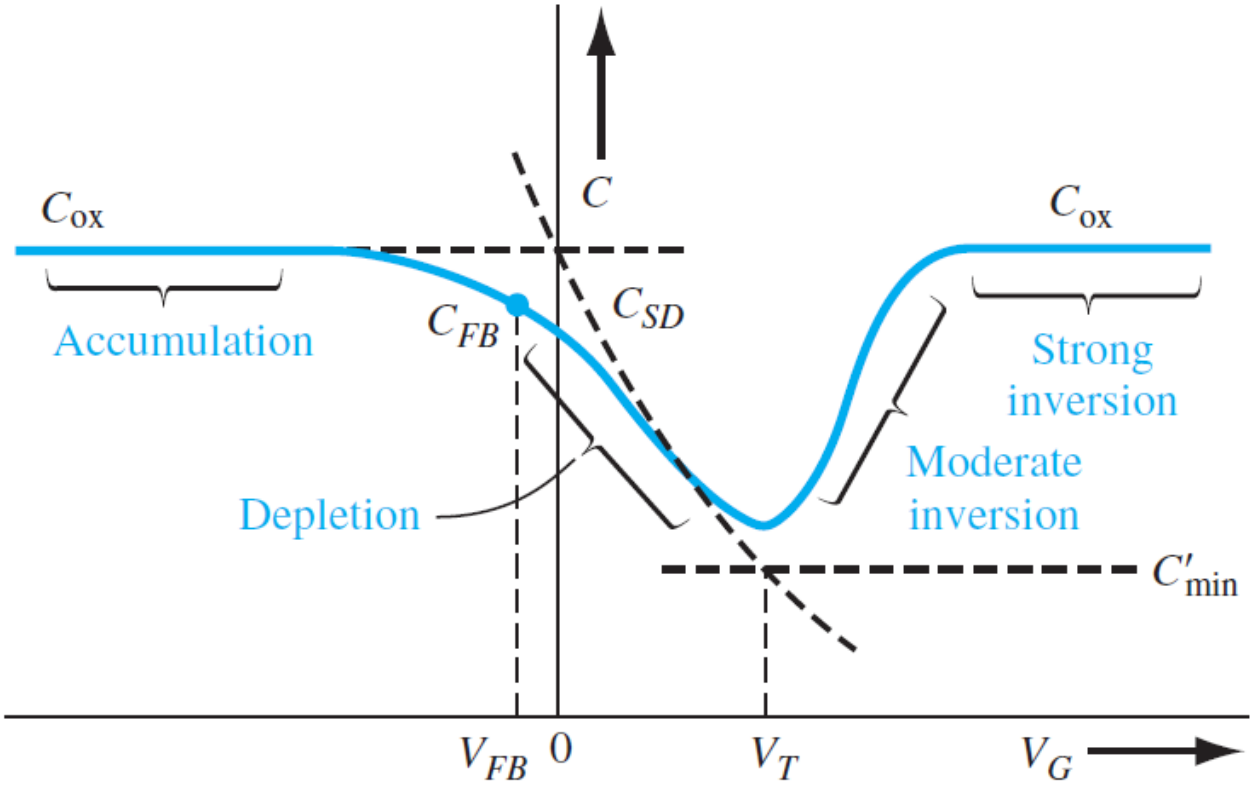
(b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

C-V Characteristics of MOS capacitor

- Figure shows the ideal capacitance versus gate voltage, or C–V, characteristics of the MOS capacitor with a p-type substrate.
- The three dashed segments correspond to the three components C_{ox}, C_{SD} , and C'_{min} .
- The solid curve is the ideal net capacitance of the MOS capacitor.
- Moderate inversion is the transition region between the point when only the space charge density changes with gate voltage and when only the inversion charge density changes with gate voltage.
- The point on the curve that corresponds to the flat-band condition is of interest. The flat-band condition occurs between the accumulation and depletion conditions. The capacitance at flat band is given by

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\frac{kT}{e}\right)\left(\frac{\epsilon_s}{eN_a}\right)}}$$

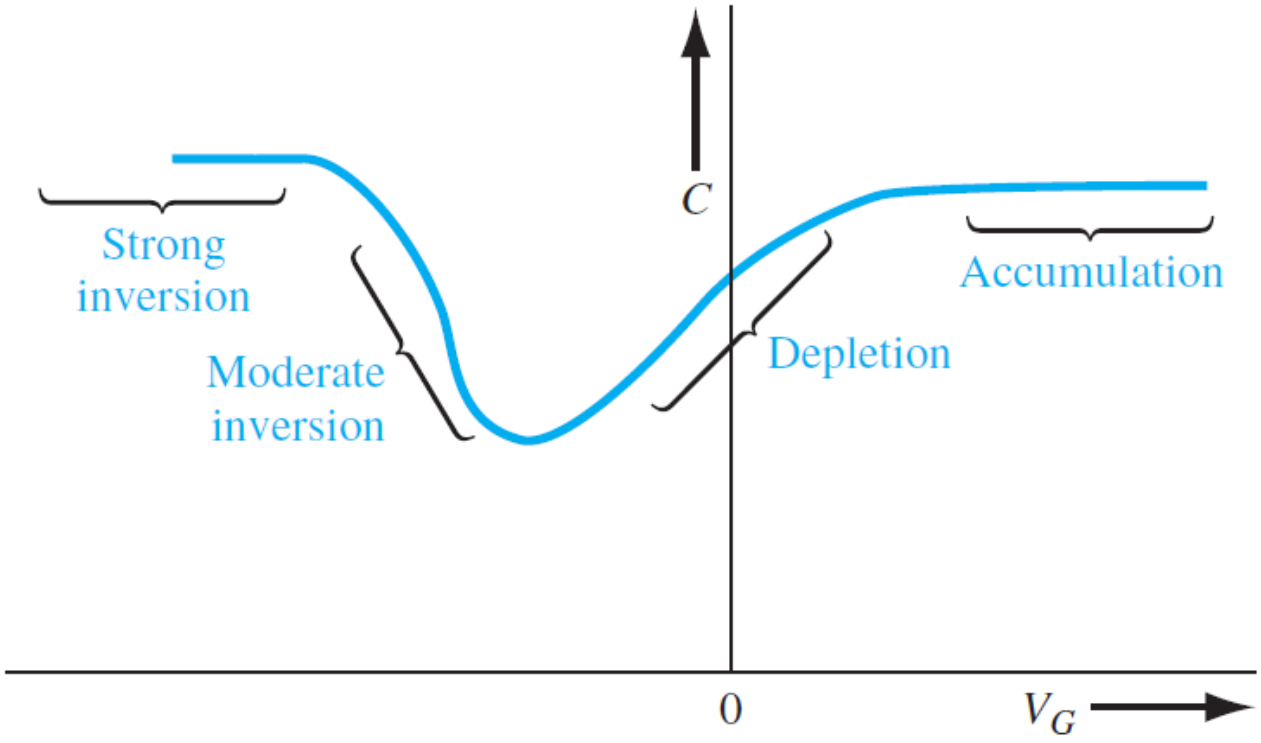
C-V Characteristics of MOS capacitor



Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate.

Individual capacitance components are also shown.

C-V Characteristics of MOS capacitor

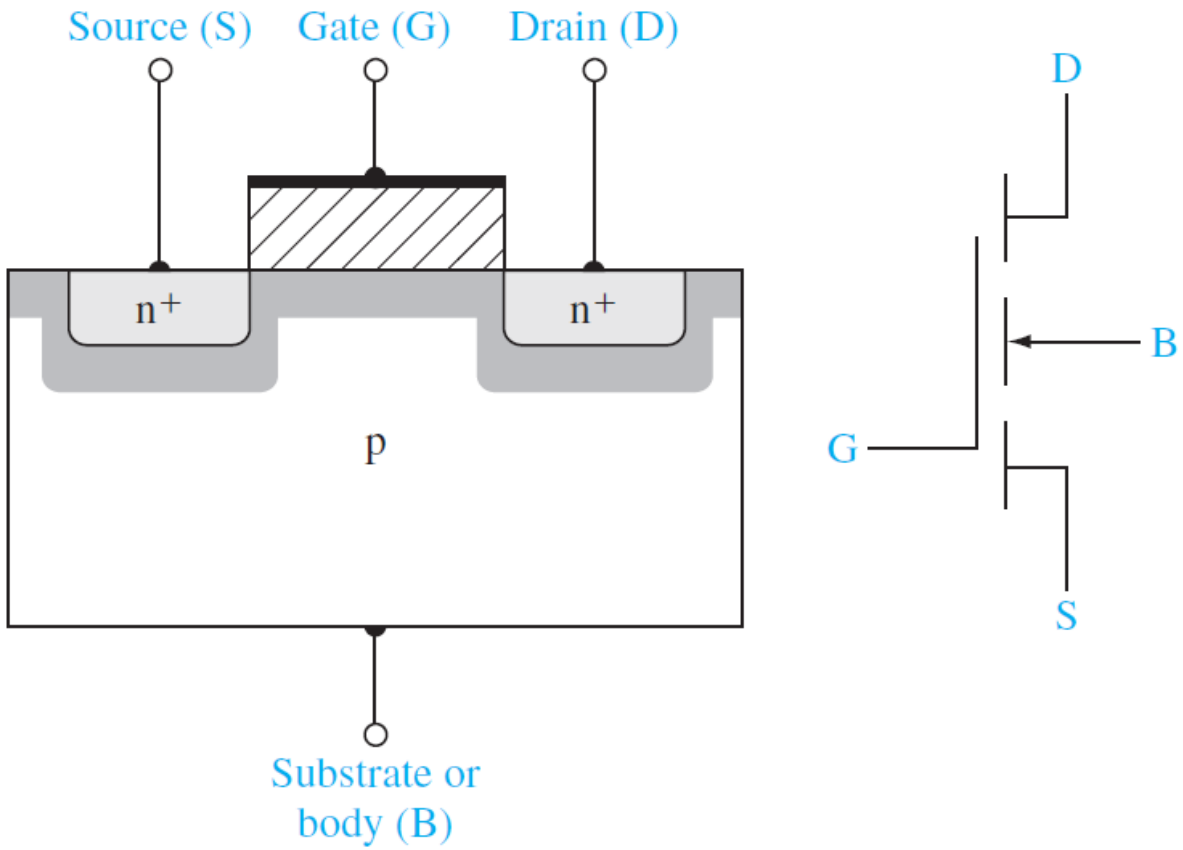


Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with an n-type substrate.

MOSFET Structures

- There are four basic MOSFET device types.
- Figure shows an n-channel enhancement mode MOSFET.
- Implicit in the enhancement mode notation is the idea that the semiconductor substrate is not inverted directly under the oxide with zero gate voltage.
- A positive gate voltage induces the electron inversion layer, which then “connects” the n-type source and the n-type drain regions.
- The source terminal is the source of carriers that flow through the channel to the drain terminal.
- For this n-channel device, electrons flow from the source to the drain so the conventional current will enter the drain and leave the source.
- The conventional circuit symbol for this n-channel enhancement mode device is also shown in the figure.

n-channel enhancement mode MOSFET

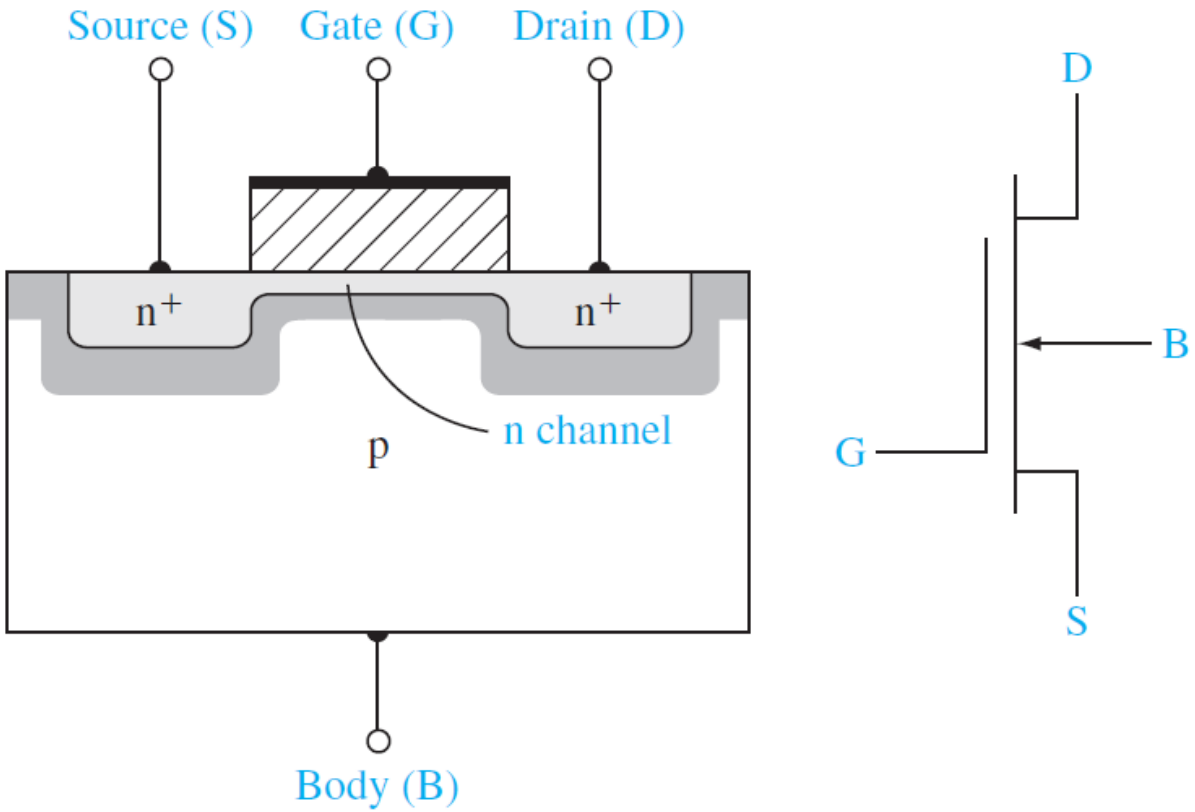


Cross section and circuit symbol for an n-channel enhancement mode MOSFET.

n-channel depletion mode MOSFET

- Figure shows an n-channel depletion mode MOSFET.
- An n-channel region exists under the oxide with 0 V applied to the gate.
- However, we have shown that the threshold voltage of a MOS device with a p-type substrate may be negative; this means that an electron inversion layer already exists with zero gate voltage applied.
- Such a device is also considered to be a depletion mode device.
- The n-channel shown in the figure can be an electron inversion layer or an intentionally doped n region.
- The conventional circuit symbol for the n-channel depletion mode MOSFET is also shown in the figure.

n-channel depletion mode MOSFET

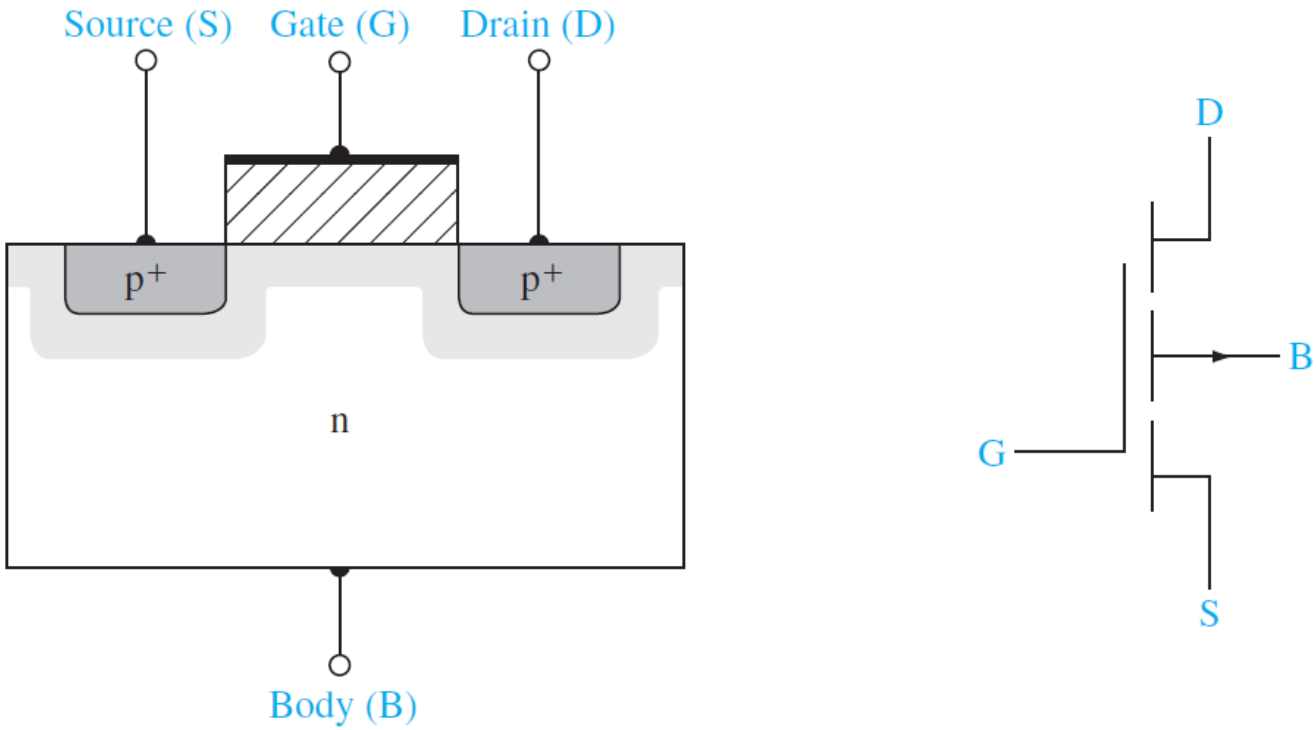


Cross section and circuit symbol for an n-channel depletion mode MOSFET.

p-channel enhancement/depletion mode MOSFET

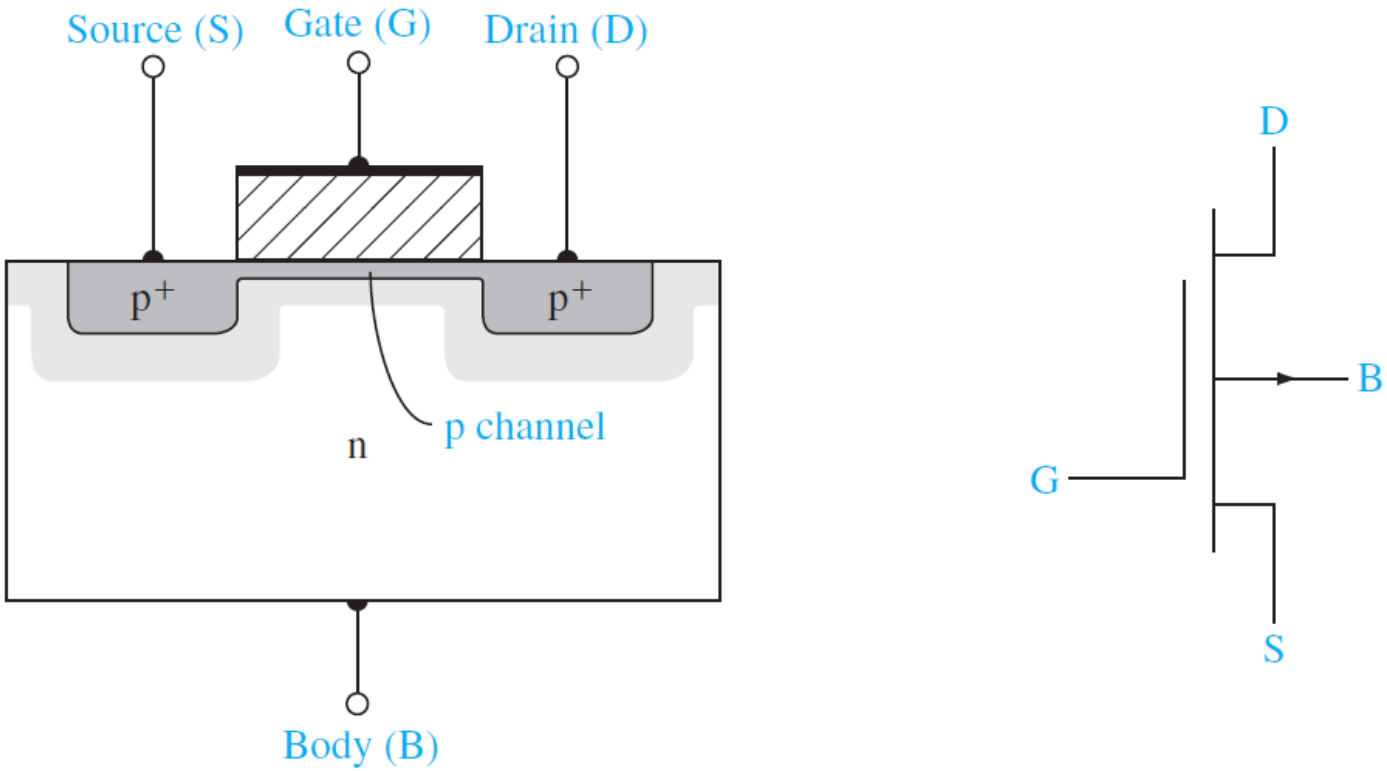
- Figures show a p-channel enhancement mode MOSFET and a p-channel depletion mode MOSFET.
- In the p-channel enhancement mode device, a negative gate voltage must be applied to create an inversion layer of holes that will “connect” the p-type source and drain regions. Holes flow from the source to the drain, so the conventional current will enter the source and leave the drain.
- A p-channel region exists in the depletion mode device even with zero gate voltage.
- The conventional circuit symbols are shown in the figure.

p-channel enhancement mode MOSFET



Cross section and circuit symbol for a p-channel enhancement mode MOSFET

p-channel depletion mode MOSFET

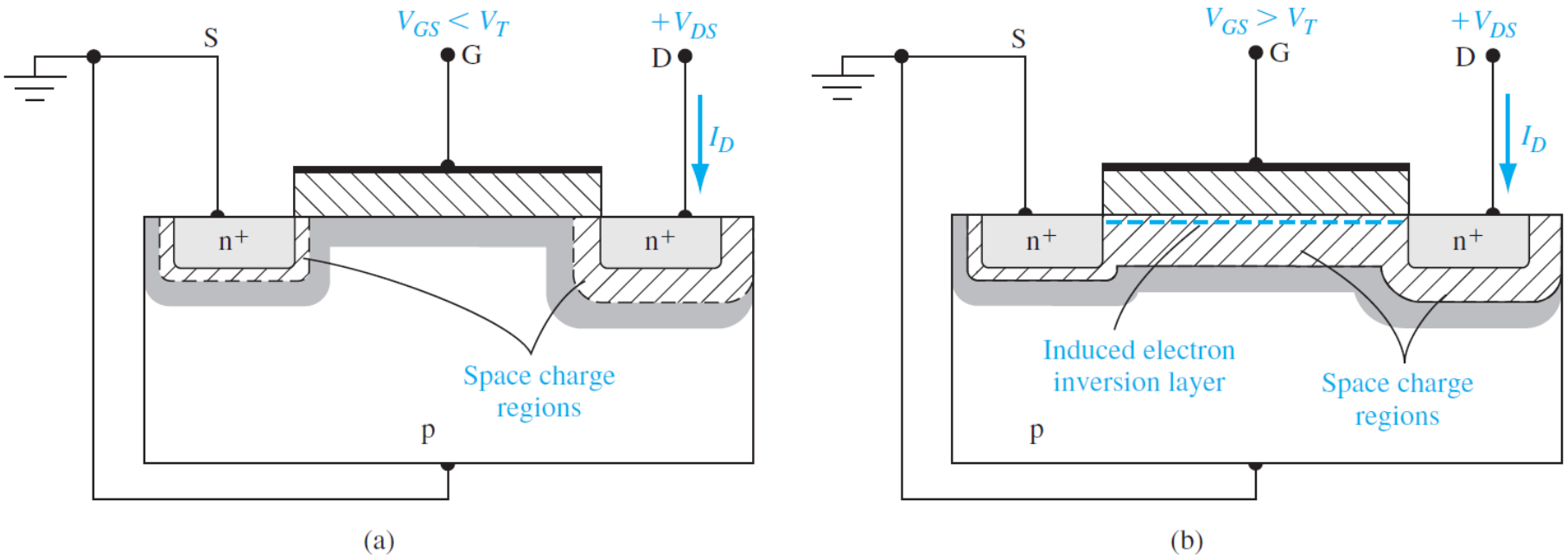


Cross section and circuit symbol for a p-channel depletion mode MOSFET

Current–Voltage Relationship—Concepts

- Figure shows an n-channel enhancement mode MOSFET with a gate-to source voltage that is less than the threshold voltage and with only a very small drain-to-source voltage.
- The source and substrate, or body, terminals are held at ground potential.
- With this bias configuration, there is no electron inversion layer, the drain-to-substrate pn junction is reverse biased, and the drain current is zero
- Figure shows the same MOSFET with an applied gate voltage such that $V_{GS} > V_T$.
- An electron inversion layer has been created so that when a small drain voltage is applied, the electrons in the inversion layer will flow from the source to the positive drain terminal.
- The conventional current enters the drain terminal and leaves the source terminal. In this ideal case, there is no current through the oxide to the gate terminal.

Current–Voltage Relationship—Concepts



The n-channel enhancement mode MOSFET

(a) With an applied gate voltage $V_{GS} < V_T$

(b) (b) with an applied gate voltage $V_{GS} > V_T$.

Current–Voltage Relationship—Concepts

- For small V_{DS} values, the channel region has the characteristics of a resistor

$$I_D = g_d V_{DS}$$

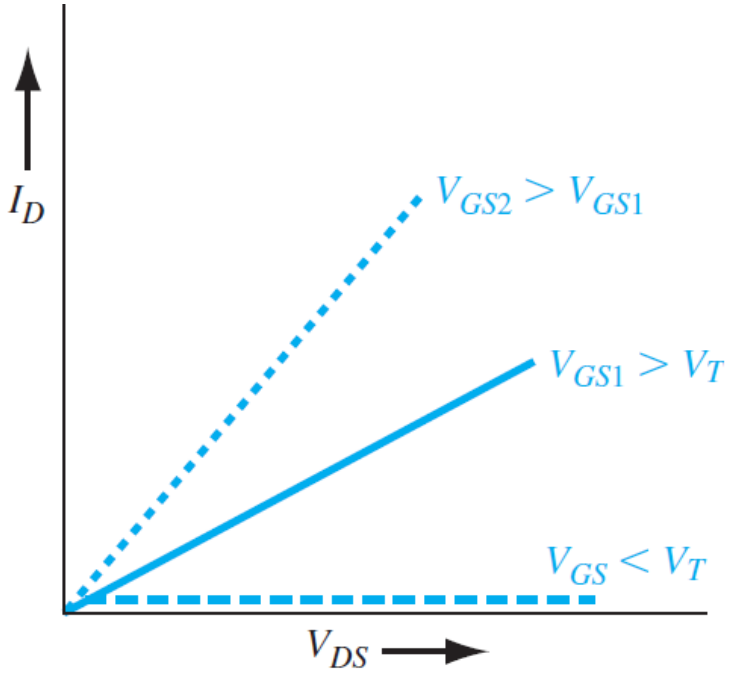
- where g_d is defined as the channel conductance in the limit as $V_{DS} \rightarrow 0$.
- The channel conductance is given by

$$g_d = \frac{W}{L} \cdot \mu_n |Q_n'|$$

- where μ_n is the mobility of the electrons in the inversion layer and Q'_n is the magnitude of the inversion layer charge per unit area.
- The inversion layer charge is a function of the gate voltage; thus, the basic MOS transistor action is the modulation of the channel conductance by the gate voltage.
- The channel conductance, in turn, determines the drain current.

Current–Voltage Relationship—Concepts

- The I_D versus V_{DS} characteristics, for small values of V_{DS}.
- When $V_{GS} < V_T$, the drain current is zero.
- As V_{GS} becomes larger than V_T, channel inversion charge density increases, which increases the channel conductance.
- A larger value of g_d produces a larger initial slope of the I_D versus V_{DS} characteristic as shown in the figure.



Current–Voltage Relationship—Concepts

- Figure shows the basic MOS structure for the case when $V_{GS} > V_T$ and the applied V_{DS} voltage is small.
- The thickness of the inversion channel layer in the figure qualitatively indicates the relative charge density, which is essentially constant along the entire channel length for this case. The corresponding I_D versus V_{DS} curve is shown in the figure.
- Figure shows the situation when the V_{DS} value increases. As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases.
- The incremental conductance of the channel at the drain decreases, which then means that the slope of the I_D versus V_{DS} curve will decrease. This effect is shown in the I_D versus V_{DS} curve in the figure.

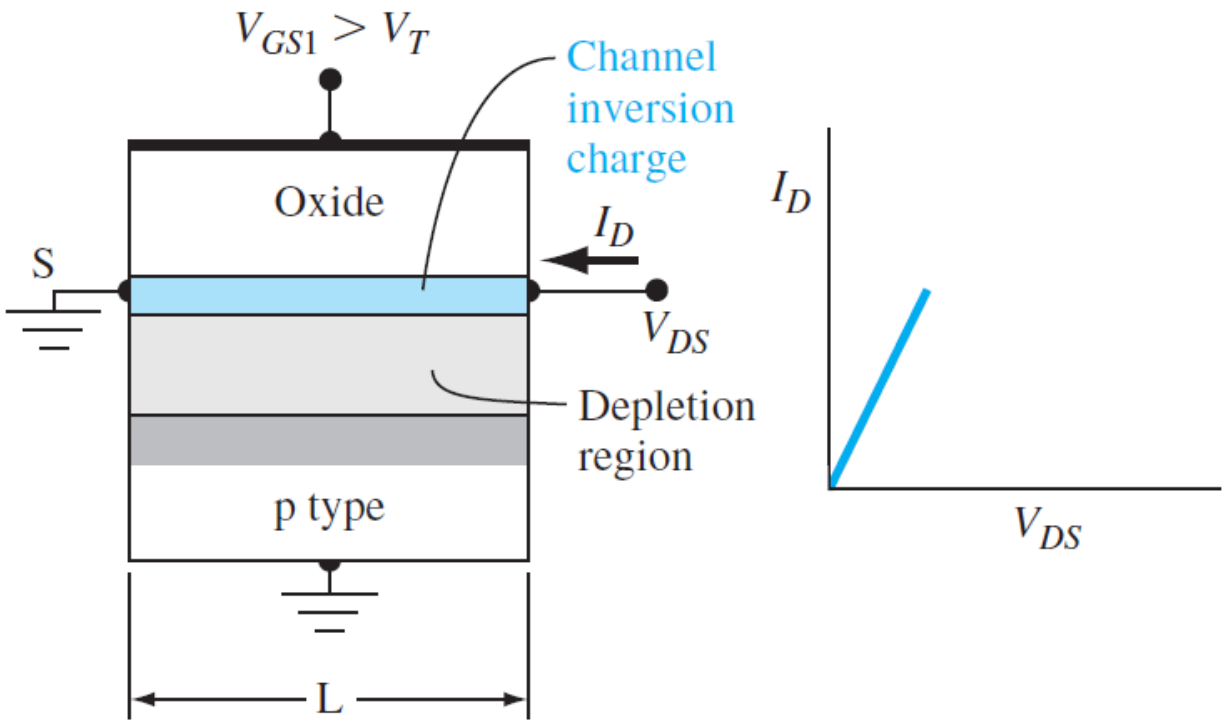
Current–Voltage Relationship—Concepts

- When V_{DS} increases to the point where the potential drop across the oxide at the drain terminal is equal to V_T, the induced inversion charge density is zero at the drain terminal.
- At this point, the incremental conductance at the drain is zero, which means that the slope of the I_D versus V_{DS} curve is zero.

$$V_{GS} - V_{DS}(\text{sat}) = V_T \qquad V_{DS}(\text{sat}) = V_{GS} - V_T$$

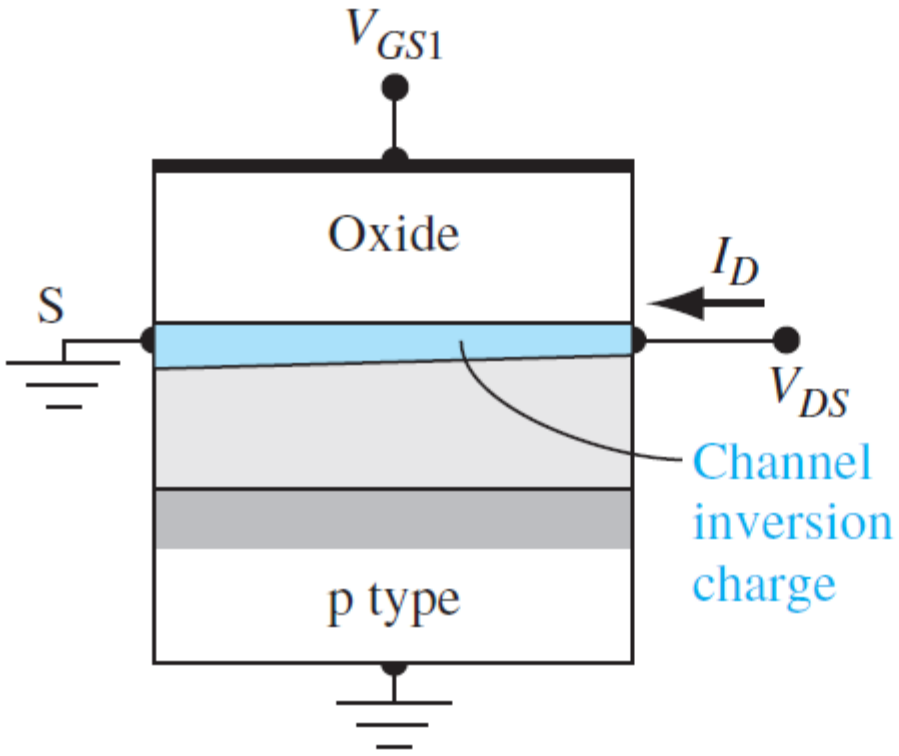
- where V_{DS}(sat) is the drain-to-source voltage producing zero inversion charge density at the drain terminal.
- When V_{DS} becomes larger than the V_{DS}(sat) value, the point in the channel at which the inversion charge is just zero moves toward the source terminal.
- In this case, electrons enter the channel at the source, travel through the channel toward the drain, and then, at the point where the charge goes to zero, the electrons are injected into the space charge region where they are swept by the E-field to the drain contact

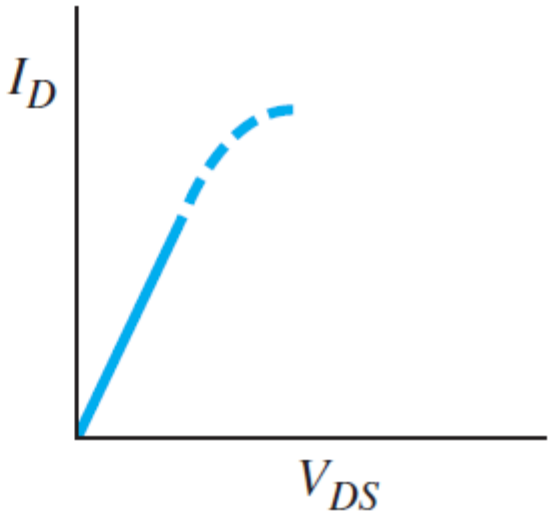
Current–Voltage Relationship—Concepts



Cross section and I_D versus V_{DS} curve when $V_{GS} > V_T$ for (a) a small V_{DS} value

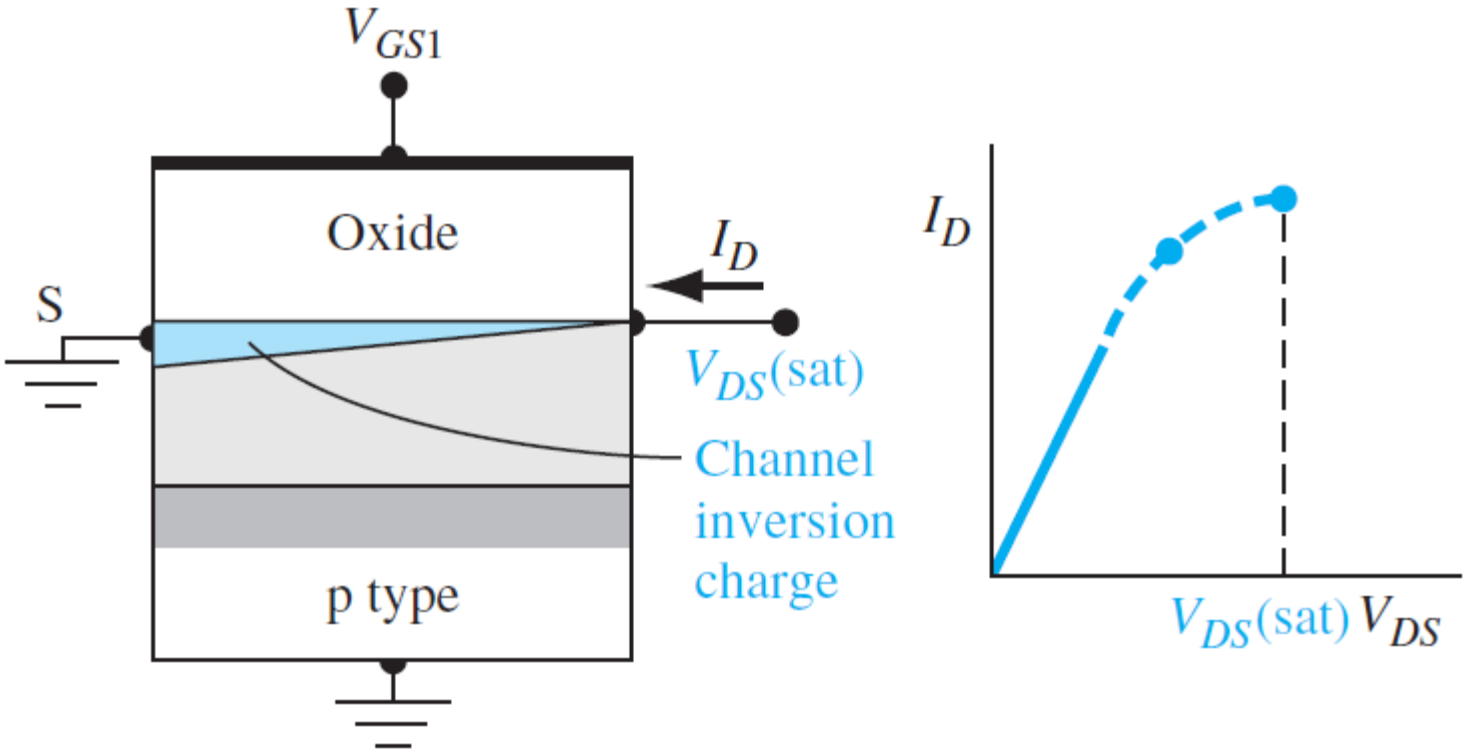
Current–Voltage Relationship—Concepts





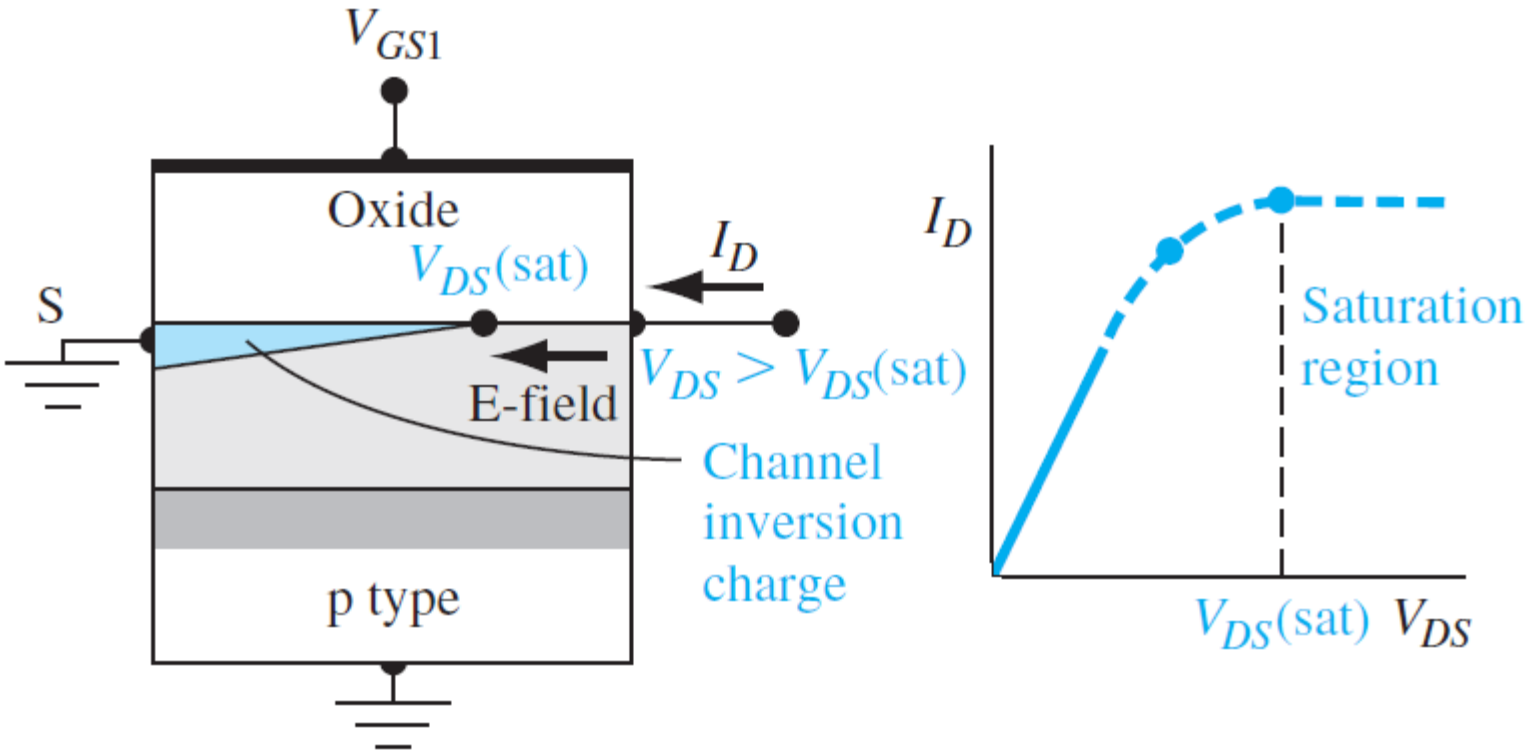
Cross section and I_D versus V_{DS} curve when $V_{GS} > V_T$ for (b) a large V_{DS} value

Current–Voltage Relationship—Concepts



Cross section and I_D versus V_{DS} curve when V_{GS} V_T for (c) a value of $V_{DS} = V_{DS}(sat)$, and (d) a value of $V_{DS} > V_{DS}(sat)$.

Current–Voltage Relationship—Concepts

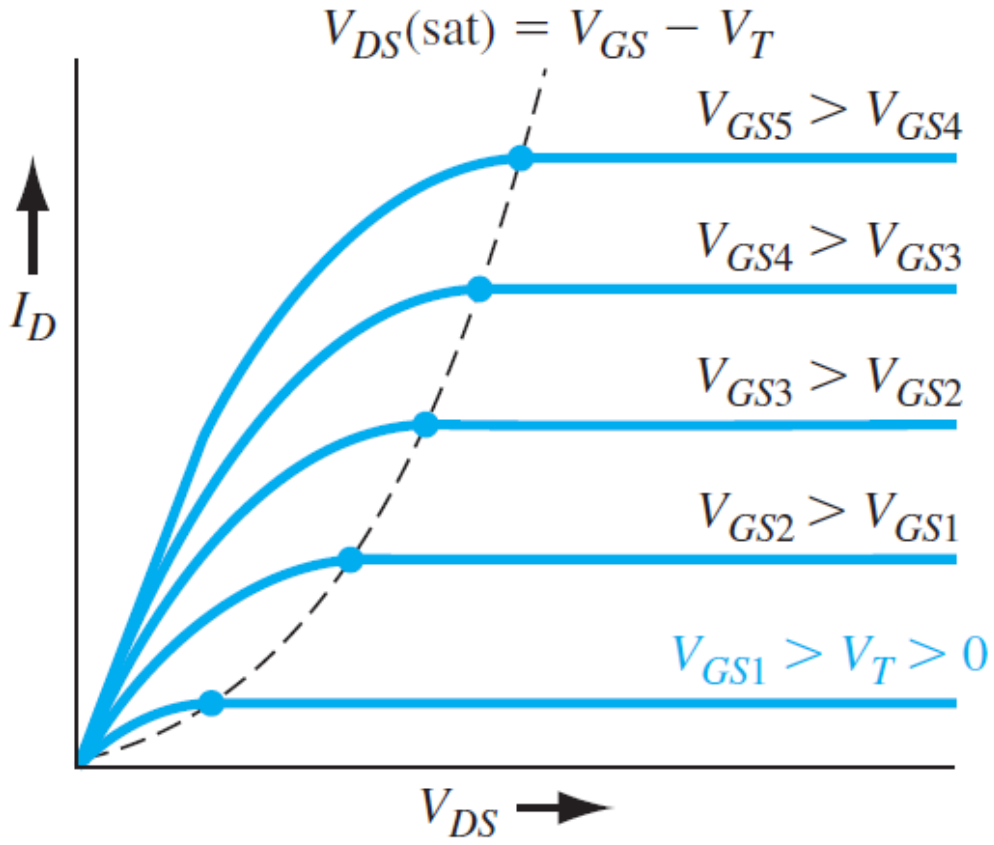


Cross section and I_D versus V_{DS} curve when V_{GS} V_T for a value of $V_{DS} > V_{DS}$(sat).

Current–Voltage Relationship—Concepts

- If we assume that the change in channel length ΔL is small compared to the original length L, then the drain current will be a constant for $V_{DS} > V_{DS}(sat)$.
- The region of the I_D versus V_{DS} characteristic is referred to as the saturation region.
- When V_{GS} changes, the I_D versus V_{DS} curve will change.
- We saw that, if V_{GS} increases, the initial slope of I_D versus V_{DS} increases.
- We can generate the family of curves for this n-channel enhancement mode MOSFET as shown in Figure

Current–Voltage Relationship—Concepts



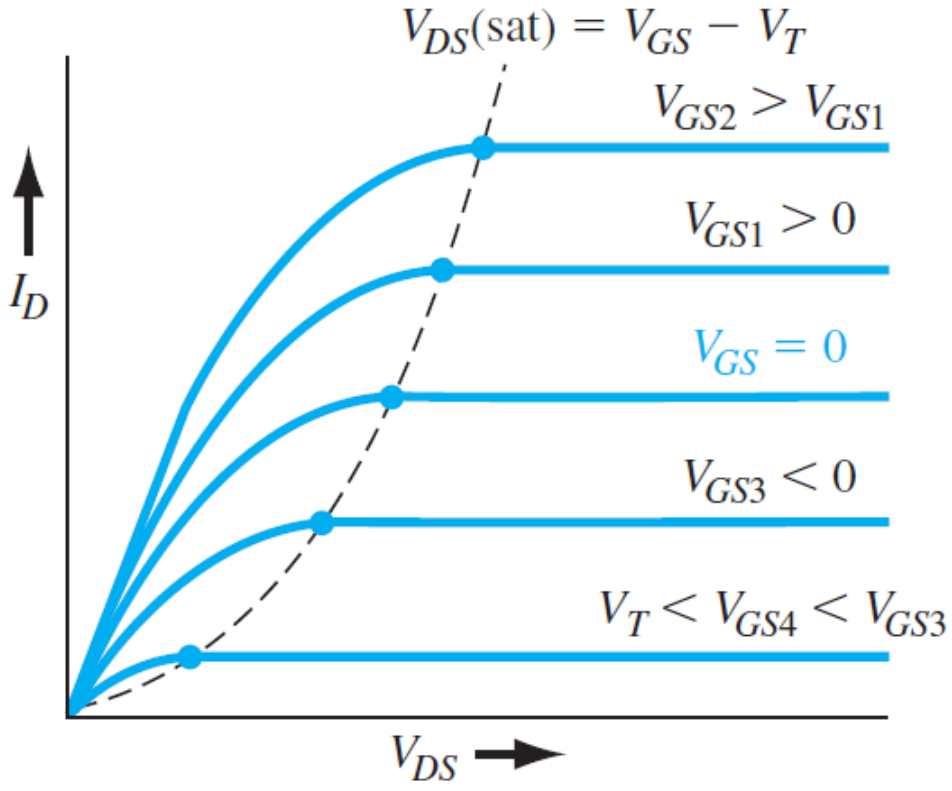
Family of ID versus VDS curves for an n-channel enhancement mode MOSFET.

n-channel depletion mode MOSFET

- If the n-channel region is actually an induced electron inversion layer created by the metal– semiconductor work function difference and fixed charge in the oxide, the current–voltage characteristics are exactly the same as we have discussed, except that V_T is a negative quantity.
- We may also consider the case when the n-channel region is actually an n-type semiconductor region.
- In this type of device, a negative gate voltage will induce a space charge region under the oxide, reducing the thickness of the n-channel region.
- The reduced thickness decreases the channel conductance, which reduces the drain current. A positive gate voltage will create an electron accumulation layer, which increases the drain current.

n-channel depletion mode MOSFET

- One basic requirement for this device is that the channel thickness t_c must be less than the maximum induced space charge width in order to be able to turn the device off.



ideal current–voltage relation for n-channel enhancement MOSFET

- In the non saturation region $0 \leq V_{DS} \leq V_{DS}(\text{sat})$

$$I_D = \frac{W\mu_n C_{\text{ox}}}{2L}\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right]$$

$$I_D = \frac{k_n'}{2} \cdot \frac{W}{L} \cdot \left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad k_n' = \mu_n C_{ox}$$

$$I_D = K_n\left[2(V_{GS} - V_T)V_{DS} - V_{DS}^2\right] \qquad K_n = (W\mu_n C_{ox})/2L = (k_n'/2) \cdot (W/L)$$

- The parameter k'_n is called the *process conduction parameter* for the n-channel MOSFET and has units of A/V^2.
- The parameter K_n is called the *conduction parameter* for the n-channel MOSFET and also has units of A/V^2.

ideal current–voltage relation for n-channel enhancement MOSFET

- When the transistor is biased in the saturation region

$$V_{DS} \geq V_{DS}(\text{sat}).$$

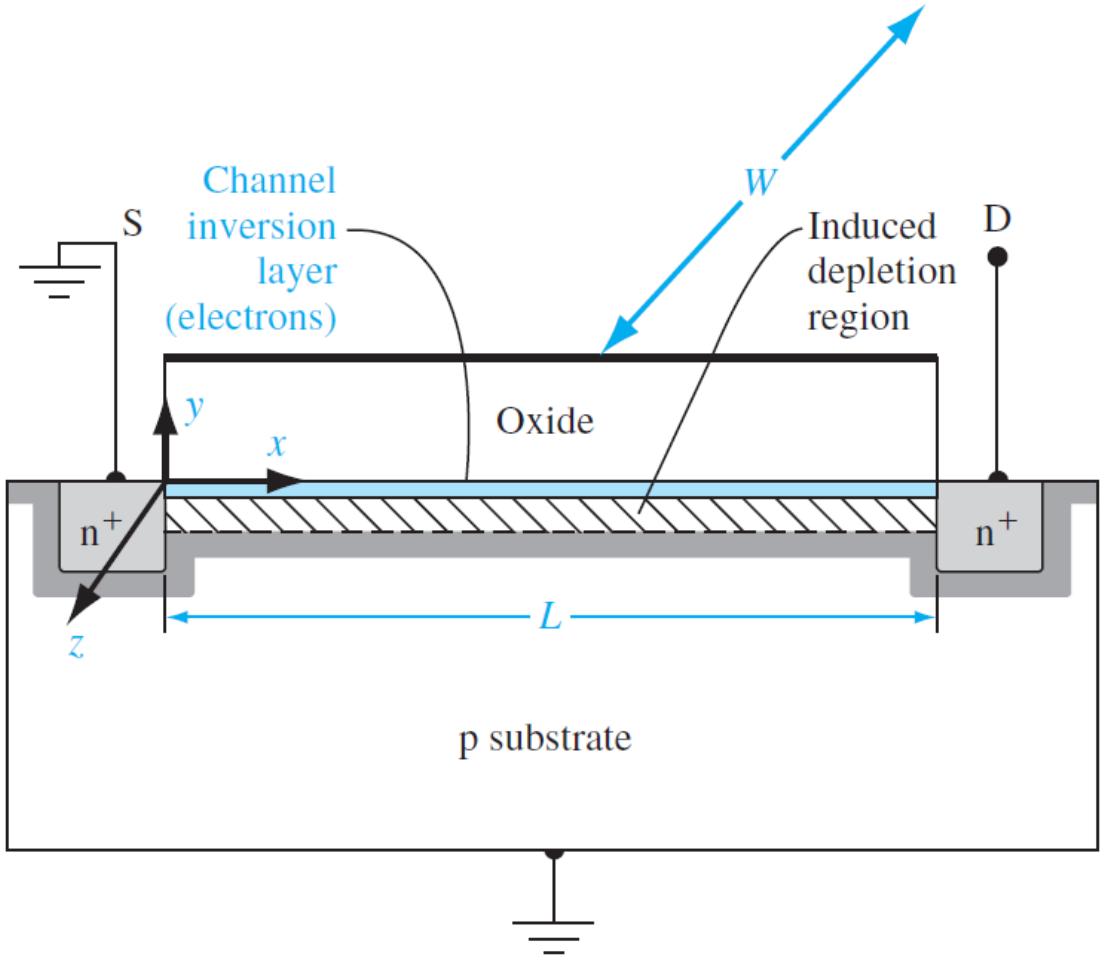
$$I_D = \frac{W\mu_n C_{\text{ox}}}{2L}(V_{GS} - V_T)^2$$

$$I_D = \frac{k'_n}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2$$

$$I_D = K_n(V_{GS} - V_T)^2$$

- the design of a MOSFET, in terms of current capability, is determined by the width-to-length parameter

n-channel enhancement MOSFET



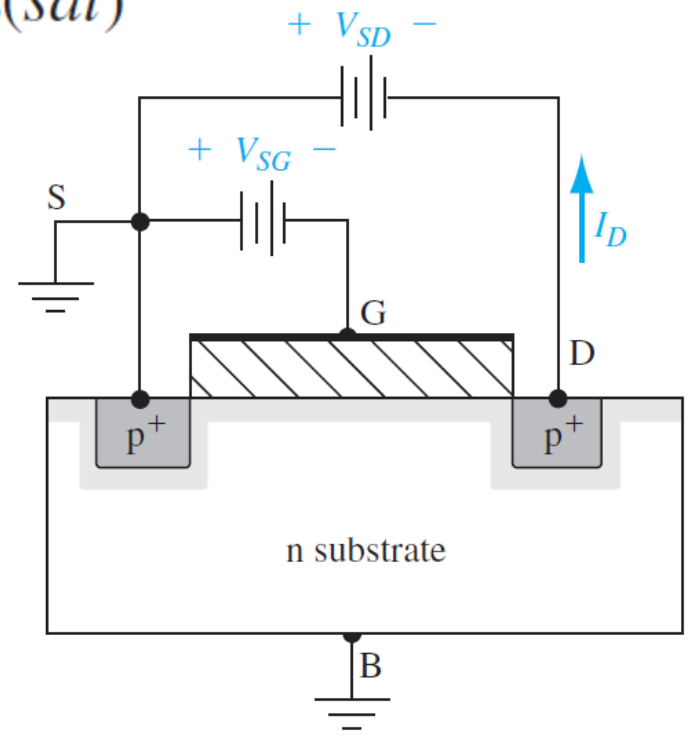
ideal current–voltage relation for p-channel enhancement MOSFET

- nonsaturation region $0 \le V_{SD} \le V_{SD}(sat)$

$$I_D = \frac{W\mu_p C_{ox}}{2L}\left[2(V_{SG} + V_T)V_{SD} - V_{SD}^2\right]$$

$$I_D = \frac{k_p'}{2} \cdot \frac{W}{L} \cdot \left[2(V_{SG} + V_T)V_{SD} - V_{SD}^2\right]$$

$$= K_p\left[2(V_{SG} + V_T)V_{SD} - V_{SD}^2\right]$$



- saturation region $V_{SD} \ge V_{SD}\,(sat)$

$$I_D(\text{sat}) = \frac{W\mu_p C_{ox}}{2L}(V_{SG} + V_T)^2$$

$$I_D = \frac{k_p'}{2} \cdot \frac{W}{L} \cdot (V_{SG} + V_T)^2 = K_p(V_{SG} + V_T)^2$$

$$k_p' = \mu_p C_{ox}$$

$$K_p = (W\mu_p C_{ox})/(2L)$$

$$= (k_p'/2) \cdot (W/L)$$

Transconductance

- The MOSFET transconductance is defined as the change in drain current with respect to the corresponding change in gate voltage

$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$

- The transconductance is sometimes referred to as the transistor gain
- If we consider an n-channel MOSFET operating in the nonsaturation region

$$g_{mL} = \frac{\partial I_D}{\partial V_{GS}} = \frac{W \mu_n C_{ox}}{L} \cdot V_{DS}$$

- The transconductance increases linearly with V_{DS} but is independent of V_{GS} in the nonsaturation region

Transconductance

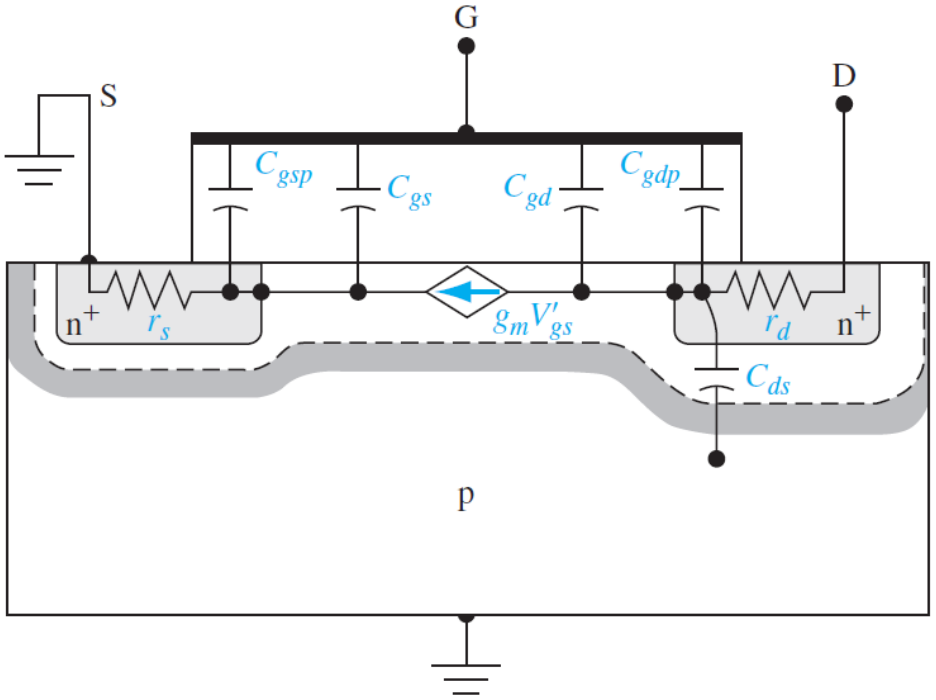
- The I–V characteristics of an n-channel MOSFET in the saturation region
- The transconductance in this region of operation is given by

$$g_{ms} = \frac{\partial I_D(\text{sat})}{\partial V_{GS}} = \frac{W\mu_n C_{\text{ox}}}{L}(V_{GS} - V_T)$$

- In the saturation region, the transconductance is a linear function of V_{GS} and is independent of V_{DS}
- The transconductance is a function of the geometry of the device as well as of carrier mobility and threshold voltage.
- The transconductance increases as the width of the device increases, and it also increases as the channel length and oxide thickness decrease.
- In the design of MOSFET circuits, the size of the transistor, in particular the channel width W, is an important engineering design parameter.

Small-Signal Equivalent Circuit

- The small-signal equivalent circuit of the MOSFET is constructed from the basic MOSFET geometry.
- A model based on the inherent capacitances and resistances within the transistor structure, along with elements that represent the basic device equations.
- One simplifying assumption we will make in the equivalent circuit is that the source and substrate are both tied to ground potential



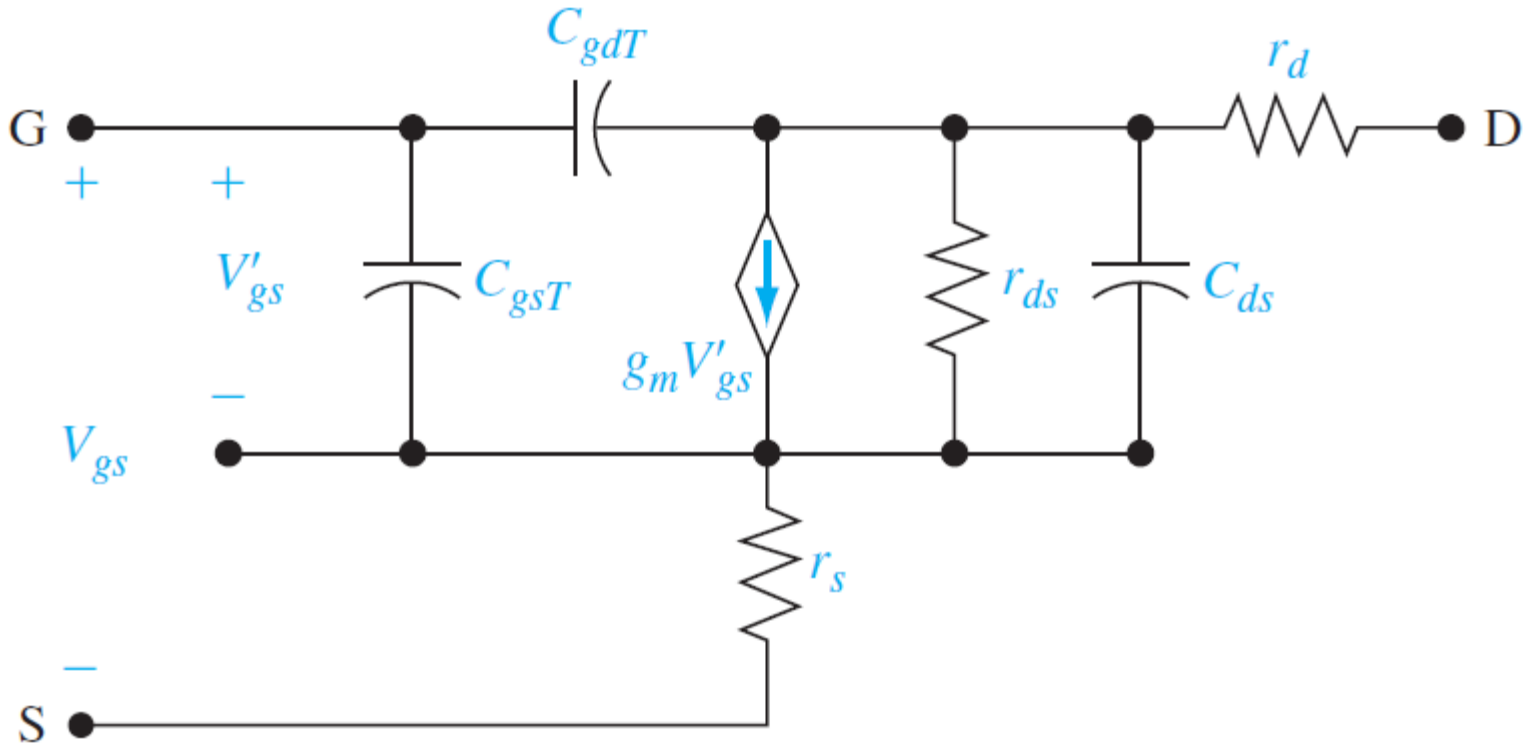
Small-Signal Equivalent Circuit

- Two of the capacitances connected to the gate are inherent in the device.
- These capacitances are C_{gs} and C_{gd}, which represent the interaction between the gate and the channel charge near the source and drain terminals.
- The remaining two gate capacitances, C_{gsp} and C_{gdp}, are parasitic or overlap capacitances.
- In real devices, the gate oxide will overlap the source and drain contacts because of tolerance or fabrication factors.
- the drain overlap capacitance—C_{gdp}, in particular—will lower the frequency response of the device.
- The parameter C_{ds} is the drain-to-substrate pn junction capacitance, and r_s and r_d are the series resistances associated with the source and drain terminals.
- The small-signal channel current is controlled by the internal gate-to-source voltage through the transconductance.

Small-Signal Equivalent Circuit (n Channel)

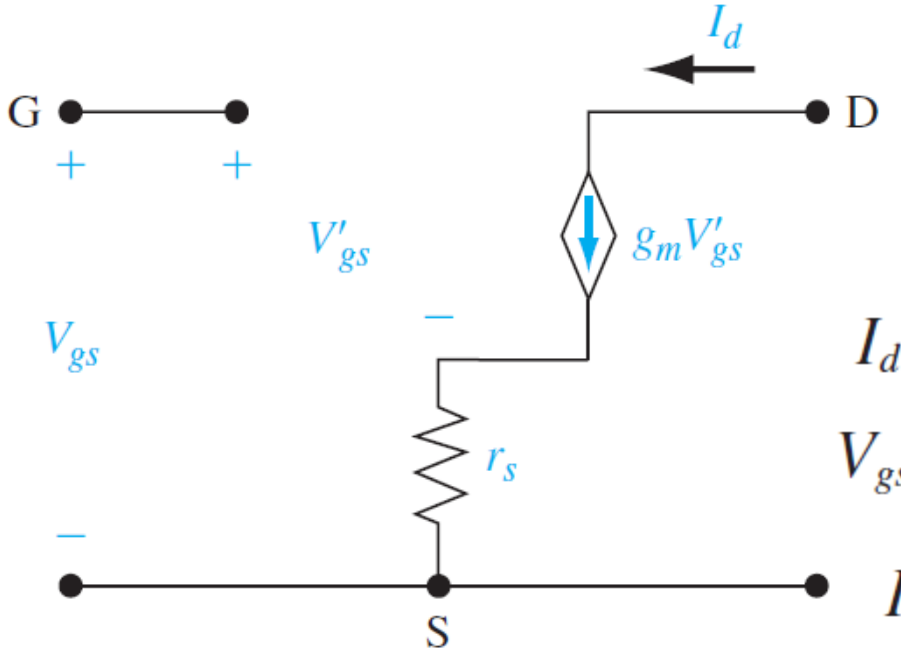
- The voltage V'_{gs} is the internal gate-to-source voltage that controls the channel current.
- The parameters C_{gsT} and C_{gdT} are the total gate-to-source
- and total gate-to-drain capacitances.
- One parameter, r_{ds}, resistance is associated with the slope I_D versus V_{DS}.
- In the ideal MOSFET biased in the saturation region, I_D is independent of V_{DS} so that r_{ds} would be infinite.
- In short-channel-length devices, in particular, r_{ds} is finite because of channel length modulation

Small-Signal Equivalent Circuit (n Channel common source MOSFET)



Simplified low frequency small-signal equivalent circuit

- The source resistance reduces the effective transconductance or transistor gain



$$I_d = g_m V'_{gs}$$

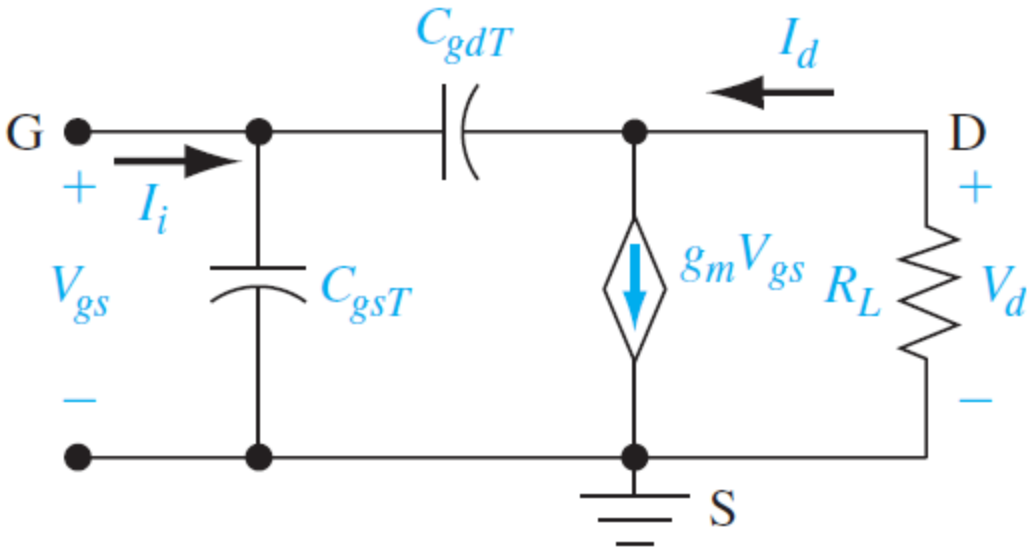
$$V_{gs} = V'_{gs} + (g_m V'_{gs}) r_s = (1 + g_m r_s) V'_{gs}$$

$$I_d = \left(\frac{g_m}{1 + g_m r_s} \right) V_{gs} = g'_m V_{gs}$$

Simplified, lowfrequency small-signal equivalent circuit of common-source n-channel MOSFET including source resistance r_s

Simplified high frequency small-signal equivalent circuit

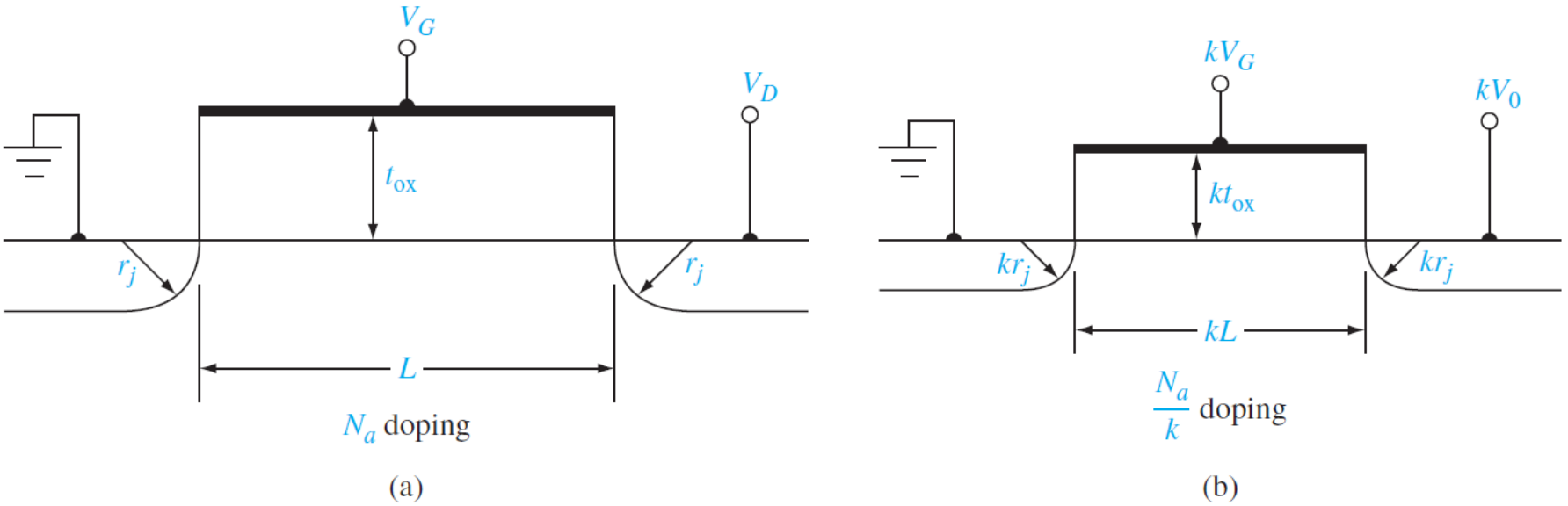
- There are two basic frequency limitation factors in the MOSFET.
- The first factor is the channel transit time. The second limiting factor is the gate or capacitance charging time.
- If we neglect r_s, r_d, r_{ds}, and C_{ds}, the resulting equivalent small-signal circuit is shown in figure



MOSFET Scaling

- Much of the progress in semiconductor integrated circuit technology can be attributed to the ability to shrink or scale the devices.
- Scaling down MOSFETs has a multitude of benefits. The improvement of packing density, speed and power dissipation.
- if lateral dimensions such as the channel length and width are reduced by a factor of K, so should the vertical dimensions such as source/drain junction depths (x_j) and gate insulator thickness.
- Scaling of depletion widths is achieved indirectly by scaling up doping concentrations. However, if we simply reduced the dimensions of the device and kept the power supply voltages the same, the internal electric fields in the device would increase.
- For ideal scaling, power supply voltages should also be reduced to keep the internal electric fields reasonably constant from one technology generation to the next.

MOSFET Scaling



Cross section of (a) original NMOS transistor and (b) scaled NMOS transistor.

MOSFET Scaling

- As seen in the figure, the channel length is scaled from L to kL.
- To maintain a constant horizontal electric field, the drain voltage must also be scaled from V_D to kV_D.
- The maximum gate voltage will also be scaled from V_G to kV_G so that the gate and drain voltages remain compatible.
- To maintain a constant vertical electric field, the oxide thickness then must also be scaled from t_{ox} to kt_{ox}.
- The maximum depletion width at the drain terminal, for a one-sided pn junction, is

$$x_D = \sqrt{\frac{2\epsilon(V_{bi} + V_D)}{eN_a}}$$

- Since the channel length is being reduced, the depletion widths also need to be reduced.
- If the substrate doping concentration is increased by the factor $(1/k)$, then the depletion width is reduced by approximately the factor k since V_D is reduced by k.

MOSFET Scaling

- The drain current per channel width, for the transistor biased in the saturation region, can be written as

$$\frac{I_D}{W} = \frac{\mu_n \epsilon_{ox}}{2 t_{ox} L} (V_G - V_T)^2 \rightarrow \frac{\mu_n \epsilon_{ox}}{2(k t_{ox})(kL)} (kV_G - V_T)^2 \approx \text{constant}$$

- The drift current per channel width remains essentially a constant, so if the channel width is reduced by *k*, then the drain current is also reduced by *k*.
- The area of the device, $A=WL$, is then reduced by k^2 and the power, $P = IV$, is also reduced by k^2.
- The power density in the chip remains unchanged.

Scaling effect on circuit parameters

Table 11.1 | Summary of constant-field device scaling

	Device and circuit parameters	Scaling factor ($k < 1$)
Scaled parameters	Device dimensions (L, t_{ox}, W, x_j)	k
	Doping concentration (N_a, N_d)	$1/k$
	Voltages	k
Effect on device parameters	Electric field	1
	Carrier velocity	1
	Depletion widths	k
	Capacitance ($C = \epsilon A/t$)	k
	Drift current	k
Effect on circuit parameters	Device density	$1/k^2$
	Power density	1
	Power dissipation per device ($P = IV$)	k^2
	Circuit delay time ($\approx CV/I$)	k
	Power−delay product ($P\tau$)	k^3

Velocity Saturation

- In the analysis of the long-channel MOSFET, we assume the mobility to be constant, which means that the drift velocity increases without limit as the electric field increases.
- In this ideal case, the carrier velocity increases until the ideal current is attained. However, we have seen that the carrier velocity saturates with increasing electric field.
- Velocity saturation will become more prominent in shorter-channel devices since the corresponding horizontal electric field is generally larger.
- In the ideal *I*–*V* relationship, current saturation occurs when the inversion charge density becomes zero at the drain terminal

$$V_{DS} = V_{DS}(\text{sat}) = V_{GS} - V_T$$

Velocity Saturation

- However, velocity saturation can change this saturation condition. Velocity saturation will occur when the horizontal electric field is approximately 10^4 V/cm. If V_{DS} = 5 V in a device with a channel length of L = 1μm, the average electric field is 5 10^4 V/cm. Velocity saturation, then, is very likely to occur in short-channel devices.
- The modified I_D(sat) characteristics are described approximately by

$$I_D(\text{sat}) = W C_{\text{ox}} (V_{GS} - V_T) v_{\text{sat}}$$

THRESHOLD VOLTAGE MODIFICATIONS

- A reduction in channel length increases the transconductance and frequency response of the MOSFET, and a reduction in channel width increases the packing density in an integrated circuit.
- A reduction in either or both the channel length and channel width can affect the threshold voltage.