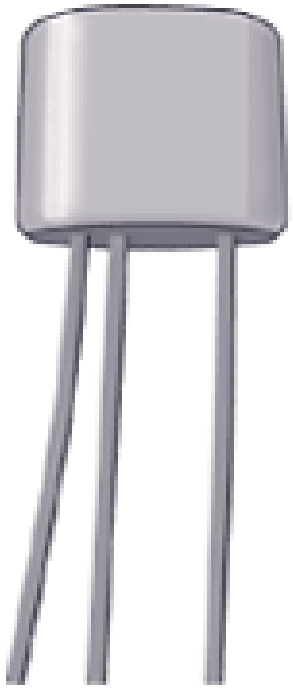
Module 5
Bipolar Junction Transistor

Module:5	Bipolar Junction Transistor	
Device structure and physical operation, Current – Voltage relationship – CB, CE, and CC configuration – Nonideal effects – Base width modulation – Ebers-Moll model. Small signal models, Device capacitances – Equivalent circuit model.		

What is a Transistor?

- Transistor is a semiconductor device that can amplify electronic signals such as radio and television signals.



Transistor Definition

- Transistor is a three-terminal semiconductor device in which the operation depends on the interaction of both majority and minority carriers and hence the name 'Bipolar'.
- The amplification is achieved by passing input current from a region of low resistance to a region of high resistance. This concept of transfer of resistance has been given the name

Transfer – resistor (Transistor)

The output current, voltage, or power are controlled by its input current.

Types of Transistors

- Unipolar Junction Transistor

Current conduction is only due to one type of carriers: **majority carriers**.

- Bipolar Junction Transistor

Current conduction is due to both majority and minority carriers

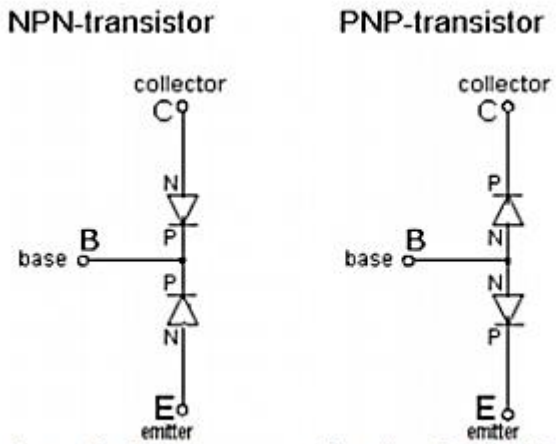
Types of Bipolar Junction Transistors (BJT's)

- NPN transistor
- PNP transistor

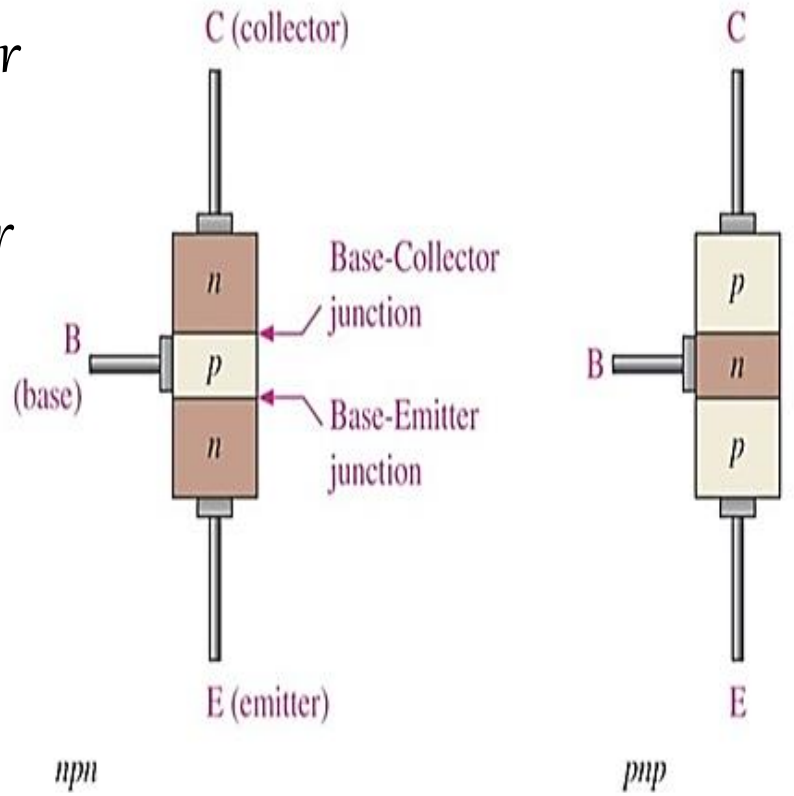
Basic construction

NPN: It is formed by sandwiching p-type semiconductor between 2 N-types.

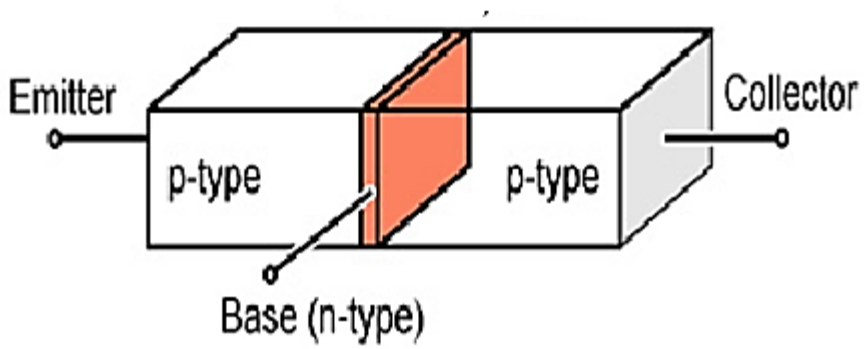
PNP: It is formed by sandwiching n-type semiconductor between 2 P-types.



The equivalent diode representation for the NPN and PNP transistors



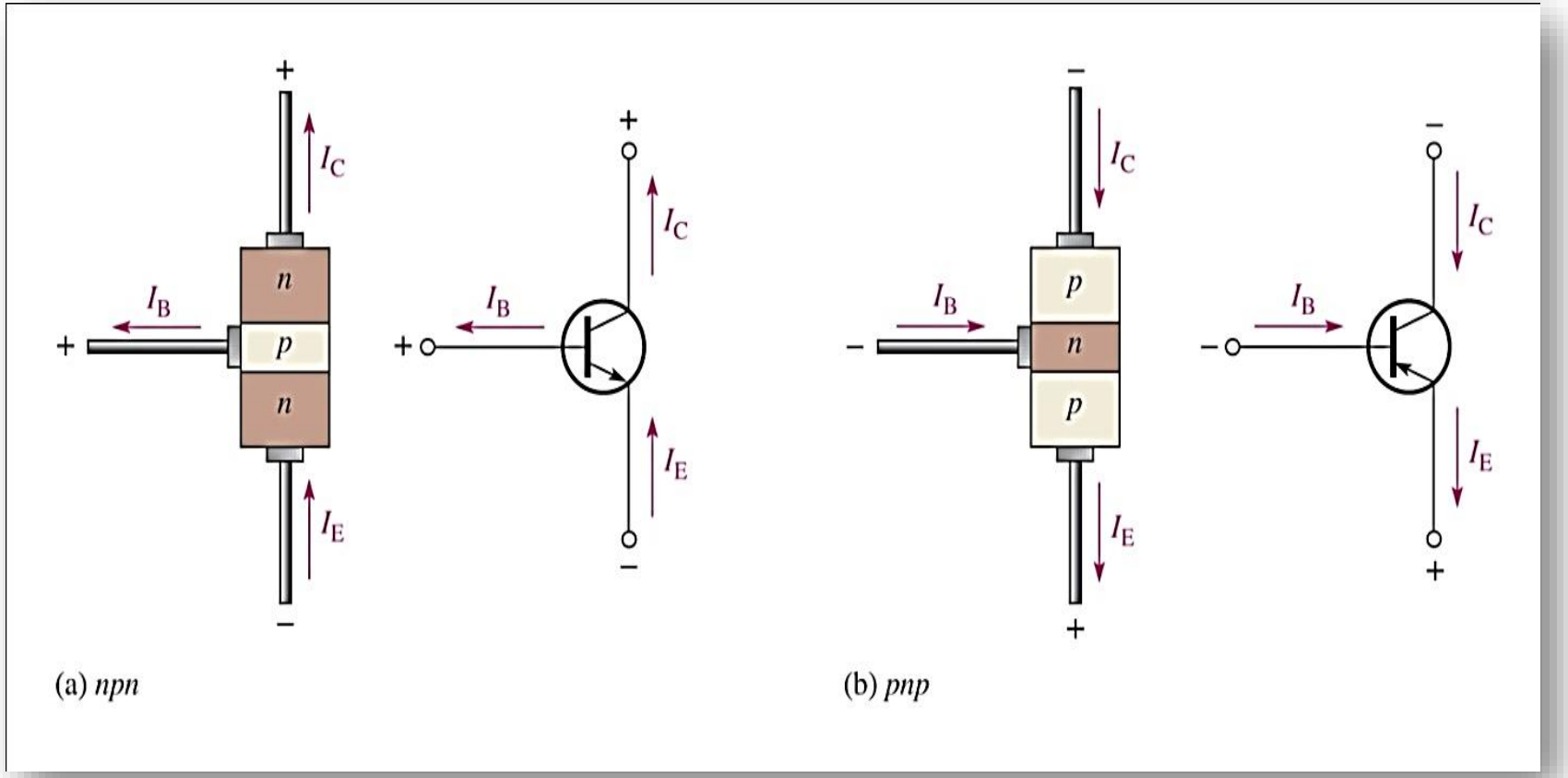
Regions of a Transistor



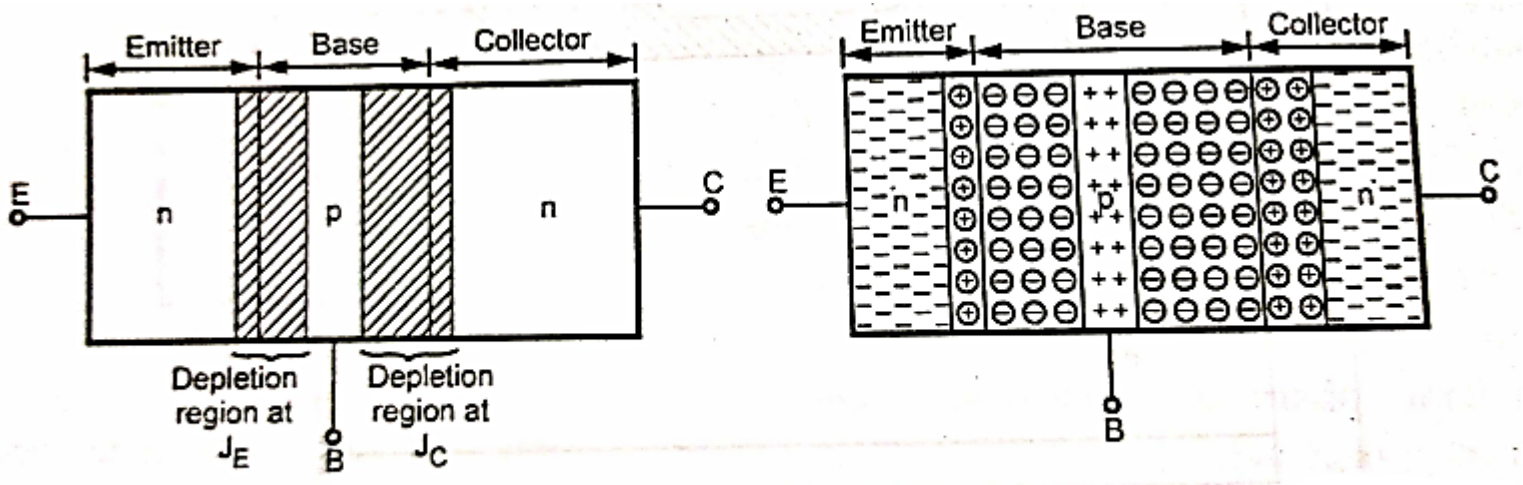
- A transistor has three regions namely,
- Emitter- heavily doped, so that it is able to supply majority charge carriers to the base.

  The emitter is always forward-biased with respect to the base so that it is able to supply the majority charge carriers to the base.
- Base- lightly doped and very thin (order of micrometer), so that it may pass most of the injected charge carriers to the collector.
- Collector – It is to collect majority charge carriers. It is always reverse-biased so as to remove the charge carriers away from its junction with the base It is moderately doped.

Transistor symbols Transistor symbols



Principle of operation of Transistor
Unbiased transistor



Unbiased n-p-n transistor

Principle of operation of Transistor

Biased transistor

Biased Transistor

In order to operate transistor properly as an amplifier, it is necessary to correctly bia the two pn junctions with external voltages. Depending upon external bias voltag polarities used, the transistor works in one of the three regions, viz.

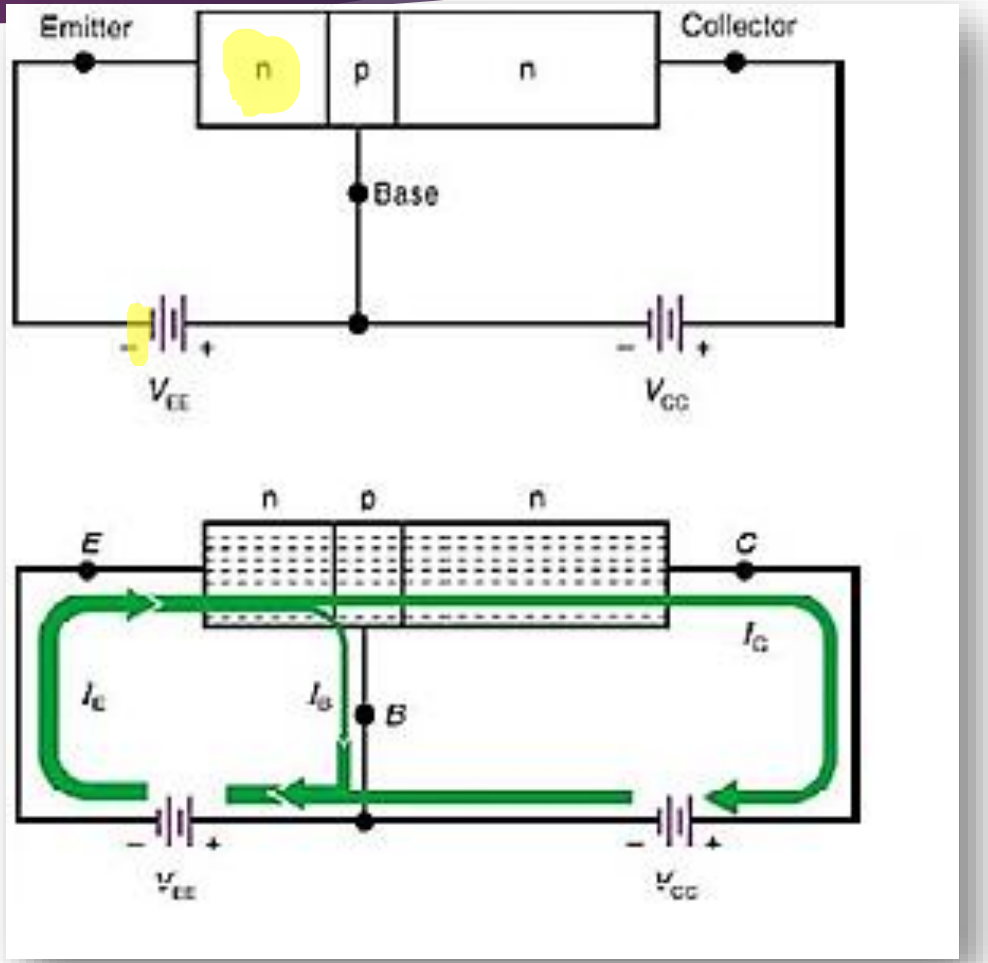
1) *Active region* 2) *Cut-off region* and 3) *Saturation region.*

Region	Emitter base junction	Collector base junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

Transistor biasing

- The base-emitter (BE) junction is forward biased
- The base-collector (BC) junction is reverse biased.

$$I_E = I_B + I_C$$



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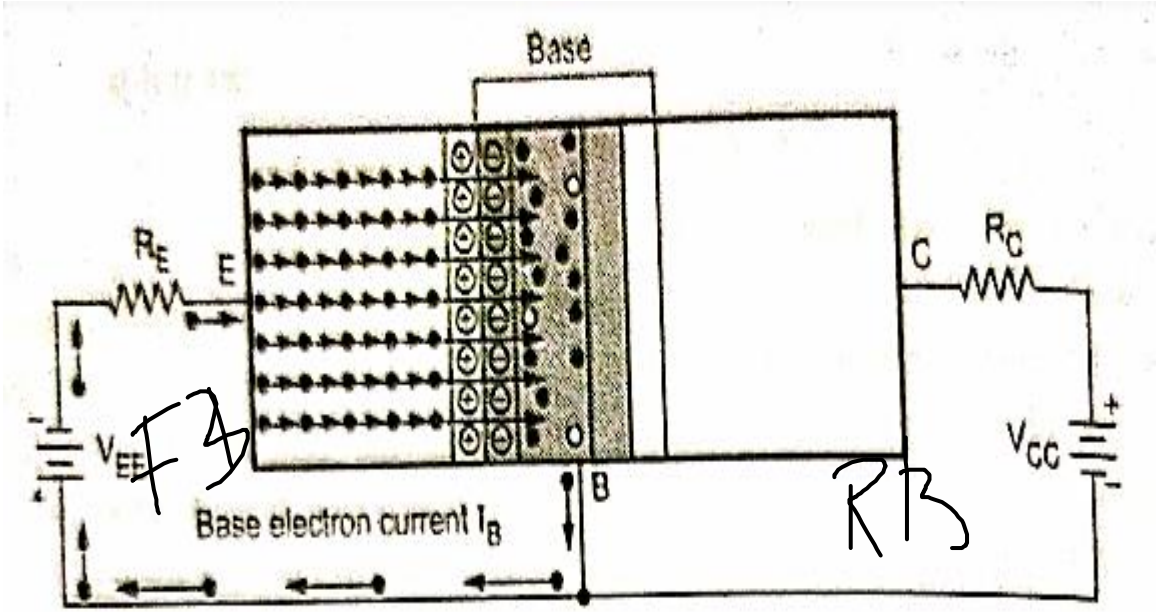
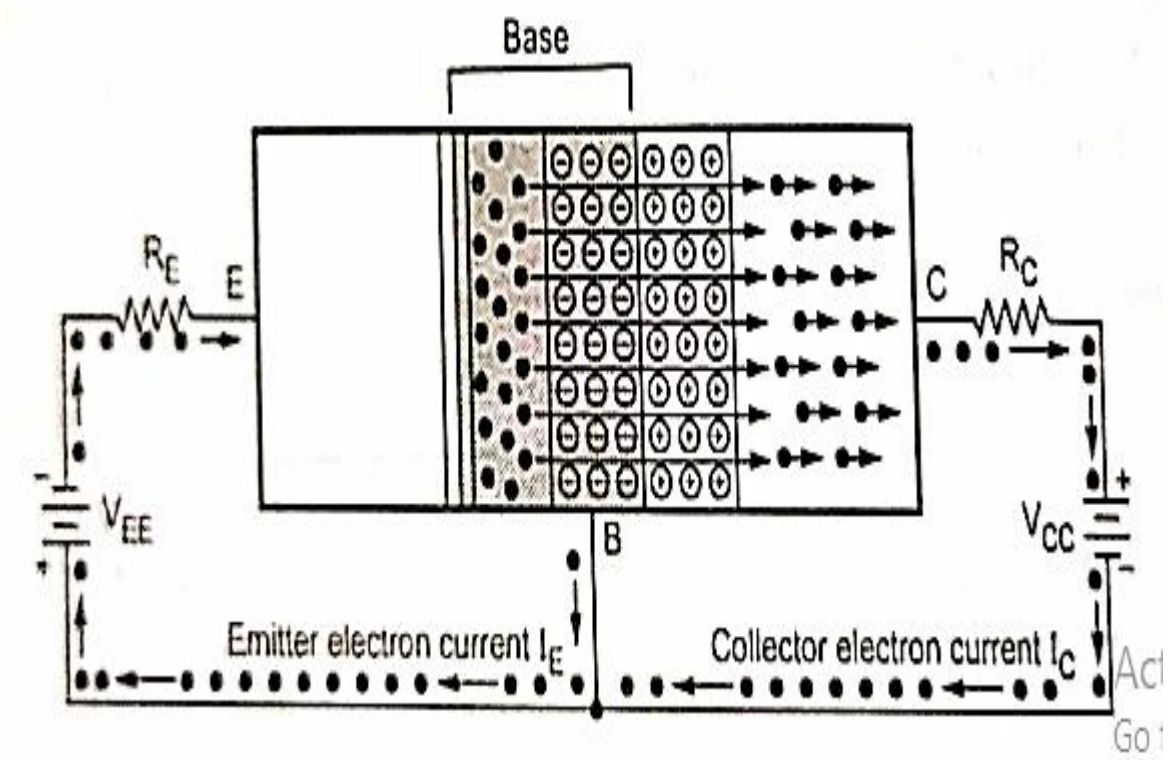
$I_E = I_B + I_C$



Electron flow across emitter-base junction



Electron flow across base-collector junction

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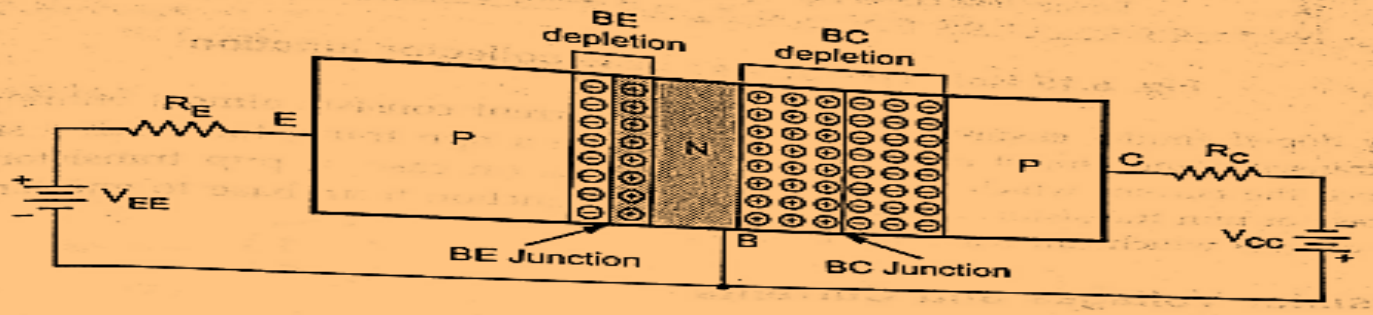
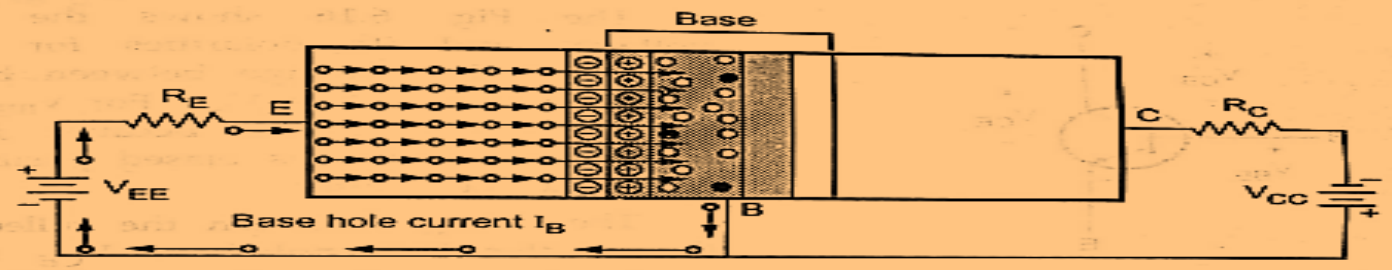
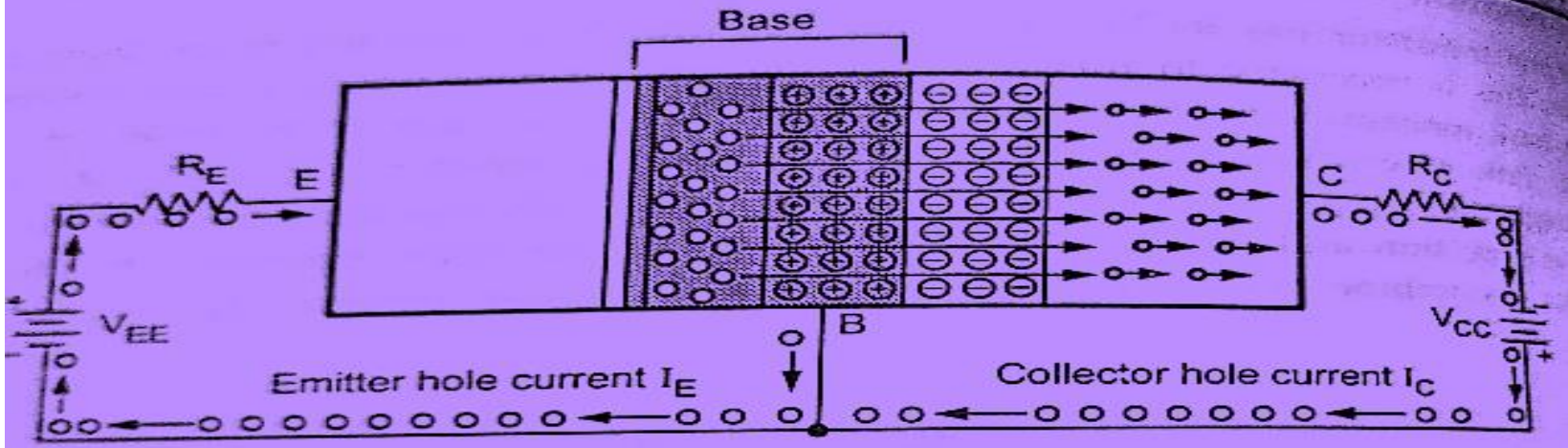


Internal effect of forward biased EB junction and reverse biased CB junction



Hole flow across base emitter junction

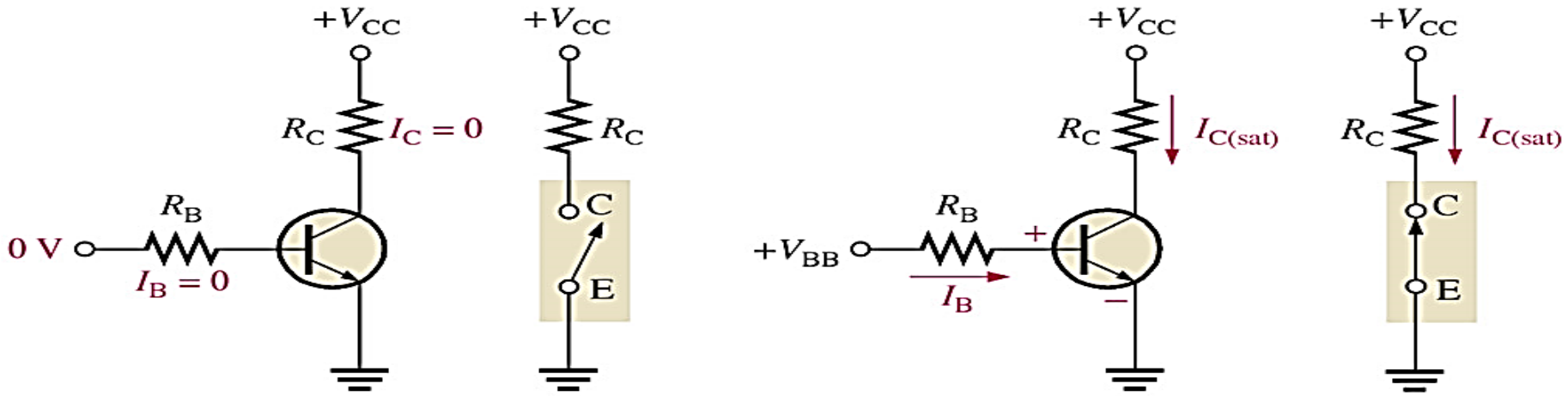


Hole flow across base-collector junction

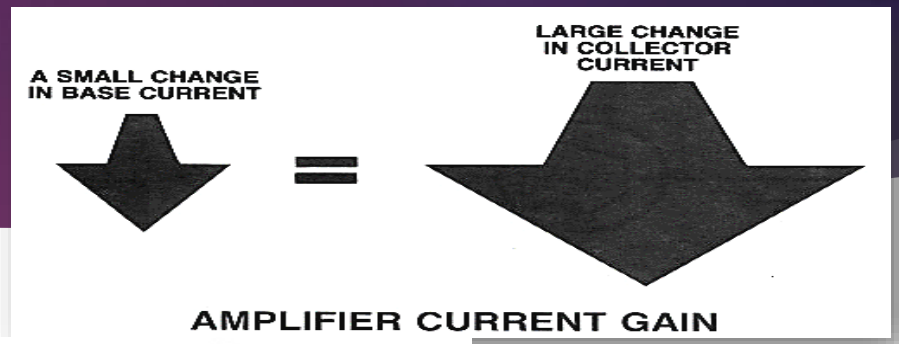
Transistor Applications

Transistor as a switch

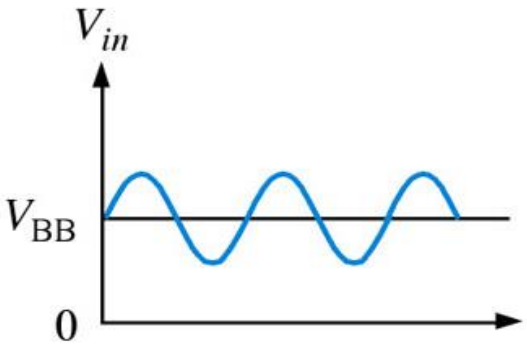
When used as an electronic switch, the transistor is normally operated alternately in cut-off and saturation regions.

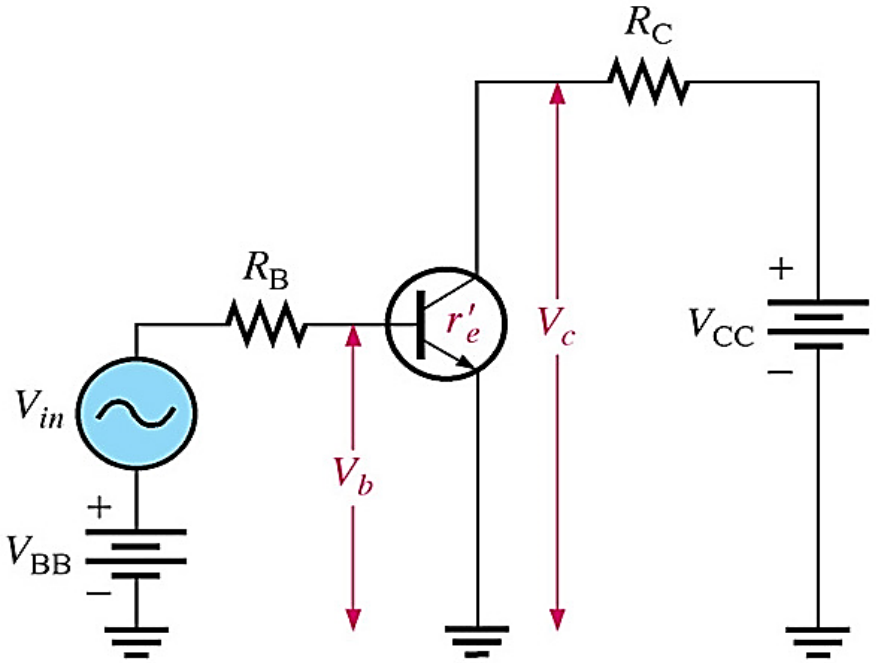


Transistor as Amplifier

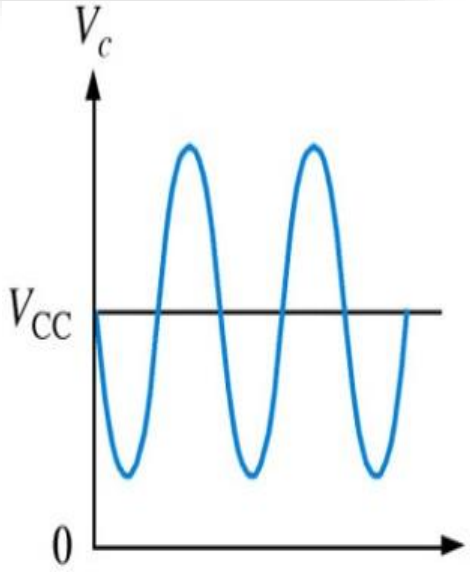


- Due to the small changes in base current the collector current will mimic the input with greater amplitude





(a) Circuit with ac input voltage V_{in} and dc bias voltage superimposed



(b) Waveforms

Why do we need Configurations?

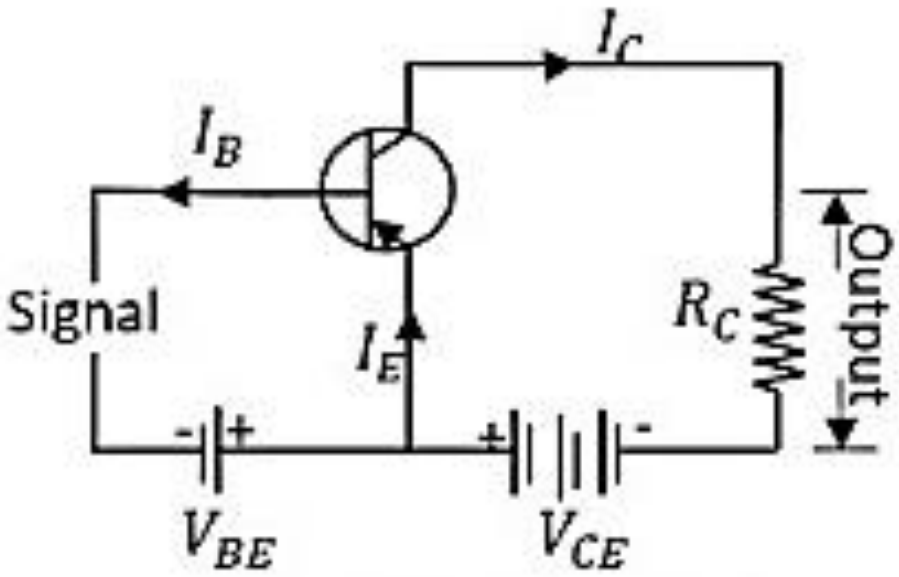
- A Transistor has 3 terminals, the emitter, the base and the collector. Using these 3 terminals the transistor can be connected in a circuit with one terminal common to both input and output in 3 different possible configurations.
- The three types of configurations are **Common Base, Common Emitter** and **Common Collector** configurations. In every configuration, the emitter junction is forward biased and the collector junction is reverse-biased.

BJT Configurations

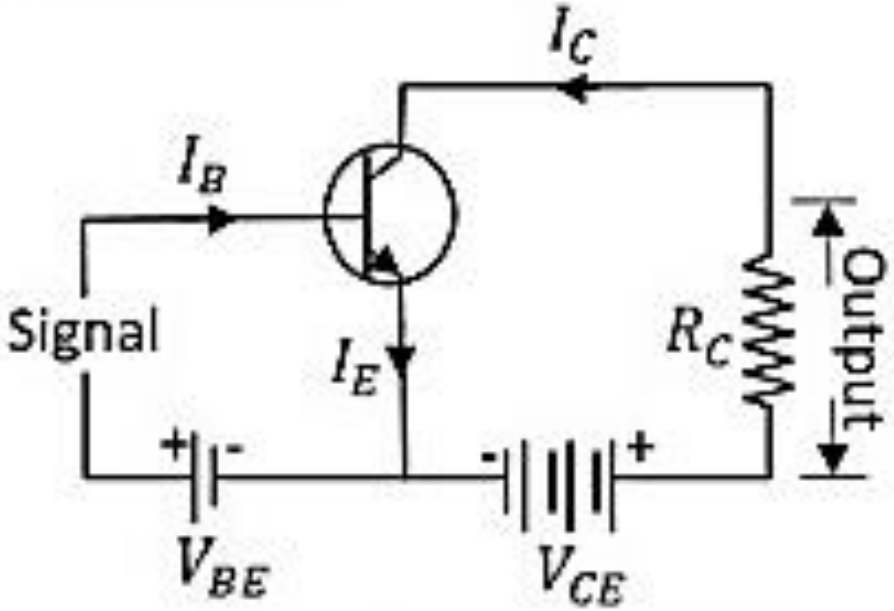
- Common Emitter Configuration
- Common Base Configuration
- Common Collector Configuration

Common Emitter CE Configuration

Common Emitter Connection



Using PNP Transistor



Using NPN Transistor

Input/ Output Characteristics

- Input Characteristics:

Output Voltage is kept Constant by varying output supply.

Measure input voltage and input current by varying input supply

- Output Characteristics:

Input Current is kept Constant by varying Input supply.

Measure Output voltage and Output current by varying the Output supply

Characteristics of CE Configuration

- This configuration provides **good current gain and voltage gain**.
- Keeping V_{CE} constant, with a small increase in V_{BE} the base current I_B increases rapidly than in CB configurations.
- For any value of V_{CE} above knee voltage, I_C is approximately equal to βI_B.

- The input resistance r_i is the ratio of change in base emitter voltage $\$\Delta V_{BE}\$$ to the change in base current $\$\Delta I_B\$$ at constant collector emitter voltage V_{CE}.

$$r_i = \frac{\Delta V_{BE}}{\Delta I_B} \; at\ constant\ V_{CE}$$

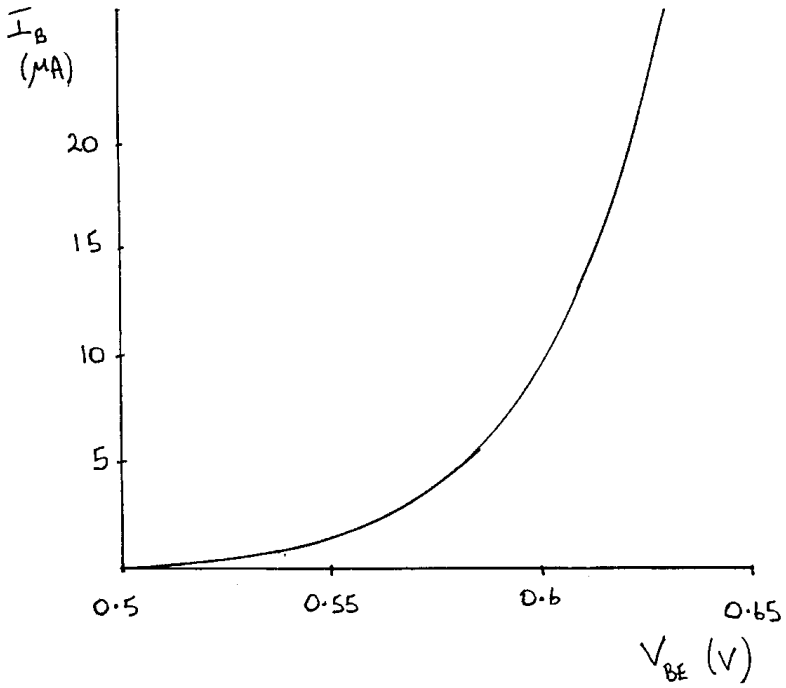
- As the output resistance of CE circuit is less than that of CB circuit.
- This configuration is usually used for bias stabilization methods and audio frequency applications.

·As the input resistance is of very low value, a small value of V_{BE} is enough to produce a large current flow of base current I_B.

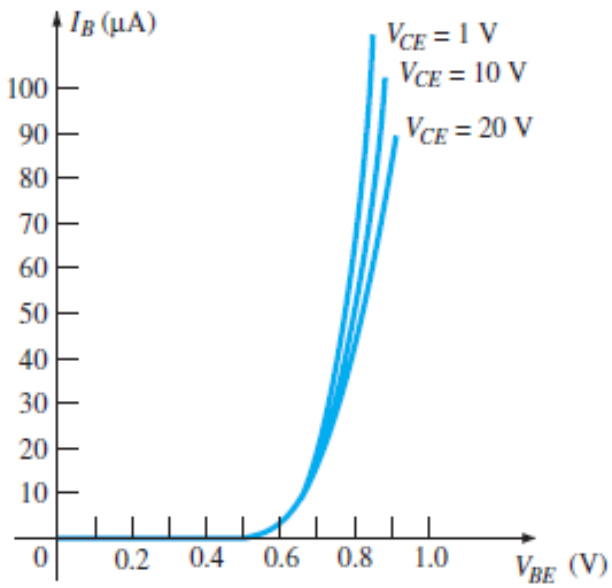
- The output resistance r_o is the ratio of change in collector emitter voltage $\$\Delta V_{CE}\$$ to the change in collector current $\$\Delta I_C\$$ at constant I_B.

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \text{ at constant } I_B$$

IDEAL CE INPUT Characteristics



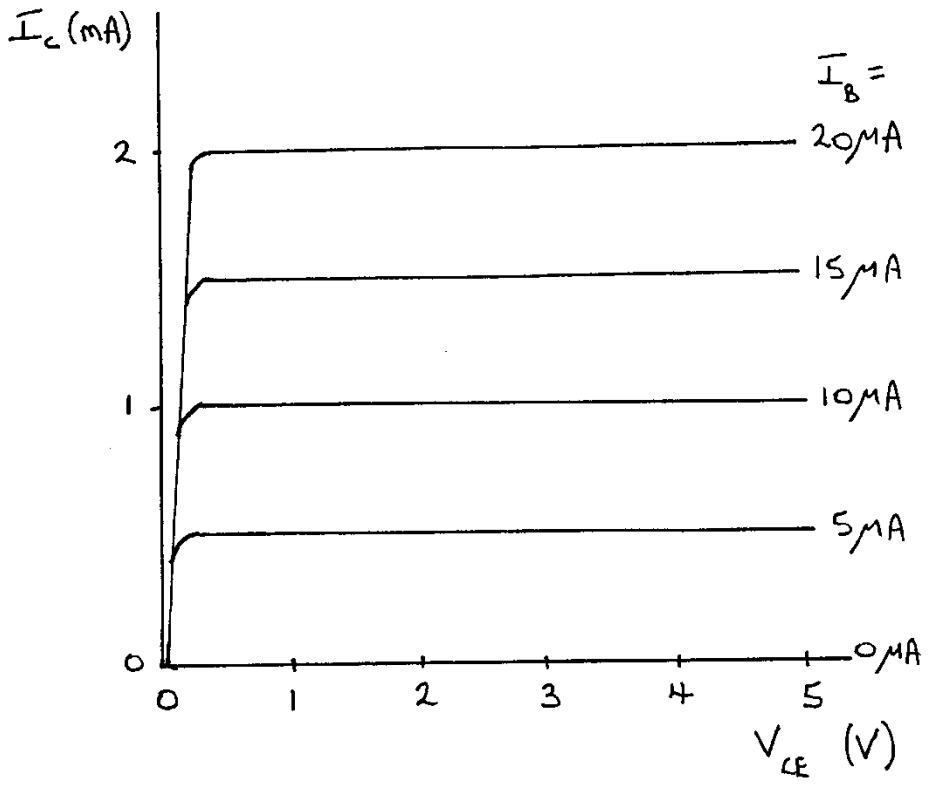
INPUT (BASE) CHARACTERISTIC



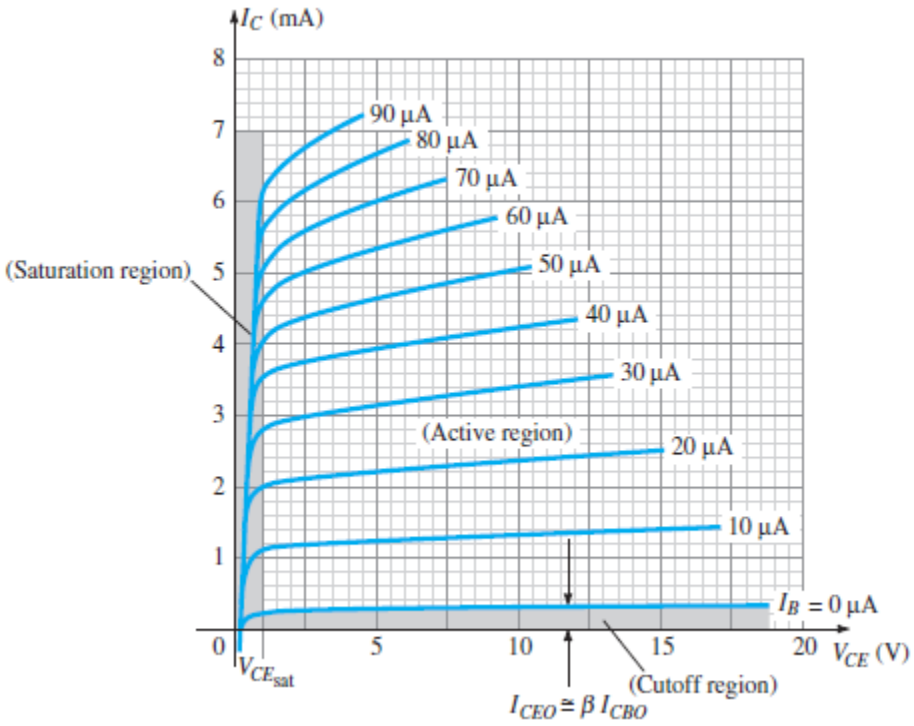
IDEAL CE INPUT Characteristics

- The plot is essentially that of a forward biased diode.
- We can thus assume $V_{BE} \approx 0.6\ V$ when designing our d.c. bias circuits.
- We can also assume everything we know about incremental diode resistance when deriving our a.c. equivalent circuit.
- In the 'non-ideal' case I_B will vary slightly with V_{CE}. This need not concern us.

IDEAL CE OUTPUT Characteristics

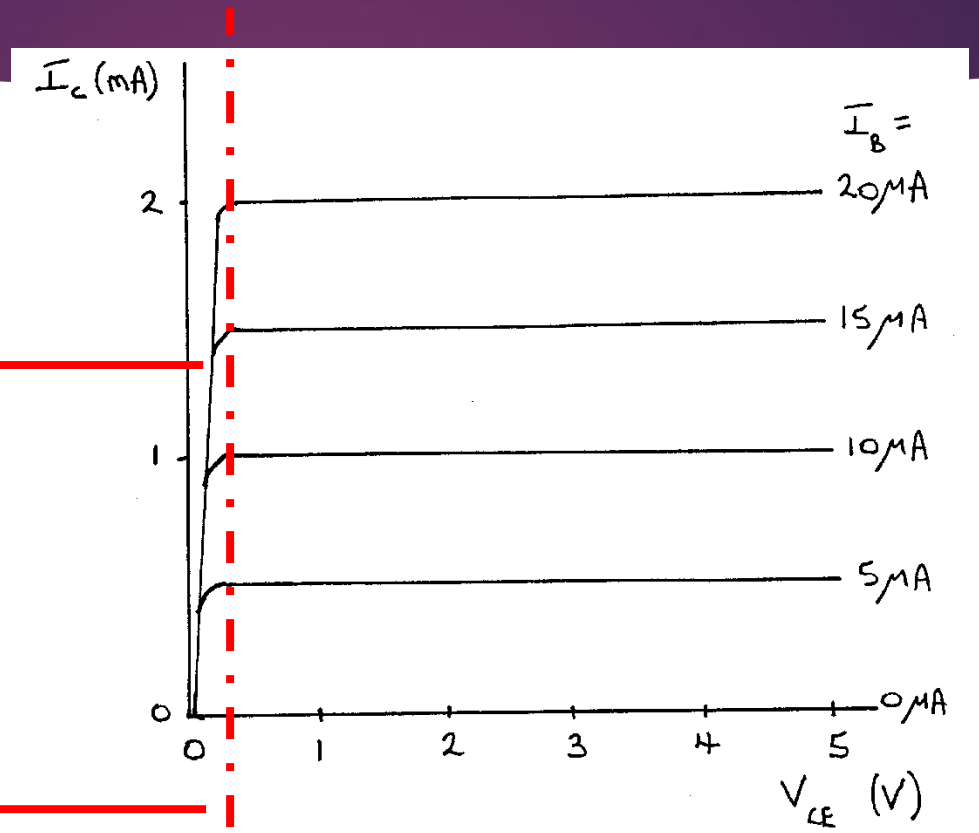


OUTPUT (COLLECTOR) CHARACTERISTIC



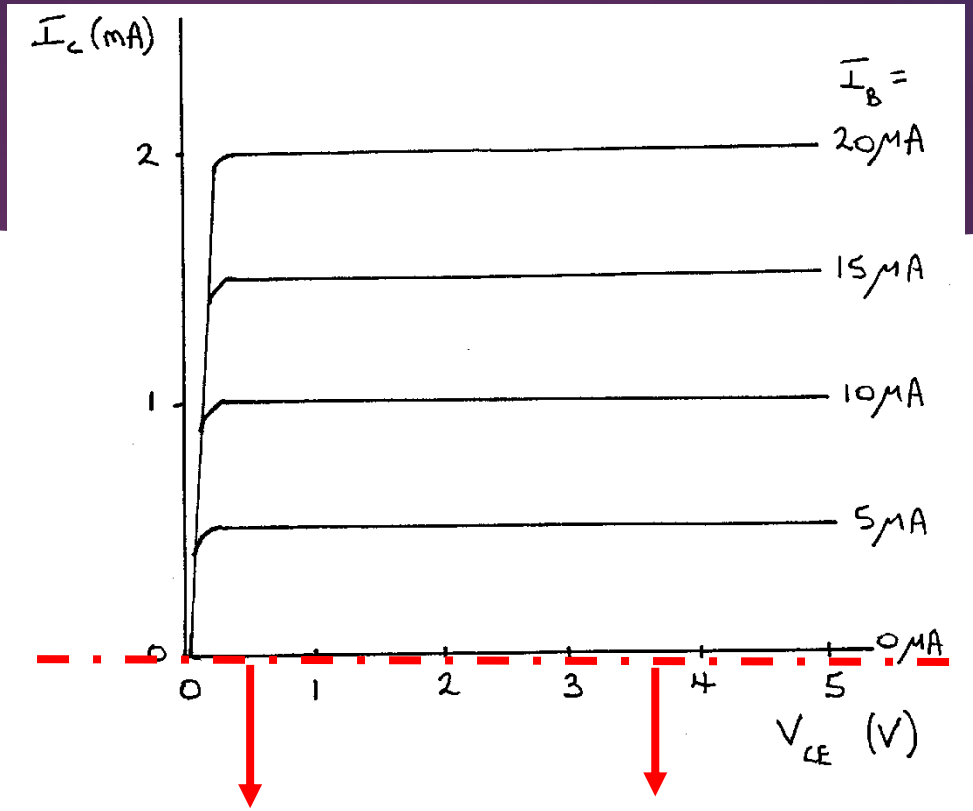
IDEAL CE OUTPUT (Collector) Characteristics

Avoid this saturation region where we try to forward bias both junctions



OUTPUT (COLLECTOR) CHARACTERISTIC

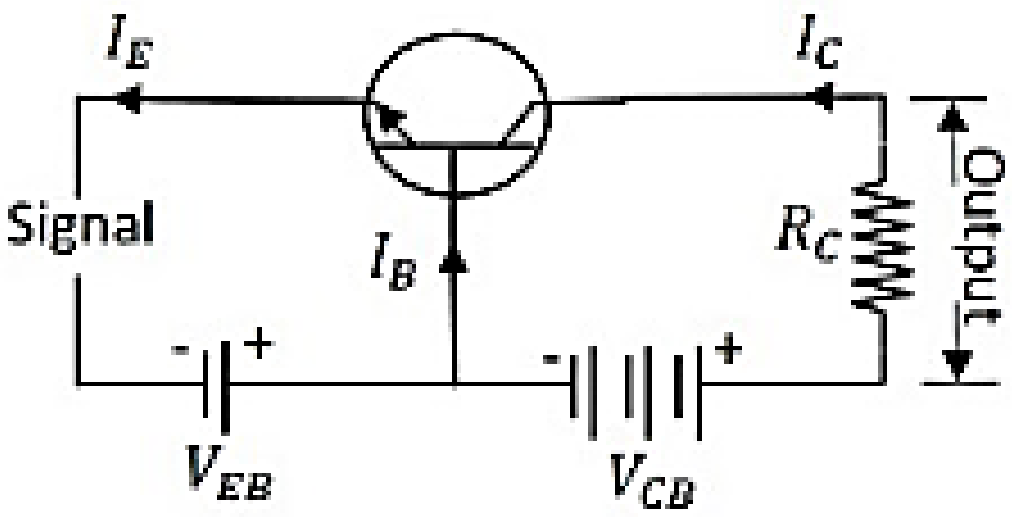
IDEAL CE OUTPUT



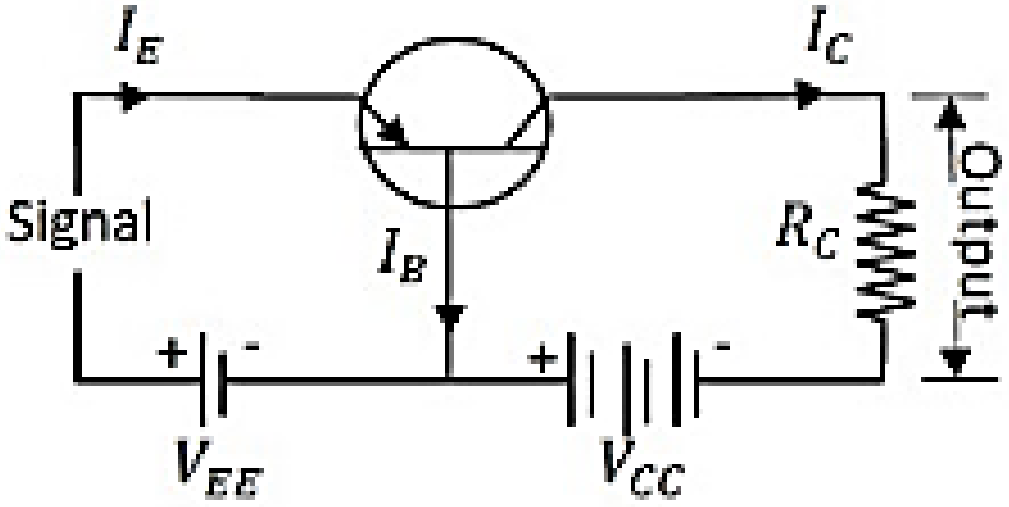
Avoid this cut-off region where we try to reverse bias both junctions (I_C approximately 0)

Common Base Configuration

Common Base Connection



Using NPN transistor



Using PNP transistor

Characteristics of CB configuration

- This configuration **provides voltage gain but no current gain.**
- Being V_{CB} constant, with a small increase in the Emitter-base voltage V_{EB}, Emitter current I_E gets increased.
- Emitter Current I_E is independent of Collector voltage V_{CB}.
- Collector Voltage V_{CB} can affect the collector current I_C only at low voltages when V_{EB} is kept constant.
- As the output resistance is of very high value, a large change in V_{CB} produces very little change in the collector current I_C.
- This Configuration provides good stability against the increase in temperature.
- The CB configuration is used for high-frequency applications.

- *As the input resistance is of very low value, a small value of V_{EB} is enough to produce a large current flow of emitter current I_E.*

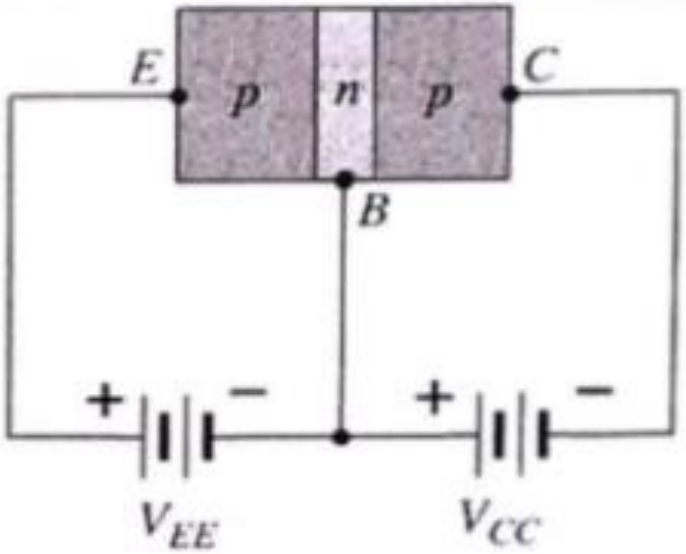
The input resistance ri is the ratio of change in emitter-base voltage $\$\Delta V_{EB}\$$ to the change in emitter current $\$\Delta I_E\$$ at constant collector base voltage V_{CB}.

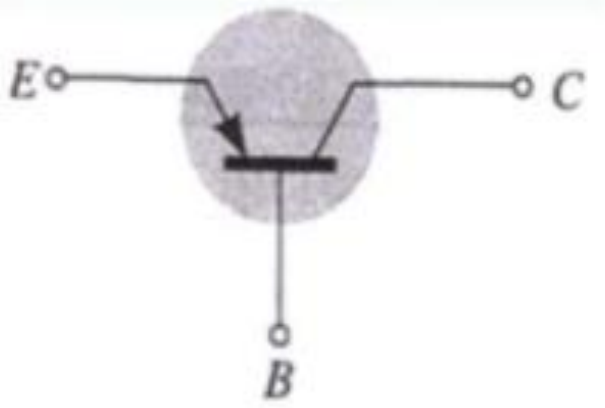
$$r_i = \frac{\Delta V_{EB}}{\Delta I_E} \text{ at constant } V_{CB}$$

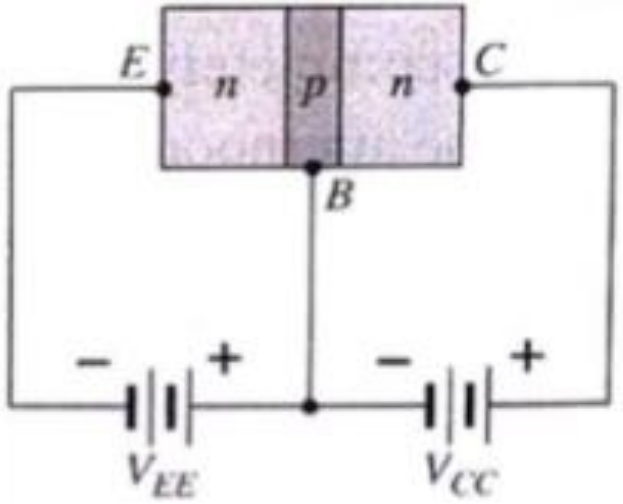
The output resistance r_o is the ratio of change in the collector base voltage $\$\Delta V_{CB}\$$ to the change in collector current $\$\Delta I_C\$$ at constant emitter current I_E.

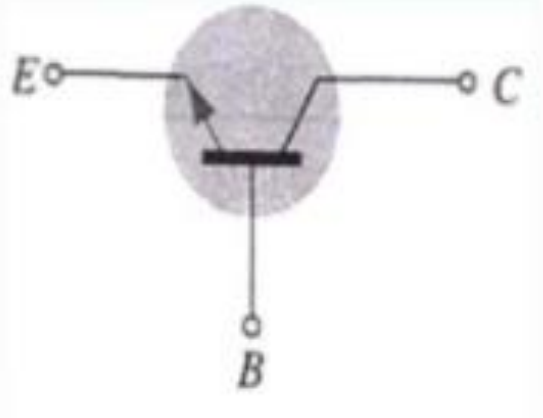
$$r_o = \frac{\Delta V_{CB}}{\Delta I_C} \text{ at constant } I_E$$

Common-Base Configuration

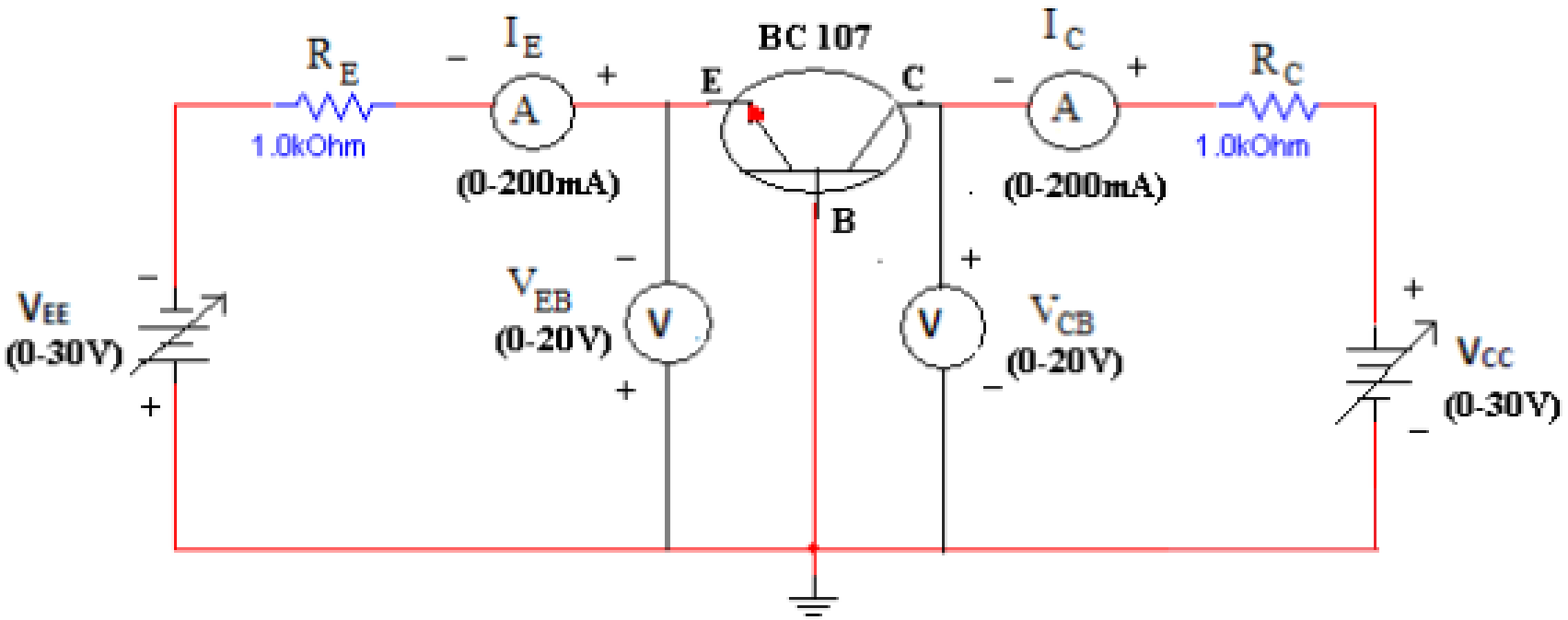








CB Circuit diagram



Common-Base Configuration

- The common-base configuration with *pnp* and *npn transistors are shown in the figures in the previous slide..*
- The term *common-base is derived from the* fact that the base is common to both the input and output sides of the configuration.
- The arrow in the symbol defines the direction of emitter current through the device.
- The applied biasing are such as to establish current in the direction indicated for each branch.
- That is, direction of I_E *is the same as the* polarity of V_{EE} *and* I_C *to* V_{CC}.
- Also, the equation $I_E = I_C + I_B$ *still holds.*

Input characteristics

The *driving point or input parameters are* shown in the figure.

An input current (I_E) *is a function of an* input voltage (V_{BE}) *for various of output* voltage (V_{CB}).

This closely resembles the characteristics of a diode.

In the dc mode, the levels of I_C *and* I_E *at the* operation point are related by:

$$\alpha_{dc} = I_C / I_E$$

Normally, $\alpha \cong 1$.

For practical devices, α is typically from 0.9 to 0.998.

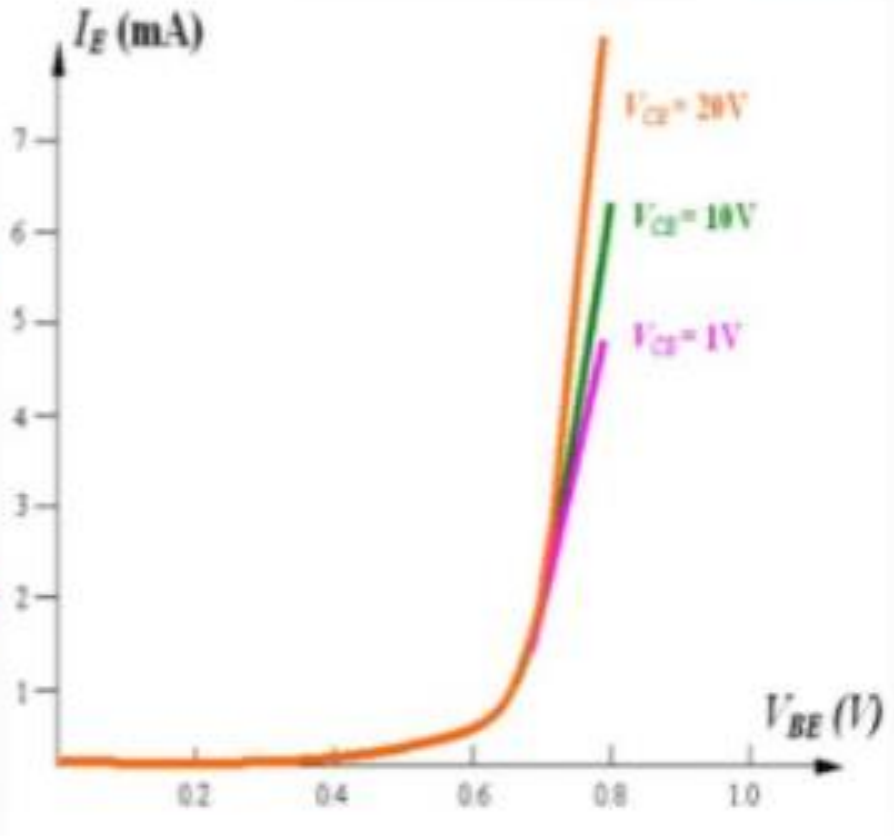
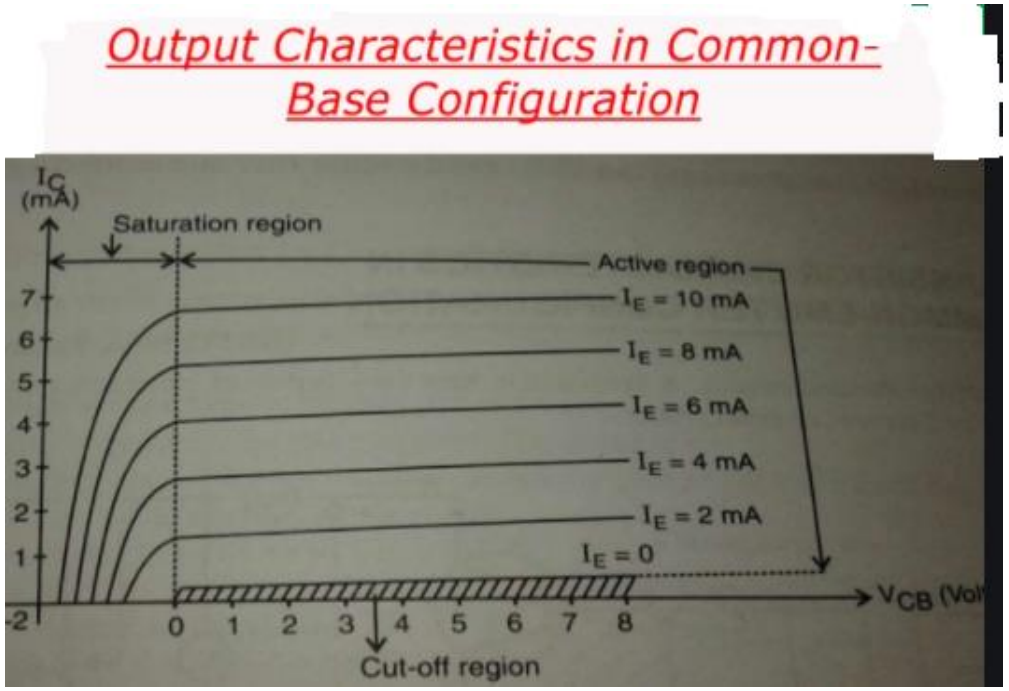


Figure: Input characteristics for common-base transistor

Input characteristics contd..

- As an approximation, the change due to changes in V_{CB} *can be ignored.*
- The characteristics can be shown in orange curve.
- If piecewise-linear approach is applied, the magenta green curve is obtain.
- Furthermore, ignoring the slop of the curve and the resistance results the magenta curve.
- It is this magenta curve that is used in the dc analysis of transistors.
- Once a transistor is in "on" state, the *B-E* voltage is assumed to be 0.7V.
- And the emitter current may be at any level as controlled by the external network.

Output characteristics of CB Transistor



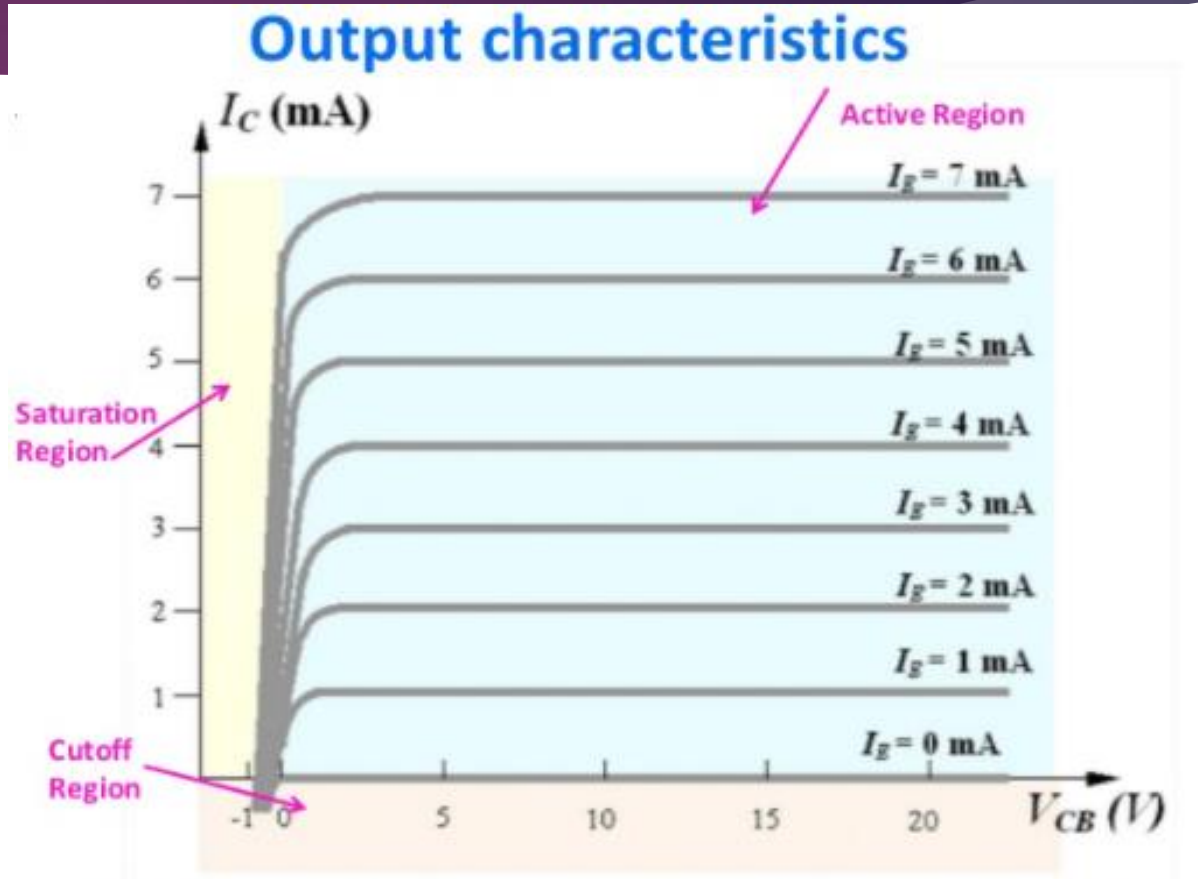


Figure: Output characteristics for common-base transistor

Output characteristics

- The output set relates an output current (I_C) to an output voltage (V_{CB}) *for various of* level of input current (I_E).

  There are three regions of interest:

Active region

- In the active region, the *b-e junction is* forward-biased, whereas the *c-b junction* is reverse-biased.
- The active region is the region normally employed for linear amplifier.

Also, in this region,

$$I_C \cong I_E$$

Cutoff region

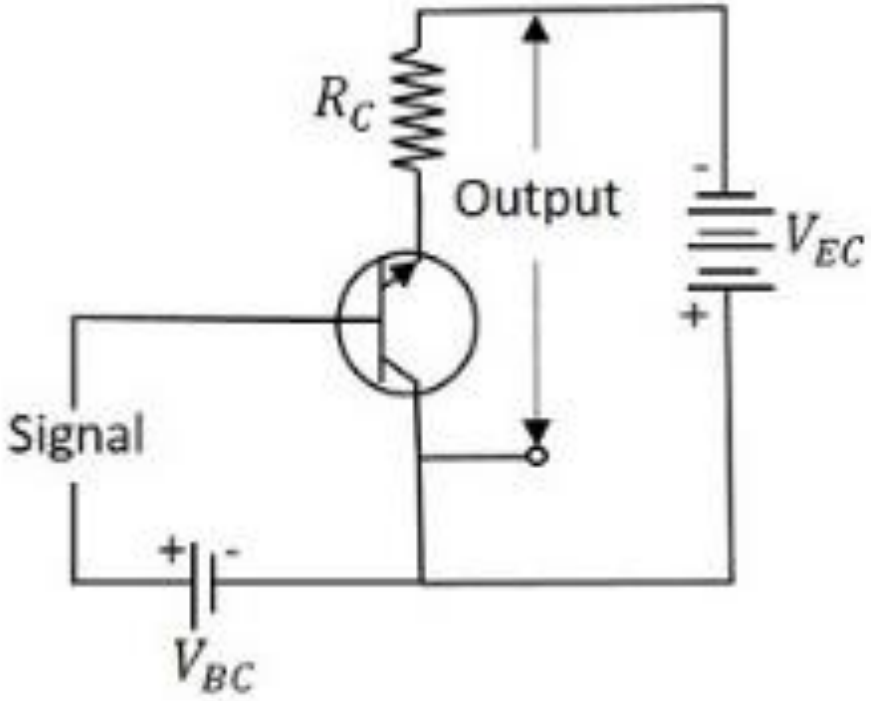
- The cutoff region is defined as that region where the collector current is 0A.
- In the cutoff region, the *B-E and C-B junctions* of a transistor are both reverse-biased.

Saturation region:

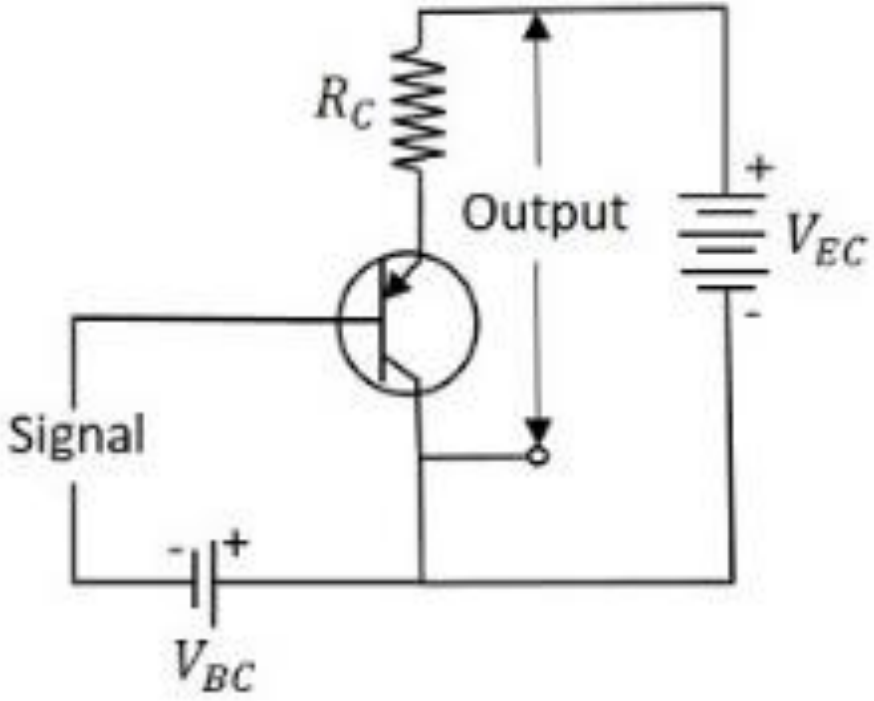
- It is defined as that region of the characteristics to the left of $V_{CB} = 0\ V$.
- In saturation region, the *B-E and C-B* junctions of a transistor are both forward biased.

Common Collector Configuration

Common Collector Connection



Using NPN transistor



Using PNP transistor

Common-Collector Configuration

- The common-collector configuration with *npn and pnp transistors are shown in the* figures.

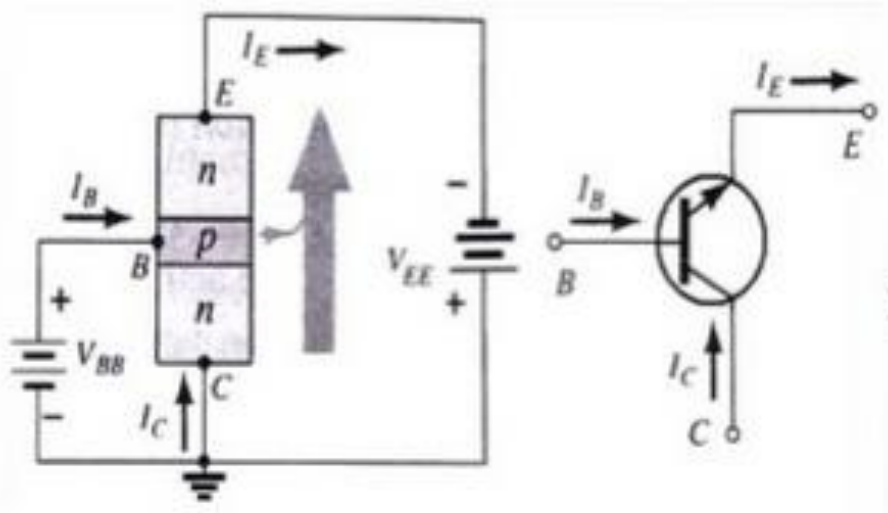


Figure: Common-collector configuration of *npn transistor*

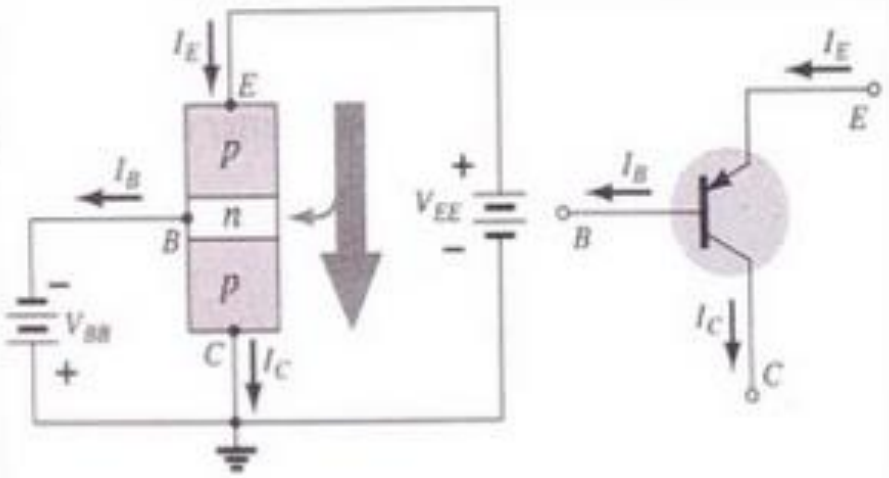


Figure: Common- collector configuration of *pnp transistor*

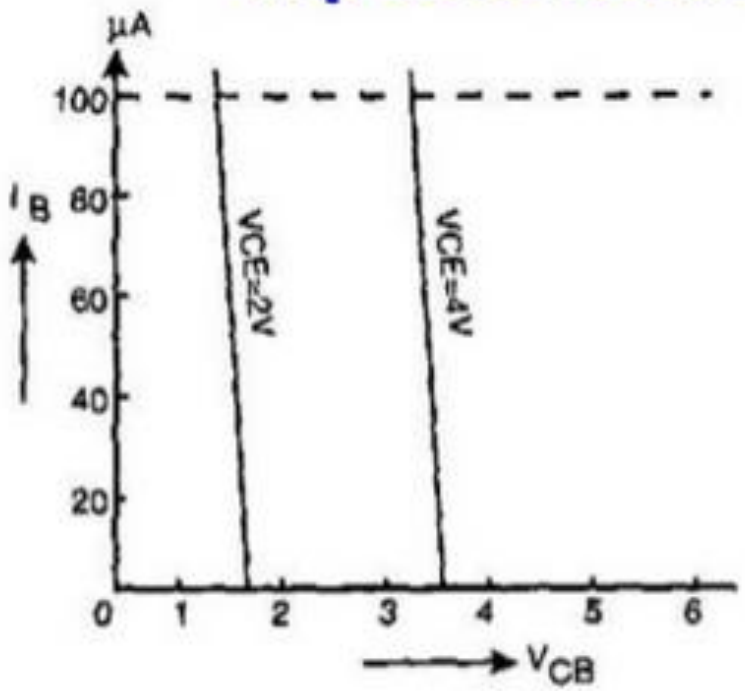
Common-Collector Configuration

- It is used primarily for impedance-matching purpose since it has a high input impedance and low output impedance.
- The load resistor can be connected from emitter to ground.
- The collector is tied to ground and the circuit resembles common-emitter circuit.
- The output set relates an output current (I_E) to an output voltage (V_{CE}) *for various of* level of input current (I_B).

Input characteristics

- It is a curve which shows the relationship between the base current, I_B and the collector base voltage V_{CB} at constant V_{CE} This method of determining the characteristic is as follows.
- First, a suitable voltage is applied between the emitter and the collector.
- Next the input voltage V_{CB} is increased in a number of steps and corresponding values of I_E are noted.
- The base current is taken on the y-axis, and the input voltage is taken on the x-axis. Fig. shows the family of the input characteristic at different collector- emitter voltages.

Input characteristics



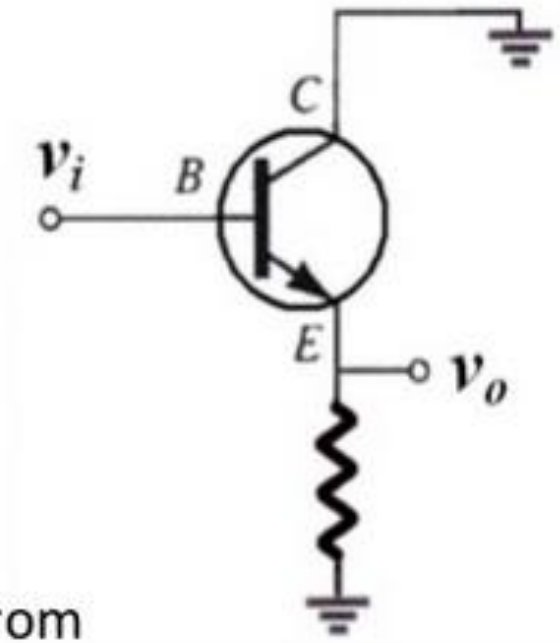


Figure: Common-collector circuit used for impedance-matching purpose

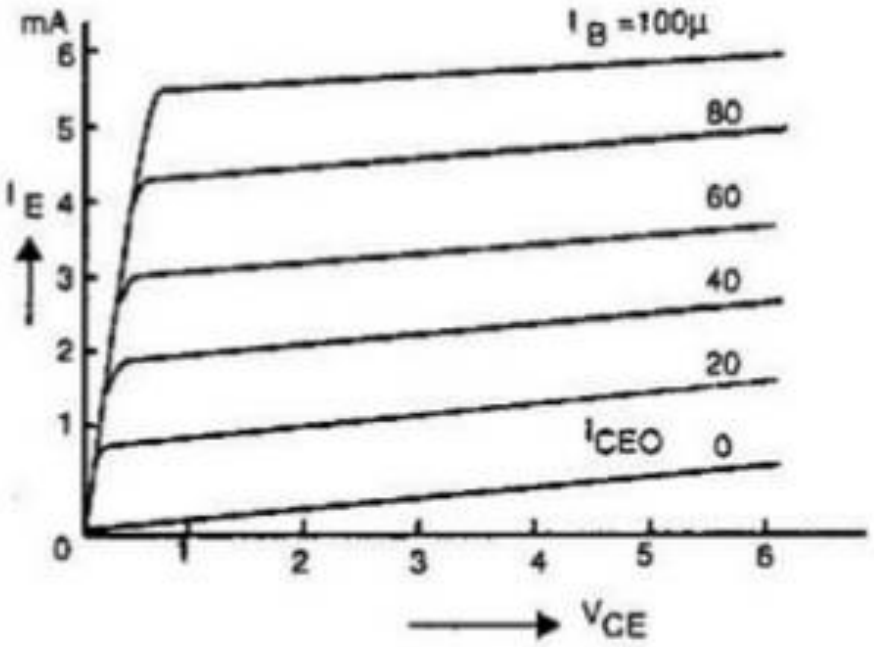
- The following points may be noted from the family of characteristic curves.
- Its characteristic is quite different from those of common base and common emitter circuits.
- When V_{CB} increases, IB is decreased.

Output characteristics

- This is almost the same as the output characteristics of common-emitter circuit, which are the relations between I_C *and* V_{CE} for various of level of input current I_B.

Since that: $I_E \cong I_C$.

Figure: Output characteristics for common-collector transistor



APPLICATION

- It is useful as an impedance matching device since its input impedance is much higher than its output impedance. It is also termed a “buffer" for this reason and is used in digital circuits with basic gates.
- When the voltage divider used but it is a poor voltage source because it is so strongly affected by the value of the load resistor. The same voltage divider with the transistor buffer will supply power to keep the voltage constant over its range of operation.
- It is also used for cascade amplifier.

Amplification factor in common collector CC configuration. It is denoted by γ.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

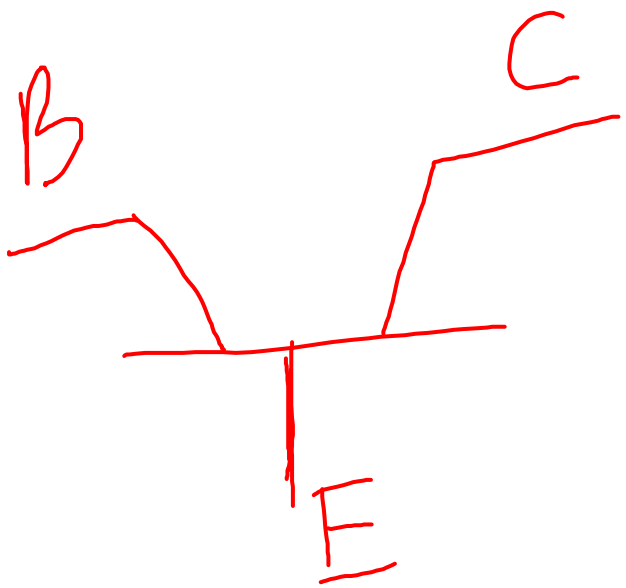
- The current gain in CC configuration is same as in CE configuration.
- The voltage gain in CC configuration is always less than 1.

Characteristics of CC Configuration

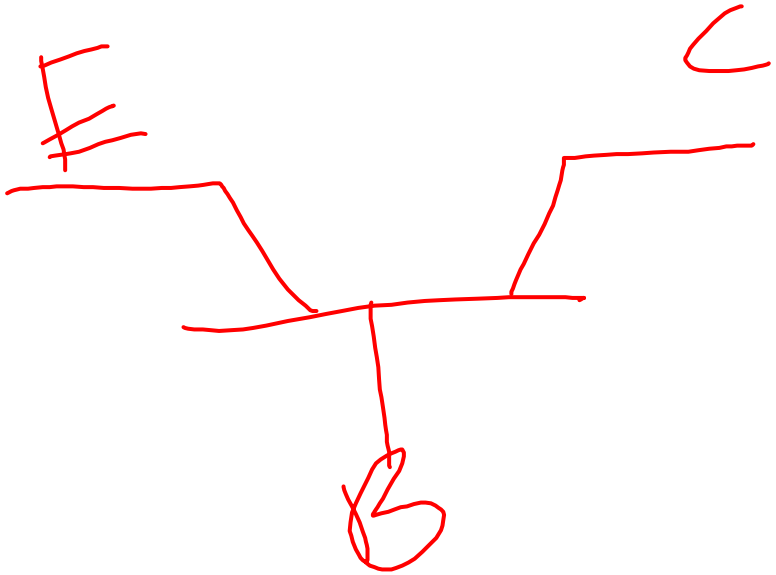
- **This configuration provides current gain but no voltage gain**.
- In CC configuration, the input resistance is high and the output resistance is low.
- The voltage gain provided by this circuit is less than 1.
- The sum of collector current and base current equals emitter current.
- The input and output signals are in phase.
- This configuration works as non-inverting amplifier output.
- This circuit is mostly used for impedance matching. That means, to drive a low impedance load from a high impedance source.

COMPARISON OF CE,CC and CB

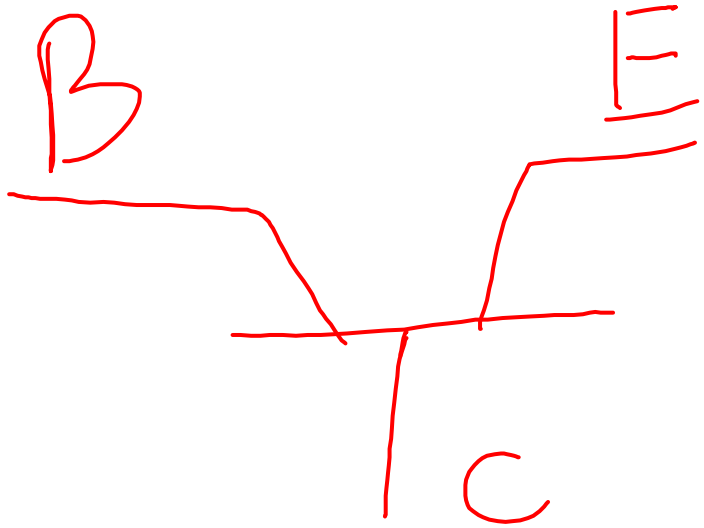
Characteristic	Common base (CB)	Common emitter,(CE)	Common collector,(CC)
Input Dynamic Resistance	Very Low(less than 100 ohm)	Low(less than 1K)	Very High(750K)
Output Dynamic Resistance	Very High	High	Low
Current Gain	Less than 1	High	Very High
Voltage gain	Greater than CC but less than CE	Highest	Lowest(less than 1)
Power gain	Medium	Highest	Medium
Leakage current	Very small	Very large	Very large
Relationship between I/p and o/p	In phase	Out of phase(180^0)	In phase
Application	For High freq. applications	For Audio freq. Applications	For impedance Matching Applications



CE

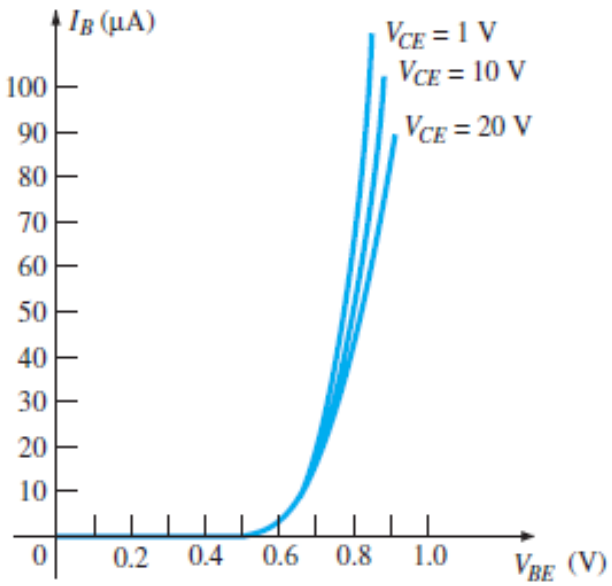


CB

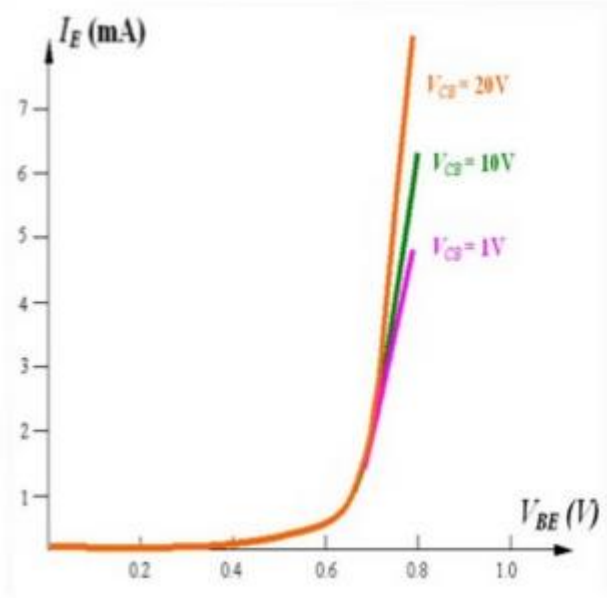


CC

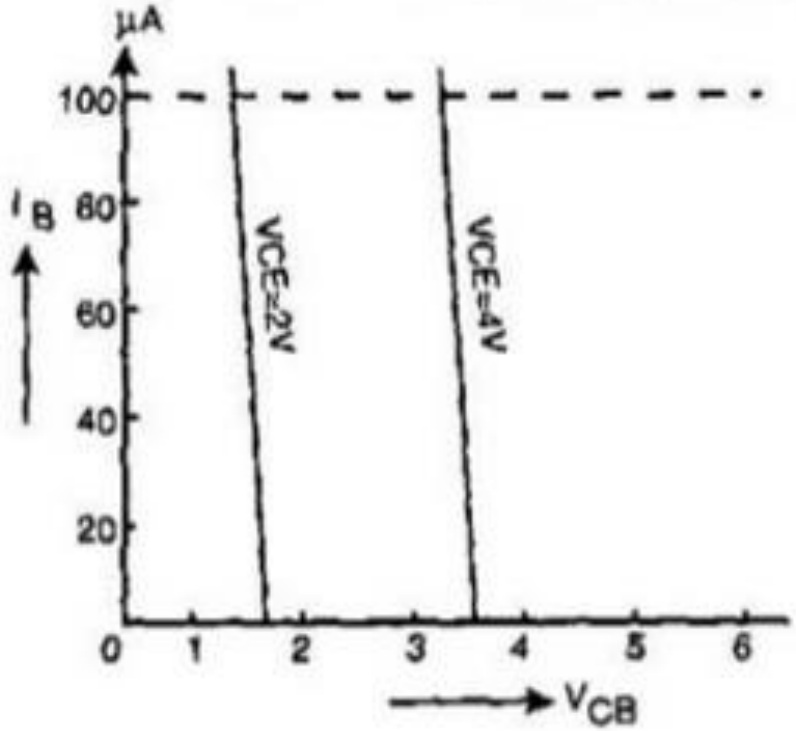
Comparison of input characteristics of CE, CC and CB



CE

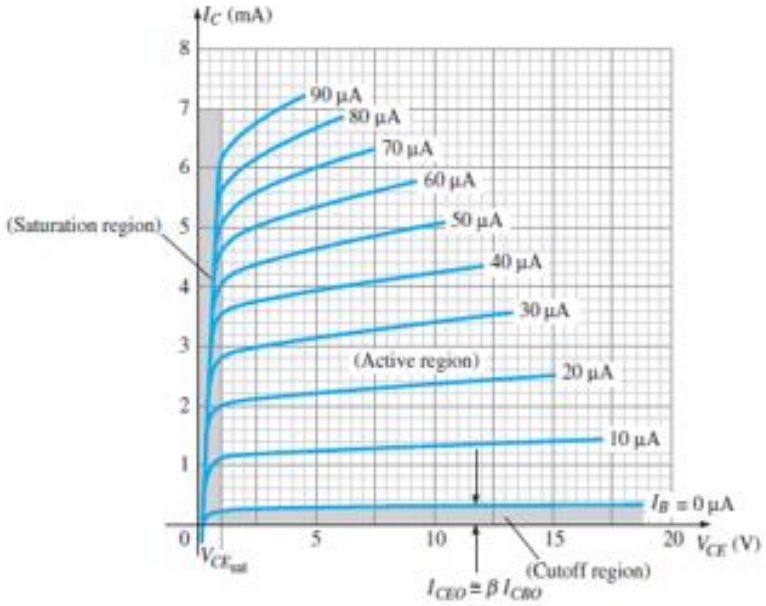


CB

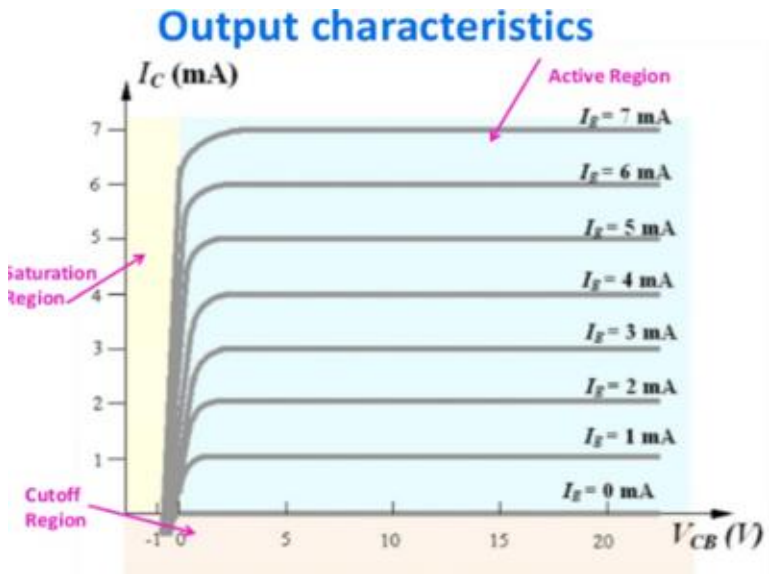


CC

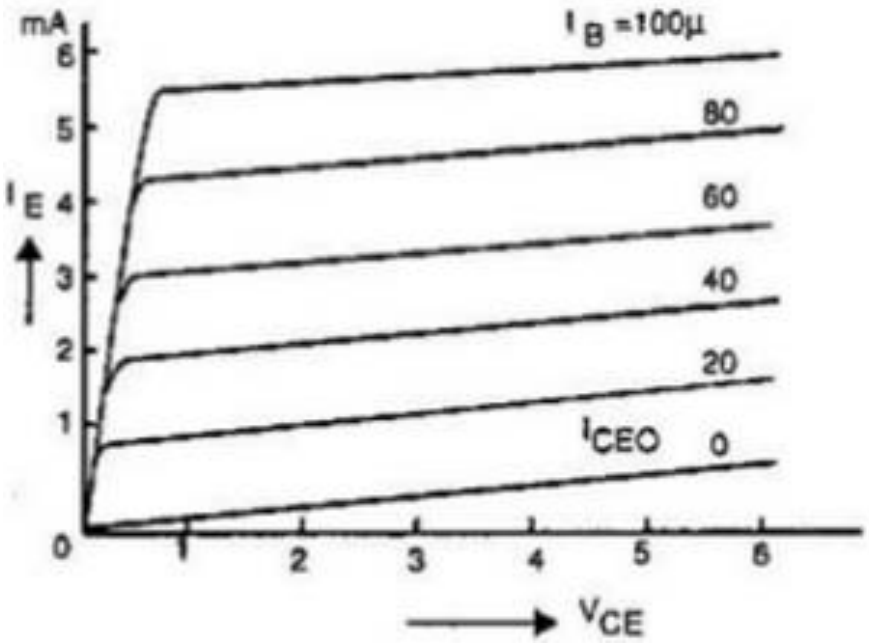
Comparison of OUTPUT characteristics of CE, CC and CB



CE



CB



CC

Current Amplification Factor

In a transistor amplifier with AC input signal, the ratio of change in output current to the change in input current is known as the current amplification factor.

In the CB configuration the current amplification factor, $\alpha = \dfrac{\Delta I_C}{\Delta I_E}$

In the CE configuration the current amplification factor, $\beta = \dfrac{\Delta I_C}{\Delta I_B}$

In the CC configuration the current amplification factor, $\gamma = \dfrac{\Delta I_E}{\Delta I_B}$

Relationship between α and β We know that $\Delta I_E = \Delta I_C + \Delta I_B$

By definition, $\Delta I_C = \alpha \Delta I_E$

Therefore, $\Delta I_E = \alpha \Delta I_E + \Delta I_B$

sub. ② in ①

i.e., $\Delta I_B = \Delta I_E (1 - \alpha)$

Dividing both sides by ΔI_C, we get

$$\frac{\Delta I_B}{\Delta I_C} = \frac{\Delta I_E}{\Delta I_C}(1 - \alpha)$$

Therefore,

$$\frac{1}{\beta} = \frac{1}{\alpha}(1 - \alpha)$$

$$\beta = \frac{\alpha}{(1 - \alpha)}$$

Rearranging, we also get $\alpha = \dfrac{\beta}{(1 + \beta)}$, or $\dfrac{1}{\alpha} - \dfrac{1}{\beta} = 1$

From this relationship, it is clear that as α approaches unity, β approaches infinity. The CE configuration is used for almost all transistor applications because of its high current gain, β.

Relation among α, β and γ In the CC transistor amplifier circuit, I_B is the input current and I_E is the output current.

From Eq. (2.22),

$$\boxed{\gamma = \frac{\Delta I_E}{\Delta I_B}}$$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

Substituting $\Delta I_B = \Delta I_E - \Delta I_C$, we get

$$\Delta I_B = \Delta I_E - \Delta I_C$$

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

$$\gamma = \frac{\Delta I_E}{\Delta I_E - \Delta I_C}$$

Dividing the numerator and denominator on RHS by ΔI_E, we get

$$\gamma = \frac{\dfrac{\Delta I_E}{\Delta I_E}}{\dfrac{\Delta I_E}{\Delta I_E} - \dfrac{\Delta I_C}{\Delta I_E}} = \frac{1}{1-\alpha}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

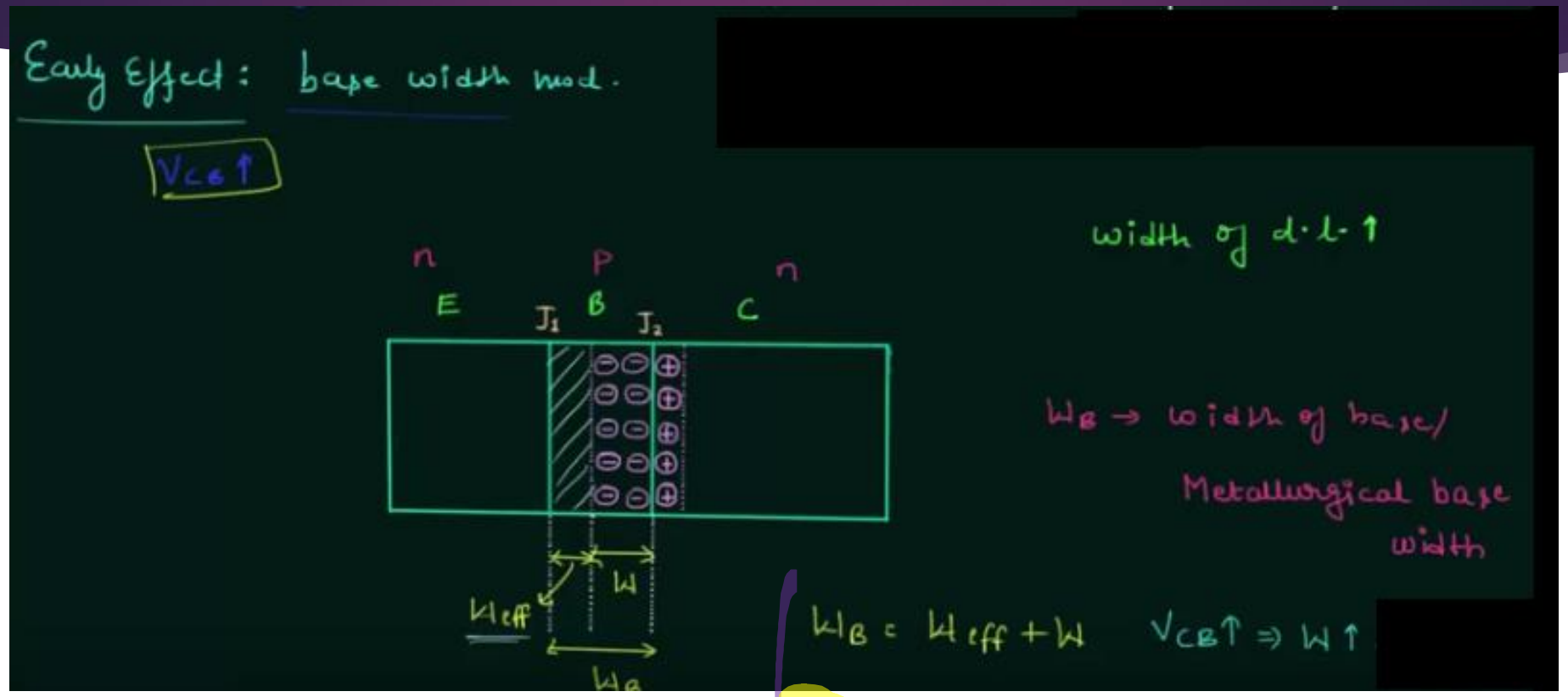
Therefore,

$$\gamma = \frac{1}{1-\alpha} = (\beta + 1)$$

$$\gamma = \frac{1}{1-\left(\frac{\beta}{1+\beta}\right)}$$

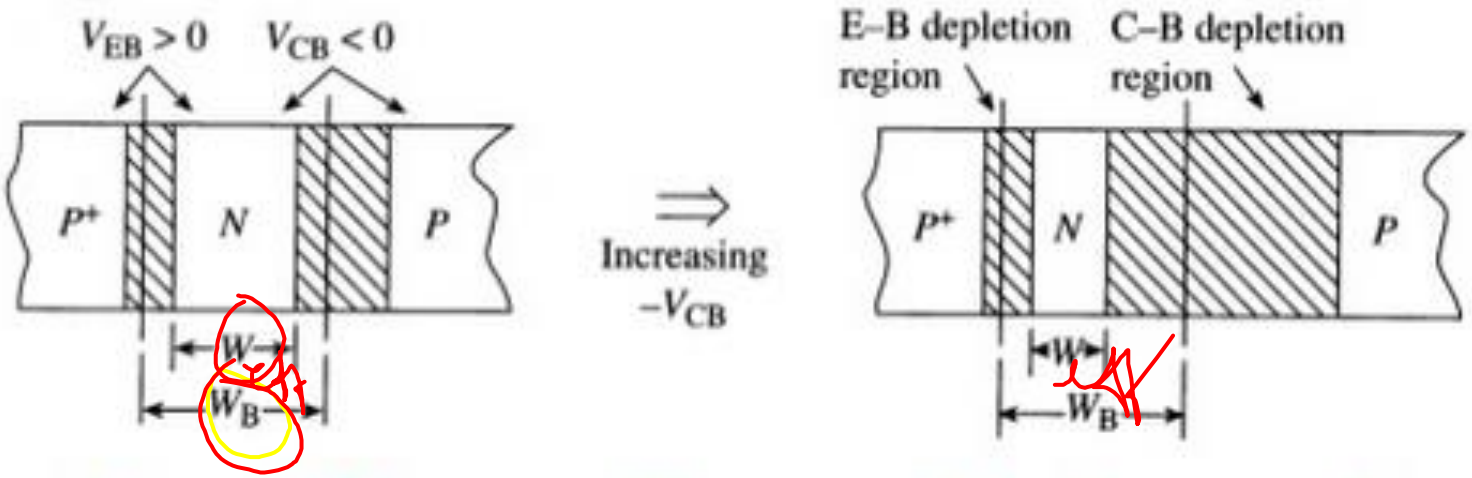
$$\gamma = \frac{1+\beta}{1+\cancel{\beta}-\cancel{\beta}} \Rightarrow \boxed{\gamma = 1+\beta}$$

Early effect in CB Configuration



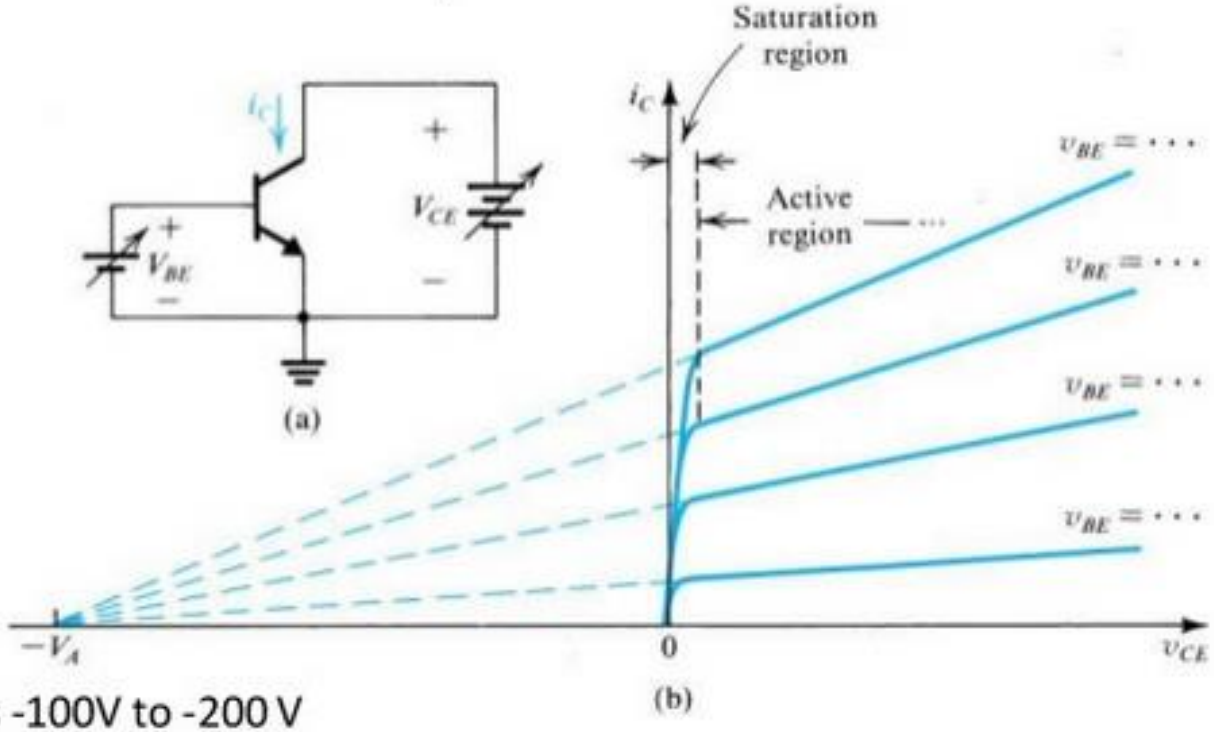
Base Width Modulation: "Early" Effect

- When bias voltages change, depletion widths change and the effective base width will be a function of the bias voltages
- Most of the effect comes from the C-B junction since the bias on the collector is usually larger than that on the E-B junction



Base width gets smaller as applied voltages get larger

The Early Effect



Range is -100V to -200 V

Converge ~ at single point called "Early Voltage" (after James Early)

Large "Early Voltage" = Absence of "Base Width Modulation"

Early effect or base-width modulation

As the collector voltage V_{CC} is made to increase the reverse bias, the space charge width between collector and base tends to increase, with the result that the effective width of the base decreases. This dependency of base-width on collector-to-emitter voltage is known as the *Early effect*. This decrease in effective base-width has three consequences:

(i) There is less chance for recombination within the base region. Hence, α increases with increasing $|V_{CB}|$.

(ii) The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

(iii) For extremely large voltages, the effective base-width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the *punch through*.

For higher values of V_{CB}, due to Early effect, the value of α increases. For example, α changes, say from 0.98 to 0.985. Hence, there is a very small positive slope in the CB output characteristics and hence the output resistance is not zero.

Transistor parameters

The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as common base *hybrid parameters* or *h-parameters*.

(a) Input impedance (h_{ib}) It is defined as the ratio of the change in (input) emitter voltage to the change in (input) emitter current with the (output) collector voltage V_{CB} kept constant. Therefore,

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E}, \; V_{CB} \text{ constant}$$

It is the slope of CB input characteristics I_E versus V_{EB} The typical value of h_{ib} ranges from 20 Ω to 50 Ω.

(b) Output admittance (h_{ob}) It is defined as the ratio of change in the (output) collector current to the corresponding change in the (output) collector voltage with the (input) emitter current I_E kept constant. Therefore,

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}}, \; I_E \text{ constant}$$

It is the slope of CB output characteristics I_C versus V_{CB} The typical value of this parameter is of the order of 0.1 to 10 μ mhos.

(c) Forward current gain (h_{fb}) It is defined as a ratio of the change in the (output) collector current to the corresponding change in the (input) emitter current keeping the (output) collector voltage V_{CB} constant. Hence,

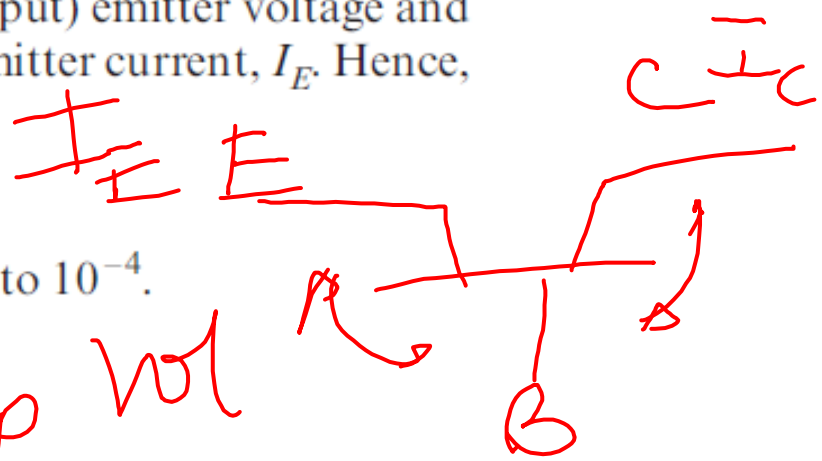
$$h_{fb} = \frac{\Delta I_C}{\Delta I_E}, V_{CB} \text{ constant.}$$

It is the slope of I_C versus I_E curve. Its typical value varies from 0.9 to 1.0.

(d) Reverse voltage gain (h_{rb}) It is defined as the ratio of the change in the (input) emitter voltage and the corresponding change in (output) collector voltage with constant (input) emitter current, I_E. Hence,

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}}, I_E \text{ constant}$$

It is the slope of V_{EB} versus V_{CB} curve. Its typical value is of the order of 10^{-5} to 10^{-4}.



Rev vol Gain $= \left(\frac{\text{o/p vol}}{\text{i/p vol}}\right)^{-1} = \frac{\text{i/p vol}}{\text{o/p vol}} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \Big/ I_E \text{ const}$

Current Equations

Large-signal current gain (α) The large signal current gain of a common base transistor is defined as the ratio of the negative of the collector-current increment to the emitter-current change from cut-off ($I_E = 0$) to I_E, i.e.,

$$\alpha = -\frac{(I_C - I_{CBO})}{I_E - 0}$$

where I_{CBO} (or I_{CO}) is the reverse saturation current flowing through the reverse biased collector-base junction, i.e., the collector to base leakage current with emitter open. As the magnitude of I_{CBO} is negligible when compared to I_E, the above expression can be written as

$$\alpha = -\frac{I_C}{I_E}$$

α +ve

Since I_C and I_E are flowing in opposite directions, α is always positive. Typical value of α ranges from 0.90 to 0.995. Also, α is not a constant but varies with emitter current I_E, collector voltage V_{CB} and temperature.

General transistor equation In the active region of the transistor, the emitter is forward biased and the collector is reverse biased. The generalised expression for collector current I_C for collector junction voltage V_C and emitter current I_E is given by

$$I_C = -\alpha I_E + I_{CBO}(1 - e^{V_C/V_T})$$

If V_C is negative and $|V_c|$ is very large compared with V_T, then the above equation reduces to

$$I_C = -\alpha I_E + I_{CBO}$$

If V_C, i.e., V_{CB}, is few volts, I_C is independent of V_C. Hence the collector current I_C is determined only by the fraction α of the current I_E flowing in the emitter.

Relation among I_C, I_B and I_{CBO} From Eq. (2.5), we have

$$I_C = -\alpha I_E + I_{CBO}$$

Since I_C and I_E are flowing in opposite directions,

$$I_E = -(I_C + I_B)$$

Therefore,

$$I_C = -\alpha[-(I_C + I_B)] + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{I_{CBO}}{1-\alpha}$$

Since

$$\beta = \frac{\alpha}{1-\alpha},$$

the above expression becomes

$$I_C = (1+\beta) I_{CBO} + \beta I_B$$

Relation among I_C, I_B and I_{CEO} In the common-emitter (CE) transistor circuit, I_B is the input current and I_C is the output current. If the base circuit is open, i.e., $I_B = 0$, then a small collector current flows from the collector to emitter. This is denoted as I_{CEO}, the collector-emitter current with base open. This current I_{CEO} is also called the collector to emitter leakage current.

In this CE configuration of the transistor, the emitter-base junction is forward-biased and collector-base junction is reverse-biased and hence the collector current I_C is the sum of the part of the emitter current I_E that reaches the collector, and the collector-emitter leakage current I_{CEO}. Therefore, the part of I_E, which reaches collector is equal to $(I_C - I_{CEO})$.

Hence, the *large-signal current gain* (β) is defined as,

$$\beta = \frac{(I_C - I_{CEO})}{I_B}$$

From the equation, we have

$$I_C = \beta I_B + I_{CEO}$$

Relation between I_{CBO} and I_{CEO}

Comparing Eqs we get the relationship between the leakage currents of transistor common-base (CB) and common-emitter (CE) configurations as

$$I_{CEO} = (1 + \beta)\, I_{CBO}$$

From this equation, it is evident that the collector-emitter leakage current (I_{CEO}) in CE configuration is $(1 + \beta)$ times larger than that in CB configuration. As I_{CBO} is temperature-dependent, I_{CEO} varies by large amount when temperature of the junction changes.

Expression for emitter current The magnitude of emitter-current is

$$I_E = I_C + I_B$$

$$I_E = (1 + \beta)\, I_{CBO} + (1 + \beta)\, I_B$$

$$I_E = \frac{1}{1 - \alpha} I_{CBO} + \frac{1}{1 - \alpha} I_B$$

DC current gain (β_{DC} or h_{FE}) The DC current gain is defined as the ratio of the collector current I_C to the base current I_B. That is,

$$\beta_{DC} = h_{FE} = \frac{I_C}{I_B}$$

As I_C is large compared with I_{CEO}, the large signal current gain (β) and the DC current gain (h_{FE}) are approximately equal.

h -PARAMETER MODEL

A transistor can be treated as a two-port network. The terminal behaviour of any two-port network can be specified by the terminal voltages V_1 and V_2 at ports 1 and 2, respectively, and currents I_1 and I_2, entering ports 1 and 2, respectively, as shown in Fig. Of these four variables, V_1, V_2, I_1 and I_2, two can be selected as independent variables and the remaining two can be expressed in terms of these independent variables. This leads to various two-port parameters out of which the following are very important.

(i) *h*-parameters or *hybrid parameters*

(ii) *Z*-parameters or *impedance parameters*

(iii) *Y*-parameters or *admittance parameters*

Fig. *Two-port network*

The h-parameter representation is widely utilised in modelling of transistors. Hence, both short-circuit and open-circuit terminal conditions are used. If the input current I_1 and the output voltage V_2 are taken as independent variables, the input voltage V_1 and output current I_2 can be written as

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$V_1 = h_{11} I_1 + h_{12} V_2 \longrightarrow (1)$$

$$I_2 = h_{21} I_1 + h_{22} V_2 \longrightarrow (2)$$

The four hybrid parameters h_{11}, h_{12}, h_{21} and h_{22} are defined as follows:

When $V_1 = 0$, i.e., with output port short-circuited,

$V_2 = 0$

put $V_2 = 0$ in (1)

$V_1 = h_{11} I_1 + 0$

h_{11}, h

$$h_{11} = \left[\frac{V_1}{I_1}\right] \text{ with } V_2 = 0$$

$$= \text{input impedance}$$

and

$$h_{21} = \left[\frac{I_2}{I_1}\right] \text{ with } V_2 = 0$$

$$= \text{forward current gain or forward transfer ratio}$$

put $V_2 = 0$ in (2)

$I_2 = h_{21} I_1 + 0$

When $I_1 = 0$, i.e., with input port open-circuited,

put $I_1 = 0$ in eqn (2)

$$h_{22} = \left[\frac{I_2}{V_2}\right] \text{ with } I_1 = 0$$

$$= \text{output admittance}$$

$I_2 = h_{22} V_2$

and

$$h_{12} = \left[\frac{V_1}{V_2}\right] \text{ with } I_1 = 0$$

$$= \text{reverse voltage gain or reverse transfer ratio}$$

put $I_1 = 0$ in eqn. (1)

$V_1 = h_{12} V_2$

The equivalent circuit of the h-parameter representation is shown in Fig. Here, $h_{12}V_2$ is the controlled voltage source and $h_{21}I_2$ is the controlled current source.

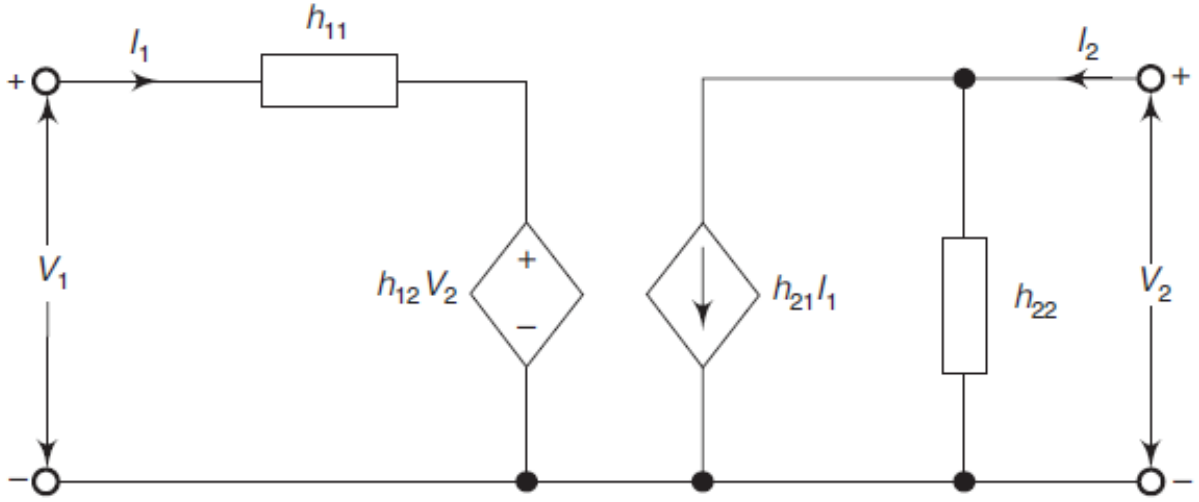
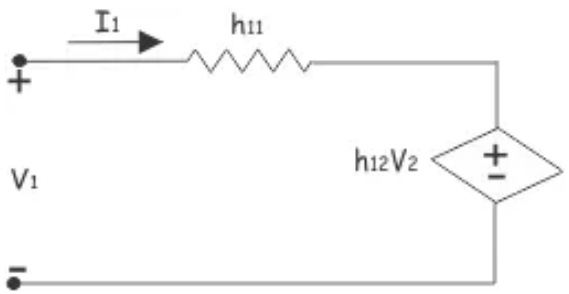


Fig. *Equivalent circuit of h-parameter model*

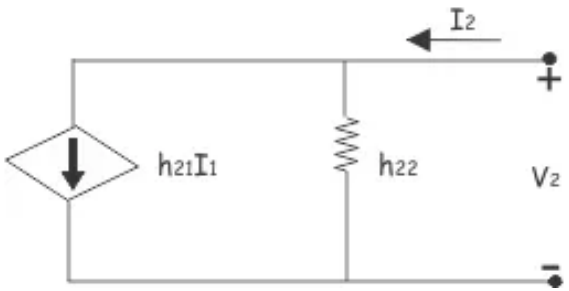
To draw **h parameter** equivalent network of a two port network, first we have to write the equation of voltages and currents using h parameters. These are:

$$V_1 = h_{11}I_1 + h_{12}V_2 \cdots\cdots\cdots\cdots\cdots (i)$$
$$I_2 = h_{21}I_1 + h_{22}V_2 \cdots\cdots\cdots\cdots\cdots (ii)$$

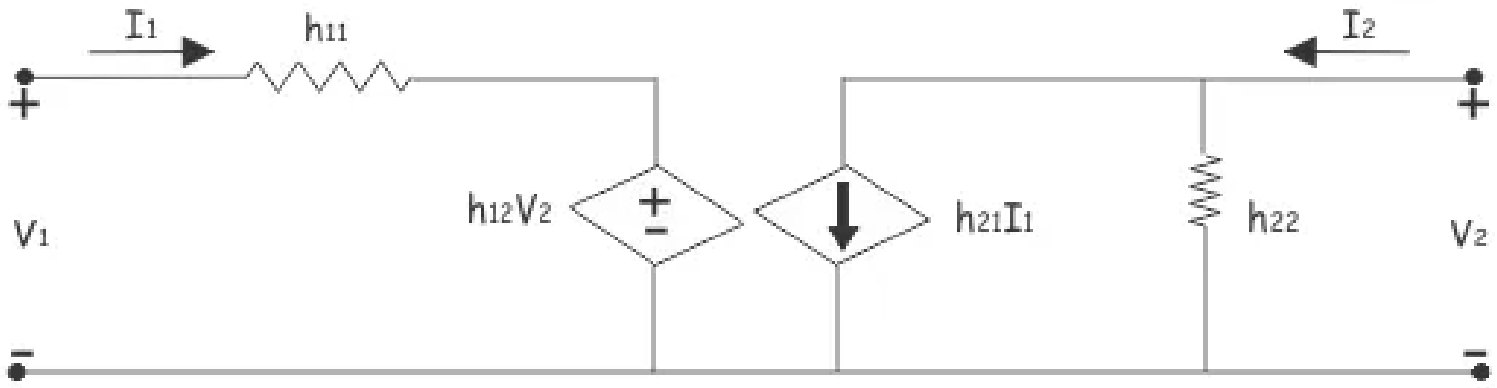
Equation (i) can be represented as a circuit based on Kirchhoff Voltage Law:



Equation (ii) can be represented as a circuit based on Kirchhoff Current Law:



Combining these two parts of the network we get:



The h parameters equivalent network of a two port network

Note: The dimensions of h-parameters are as follows:

$h_{11} \rightarrow \Omega$ **INPUT IMPEDANCE** *in ohms*

$h_{22} \rightarrow \mho$ **OUTPUT ADMITTANCE** *in mho*

$h_{12}, h_{21} \rightarrow$ dimensionless

As the dimensions are not alike, i.e., they are hybrid in nature, these parameters are called *hybrid parameters.*

The alternative subscript notations recommended by IEEE commonly used are

$$i = 11 = \text{input}, \quad o = 22 = \text{output}$$

$$f = 21 = \text{forward transfer}, \quad r = 12 = \text{reverse transfer}$$

Based on the definition of hybrid parameters, the mathematical model for two-port networks known as h-parameter model can be developed as shown in Fig.

When h-parameters are applied to transistors, it is a common practice to add a second subscript to designate the type of configuration considered, e for common emitter, b for common base and c for common collector. Thus, for a common emitter (CE) configuration,

CE INPUT IMPEDANCE → $h_{ie} = h_{11e}$ = short-circuit input impedance

CE OUPUT ADMITTANCE → $h_{oe} = h_{22e}$ = open-circuit output admittance

CE REVERSE VOLTAGE GAIN → $h_{re} = h_{12e}$ = open-circuit reverse-voltage gain

CE forward current GAIN → $h_{fe} = h_{21e}$ = short-circuit forward-current gain

The proposed model shown in Fig. should satisfy the h-parameter equations and it can be readily verified by writing Kirchhoff's voltage-law equation in the input loop and Kirchhoff's current-law equation for the output node. It is to be noted that the input circuit has a dependent voltage generator and the output circuit contains a dependent current generator.

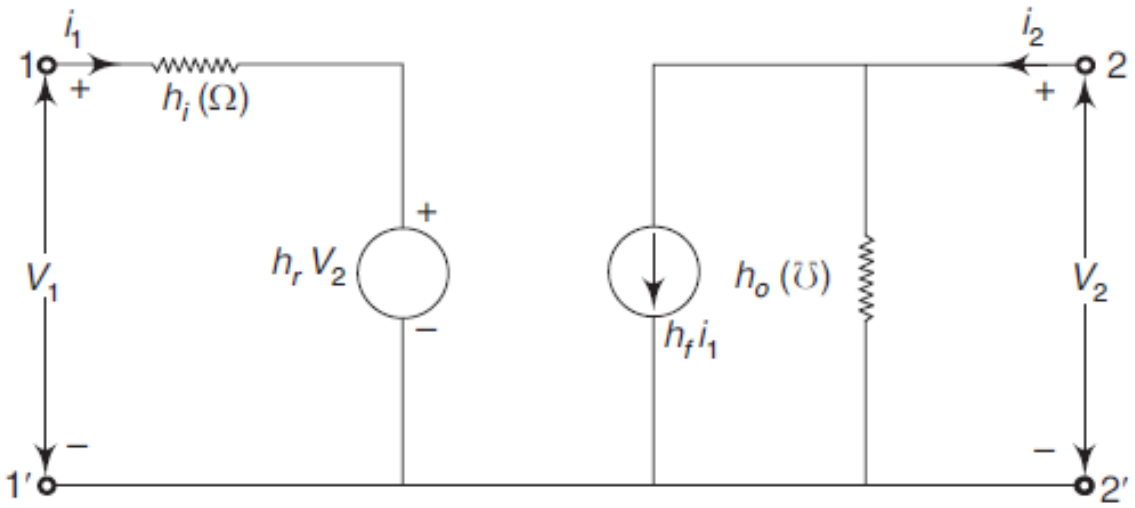


Fig. *h-parameter model for two-port network*

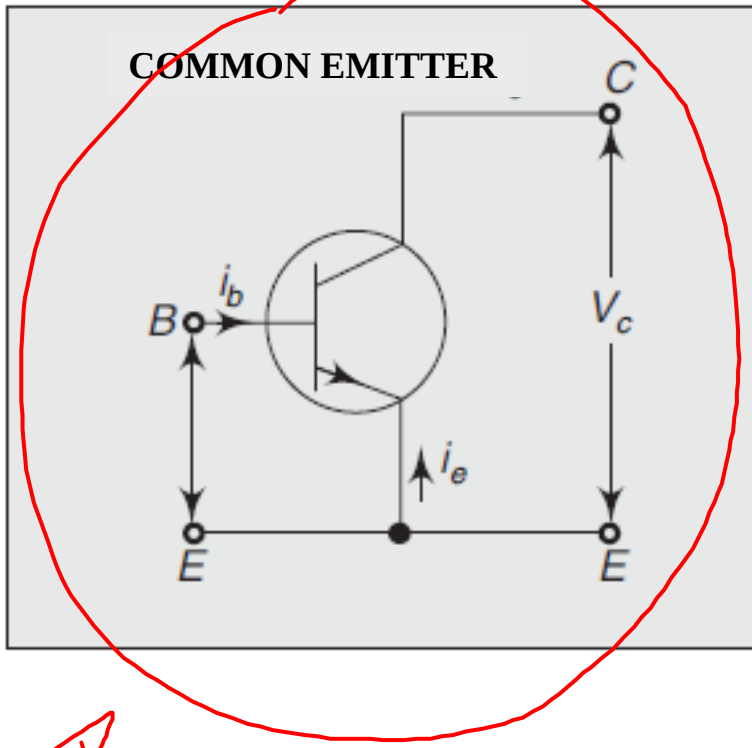
The h-parameter models and equations given in Table 2.2 are valid for NPN as well as PNP transistors and hold good for all types of loads and methods of biasing. Table 2.3 gives the typical h-parameter values for a transistor and Table 2.4 gives the conversion formulae to find the h-parameters for CC and CB configurations given the h-parameters for CE configuration.

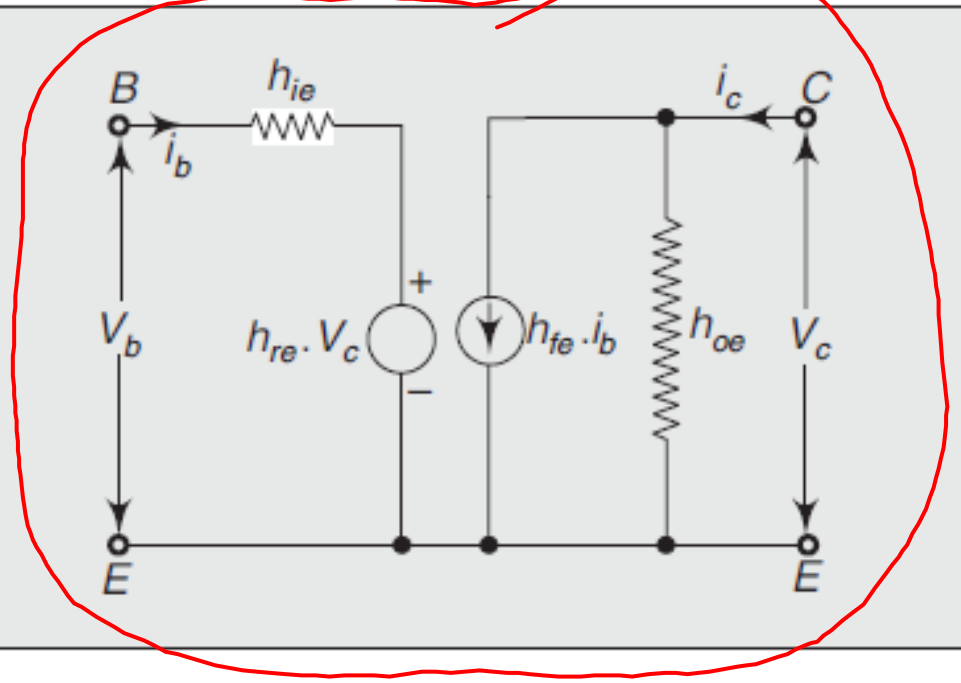
$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$

Table 2.2 *h-parameter model for the transistor in three different configurations*

COMMON EMITTER





$$v_b = h_{ie}.i_b + h_{re}.V_c$$
$$i_c = h_{fe}.i_b + h_{oe}.V_c$$

(Contd.)

CE A

CC equivalent for h-parameter

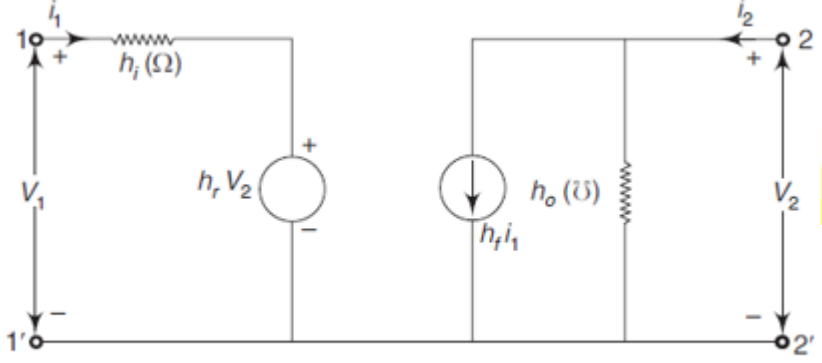
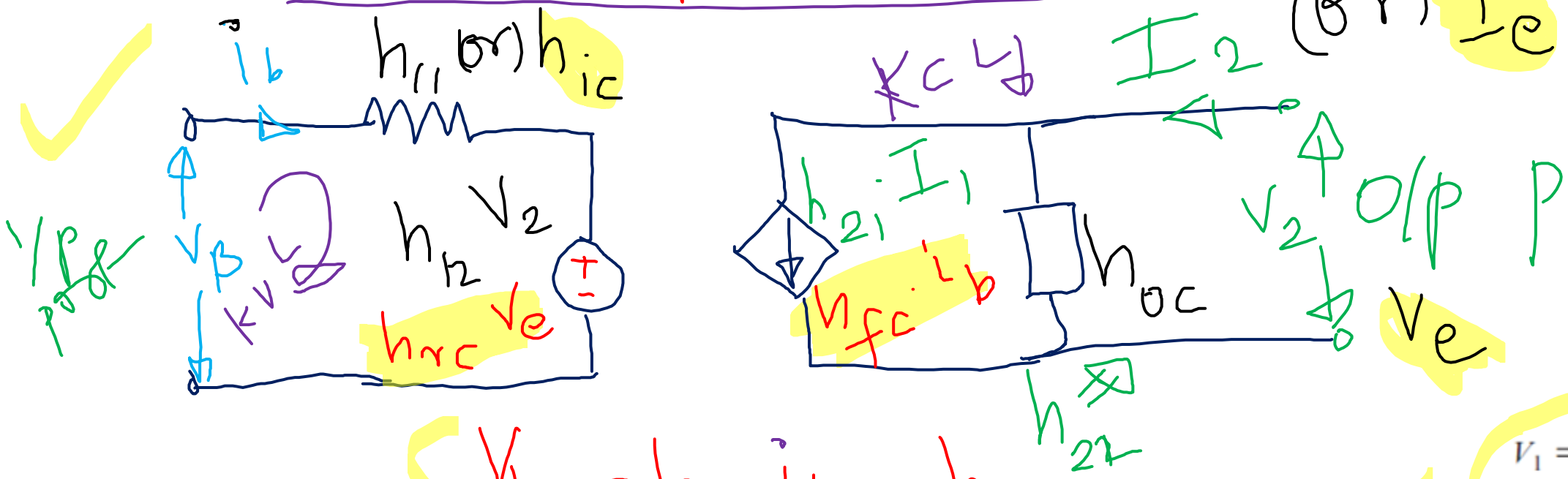


Fig. *h-parameter model for two-port network*



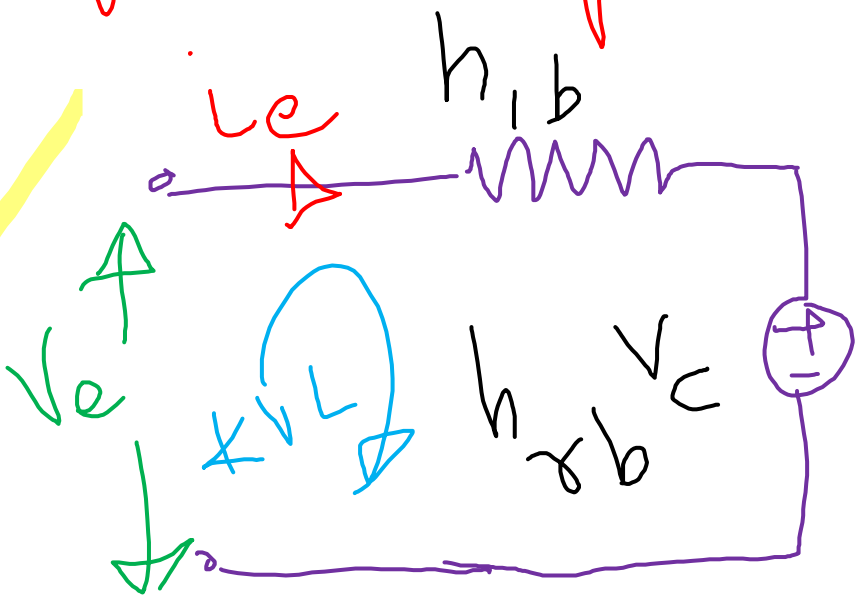
$$V_b = h_{ic}\, i_b + h_{rc} \cdot V_e$$

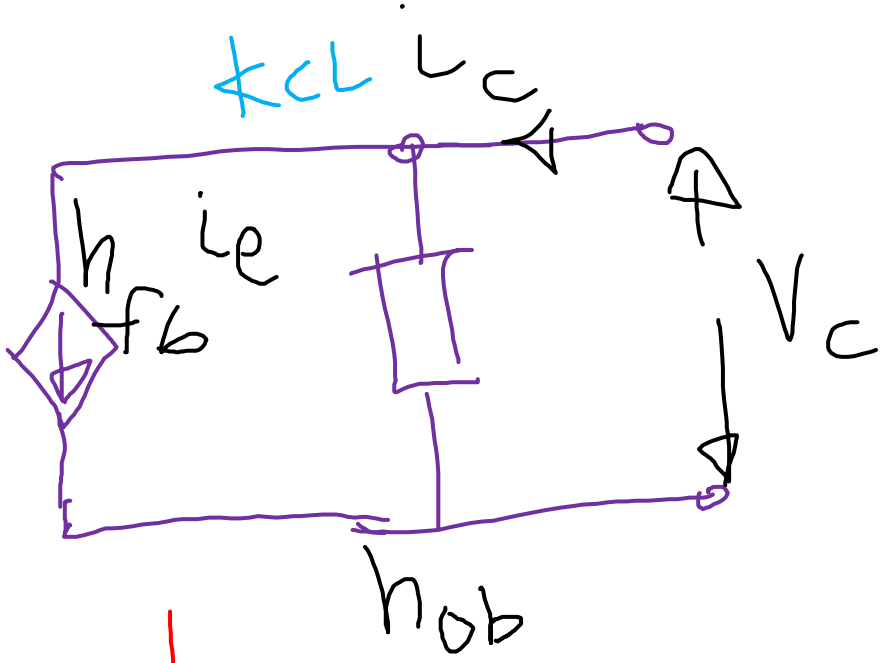
$$i_e = h_{fc}\, i_b + h_{oc}\, V_e$$

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

CB equivalent ckt for h-parameter model

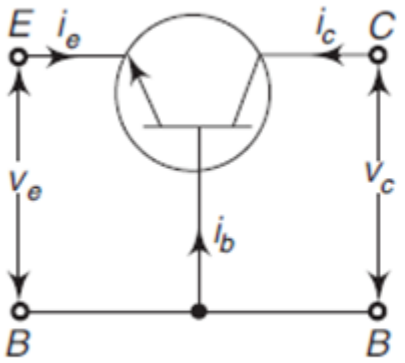


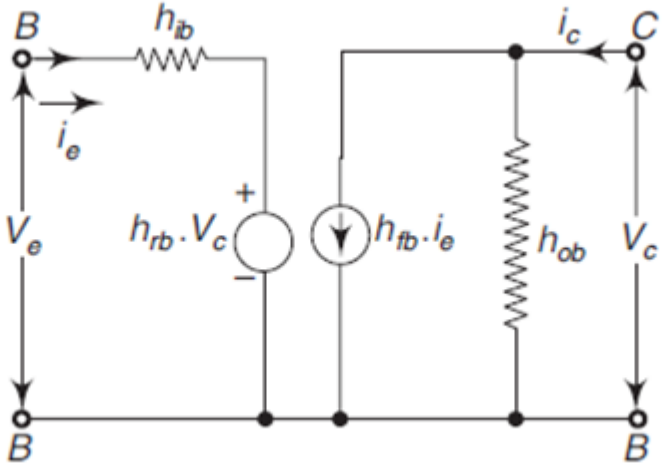


$$V_e = h_{ib} i_e + h_{rb} V_c \longrightarrow (1)$$

$$i_c = h_{fb} i_e + h_{ob} V_c \longrightarrow (2)$$

COMMON BASE





$$v_e = h_{ib}.i_e + h_{rb}.v_c$$
$$i_c = h_{fb}.i_e + h_{ob}.v_c$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

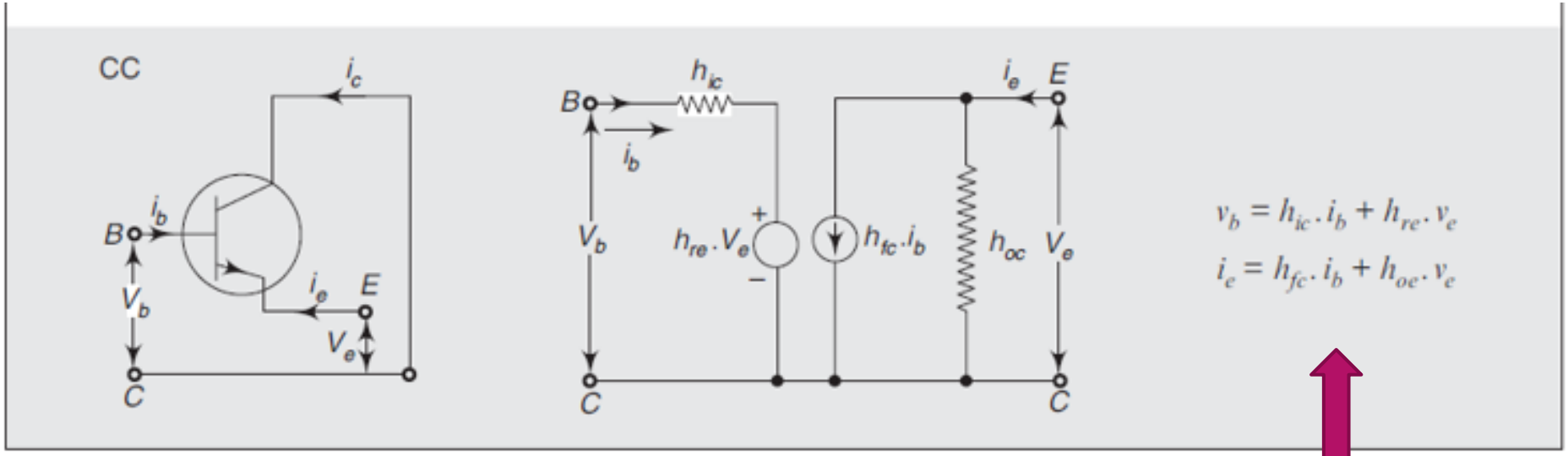
$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$

i/p ct : I_E
i/p v : V_E

E
i/p B

C
o/p

o/p ct. I_C
o/p v V_C



$$v_b = h_{ic}.i_b + h_{re}.v_e$$
$$i_c = h_{fc}.i_b + h_{oe}.v_e$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$V_1 = h_{11} I_1 + h_{12} V_2$$
$$I_2 = h_{21} I_1 + h_{22} V_2$$

Table *Typical h-parameter values for a transistor*

Parameter	*CE*	*CC*	*CB*
h_i	1,100 Ω	1,100 Ω	22 Ω
h_r	2.5×10^{-4}	1	2.5×10^{-4}
h_f	50	–51	–0.98
h_o	25 μA/V	25 μA/V	0.49 μA/V

Ebers-Moll Model

- Jewel James Ebers and John L. Moll introduced this mathematical model of transistor currents in 1954.

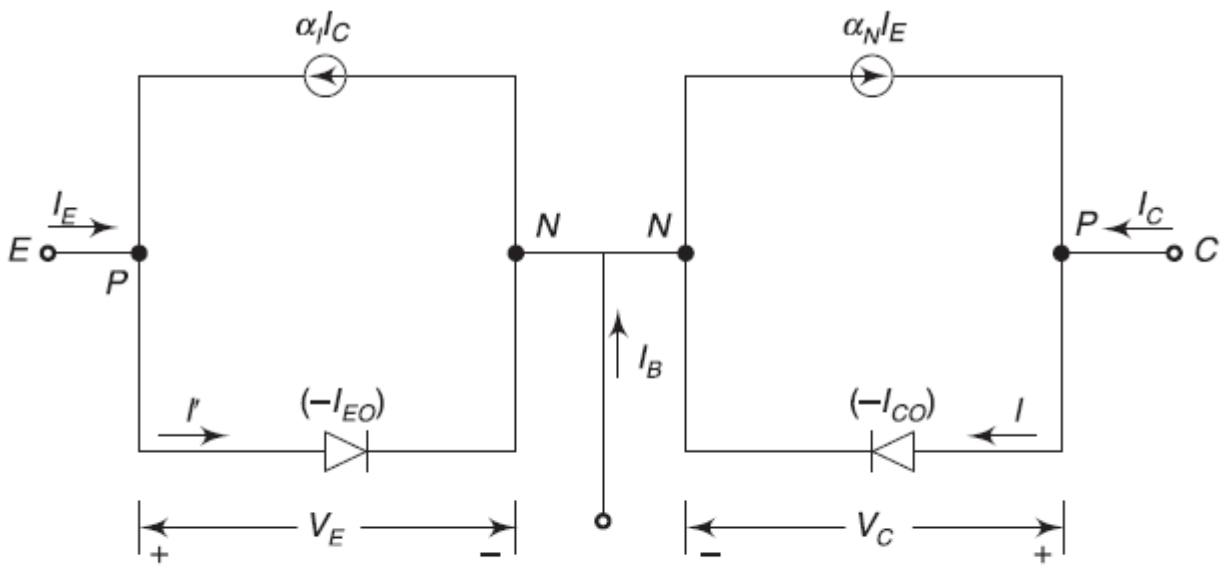


Fig. *Ebers–Moll model for a PNP transistor*

The general expression for collector current I_C of a transistor for any voltage across collector junction V_C and emitter current I_E is

$$I_C = -\alpha_N I_E - I_{CO}\left(e^{\frac{V_C}{V_T}} - 1\right) \longrightarrow (1)$$

where α_N is the current gain in *normal* operation and I_{CO} is the collector junction reverse saturation current.

interchange E & C in (1)

In inverted mode of operation, the above equation can be written as

$$I_E = -\alpha_I I_C - I_{EO}\left(e^{\frac{V_E}{V_T}} - 1\right) \longrightarrow (2)$$

where α_I is the inverted common-base current gain and I_{EO} is the emitter junction reverse saturation current.

The above four parameters are related by the condition

$$\boxed{\alpha_I I_{CO} = \alpha_N I_{EO}} \longrightarrow (3)$$

For many transistors I_{EO} lies in the range $0.5\,I_{CO}$ to I_{CO}.

Figure shows the Ebers–Moll model for a *PNP* transistor. Here, two separate ideal diodes are connected back to back with saturation currents $-I_{EO}$ and $-I_{CO}$ and there are two dependent current-controlled current sources shunting the ideal diodes. The current sources account for the minority carrier transport across the base. An application of Kirchhoff's current law to the collector node of Fig. gives

$$I_C = -\alpha_N I_E + I = -\alpha_N I_E + I_O\left(e^{\frac{V_C}{V_T}} - 1\right)$$

$I_C + I_E \alpha_N = I$

$I_C = I - \alpha_N I_E$

I_O = rev. sat. cr

$I_O = -I_{CO}$

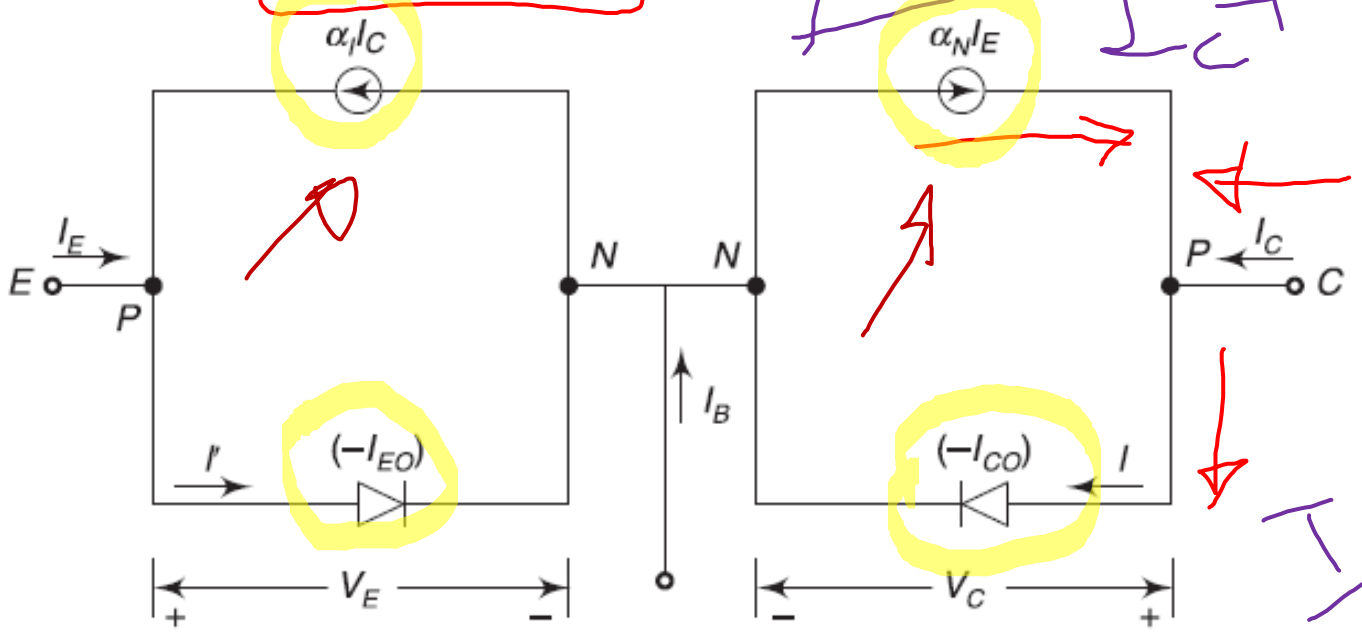


Fig. *Ebers–Moll model for a PNP transistor*

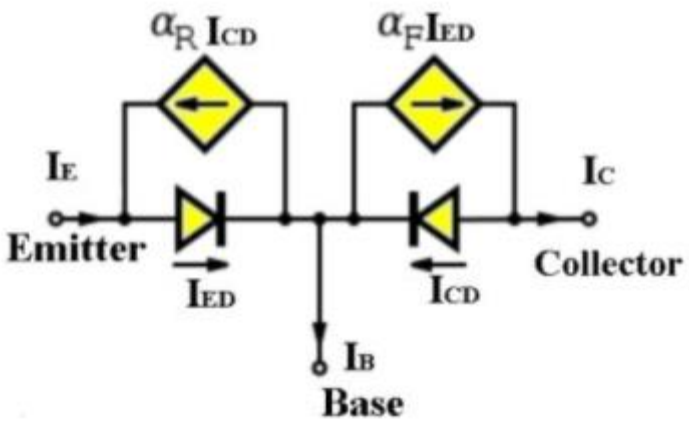
where I is the diode current. As I_O is the magnitude of reverse saturation current, then $I_O = -I_{CO}$.

$$I_C = -\alpha_N I_E - I_{CO}\left(e^{\frac{V_C}{V_T}} - 1\right)$$

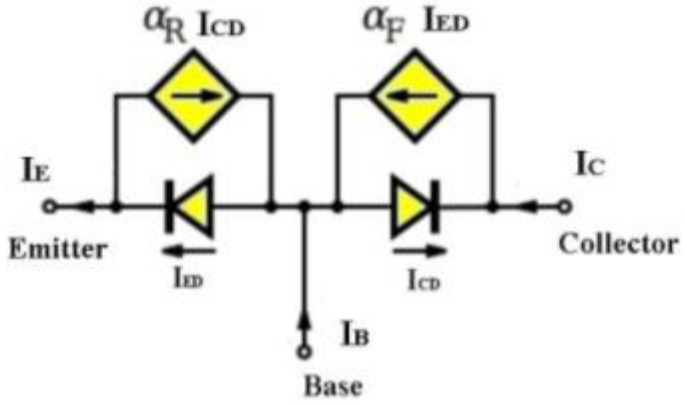
which is nothing but the general expression for collector current of a transistor
Hence, this model is valid for both forward and reverse static voltages applied across the transistor junctions. Here, base spreading resistance has been omitted and the difference between I_{CBO} and I_{CO} have been neglected.

The dependent current sources may be removed from the Fig. , provided $\alpha_N = \alpha_I = 0$. If the base-width is made much larger than the diffusion length of minority carriers in the base, all minority carriers will recombine in the base and no minority carrier will be available to reach the collector. Therefore, the transistor amplification factor α will become zero. As a result, transistor action ceases. Hence, it is not possible to construct a transistor by simply placing two isolated diodes back to back.

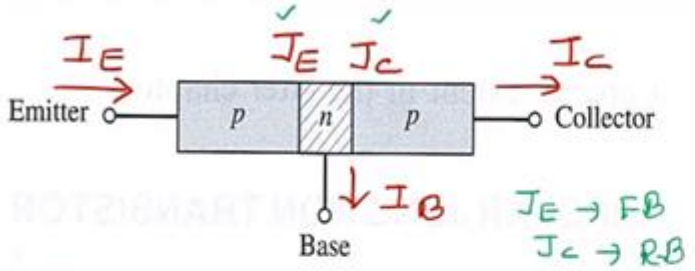
Ebers-Moll PNP model



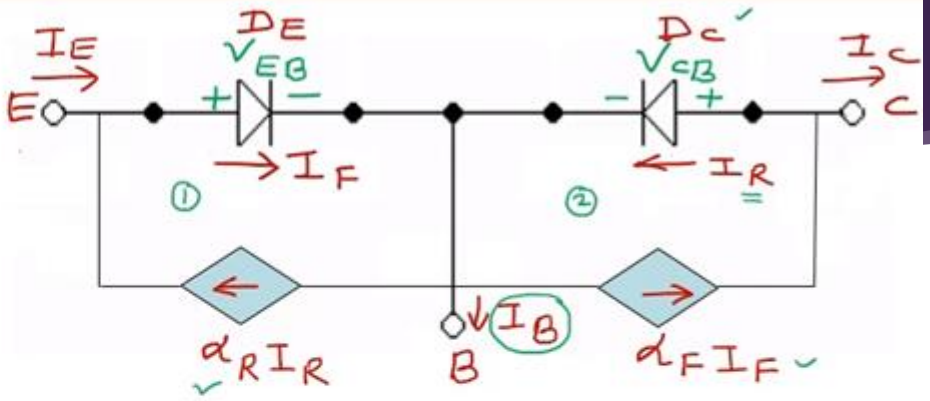
Ebers-Moll NPN model



Ebers Moll Model



$I_E = I_C + I_B \Rightarrow \boxed{I_B = I_E - I_C}$



- I_F current will also flow through collector junction
- Let us represent it as Current Dependent Current Source

- Let BJT works in inverse region, now J_C will be FB and J_E will be RB
- If now, I_R current flows through collector junction in inverse active region
- Because of this I_R, current in emitter junction is represented by Current Dependent Current Source

Assume Diodes as ideal diode

$$I_E = I_F - \alpha_R I_R \quad \text{—— ①}$$

$$I_C = \alpha_F I_F - I_R \quad \text{—— ②}$$

$$I_B = I_F + I_R - \alpha_F I_F - \alpha_R I_R$$

$$= (I_F - \alpha_R I_R) - (\alpha_F I_F - I_R)$$

$$\boxed{I_B = I_E - I_C}$$

Ebers Moll Model

$$I_E = I_F - \alpha_R I_R$$

$$I_E = I_{E_0}\left(e^{V_{EB}/V_T} - 1\right) - \alpha_R \times I_{C0}\left(e^{V_{CB}/V_T} - 1\right) \quad \text{—} (3)$$

$$I_C = \alpha_F I_F - I_R$$

$$I_C = \alpha_F I_{E_0}\left(e^{V_{EB}/V_T} - 1\right) - I_{C_0}\left(e^{V_{CB}/V_T} - 1\right) \quad \text{—} (4)$$

I_{EO}:
leakage current through J_E

I_{CO}:
leakage current through J_C

In Active mode of operation:

$J_E \rightarrow FB$, $V_{EB} \rightarrow +ve$, $J_C \rightarrow RB$ and $V_{CB} \rightarrow -ve$

$$I_E = I_{E_0}\left(e^{V_{EB}/V_T} - 1\right) + \alpha_R I_{C_0}$$

$$I_C = \alpha_F I_{E_0}\left(e^{V_{EB}/V_T} - 1\right) + I_{C_0}$$

$$\alpha_F I_{E_0} = \alpha_R I_{C_0} = I_S$$

$$I_{E_0} = \frac{I_S}{\alpha_F} \quad \& \quad I_{C_0} = \frac{I_S}{\alpha_R}$$

Rewriting equation 1 and 2, we get:

$$I_E = \frac{I_s}{\alpha_F}\left(e^{V_{EB}/V_T} - 1\right) - I_s\left(e^{V_{CB}/V_T} - 1\right) \quad (5)$$

$$I_C = I_s\left(e^{V_{EB}/V_T} - 1\right) - \frac{I_s}{\alpha_R}\left(e^{V_{CB}/V_T} - 1\right) \quad (6)$$

Rewriting both of above equations in terms of β_F, we get:

$$\alpha_F = \frac{\beta_F}{1+\beta_F} \quad \text{and} \quad \alpha_R = \frac{\beta_R}{1+\beta_R}$$

$$I_E = I_s\left[\left(e^{V_{EB}/V_T} - e^{V_{CB}/V_T}\right) + \frac{1}{\beta_F}\left(e^{V_{EB}/V_T} - 1\right)\right] \quad (7)$$

$$I_C = I_s\left[\left(e^{V_{EB}/V_T} - e^{V_{CB}/V_T}\right) - \frac{1}{\beta_R}\left(e^{V_{CB}/V_T} - 1\right)\right] \quad (8)$$

$$I_B = I_s\left[\frac{1}{\beta_F}\left(e^{V_{EB}/V_T} - 1\right) - \frac{1}{\beta_R}\left(e^{V_{CB}/V_T} - 1\right)\right] \quad (9)$$

$$I_B = I_E - I_C$$

For NPN transistor, change V_{EB} as V_{BE} and V_{CB} as V_{BC} in all three equations I_E, I_C, I_B