Reg. No.:

Name :

VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Model QP

Programme	:	**B.Tech(ECE & ECM)**	Semester	:	
Course	:	**Microprocessor and Interfacing**	Code	:	**BECE204L**
Faculty	:		Slot		
Time	:	**3 Hours**	Max. Marks	:	**100**
			Class Nbr		

Answer ALL Questions

Q.No.	Sub. Sec.	Question Description	Marks
1.	a.	Explain the function of the following signals of 8086 (i) $\overline{\text{LOCK}}$ (ii) $\overline{\text{TEST}}$ (iii) MN/$\overline{\text{MX}}$ (iv) $\overline{\text{BHE}}$ (v) READY (vi) M/$\overline{\text{IO}}$	**6**
	b.	State whether the following instructions are permitted or not and comment on them (i) MOV AX, DL (ii) DIV BL (iii) MOV [SI], [DI] (iv) MOV AX, [SI] (v) MOV 55H, AL (vi) ADD 5779H, AX (vii) ADD AX, 5779H (viii) AND DS, ES	**4**
2.		Write an 8086 ALP with necessary flow chart to calculate squares of BCD numbers from 0 to 9 and store them sequentially from 4000H offset onwards in the current data segment. The numbers and their squares are in the BCD format. Use a subroutine for the calculation of the square of a number	**10**
3.		State different techniques to pass input data/parameter to procedures in assembly language program and illustrate the same with examples.	**10**
4.		Write an 8086 ALP to create a file called DATA and store in it 100 bytes from memory block starting at 2000:2000, if either an interrupt appears at INTR pin with Type 0AH or an instruction equivalent to the above interrupt is executed. Also draw necessary flow chart.	**10**
5.		It is required to interface two chips of 32K X 8 ROM and four chips of 32K X 8 RAM with 8086 according to the following map ROM 1 and ROM 2 F0000H - FFFFFH, RAM 1 and RAM 2 D0000H - DFFFFH RAM 3 and RAM 4 E0000H - EFFFFH Show the implementation of this memory system.	**10**
6		Design a programmable timer using 8253 and 8086. Interface 8253 at an address 0050H for counter 0 and write the following ALPs. The 8086 and 8253 run at 6 MHz and 2 MHz respectively. (i) To generate a square wave of period 5 ms (ii) To interrupt the processor after 10 ms	**10**
7.		Discuss the bus structure of 8051 microcontroller to perform various operations.	**10**

8.		Show the stack and stack pointer for each line of the following program for 8051.
		MOV SP,#70H
		MOV R5,#66H
		MOV R2,#7FH
		MOV R7,#5DH
		PUSH 5
		PUSH 2
		PUSH 7
		CLR A
		MOV R2,A
		MOV R7,A
		POP 7
		POP 2
		POP 5
			10

9.		Assume that there is an inter college sports competition between five colleges in VIT and their final scores are stored in memory location starting from 40H.Write an assembly language program for 8051 to find out the winner of the competition and store the score of the winner in the memory location 70H.	**10**
10.	a.	Write an 8051 assembly language program to transfer "YOU" serially continuously with 9600 baud rate. Assume one start and stop bit for framing the data.	**10**
		Total Marks	**[100]**

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