

BECE204P-Microprocessors & Microcontrollers Lab

LAB-7

**ASSEMBLY PROGRAMMING WITH BIT-ORIENTED
AND PROGRAM CONTROL INSTRUCTIONS OF
8051**

CHALLENGING TASKS

1. Write an 8051 assembly language program to add the first 10 natural numbers
2. Write an ALP to compare two eight bit numbers NUM1 and NUM2 stored in external memory locations 8000h and 8001h respectively. Reflect your result as:
 - If $NUM1 < NUM2$, SET LSB of data RAM location 2FH (bit address 78H).
 - If $NUM1 > NUM2$, SET MSB of location 2FH (bit address 7FH).
 - If $NUM1 = NUM2$, then CLR both LSB & MSB of bit addressable memory location 2FH.

INSTRUCTIONS REQUIRED

PROGRAM CONTROL INSTRUCTIONS

- In the sequence of instructions to be executed, it is often necessary to transfer program control to a different location. There are **two categories** of instructions in the 8051 to achieve this.
 - **JUMP Instruction: Conditional and Unconditional**
 - **CALL Instruction**
- List of **Conditional JUMP** instructions in 8051
 - JZ - Jump if Zero
 - JNZ - Jump if Not Zero
 - JC - Jump if Carry is set.
 - JNC - Jump if Not Carry is set
 - JB - Jump if Bit is set.
 - JNB - Jump if Bit is Not set.
 - JBC - Jump if Bit is set and Clear the bit.
 - CJNE - Compare and Jump if Not Equal
 - DJNZ - Decrement and Jump if Not Zero

INSTRUCTIONS REQUIRED

PROGRAM CONTROL INSTRUCTIONS

➤ List of Unconditional JUMP instructions in 8051:

- JMP - JuMP
- SJMP - Short JuMP
- LJMP - Long JuMP
- AJMP - Absolute JuMP

➤ List of CALL instructions in 8051:

- ACALL - Absolute CALL
- LCALL - Long CALL

➤ Other types of control instructions in 8051:

- NOP - No OPeration
- RET - RETurn
- RETI - RETurn from Interrupt

INSTRUCTIONS REQUIRED

LOOPING IN 8051 - DJNZ

- Repeating a sequence of instructions a certain number of times is called a loop.
- In the 8051, the loop action is performed by the instruction,
DJNZ reg, Label or DJNZ Addr., Label
- In this instruction, the register is decremented; if it is not zero, it jumps to the target address referred to by the label.
- Prior to the start of the loop the register is loaded with the counter for the number of repetitions.
- Notice that in this instruction both the register decrement and the decision to jump are combined into a single instruction.

INSTRUCTIONS REQUIRED

COMPARISON IN 8051 - CJNE

- CJNE compares the value of operand1 and operand2 and branches to the indicated relative address if operand1 and operand2 are not equal.

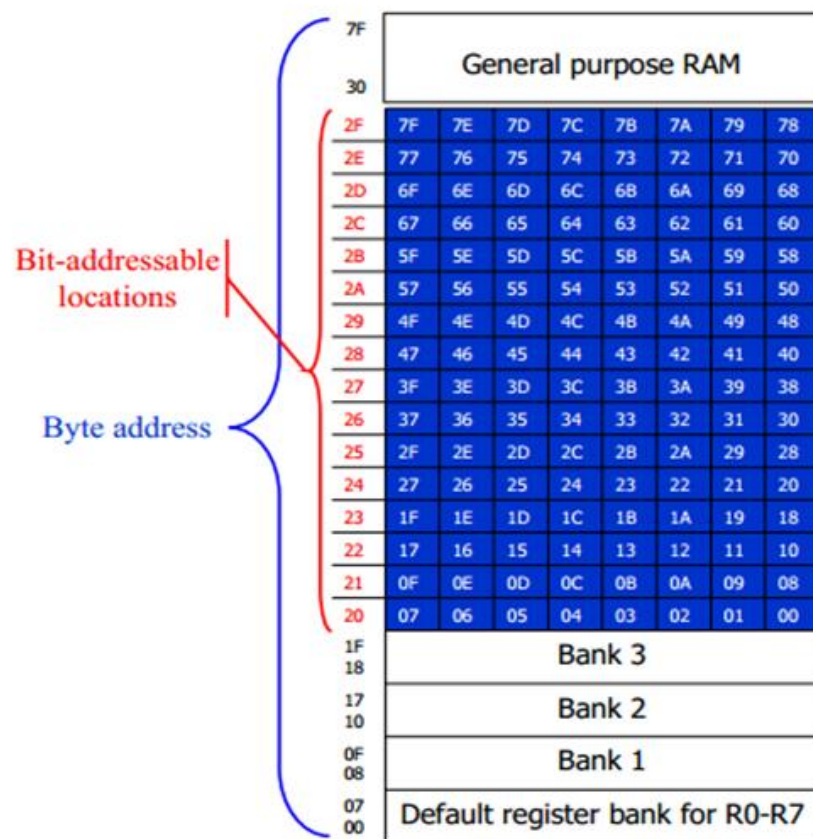
CJNE operand1, operand2, reladdr

- If the two operands are equal program flow continues with the instruction following the CJNE instruction.
- The Carry bit (C) is set if operand1 is less than operand2, otherwise it is cleared.

INSTRUCTIONS REQUIRED

BIT ORIENTED INSTRUCTIONS

- The Boolean or Bit Manipulation Instructions will **deal with bit variables**.
- There is a **special bit-addressable area in the RAM** and some of the Special Function Registers (SFRs) are also bit addressable.
- List of bit oriented instructions are:
 - CLR
 - SETB
 - CPL
 - MOV
 - ANL
 - ORL



INSTRUCTIONS REQUIRED

BIT ORIENTED INSTRUCTIONS

Mnemonic	Instruction	Description	# of Bytes	# of Cycles
CLR	C	$C \leftarrow 0$ (C = Carry Bit)	1	1
	Bit	$\text{Bit} \leftarrow 0$ (Bit = Direct Bit)	2	1
SET	C	$C \leftarrow 1$	1	1
	Bit	$\text{Bit} \leftarrow 1$	2	1
CPL	C	$C \leftarrow \overline{C}$	1	1
	Bit	$\text{Bit} \leftarrow \overline{\text{Bit}}$	2	1
ANL	C, /Bit	$C \leftarrow C \cdot \overline{\text{Bit}}$ (AND)	2	1
	C, Bit	$C \leftarrow C \cdot \text{Bit}$ (AND)	2	1
ORL	C, /Bit	$C \leftarrow C + \overline{\text{Bit}}$ (OR)	2	1
	C, Bit	$C \leftarrow C + \text{Bit}$ (OR)	2	1
MOV	C, Bit	$C \leftarrow \text{Bit}$	2	1
	Bit, C	$\text{Bit} \leftarrow C$	2	2

LAB TASK-1

Write a program to move a block of FIVE data starting from RAM 40H to external RAM memory 3000H onwards and perform complement operation before storing to RAM.

```
ORG 0000H
MOV R0, #40H
MOV DPTR, #3000H
MOV R2, #05H
LOOP:  MOV A,@R0
        CPL A
        MOVX @DPTR,A
        INC R0
        INC DPTR
        DJNZ R2, LOOP
        END
```

INPUT:

Memory 1															
Address: D:40H															
D:0x40:	01	02	03	04	05	00	00	00	00	00	00	00	00	00	00
D:0x5C:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
D:0x78:	00	00	00	00	00	00	00	00	00	FF	07	00	00	00	00
D:0x94:	00	00	00	FF	00	00	00	00	00	00	00	00	00	FF	FF

OUTPUT:

Memory 1															
Address: X:3000H															
X:0x003000:	FE	FD	FC	FB	FA	00	00	00	00	00	00	00	00	00	00
X:0x00301C:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
X:0x003038:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
X:0x003054:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
X:0x003070:	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00

LAB TASK-2

Assume that RAM bit location 24H holds the status of PIR sensor to indicate whether there has been a human presence or not inside a hall. Write an 8051 assembly language program to set port P1.0 bit as high if 24H is high. If it is low, set port P1.0 bit as low.

```
                ORG 0000H
                MOV P1, #00H

AGAIN:          MOV C, 24H
                JNC NO
                SETB P1.0
                SJMP AGAIN

NO:             CLR P1.0
                SJMP AGAIN
                END
```

INPUT:

Memory 1	
Address:	D:24H
D:0x24:	00 00 00 00 00 00 00 00
D:0x40:	00 00 00 00 00 00 00 00
D:0x5C:	00 00 00 00 00 00 00 00
D:0x78:	00 00 00 00 00 00 00 00

Memory 1	
Address:	D:24H
D:0x24:	10 00 00 00 00 00 00 00
D:0x40:	00 00 00 00 00 00 00 00
D:0x5C:	00 00 00 00 00 00 00 00
D:0x78:	00 00 00 00 00 00 00 00

OUTPUT:

Parallel Port 1

Port 1

P1: 0x00 7 Bits 0

Pins: 0x00

Parallel Port 1

Port 1

P1: 0x01 7 Bits 0

Pins: 0x01

LAB TASK-3

Write an 8051 ASM program to read a temperature value (T) from RAM location 55H. According to the test results, place the temperature value into the registers indicated below:

- If $T=30H$ then $A=30H$
- If $T<30H$ then $R1=T$
- If $T>30H$ then $R2=T$

```

ORG 0000H
MOV A, 55H
CJNE A, #30H, OVER
SJMP EXIT
OVER:  JNC NEXT
      MOV R1, A
      SJMP EXIT
NEXT:  MOV R2, A
EXIT:  NOP
      END
    
```

CASE (i) $T=30H$

INPUT:

Memory 1	
Address:	D:55H
D:0x55:	30 00 00 00 00 00 00 00
D:0x71:	00 00 00 00 00 00 00 00
D:0x8D:	00 08 00 FF 00 00 00 00
D:0xA9:	00 00 00 00 00 00 00 00

OUTPUT:

Register	Value
Regs	
r0	0x00
r1	0x00
r2	0x00
r3	0x00
r4	0x00
r5	0x00
r6	0x00
r7	0x00
Sys	
a	0x30
b	0x00

CASE (ii) $T<30H$

INPUT:

Memory 1	
Address:	D:55H
D:0x55:	25 00 00 00 00 00 00 00
D:0x71:	00 00 00 00 00 00 00 00
D:0x8D:	00 08 00 FF 00 00 00 00
D:0xA9:	00 00 00 00 00 00 00 00

OUTPUT:

Register	Value
Regs	
r0	0x00
r1	0x25
r2	0x00
r3	0x00
r4	0x00
r5	0x00
r6	0x00
r7	0x00
Sys	
a	0x25
b	0x00

CASE (iii) $T>30H$

INPUT:

Memory 1	
Address:	D:55H
D:0x55:	35 00 00 00 00 00 00 00
D:0x71:	00 00 00 00 00 00 00 00
D:0x8D:	00 08 00 FF 00 00 00 00
D:0xA9:	00 00 00 00 00 00 00 00

OUTPUT:

Register	Value
Regs	
r0	0x00
r1	0x25
r2	0x35
r3	0x00
r4	0x00
r5	0x00
r6	0x00
r7	0x00
Sys	
a	0x35
b	0x00