8

555 TIMER

8.1 INTRODUCTION

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8-pin circular style, TO-99 can or 8-pin mini DIP or as 14-pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package. A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

The 555 timer can be used with supply voltage in the range of + 5V to + 18V and can drive load upto 200 mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply voltage, the 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

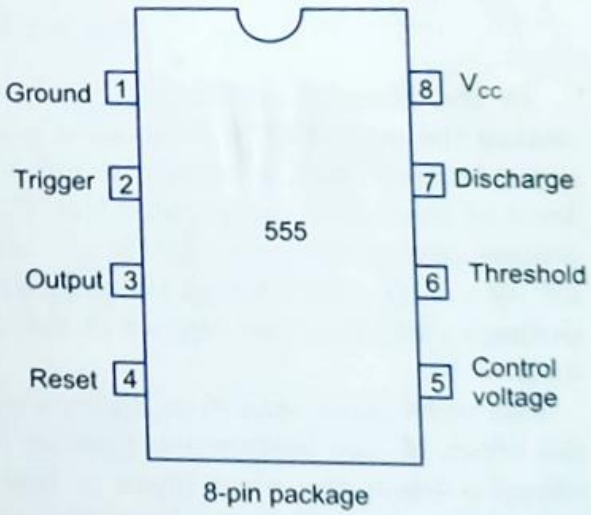

Fig. 8.1 Pin diagram

8.2 DESCRIPTION OF FUNCTIONAL DIAGRAM

Figure 8.1 gives the pin diagram and Fig. 8.2 gives the functional diagram for 555 IC timer. Referring to Fig. 8.2, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) V_{CC} to the upper comparator (UC) and (1/3) V_{CC} to the lower comparator (LC), where V_{CC} is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5). In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

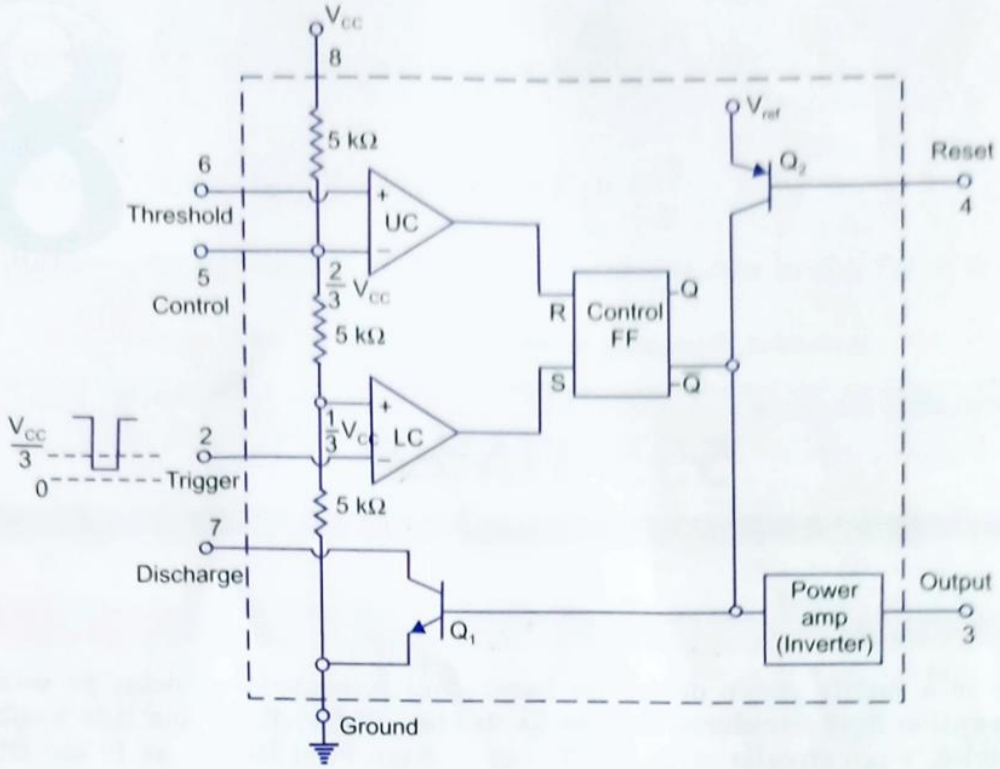

Fig. 8.2 Functional diagram of 555 timer

In the standby (stable) state, the output $\bar{Q}$ of the control flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e. $V_{CC}/3$). At the negative going edge of the trigger, as the trigger passes through ($V_{CC}/3$), the output of the lower comparator goes HIGH and sets the FF ($Q = 1$, $\bar{Q} = 0$). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3) V_{CC}, the output of the upper comparator goes HIGH and resets the FF ($Q = 0$, $\bar{Q} = 1$).

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to V_{CC}. The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{CC}.

8.3 MONOSTABLE OPERATION

Figure 8.3 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig. 8.4. In the standby state, FF holds transistor Q_1 ***on***, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e. LOW. As the trigger passes through $V_{CC}/3$, the FF is set, i.e. $\bar{Q} = 0$. This makes the transistor Q_1 ***off*** and the short circuit across the timing capacitor C is released. As Q is LOW, output goes HIGH ($= V_{CC}$). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards V_{CC} with a time constant RC as in Fig. 8.5 (b). After

a time period T (calculated later), the capacitor voltage is just greater than (2/3) V_{CC} and the upper comparator resets the FF, that is, $R = 1$, $S = 0$ (assuming very small trigger pulse width). This makes $\overline{Q} = 1$, transistor Q_1 goes **on** (i.e. saturates), thereby discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential as shown in Fig. 8.5 (c).

The voltage across the capacitor as in Fig. 8.5 (b) is given by

$$v_c = V_{CC}\,(1 - e^{-t/RC}) \qquad (8.1)$$

At $t = T$, $\quad v_c = (2/3)\,V_{CC}$

Therefore, $\dfrac{2}{3}V_{CC} = V_{CC}\,(1 - e^{-T/RC})$

or, $\quad T = RC \ln (1/3)$

or, $\quad T = 1.1\,RC$ (seconds) $\qquad (8.2)$

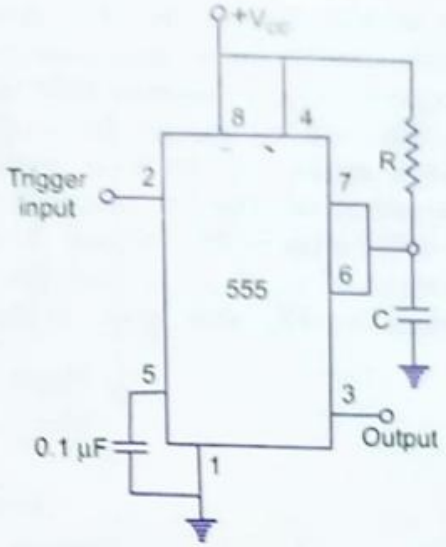

Fig. 8.3 Monostable multivibrator

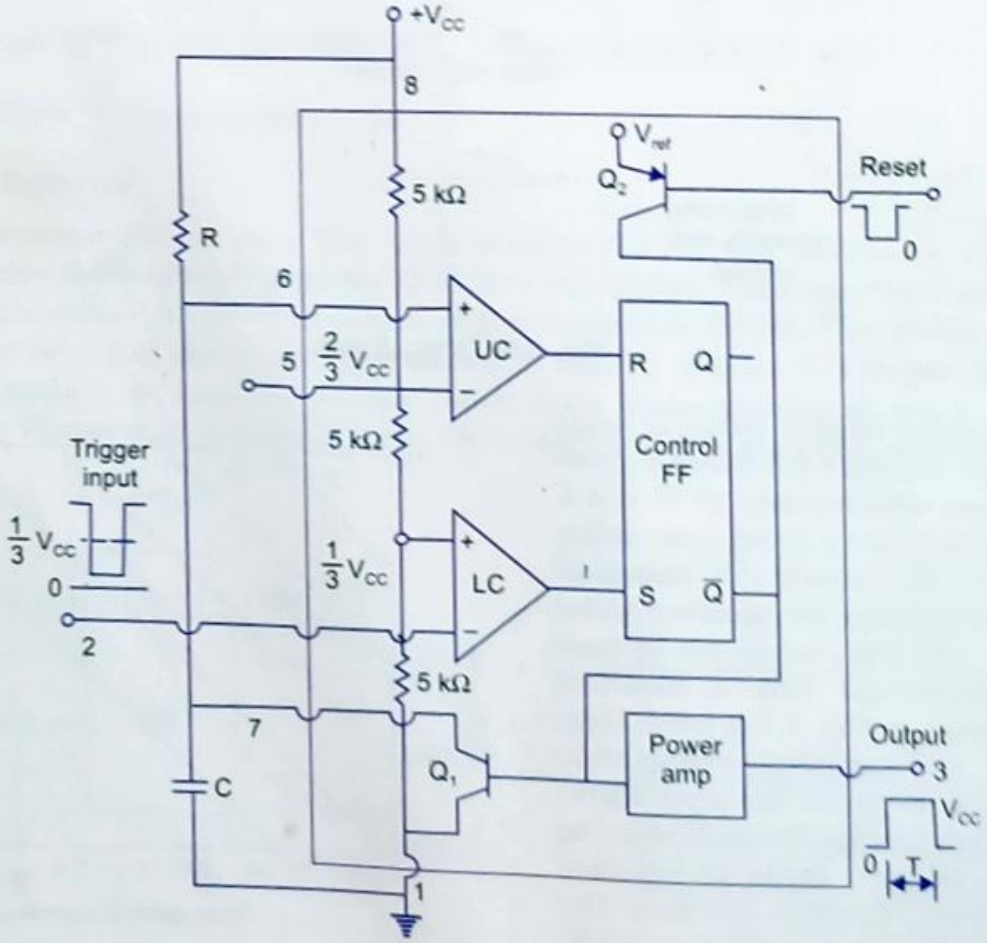

Fig. 8.4 Timer in monostable operation with functional diagram

It is evident from Eq. (8.2) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse as in Fig. 8.5(d) is applied to the reset terminal (pin-4) during the timing cycle, transistor Q_2 goes ***off***, Q_1 becomes ***on*** and the external timing capacitor C is immediately discharged. The output now will be as in Fig. 8.5 (e). It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn ***on*** Q_1 immediately and thereby avoid the propagation delay through the FF. Now, even if the reset is released, the output will still remain LOW until

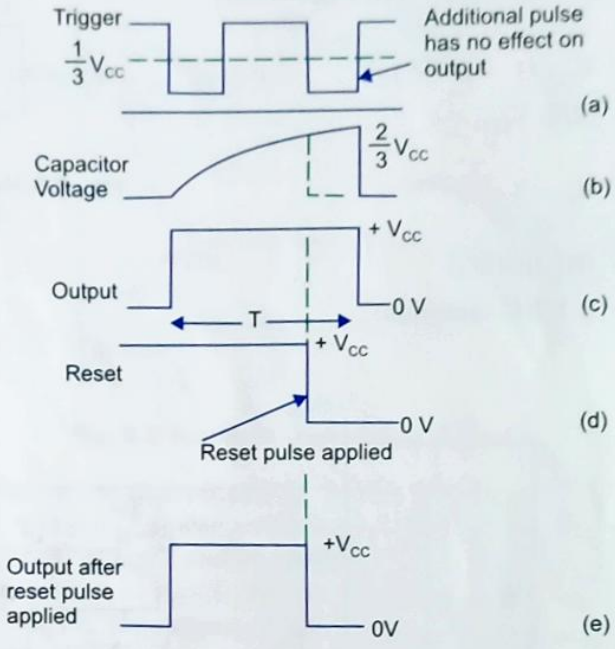

Fig. 8.5 Timing pulses

a negative going trigger pulse is again applied at pin 2. Figure 8.6 shows a graph of the various combinations of R and C necessary to produce a given time delay.

Sometimes the monostable circuit of Fig. 8.3 mistriggers on positive pulse edges, even with the control pin by pass capacitor. To prevent this, a modified circuit as shown in Fig. 8.7 is used. Here the resistor and capacitor combination of 10 kΩ and 0.001 μF at the input forms a differentiator. During the positive going edge of the trigger, diode D becomes forward biased, thereby limiting the amplitude of the positive spike to 0.7 V.

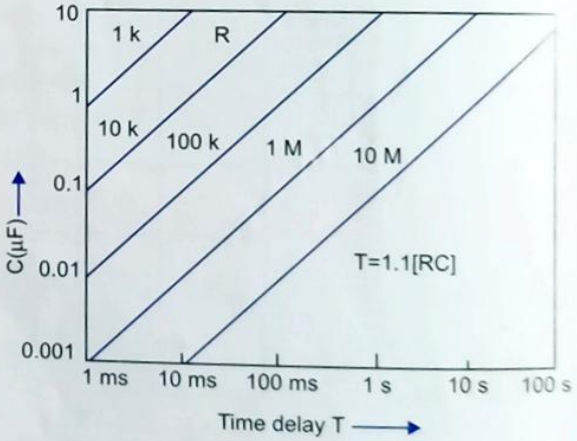

Fig. 8.6 Graph of *RC* combinations for different time delays

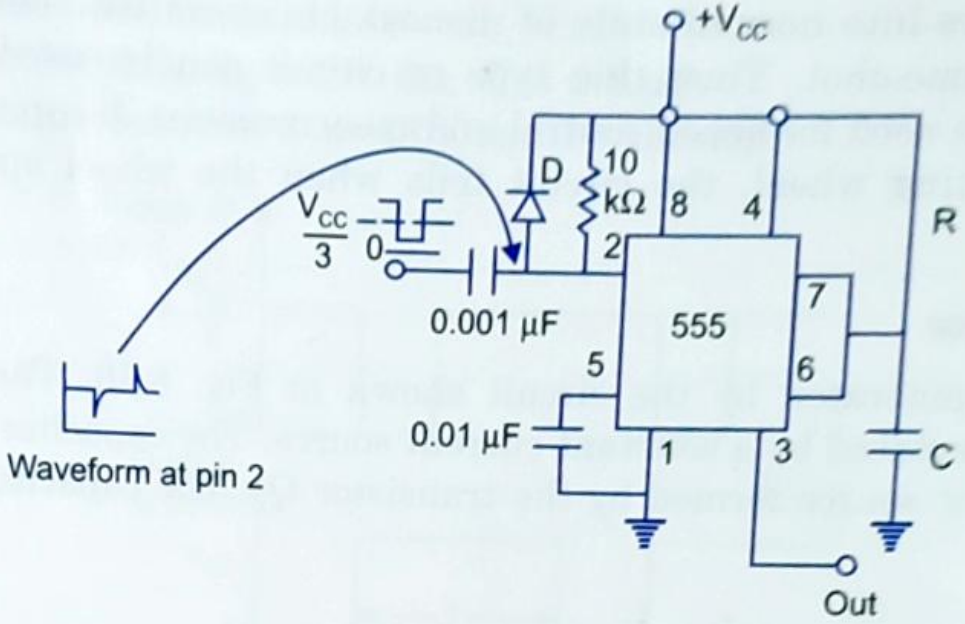

Fig. 8.7 Modified monostable circuit

Example 8.1

In the monostable multivibrator of Fig. 8.3, $R = 100$ kΩ and the time delay $T = 100$ mS. Calculate the value of C. Verify the value of C obtained from the graphs of Fig. 8.6.

Solution

From Eq. (8.2), we get

$$C = T/1.1\ R = 100 \times 10^{-3}/1.1 \times 100 \times 10^{3} = 0.9\ \mu F$$

From the graph of Fig. 8.6, the value of C is found to be 0.9 μF also.

8.3.1 Applications in Monostable Mode

8.4 ASTABLE OPERATION

The device is connected for astable operation as shown in Fig. 8.15. For better understanding, the complete diagram of astable multivibrator with detailed internal diagram of 555 is shown in Fig. 8.16. Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. When the power supply V_{CC} is connected, the external timing capacitor C charges towards V_{CC} with a time constant $(R_A + R_B)C$. During this time, output (pin 3) is high (equals V_{CC}) as Reset $R = 0$, Set $S = 1$ and this combination makes $\overline{Q} = 0$ which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) V_{CC} the upper comparator triggers the control flip-flop so that $\overline{Q} = 1$. This, in turn, makes transistor Q_1 ***on*** and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC (neglecting the forward resistance of Q_1). Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1. The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2 A is the maximum current through the ***on*** transistor Q_1.

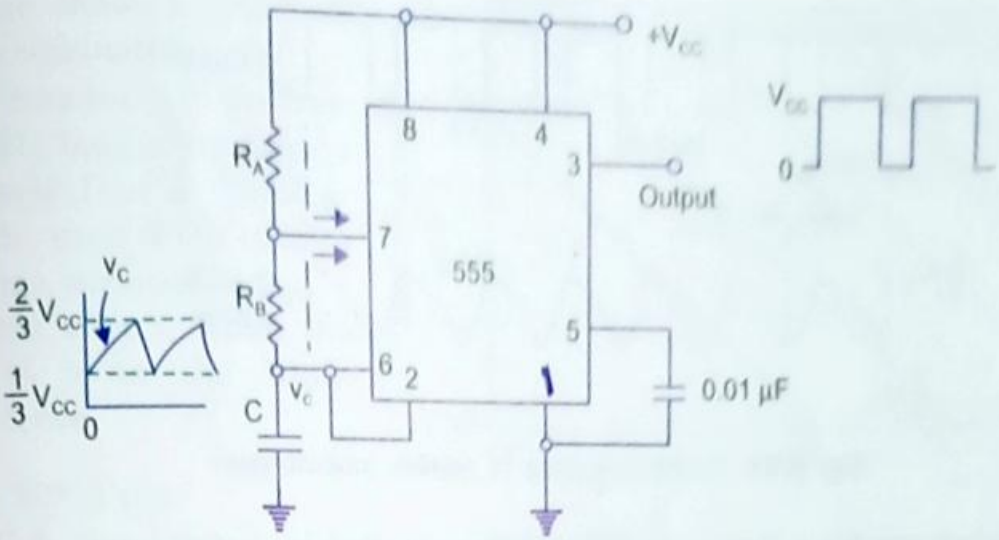

Fig. 8.15 Astable multivibrator using 555 timer

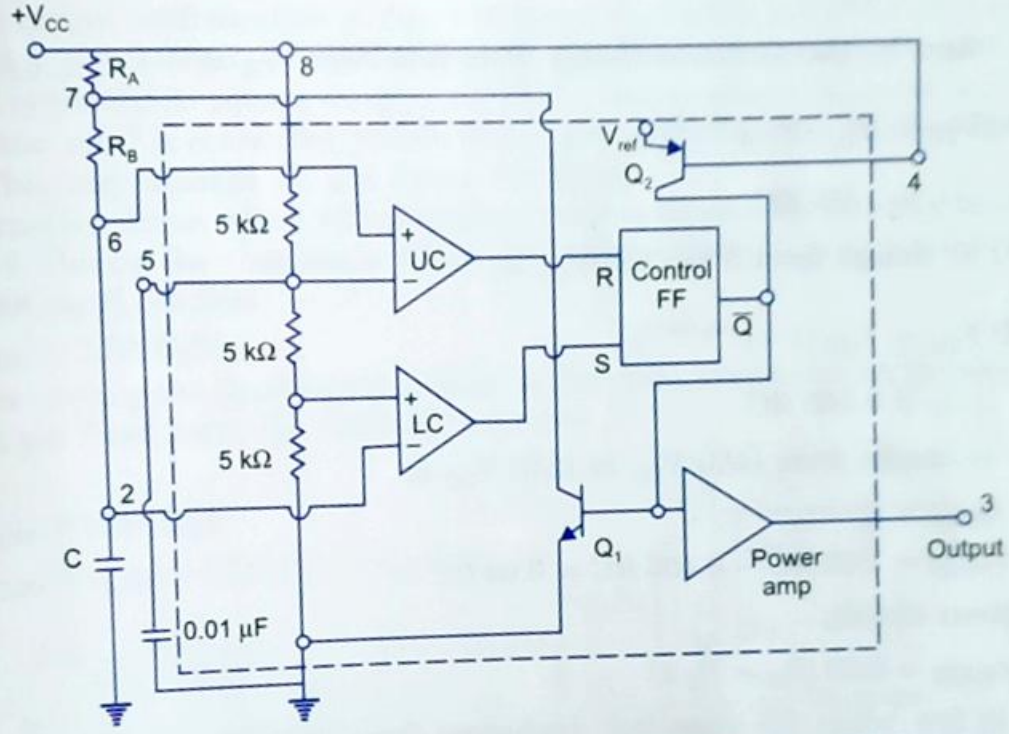

Fig. 8.16 Functional diagram of astable multivibrator using 555 timer

During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) $V_{CC}/3$, the lower comparator is triggered and at this stage $S = 1$, $R = 0$, which turns $\overline{Q} = 0$. Now $\overline{Q} = 0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) V_{CC} and (1/3) V_{CC} respectively. Figure 8.17 shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) V_{CC} to (2/3) V_{CC}. It may be calculated as follows:

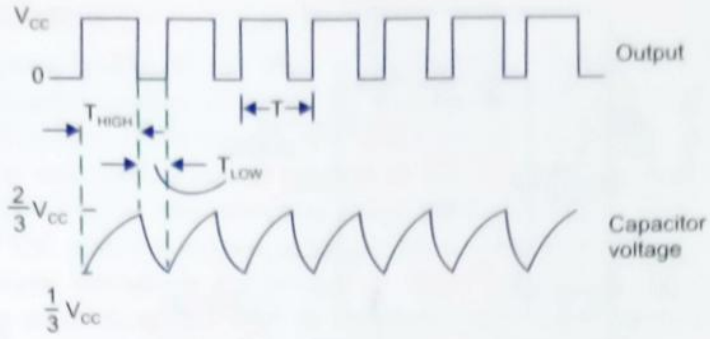

Fig. 8.17 Timing sequence of astable multivibrator

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{CC} volts is given by

$$v_c = V_{CC}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{CC} is,

$$(2/3)\,V_{CC} = V_{CC}\,(1 - e^{-t_1/RC}) \tag{8.9}$$

or, $$t_1 = 1.09\,RC$$

and the time t_2 to charge from 0 to (1/3) V_{CC} is,

$$(1/3)\,V_{CC} = V_{CC}\,(1 - e^{-t_2/RC}) \tag{8.10}$$

or, $$t_2 = 0.405\,RC$$

So the time to charge from (1/3) V_{CC} to (2/3) V_{CC} is

$$t_{HIGH} = t_1 - t_2$$

$$t_{HIGH} = 1.09\,RC - 0.405\,RC = 0.69\,RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\,(R_A + R_B)C \tag{8.11}$$

The output is low while the capacitor discharges from (2/3) V_{CC} to (1/3) V_{CC} and the voltage across the capacitor is given by

$$(1/3)\,V_{CC} = (2/3)V_{CC}\,e^{-t/RC}$$

Solving, we get $t = 0.69\,RC$

So, for the given circuit, $t_{LOW} = 0.69\,R_BC$ (8.12)

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or, $$T = 0.69\,(R_A + 2R_B)\,C$$

So, $$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \tag{8.13}$$

Figure 8.18 shows a graph of the various combinations of $(R_A + R_B)$ and C necessary to produce a given stable output frequency. The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$. In this circuit, when the transistor Q_1 is ***on***, the output goes low. Hence,

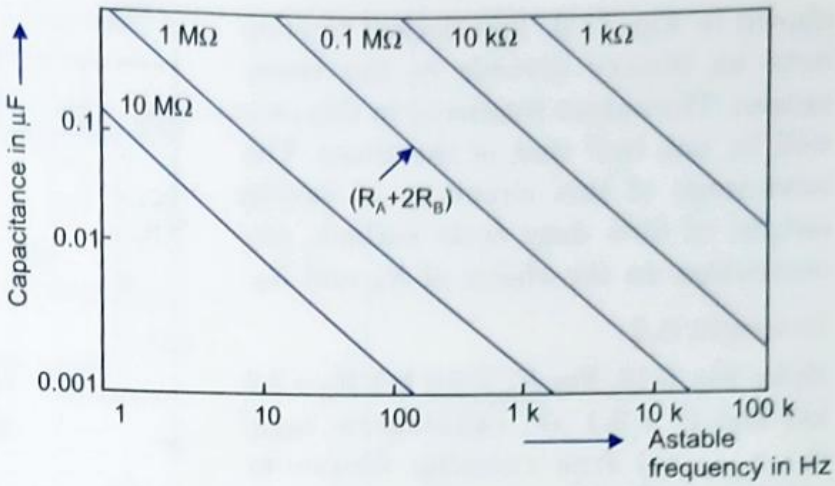

Fig. 8.18 Frequency dependence of R_A, R_B and C

$$D\% = \frac{t_{LOW}}{T} \times 100$$

$$= \frac{R_B}{R_A + 2R_B} \times 100 \qquad (8.14)$$

With the circuit configuration of Fig. 8.15 it is not possible to have a duty cycle more than 50% since $t_{HIGH} = 0.69\ (R_A + R_B)\ C$ will always be greater than $t_{LOW} = 0.69\ R_B C$. In order to obtain a symmetrical square wave i.e. $D = 50\%$, the resistance R_A must be reduced to zero. However, now pin 7 is connected directly to V_{CC} and extra current will flow through Q_1 when it is ***on***. This may damage Q_1 and hence the timer.

An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 8.19. During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that

$$t_{HIGH} = 0.69\ R_A C$$

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So $t_{LOW} = 0.69\ R_B C$ (8.15)

$T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + R_B)\ C$ (8.16)

or, $f = \dfrac{1.45}{(R_A + R_B)C}$ (8.17)

and duty cycle $D = \dfrac{R_B}{R_A + R_B}$

Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width. However, a series resistor of atleast 100 Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value. And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the nonsymmetrical square wave generator is

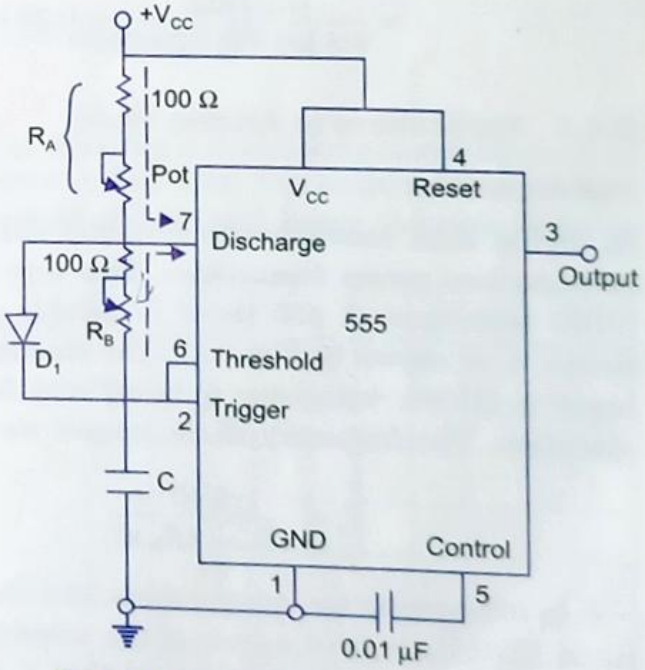

Fig. 8.19 Adjustable duty cycle rectangular wave generator

shown in Fig. 8.20. The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer. The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

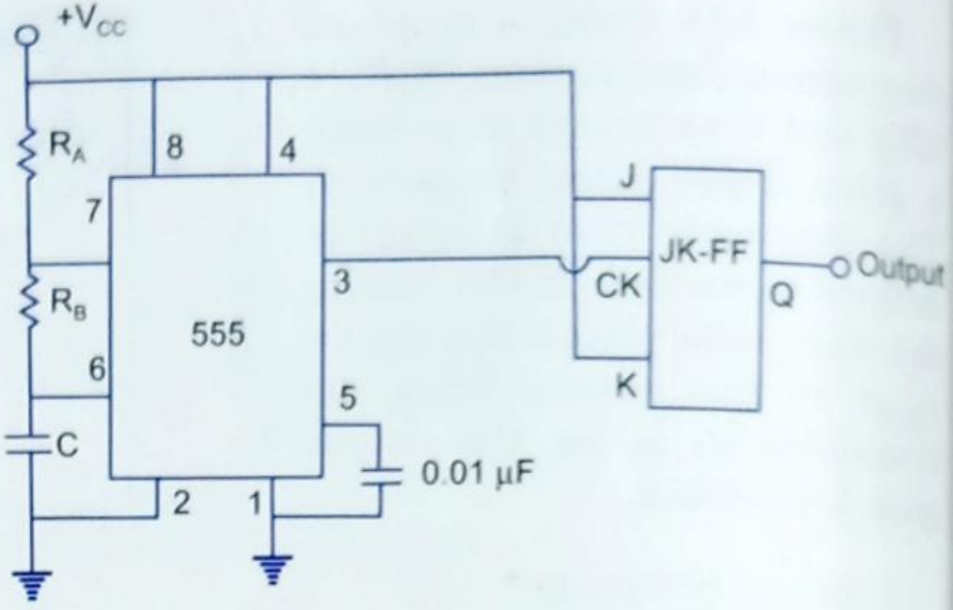

Fig. 8.20 Symmetrical waveform generator

Example 8.2

Refer Fig. 8.15. For $R_A = 6.8\ k\Omega$, $R_B = 3.3\ k\Omega$ and $C = 0.1\ \mu F$, calculate (a) t_{HIGH} (b) t_{LOW} (c) free running frequency (d) duty cycle, D.

Solution

(a) By Eq. (8.11)

$$t_{HIGH} = 0.69\,(6.8\ k\Omega + 3.3\ k\Omega)\,(0.1\ \mu F) = 0.7\ ms$$

(b) By Eq. (8.12)

$$t_{LOW} = 0.69\,(3.3\ k\Omega)\,(0.1\ \mu F) = 0.23\ ms$$

(c) $$f = \frac{1.45}{[(6.8\ k\Omega) + (2)(3.3\ k\Omega)](0.1\ \mu F)} = 1.07\ kHz$$

(d) $$D = \frac{t_{LOW}}{T} = \frac{R_B}{R_A + 2R_B}$$

$$= \frac{3.3\ k\Omega}{6.8\ k\Omega + 2(3.3\ k\Omega)} = 0.25 \text{ or, } 25\%$$