35. a) Derive the transfer function of low pass filter and plot it's frequency response.

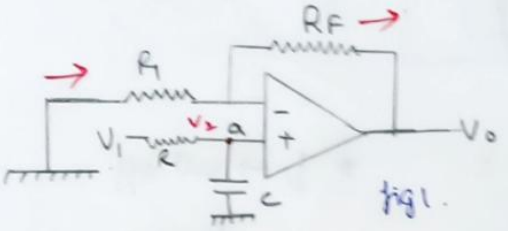


fig 1.

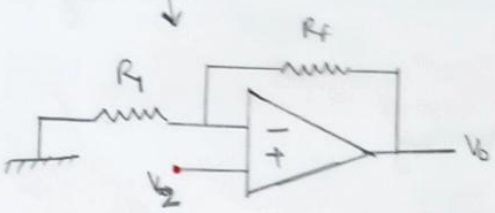


fig. 2

NOTE :- fig.2 is the same a fig.1.

$\therefore V_a = V_2$

Let the gain be A_0

from fig. 2, $A_0 = \frac{V_o}{V_2} = 1 + \frac{R_f}{R_1}$ — (1)

[non-inverting op amp]

In fig.1, applying KCL @ node a →

$\frac{V_1 - V_2}{R} = \frac{V_2}{\frac{1}{sC}}$ (current through a capacitor is $\frac{V}{1/sC}$)

$\Rightarrow \frac{V_1 - V_2}{R} = V_2 sC$

$\Rightarrow \frac{V_1}{R} = V_2 (sC + \frac{1}{R})$

$\Rightarrow \frac{V_2}{V_1} = \frac{1}{1+sRC}$ — (2)

Overall gain $\frac{V_o}{V_i}$,

$\frac{V_o}{V_i} = \frac{V_o}{V_i} \times \frac{V_2}{V_2}$ (multiplying & dividing by V_2)

$= \frac{V_o}{V_2} \times \frac{V_2}{V_i} = \left(1 + \frac{R_F}{R_1}\right) \times \left(\frac{1}{1+sRC}\right)$ $\quad 1 + \frac{R_F}{R_1} = A_0$

$\Rightarrow \frac{V_o(s)}{V_i(s)} = A_0 \times \frac{1}{1+sRC} = H(s)$ (from (1) & (2))

$\Rightarrow \boxed{h(\omega) = \frac{A_0}{1+j\omega RC}}$ (converting to time domain)

$\Rightarrow h(f) = \frac{A_0}{1+j2\pi fRC}$ $\quad (\omega = 2\pi f)$

$\Rightarrow H(jw) = \frac{A_0}{1 + j\frac{f}{f_c}}$ $\quad \left(f_c = \frac{1}{2\pi RC}\right)$

2) $$|H(j\omega)| = \frac{A_0}{\sqrt{1+\left(\frac{f}{f_c}\right)^2}}$$

@ $f=0$, $|H(j\omega)| = A_0$

* $f_c \rightarrow$ cut off frequency

@ $f=f_c$, $|H(j\omega)| = 0.707 A_0$

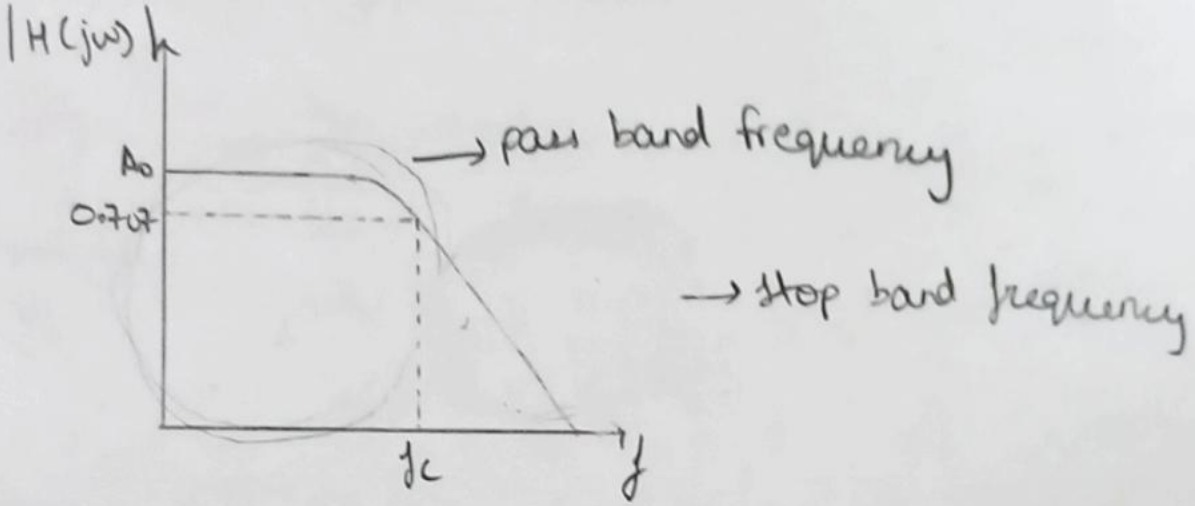
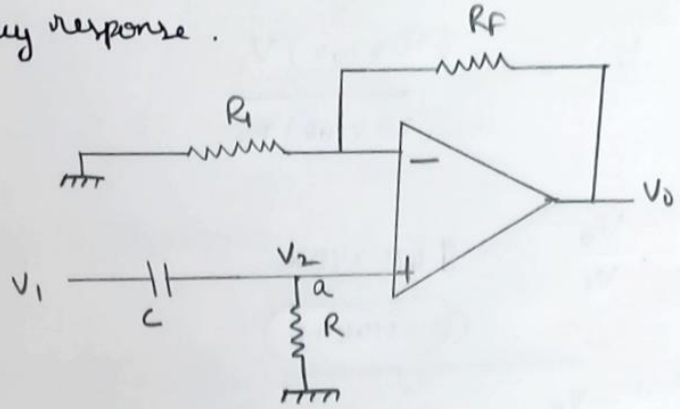


fig. 3 → FREQUENCY RESPONSE OF LOW PASS FILTER

36. a) Derive the transfer function of a high pass filter and plot its frequency response.

Soln :-



Let the pass band (or) closed loop gain be A_0.

By applying KCL @ node a, we get

$$\frac{V_1 - V_2}{1/sC} = \frac{V_2}{R}$$

$$\Rightarrow RsC(V_1 - V_2) = V_2$$

$$\Rightarrow RsC\,V_1 = V_2(1 + sRC)$$

$$\Rightarrow \frac{V_1}{V_2} = \frac{1+sRC}{sRC}$$

$$\frac{V_o}{V_1} = \frac{V_o}{V_2} \times \frac{V_2}{V_1} \Rightarrow H(s) = A_0 \times \frac{sRC}{1+sRC}$$

$$= A_0 \times \frac{j\omega RC}{1+j\omega RC} = A_0 \frac{j2\pi RCf}{1+j2\pi RCf}$$

$$\therefore H(j\omega) = \frac{A_0\, j\frac{f}{f_c}}{1 + j\frac{f}{f_c}}$$

$$\left(* f_c = \frac{1}{2\pi RC}\right)$$

* $\frac{V_o}{V_2} = A_0$

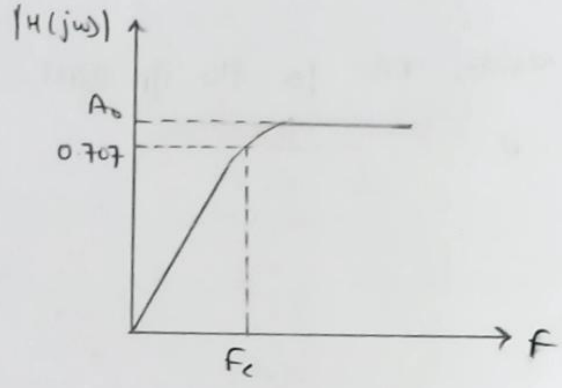
* $H(s) = \frac{V_o(s)}{V_i(s)}$

$$|H(j\omega)| = \frac{A_0 f/f_c}{\sqrt{1+(f/f_c)^2}}$$

as $f \to \infty$, $|H(j\omega)| = A_0$

when $f = f_c$, $|H(j\omega)| = \frac{A_0}{\sqrt{2}} = 0.707 A_0$

FREQUENCY RESPONSE :-



b) Design a high pass filter with a cutoff frequency of 10kHz & a pass band gain of 10.

Ans :- $A_0 = 10 = 1 + \frac{R_f}{R_1} \Rightarrow R_f = 9R_1$

$f_c = \frac{1}{2\pi RC}$

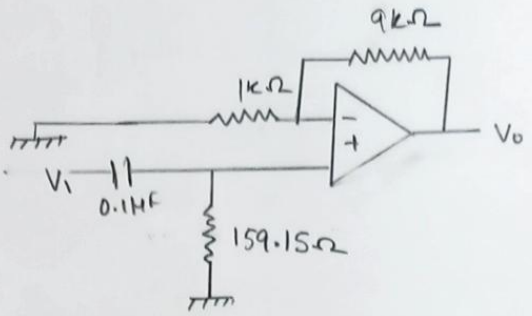
Let $C = 0.1\,\mu F$

$\Rightarrow 10 \times 10^3 \times 2\pi \times 0.1 \times 10^{-6} = \frac{1}{R}$

$\Rightarrow$ **$R = 159.15\,\Omega$**

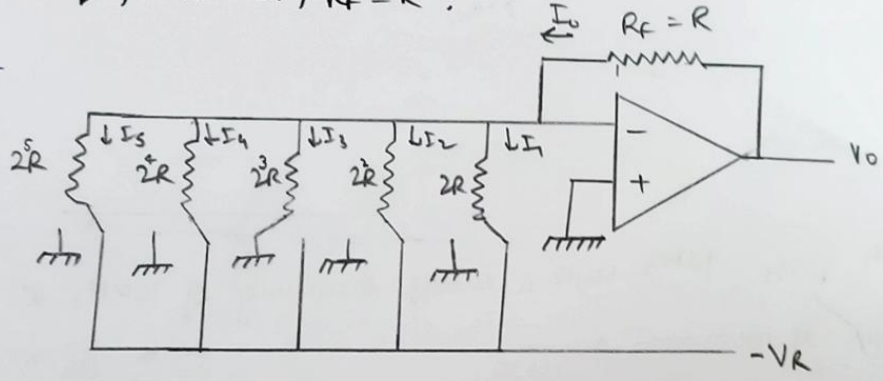
Let $R_1 = 1k\Omega$. $\Rightarrow R_F = 9k\Omega$

Ckt. diagram :-

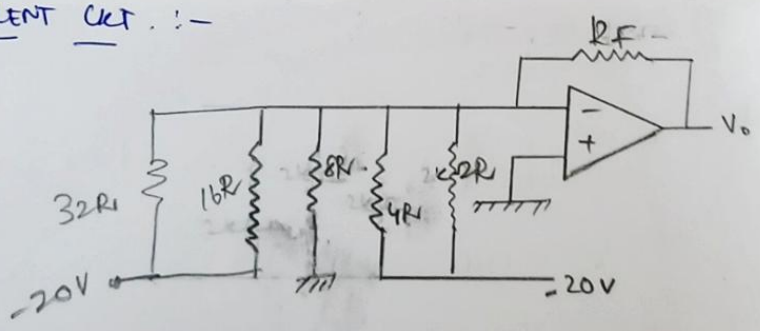


37. Design a weighted resistor DAC for the i/p 11011. Find the O/P voltage, $V_R = 20V$, $R_f = R$. Assume $R = 1k\Omega$.

Ans :-



EQUIVALENT CKT. :-



(Assume $R_f = 1k\Omega$

$\therefore 2R = 2k\Omega$)

d_1	d_2	d_3	d_4	d_5
1	1	0	1	1

$$V_o = I_o R_f$$

$$I_o = \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \dots + \frac{V_R}{2^n} d_n$$

Here, $$I_o = \frac{20}{2k}(1) + \frac{20}{2^2 k}(1) + \frac{20}{2^3 k}(0) + \frac{20}{2^4 k}(1) + \frac{20}{2^5 k}(1)$$

$$= \frac{1}{k}(16.875) = 16.875\,mA$$

$\therefore V_o = 16.875 \times 10^{-3} \times 10^3$

$= \boxed{16.875\,V}$

10.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 10.5 (a), where the switch position $d_1\, d_2\, d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 10.5 (b) and finally to Fig. 10.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R + \frac{2}{3}R} = -\frac{V_R}{4}$$

The output voltage is

$$V_o = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

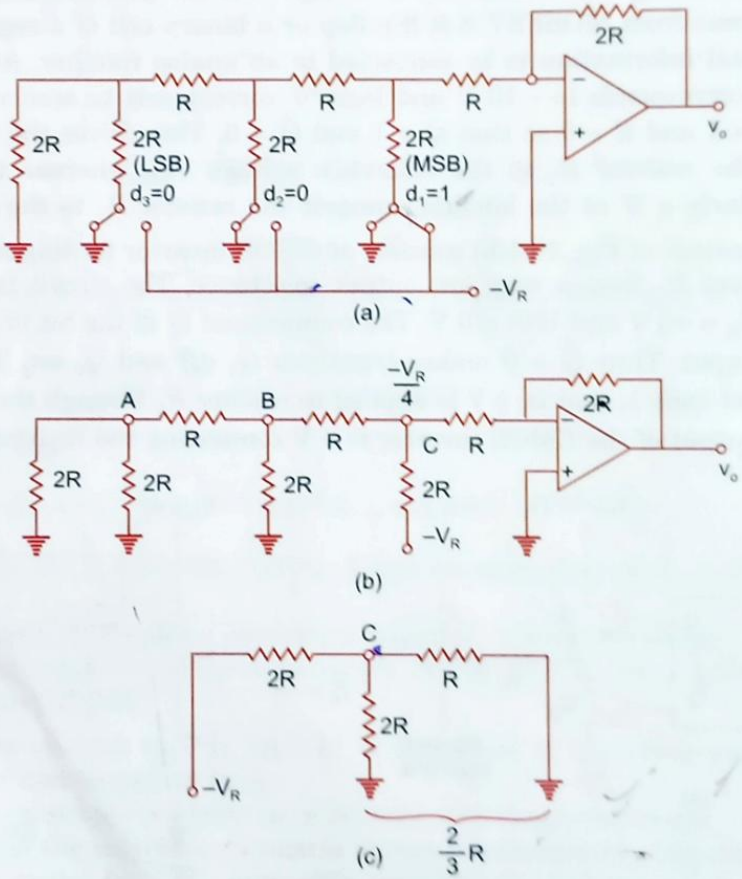


Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 6 (a). The circuit can be simplified to the equivalent form of Fig. 10.6 (b). The voltages the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion d the output voltage becomes

$$V_o = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

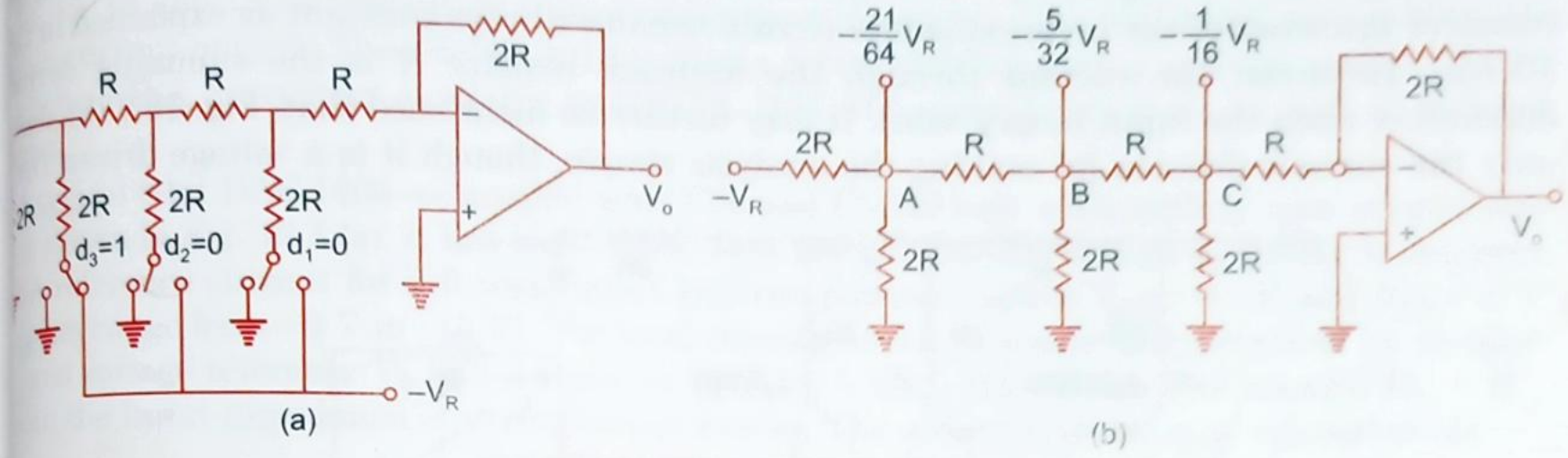


Fig. 10.6 (a) R-2R ladder DAC for switch positions 001 (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other bit binary words can be calculated.

DIRECT TYPE ADCs

10.3.1 The Parallel Comparator (Flash) A/D Converter

This is the simplest possible A/D converter. It is at the same time, the fastest and most expensive technique. Figure 10.10 (a) shows a 3-bit A/D converter. The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder). The comparator and its truth table is shown in Fig. 10.10 (b). A small amount of hysteresis is built into the comparator to resolve any problems that might occur if both inputs were of equal voltage as shown in the truth table. Coming back to Fig. 10.10 (a), at each node of the resistive divider, a comparison voltage is available. Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between the reference voltage V_R and the ground. The purpose of the circuit is to compare the analog input voltage V_a with each of the node voltages. The truth table for the flash type A/D converter is shown in Fig. 10.10 (c). The circuit has the advantage of high speed as the

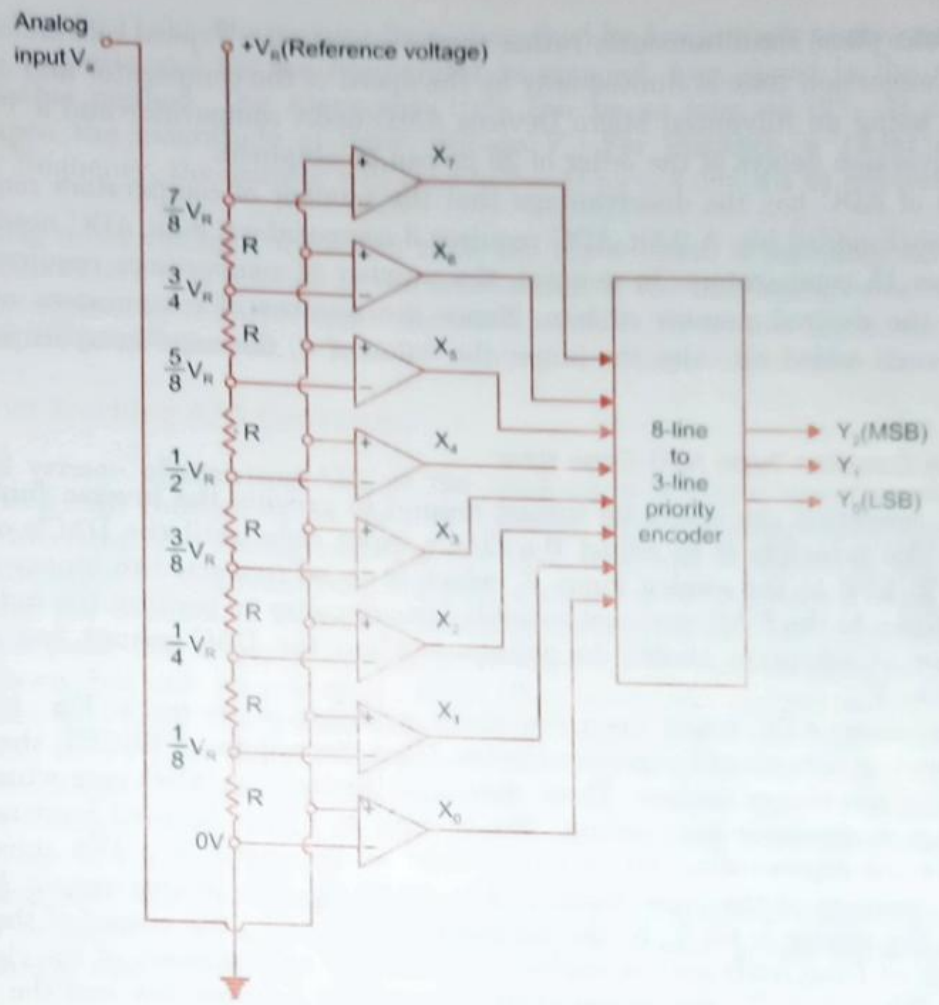


Fig. 10.10 (a) Basic circuit of a flash type A/D converter

Voltage input	*Logic output X*
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

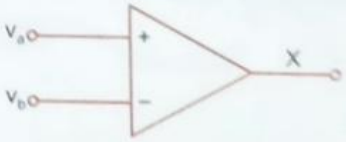


Fig. 10.10 (b) Comparator and its truth table

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Fig. 10.10 (c) Truth table for a flash type A/D converter

conversion take place simultaneously rather than sequentially. Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro Devices AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20 ns can be obtained.

This type of ADC has the disadvantage that the number of comparators required almost doubles for each added bit. A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators. In general, the number of comparators required are $2^n - 1$ where n is the desired number of bits. Hence the number of comparators approximately doubles for each added bit. Also the larger the value of n, the more complex is the priority encoder.