Module - 02

MOSFET Power Amplifiers

Power Amplifiers, Power Transistors, Classes of Amplifiers, Class A Power Amplifiers, Class B, Class AB Push-Pull Complementary Output Stages.

Functions of Power amplifiers

- to provide a low output resistance
  - so that it can deliver the signal power to the load without loss of gain and to
- maintain linearity in the output signal
  - A measure of the linearity of the output signal is the **total harmonic distortion (THD)**

Limitations of Transistors

- Maximum rated current
  - On the order of amperes
- Maximum rated voltage
  - On the order of 100 V
- Maximum rated power
  - On the order of Watts or tens of Watts
  - Related to maximum allowed temperature
    - Which in turn depends on heat removal

Comparison with Power BJTs

Table 8.1 Comparison of the characteristics and maximum ratings of a small-signal and power BJT

Parameter	Small-Signal BJT (2N2222A)	Power BJT (2N3055)	Power BJT (2N6078)
V_{CE}(max) (V)	40	60	250
I_C(max) (A)	0.8	15	7
P_D(max) (W) (at $T = 25$ °C)	1.2	115	45
β	35–100	5–20	12–70
f_T (MHz)	300	0.8	1

Characteristics of two Power MOSFETs

Parameter	2N6757	2N6792
V_{DS} (max) (V)	150	400
I_D (Max)	8	2
P_D (W)	75	20

Difference between Power BJT and MOSFET

- faster switching times,
- no second breakdown,
- stable gain and
- Response time over a wide temperature range

CLASSES OF AMPLIFIERS

Objective: • Define various classes of power amplifiers, and investigate the characteristics, including power efficiency, of a few of these amplifiers.

Some power amplifiers are classified according to the percent of time the output transistors are conducting, or "turned on."

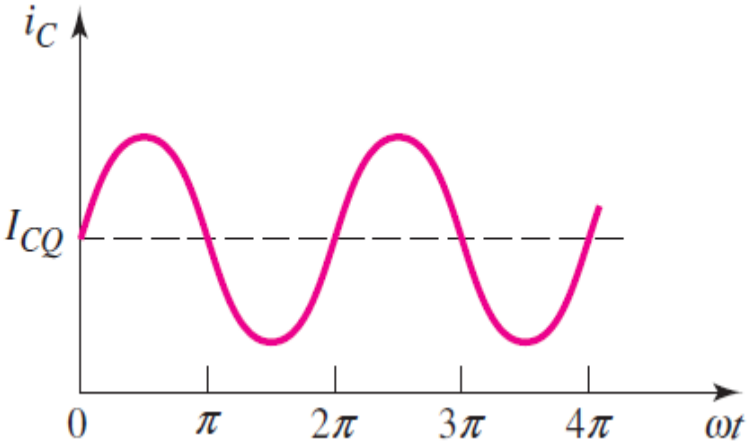
Four of the principal classifications are:
class A, class B, class AB, and class C.

In **class-A operation,** an output transistor is biased at a quiescent current *IQ* and conducts for the entire cycle of the input signal.

For **class-B operation,** an output transistor conducts for only one-half of each sine wave input cycle.

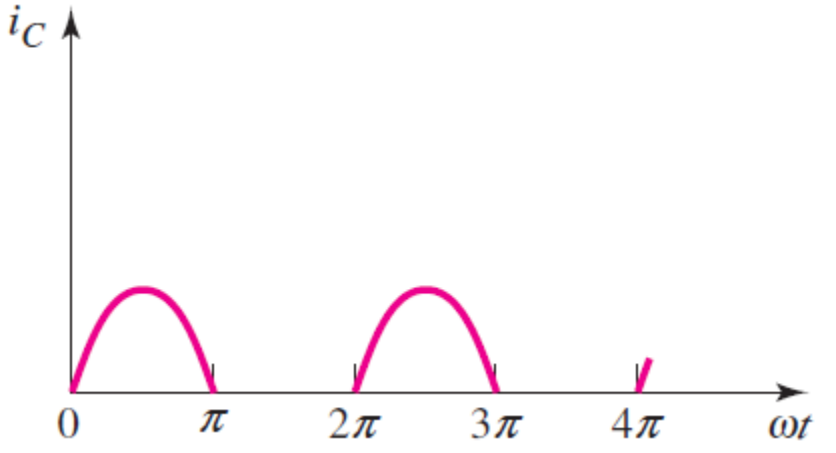
In **class-AB operation,** an output transistor is biased at a small quiescent current *IQ* and conducts for slightly more than half a cycle.

class-A amplifier



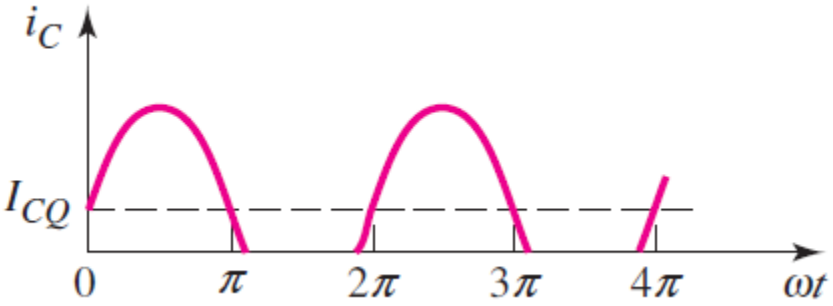
Collector current versus time characteristics

class-B amplifier



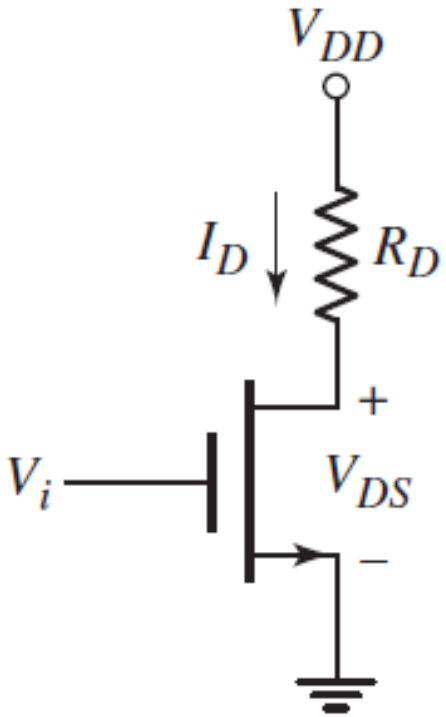
Collector current versus time characteristics

class-AB amplifier



Collector current versus time characteristics

class-A amplifier



The load line is given by

$$V_{DS} = V_{DD} - I_D R_D$$

At the transition point,

$$V_{DS}(\text{sat}) = V_{GS} - V_{TN}$$

and

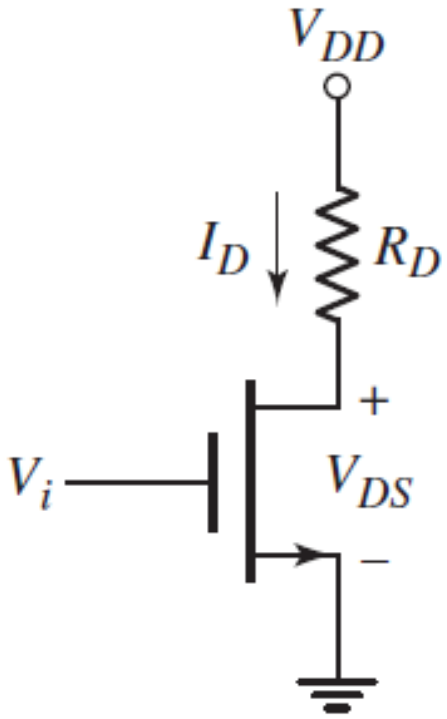
$$I_D = K_n(V_{GS} - V_{TN})^2$$

Combining these expressions, the transition point is determined from

$$V_{DS}(\text{sat}) = V_{DD} - K_n R_D V_{DS}^2(\text{sat})$$

For sinusoidal input signals, the average ac power delivered to the load is

$$= \frac{^2}{2}$$



The quiescent drain current is found to be

$$= \frac{-}{\qquad\qquad}$$

The average power supplied by the source is

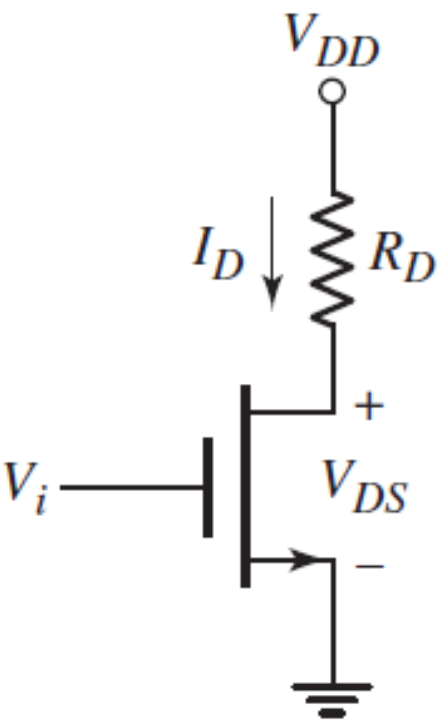
$$=$$

The power conversion efficiency

$$= \frac{}{\quad}$$

Problem : Calculate the actual efficiency of a class-A output stage.

The circuit parameters are $V_{DD} = 10$ V and $R_D = 5$ kΩ, and the transistor parameters are: $K_n = 1$ mA/V^2, $V_{TN} = 1$ V, and $\lambda = 0$. Assume the output voltage swing is limited to the range between the transition point and $v_{DS} = 9$ V, to minimize nonlinear distortion.



Solution: The load line is given by

$$V_{DS} = V_{DD} - I_D R_D$$

At the transition point, we have

$$V_{DS}(\text{sat}) = V_{GS} - V_{TN}$$

and

$$I_D = K_n(V_{GS} - V_{TN})^2$$

Combining these expressions, the transition point is determined from

$$V_{DS}(\text{sat}) = V_{DD} - K_n R_D V_{DS}^2(\text{sat})$$

$$(1)(5)V_{DS}^2(\text{sat}) + V_{DS}(\text{sat}) - 10 = 0$$

which yields

$$V_{DS}(\text{sat}) = 1.32\,\text{V}$$

To obtain the maximum symmetrical swing under the conditions specified, the Q-point midway between $V_{DS} = 1.32$ V and $V_{DS} = 9$ V, or

$$V_{DSQ} = 5.16\,\text{V}$$

The maximum ac component of voltage across the load resistor is then

$$v_r = 3.84 \sin \omega t$$

and the average power delivered to the load is

$$\bar{P}_L = \frac{1}{2} \cdot \frac{(3.84)^2}{5} = 1.47\,\text{mW}$$

The quiescent drain current is found to be

$$I_{DQ} = \frac{10 - 5.16}{5} = 0.968\,\text{mA}$$

The average power supplied by the V_{DD} source is

$$\bar{P}_S = V_{DD} I_{DQ} = (10)(0.968) = 9.68\,\text{mW}$$

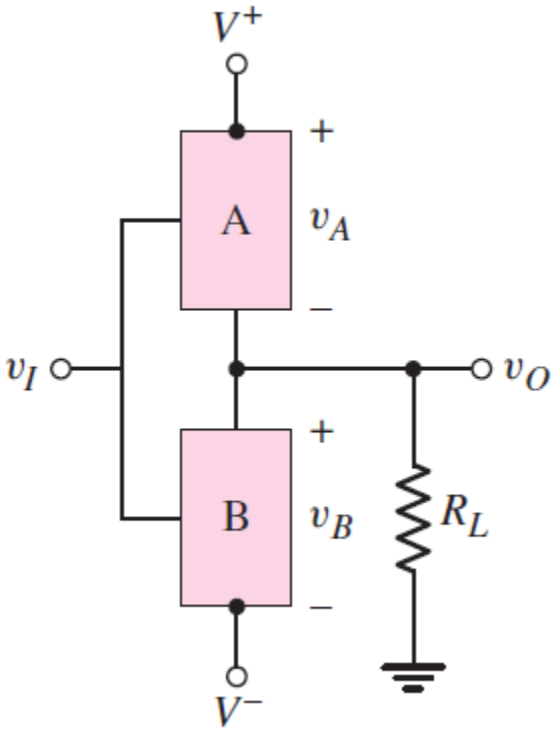
and the power conversion efficiency,

$$\eta = \frac{\bar{P}_L}{P_S} = \frac{1.47}{9.68} \Rightarrow 15.2\%$$

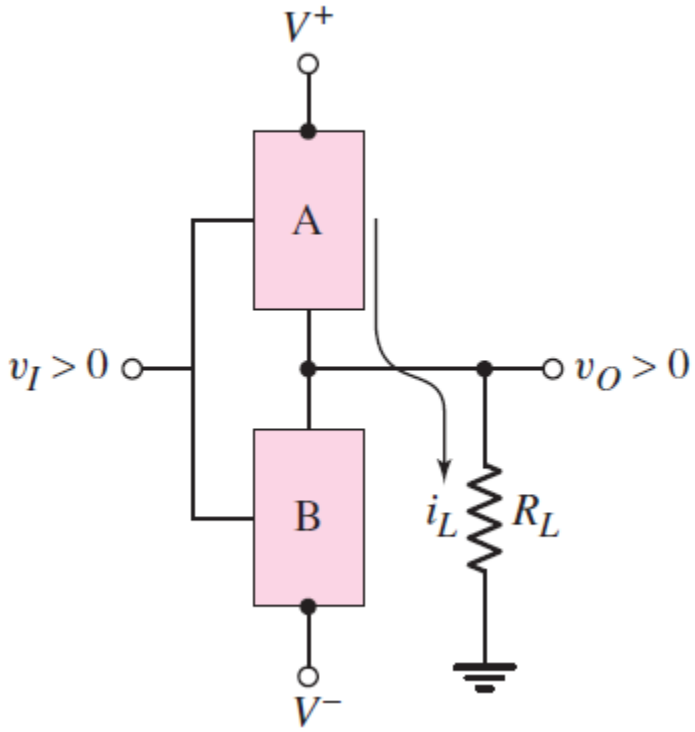
Comment: By limiting the swing in the drain–source voltage, to avoid nonsaturation and cutoff and the resulting nonlinear distortion, we reduce the output stage power conversion efficiency considerably, compared to the theoretical maximum possible value of 25 percent for the standard class-A amplifier.

class-B amplifier

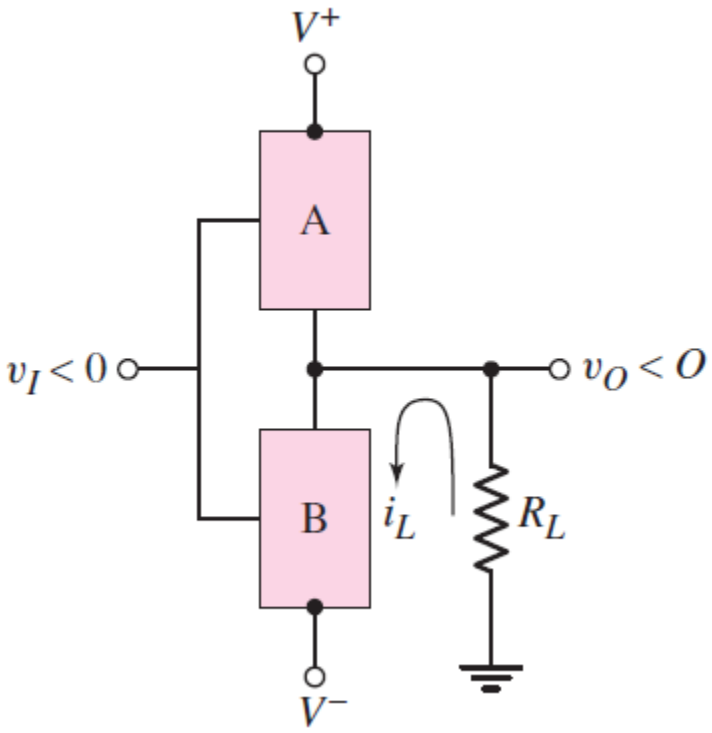
This circuit is called a **complementary push–pull** output stage. Transistor *NMOS* conducts during the positive half of the input cycle, and *PMOS* conducts during the negative half-cycle. The transistors do not both conduct at the same time.



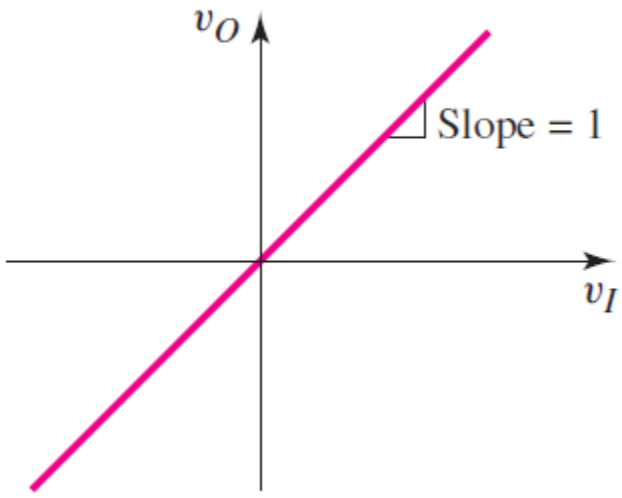
Idealized class-B output stage with complementary pair, A and B, of electronic devices



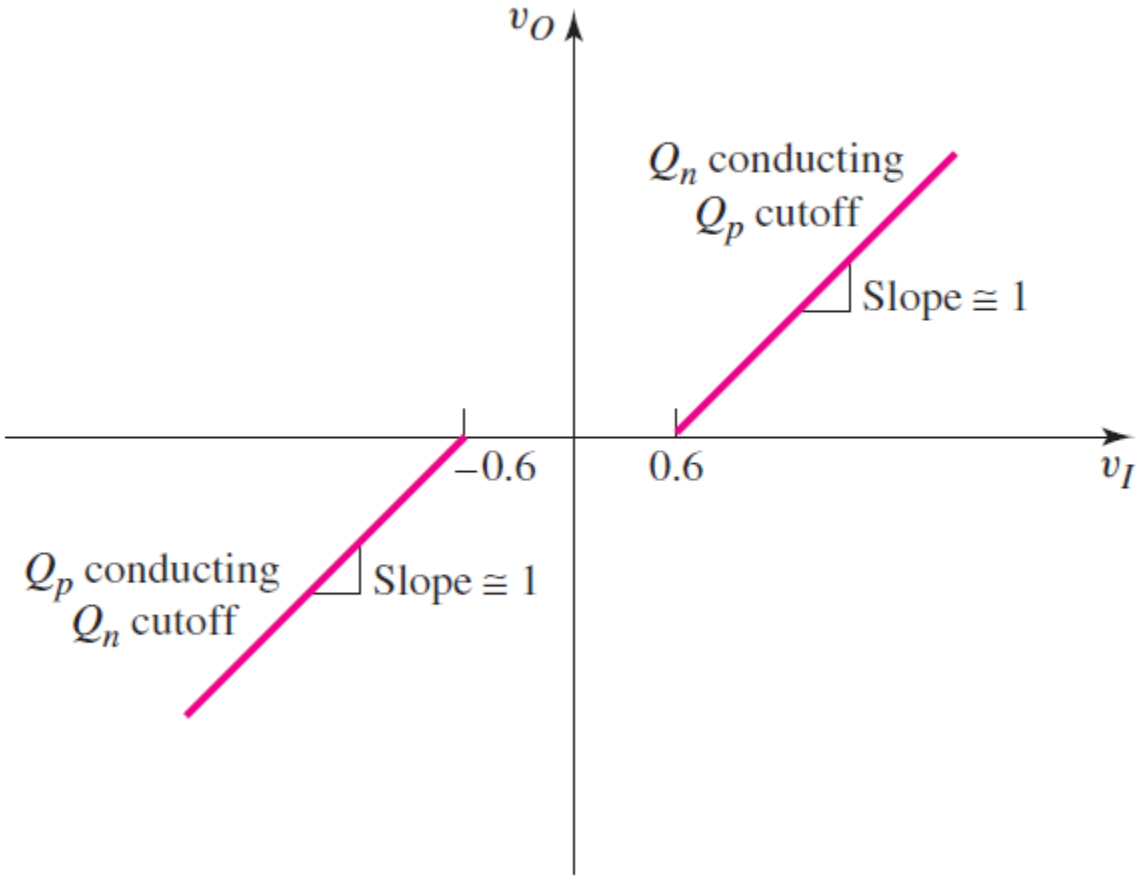
Device A turns on for > 0, supplying current to the load



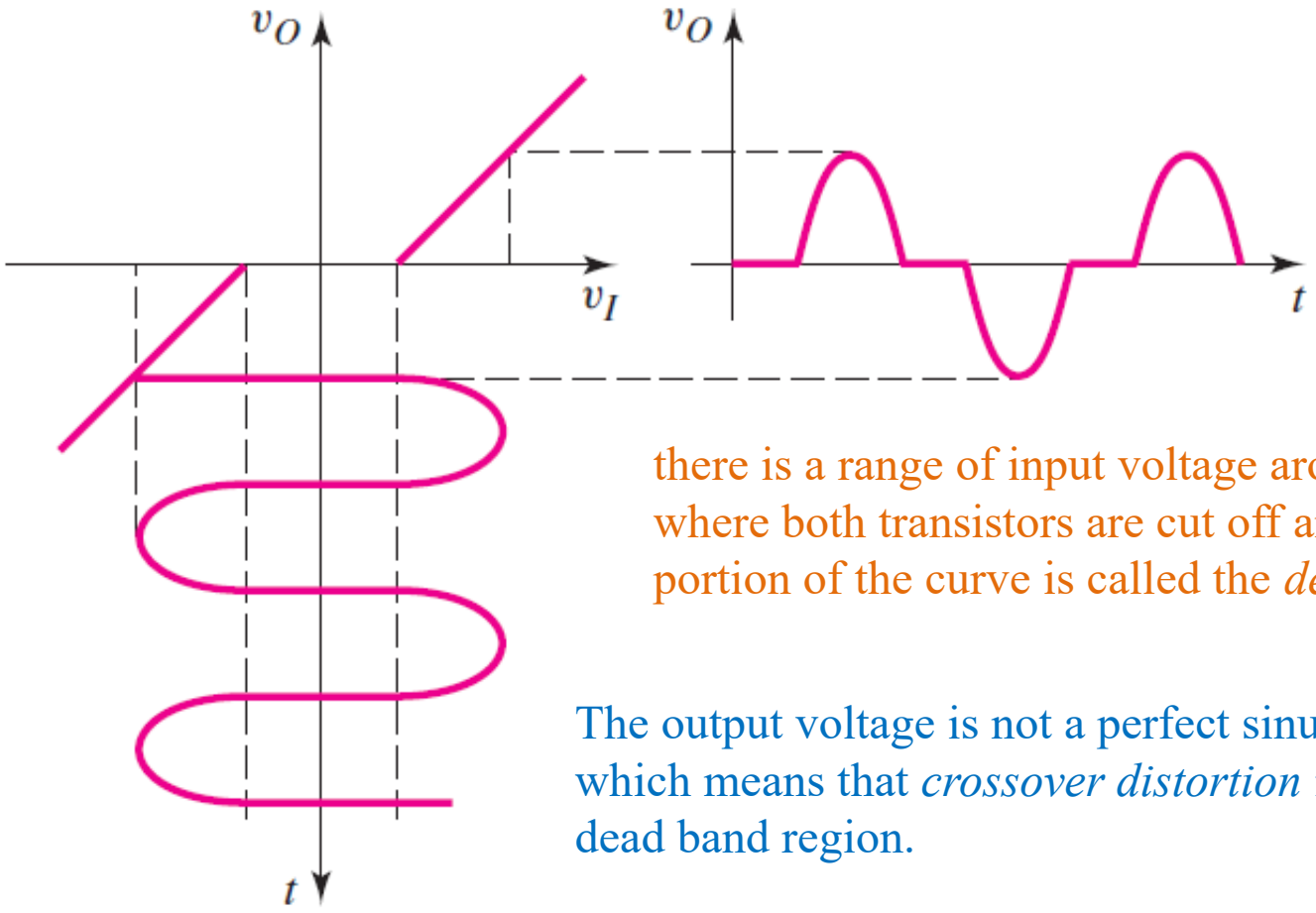
device B turns on for < 0, sinking current from the load



ideal voltage transfer characteristics



Voltage transfer characteristics of basic complementary push–pull output stage

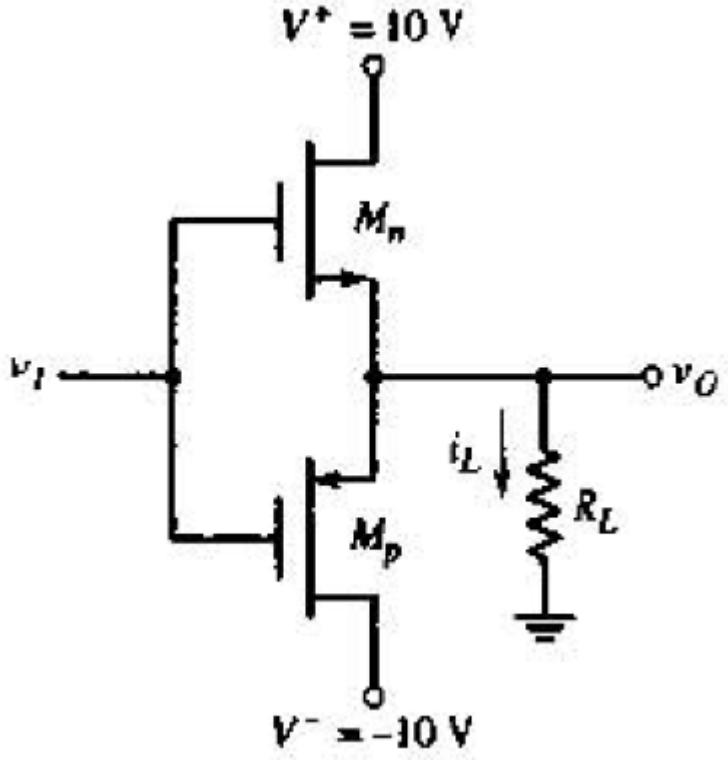


there is a range of input voltage around zero volts where both transistors are cut off and is zero. This portion of the curve is called the *dead band*.

The output voltage is not a perfect sinusoidal signal, which means that *crossover distortion* is produced by the dead band region.

Crossover distortion of basic complementary push–pull output stage

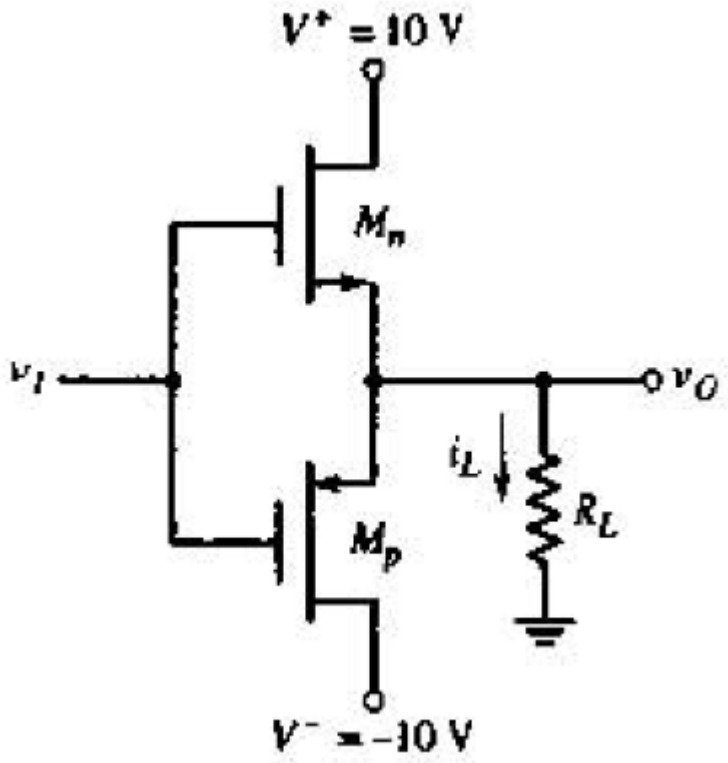
Crossover distortion can be virtually eliminated by biasing both *PMOS* and *NMOS* with a small quiescent drain current when is zero. The crossover distortion effect can also be minimized with an op-amp used in a feedback configuration.



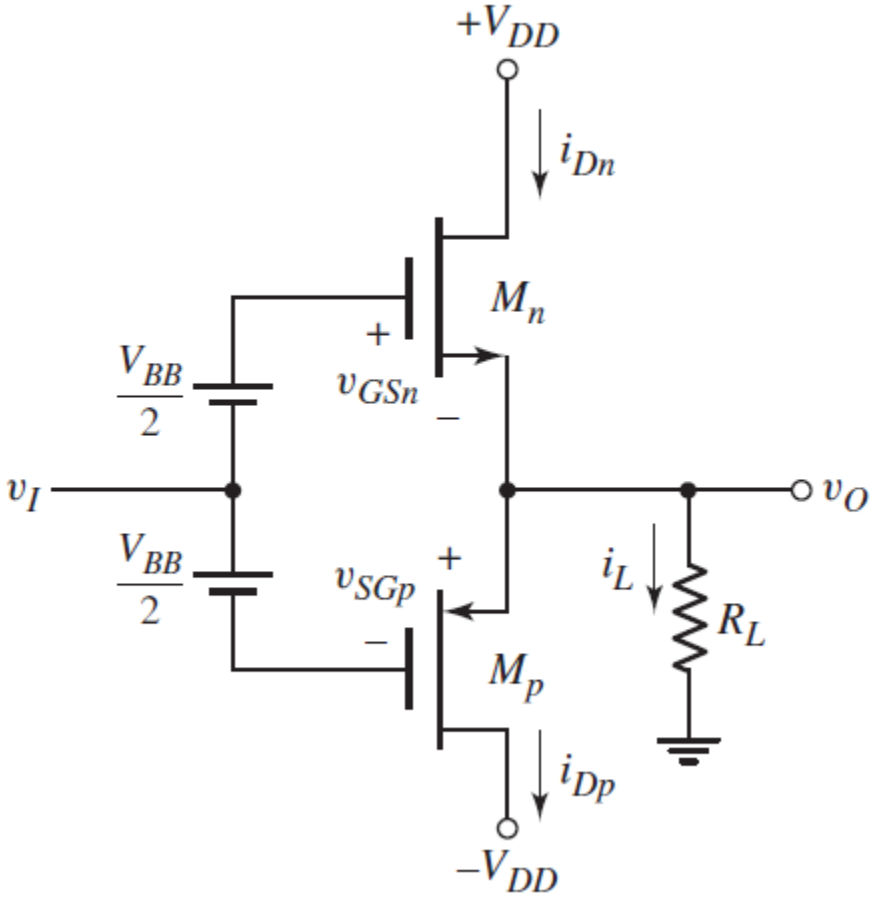
Derivation

Refer class notes

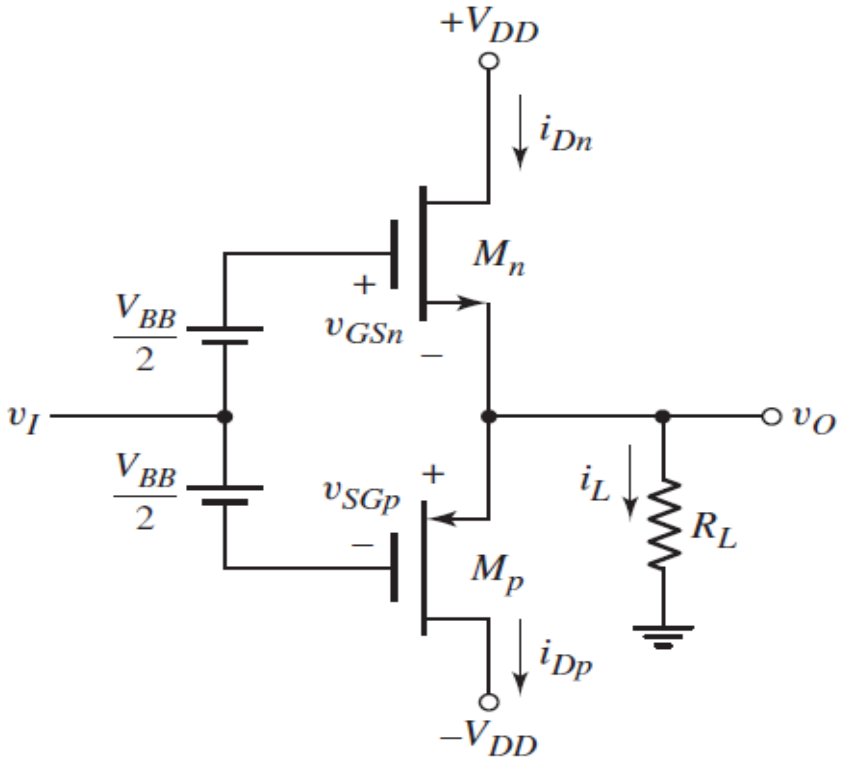
Consider the class B output stage with complementary MOSFET. The transistor parameters are and . Let (a) Find the maximum output voltage such that remains biased in the saturation region. What are the corresponding values of for this condition? (b) Determine the conversion efficiency for a symmetrical sine-wave output signal with the peak value found in part (a).



MOSFET class-AB output stage



As v_I increases, the voltage at the gate of M_n increases and v_O increases. Transistor M_n operates as a source follower, supplying the load current to R_L. Since i_{Dn} must increase to supply the load current, v_{GSn} must also increase. Assuming V_{BB} remains constant, an increase in v_{GSn} implies a decrease in v_{SGp} and a resulting decrease in i_{Dp}. As v_I goes negative, the voltage at the base of M_p decreases and v_O decreases. Transistor M_p then operates as a source follower, sinking current from the load.



The output voltage is

=

The input voltage for positive is

$$v_I = v_O + v_{GSn} - \frac{V_{BB}}{2}$$

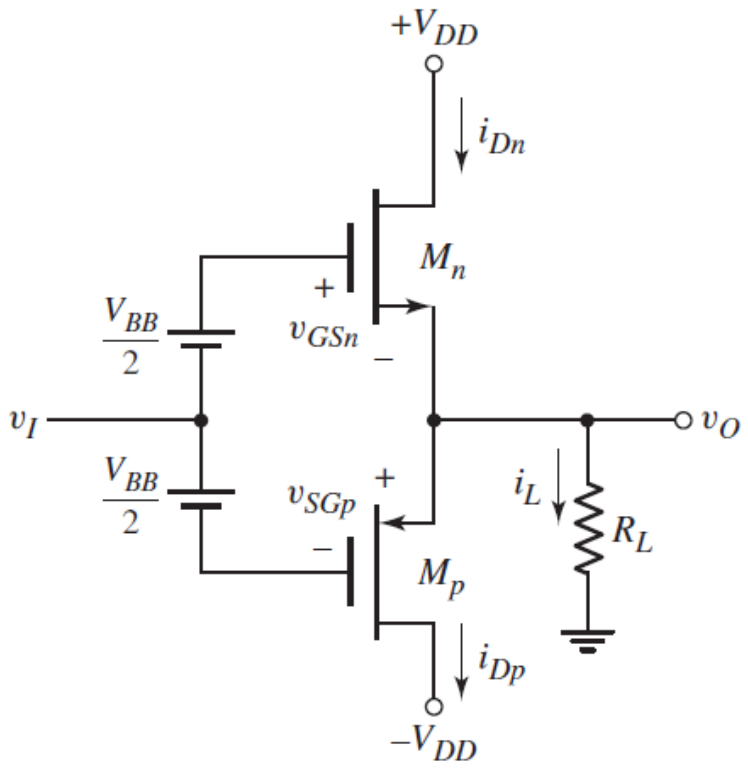
$$v_{GSn} = \sqrt{\frac{i_{Dn}}{K}} + |V_T|$$

The source-to-gate voltage of is

$$v_{SGp} = V_{BB} - V_{GSn}$$

$$i_{Dn} = i_{Dp} = I_{DQ} = K\left(\frac{V_{BB}}{2} - |V_T|\right)^2$$

Problem : Determine the required biasing in a MOSFET class-AB output stage.



The parameters are $V_{DD} = 10$ V and $R_L = 20\ \Omega$. The transistors are matched, and the parameters are $K = 0.20$ A/V^2 and $|V_T| = 1$ V. The quiescent drain current is to be 20 percent of the load current when $v_O = 5$ V.

Solution: For $v_O = 5$ V,

$$i_L = 5/20 = 0.25 \text{ A}$$

Then, for $I_Q = 0.05$ A when $v_O = 0$, we have

$$I_{DQ} = 0.05 = K\left(\frac{V_{BB}}{2} - |V_T|\right)^2 = (0.20)\left(\frac{V_{BB}}{2} - 1\right)^2$$

which yields

$$V_{BB}/2 = 1.50 \text{ V}$$

The input voltage for v_O positive is

$$v_I = v_O + v_{GSn} - \frac{V_{BB}}{2}$$

For $v_O = 5$V and $i_{Dn} \cong i_L = 0.25$ A, we have

$$v_{GSn} = \sqrt{\frac{i_{Dn}}{K}} + |V_T| = \sqrt{\frac{0.25}{0.20}} + 1 = 2.12 \text{ V}$$

The source-to-gate voltage of M_p is

$$v_{SGp} = V_{BB} - V_{GSn} = 3 - 2.12 = 0.88\,\text{V}$$

which means that M_p is cut off and $i_{Dn} = i_L$. Finally, the input voltage is

$$v_I = 5 + 2.12 - 1.5 = 5.62\,\text{V}$$

Comment: Since $v_I > v_O$, the voltage gain of this output stage is less than unity, as expected.