VIT Vellore Institute of Technology

Reg. No. : 21BEC1514

Final Assessment Test (FAT) – November/December 2022

Programme	**B.Tech.**	Semester	**Fall Semester 2022-23**
Course Title	**ANALOG CIRCUITS**	Course Code	**BECE206L**
Faculty Name	**Prof. Sangeetha R G**	Slot	**C2+TC2**
		Class Nbr	**CH2022231001118**
Time	**3 Hours**	Max. Marks	**100**
If any data is missing assume and justify			

SECTION A (7 X 10 Marks)
Answer All questions

1. The Common-Emitter bias configuration is shown in Figure.1 **[10]**

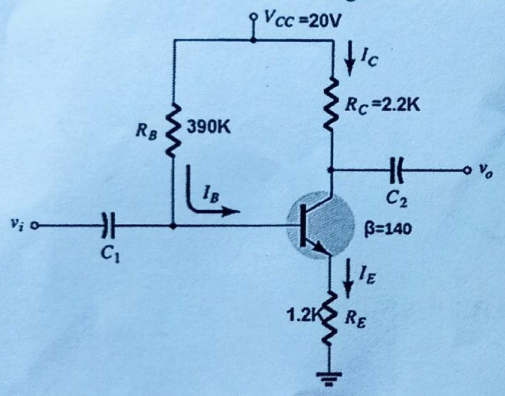

Figure. 1 Common-Emitter bias circuit

(a) Find R_i, R_o, and A_v considering early voltage $V_A=\infty$, (b) Repeat part (a) for early voltage V_A=50 V.

2. For the transistor in the circuit shown in Figure. 2, the nominal parameter values are V_{TN} = 1 V and K_n = 0.5 mA/V^2. **[10]**

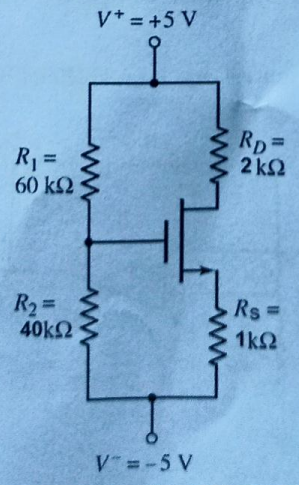

Figure 2. Voltage divider MOSFET Circuit

(a) Determine the quiescent values V_{GSQ}, I_{DQ}, and V_{DSQ}. (b) Determine the range in I_D and V_{DS} values for a +5% variation in V_{TN} and K_n.

3. For a class B amplifier providing a 20 V peak-peak signal to a 16 Ω load (speaker) and a power supply of V_{DD} = 30 V. **[10]**

Determine the

(a) Input power **(2.5 Marks)**

(b) Output power **(2.5 Marks)**

(c) Power efficiency **(2.5 Marks)**

(d) Power dissipated by heat **(2.5 Marks)**

4. (a) Sketch the basic MOSFET two-transistor current mirror and explain the operation. **(5 marks)** **[10]**

(b) Sketch a MOSFET cascode current mirror circuit and discuss the advantages of this design. **(5 marks)**

5. (a) Determine a circuit that is not stable in either state that utilizes timer IC. Briefly discuss the functionality. **(5 Marks)** **[10]**

(b) Derive the expression of the duty cycle for the above circuit **(5 Marks)**

6. The inverting summer amplifier is given in Figure 3. **[10]**

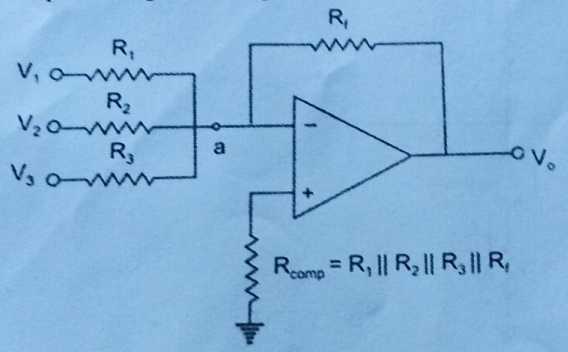

Figure 3

a) Derive the expression of output voltage in terms of input voltages V_1, V_2, and V_3 for the given circuit. **(6 marks)**

b) For the special case of R_1=R_2=R_3=R_f, what will be the output voltage in terms of input voltages? **(2 marks)**

c) For the special case of R_1=R_2=R_3=3R_f, what will be the output voltage in terms of input voltages? **(2 marks)**

7. A Non-inverting amplifier shown in Figure 4, has R_1 = 1kΩ and R_f = 8kΩ. This opamp has V_{ios}=10mV; I_B=400nA and I_{os}=50nA. **[10]**

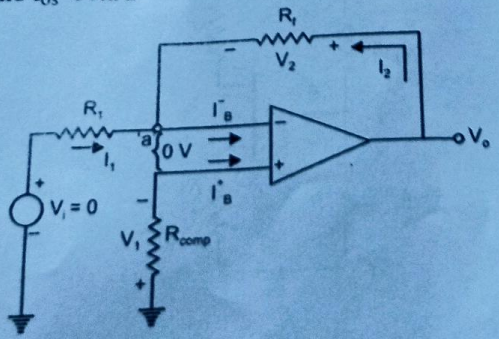

Figure 4

a) Find maximum output offset voltage due to V_{ios} and I_B **(4 marks)**

b) Calculate the value of R_{comp} needed to reduce the effect of I_B **(2 marks)**

C) Calculate max output offset voltage if R_{comp} calculated in (b) is connected in the circuit **(4 marks)**

SECTION B (2 X 15 Marks)

Answer All questions

8. (a) Explain the RC Phase shift oscillator with a neat circuit diagram and derive its frequency of oscillation. Also, design an RC phase shift oscillator so that f_o = 500 Hz. Assume C=1 μF **(7 marks)** **[15]**

(b) (i) Design a first-order high pass filter at a cut-off frequency of 1 kHz with a pass band gain of 2. **(4 marks)**

(ii) Plot the frequency response of the filter designed in part b(i). **(4 marks)**

9. Explain the function of a three-bit R-2R ladder digital to analog converter (DAC) with the necessary diagram and derive the expression for the output voltage. **[15]**