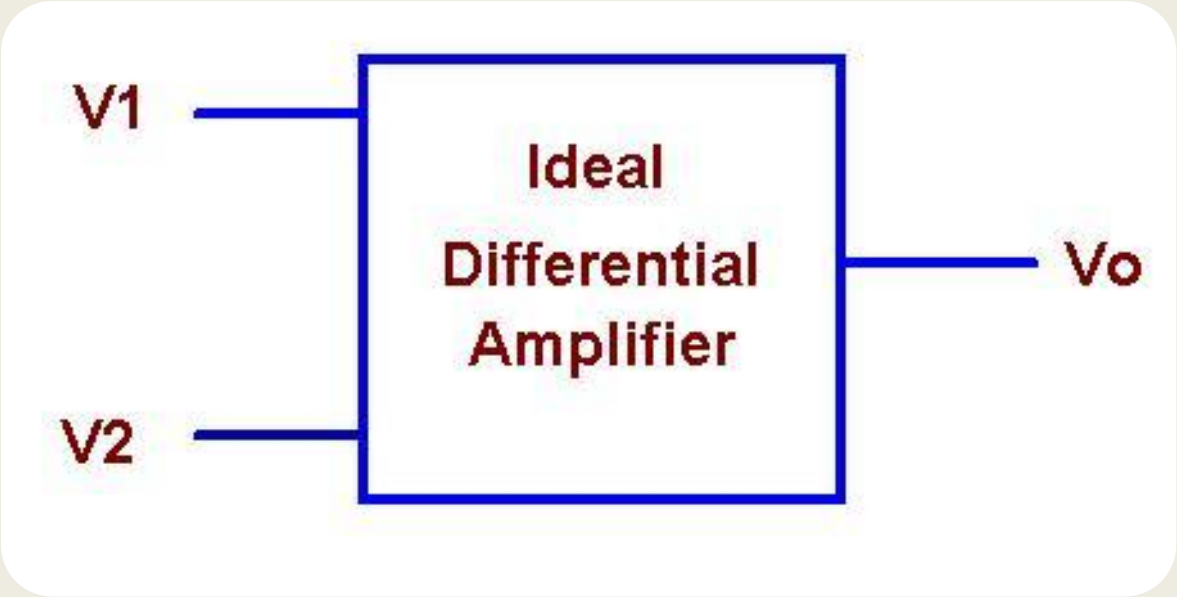
Differential Amplifier



Differential Amplifier

1. The differential amplifier amplifies the difference between two input voltage signals
2. If V_1 & V_2 are two input signals wrt ground & V_o is the output voltage then

The ideal output voltage given as

$$\mathbf{V_o \alpha (V_1 - V_2) \text{ Or } V_o = A_{vol}(V_1 - V_2)}$$

A_{vol} is called the **open loop voltage Gain**

Generally in ideal case:

if **V1=V2** $\quad \mathbf{(V_1 - V_2) = 0}$

if **V1≠V2** $\quad \mathbf{(V_1 - V_2) \neq 0}$

Differential Amplifier

But Practically speak:

Differential mode input voltage as $V_d = V_1 - V_2$ (Signal of Interest)

Common mode signal component

(Typically reference level or noise level, not desired)

$$v_{cm} = \frac{v_1 + v_2}{2}$$

The circuit which amplifies the difference between the two input signals is called **differential Amplifier**

We can write the output voltage in the general form

$$V_o = A_d V_d + A_{cm} V_{cm}$$

Performance parameters:

The ability of a differential amplifier to reject a common-mode signal is described in terms of the common-mode rejection ratio (CMRR). The CMRR is a figure of merit for the diff-amp and is defined as

$$\text{CMRR} = \left| \frac{A_d}{A_{cm}} \right|$$

For an ideal diff-amp, Acm = 0 and CMRR=∞. Usually, the CMRR is expressed in decibels, as follows:

$$\text{CMMR}_{\text{dB}} = 20 \log_{10} \left| \frac{A_d}{A_{cm}} \right|$$

Applications

- Basic building block in many Analog circuits
- High speed switching circuits
- Operational Amplifier-Many electronic Applications
- Integrated circuits

Essential Formulas

Region	NMOS	PMOS
Saturation	$v_{DS} \geq v_{DS}(\text{sat})$ $i_D = K_n[v_{GS} - V_{TN}]^2$	$v_{SD} \geq v_{SD}(\text{sat})$ $i_D = K_p[v_{SG} + V_{TP}]^2$
Transition Point	$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$	$v_{SD}(\text{sat}) = v_{SG} + V_{TP}$

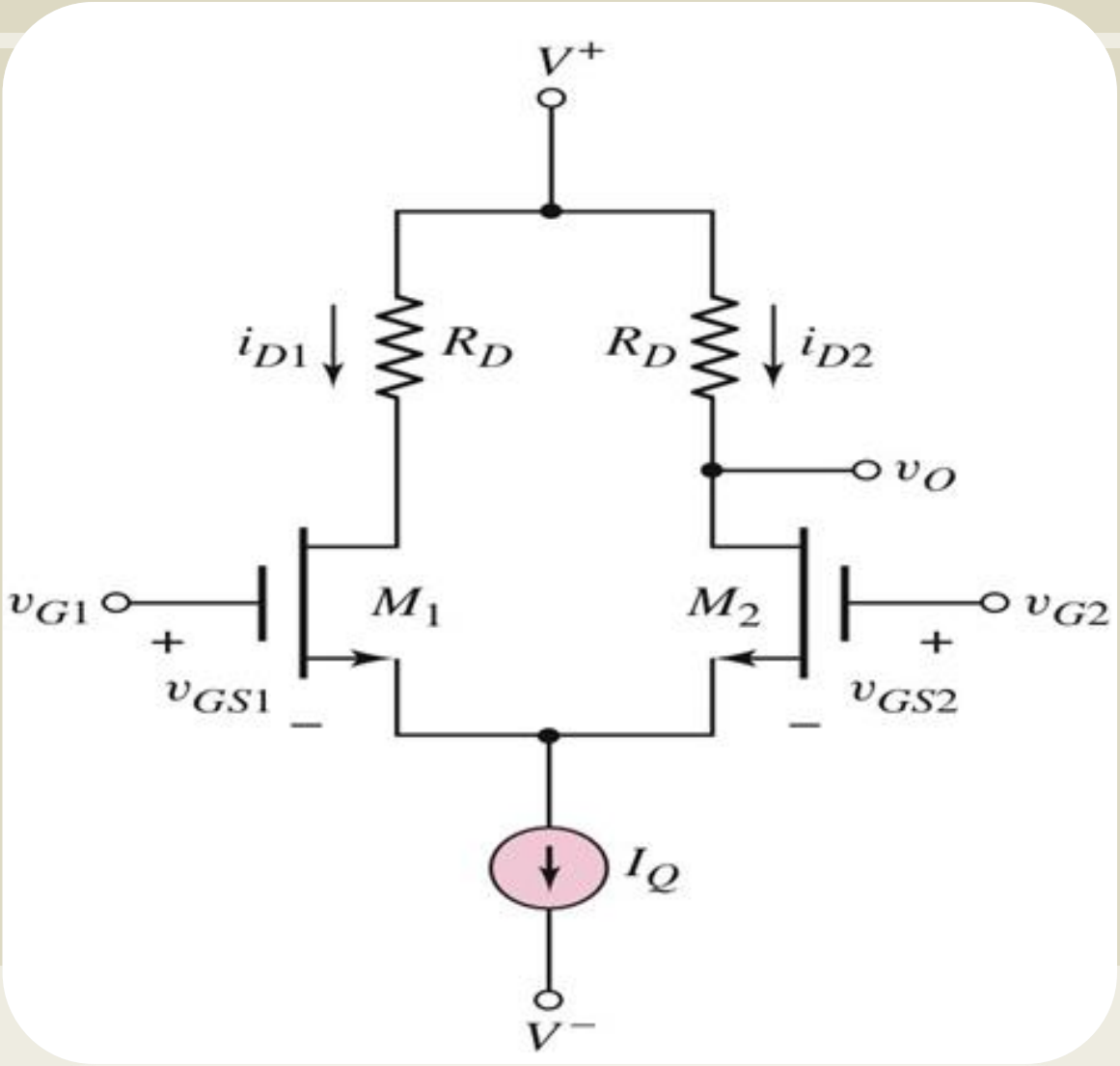
$$K_n = \frac{\mu_n C_{ox} W}{2L} = \frac{k_n'}{2} \cdot \frac{W}{L}$$

$$K_p = \frac{\mu_p C_{ox} W}{2L} = \frac{k_p'}{2} \cdot \frac{W}{L}$$

$$C_{ox} = \varepsilon_{ox} / t_{ox}$$

μ_n, μ_p	Mobility of electrons, holes
ε_{ox}	Oxide permittivity
t_{ox}	Oxide thickness
W, L	Channel Width, Length
$k_n' = \mu_n C_{ox}$ $k_p' = \mu_p C_{ox}$	Process conduction parameter (provided by manufacturer)

MOSFET Differential Amplifier (DC Analysis)



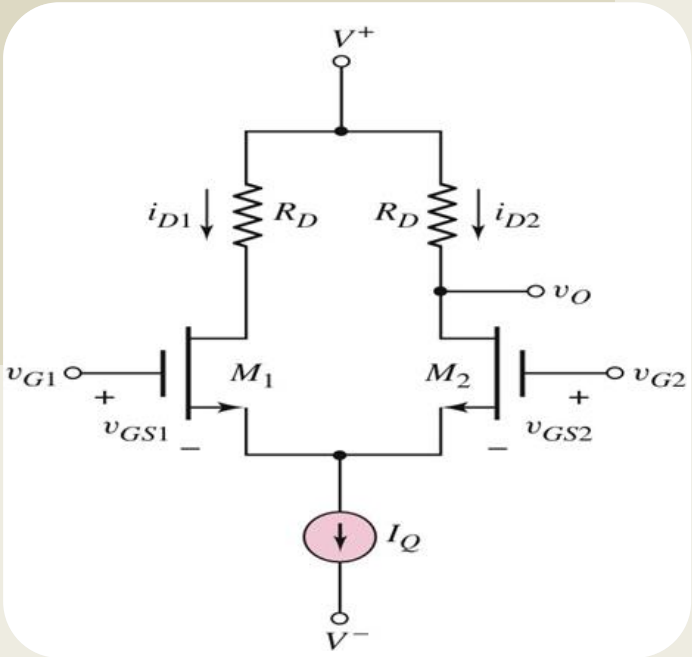
with matched transistors *M1* and *M2 biased with a constant current IQ.*
***We assume that M1 and M2 are always* biased in the saturation region.**

Two matched MOS transistors (M1 and M2) are joined
Same Technology:Vth,L,W.

Same: μ,Cox, and k’

Two circuits joints symmetrically

Same Load RD
Source Terminals Joined
Equal gate bias(vG1,vG2)(Zero)



Device biased using constant current source IQ

DC Transfer characteristics

Assume M1 and M2 are matched and neglecting their output resistances

$$i_{D1} = K_n \left(v_{GS1} - V_{TN} \right)^2$$

$$i_{D2} = K_n \left(v_{GS2} - V_{TN} \right)^2$$

Taking square roots and subtracting

$$\sqrt{i_{D1}} - \sqrt{i_{D2}} = \sqrt{K_n} \left(v_{GS1} - v_{GS2} \right) = \sqrt{K_n} . v_d$$

where $v_d = v_{G1} - v_{G2} = v_{GS1} - v_{GS2}$

If $vd > 0$,

then $v_{G1} > v_{G2}$ *and* $v_{GS1} > v_{GS2}$ *which implies that* $i_{D1} > i_{D2}$

$$i_{D1} + i_{D2} = I_Q$$

$$\left(\sqrt{i_{D1}} - \sqrt{I_Q - i_{D1}}\right)^2 = K_n v^2{}_d$$

$$\left(\sqrt{i_{D1}}\right)^2 + \left(\sqrt{I_Q - i_{D1}}\right)^2 - 2\sqrt{i_{D1}}\sqrt{I_Q - i_{D1}} = K_n v^2{}_d$$

$$i_{D1} + I_Q - i_{D1} - 2\sqrt{i_{D1}}\sqrt{I_Q - i_{D1}} = K_n v^2{}_d$$

$$I_Q - K_n v^2{}_d = 2\sqrt{i_{D1}\left(I_Q - i_{D1}\right)}$$

$$\frac{1}{2}\left(I_Q - K_n v^2{}_d\right) = \sqrt{i_{D1}\left(I_Q - i_{D1}\right)}$$

Taking square on both sides

$$\left(\frac{1}{2}\left(I_Q - K_n v^2{}_d\right)\right)^2 = \left(\sqrt{i_{D1}\left(I_Q - i_{D1}\right)}\right)^2$$

$$i_{D1}\left(I_Q - i_{D1}\right) = \frac{1}{4}\left(I_Q - K_n v^2{}_d\right)^2$$

$$i_{D1} I_Q - i_{D1}{}^2 = \frac{1}{4}\left(I_Q - K_n v^2{}_d\right)^2$$

$$i_{D1}{}^2 - i_{D1} I_Q + \frac{1}{4}\left(I_Q - K_n v^2{}_d\right)^2 = 0$$

Applying the quadratic formula, rearranging terms, and noting that $i_{D1} > I_Q/2$ and $v_d > 0$, we obtain

Applying the quadratic formula, rearranging terms, and noting that $i_{D1} > I_Q/2$ and $v_d > 0$, we obtain

$$i_{D1} = \frac{I_Q}{2} + \sqrt{\frac{K_n I_Q}{2}}.v_d\sqrt{1-\left(\frac{K_n}{2I_Q}\right)v_d^2}$$

Using Eq.(5)

$$i_{D2} = \frac{I_Q}{2} - \sqrt{\frac{K_n I_Q}{2}}.v_d\sqrt{1-\left(\frac{K_n}{2I_Q}\right)v_d^2}$$

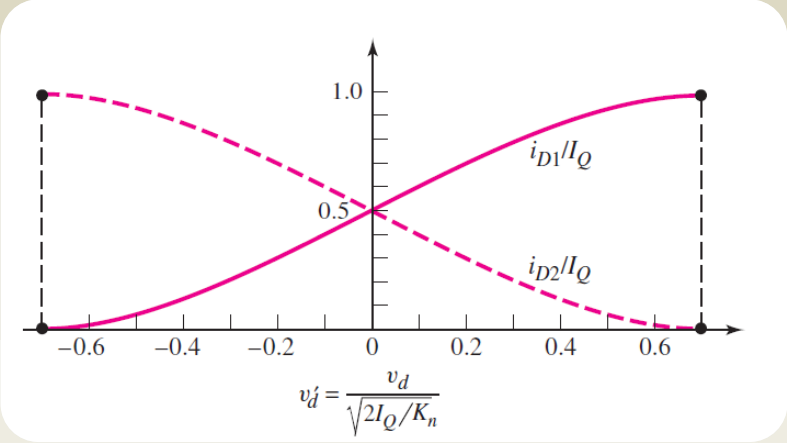
$$\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$$

The normalized drain currents are

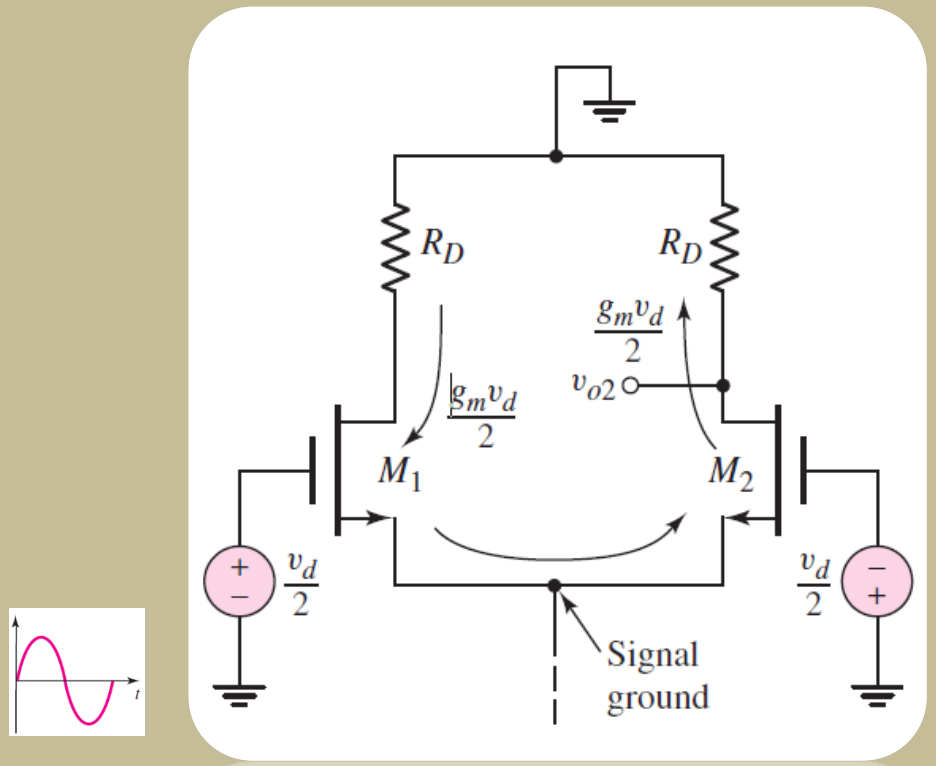
$$\frac{i_{D1}}{I_Q} = \frac{1}{2} + \sqrt{\frac{K_n}{2I_Q}}.v_d\sqrt{1-\left(\frac{K_n}{2I_Q}\right)v_d^2}$$

$$\frac{i_{D2}}{I_Q} = \frac{1}{2} - \sqrt{\frac{K_n}{2I_Q}}.v_d\sqrt{1-\left(\frac{K_n}{2I_Q}\right)v_d^2}$$

These equations describe the dc transfer characteristics for this circuit. They are plotted in Figure as a function of a normalized differential input voltage $vd/\sqrt{(2I_Q/K_n)}$



The ac equivalent circuit of the diff-amp configuration, showing only the differential voltage and **signal currents** as a function of the transistor transconductance *gm.*

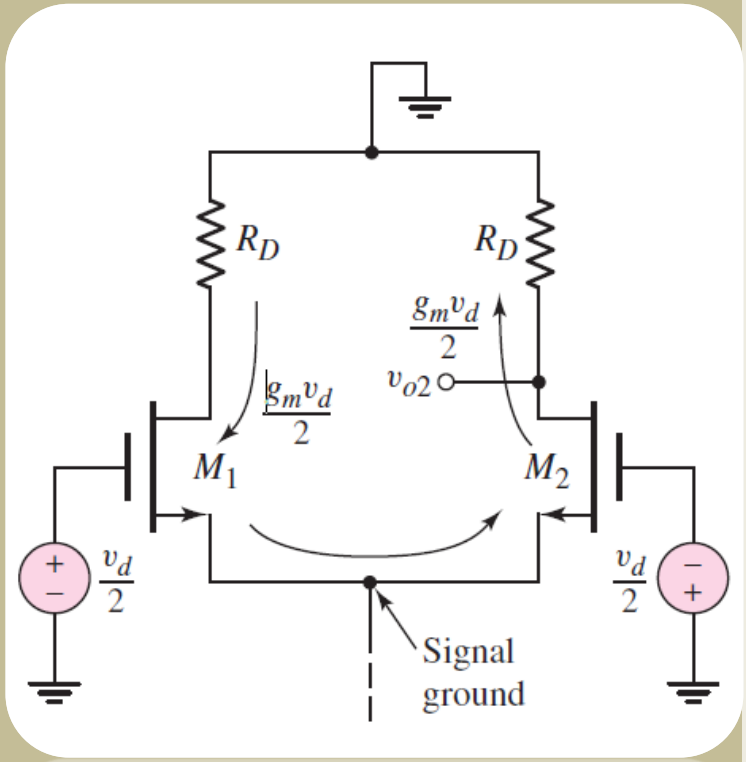


one-sided output voltage at *vo2*, as follows

$$g_m = 2\sqrt{K_n I_{DQ}}$$

$$= 2\sqrt{K_n \frac{I_Q}{2}}$$

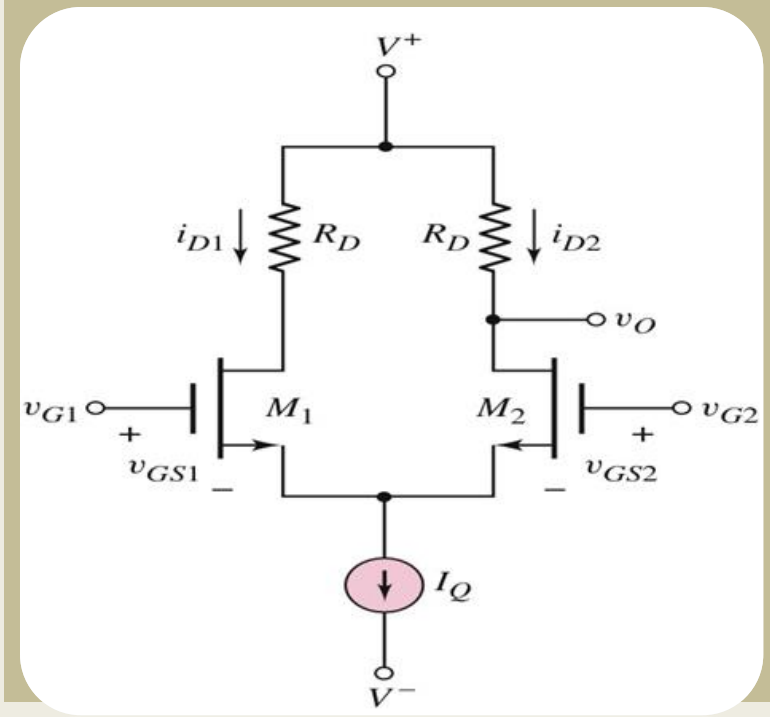
$$= \sqrt{2}\sqrt{2}\sqrt{K_n \frac{I_Q}{2}} = \sqrt{2K_n I_Q}$$

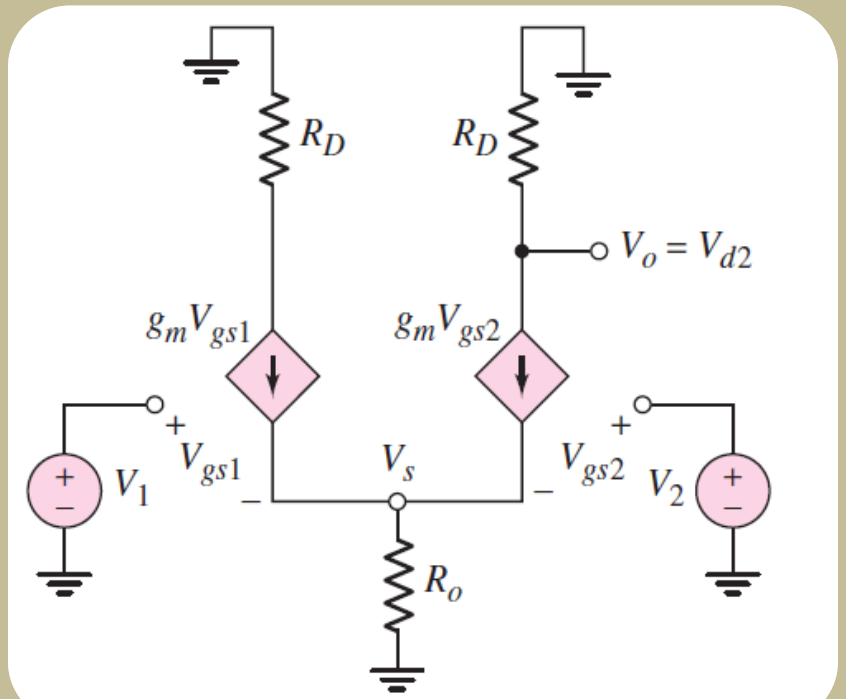


$$v_{o2} \equiv v_o = +\frac{g_m v_d}{2} R_D \longrightarrow \sqrt{2}\sqrt{2}$$

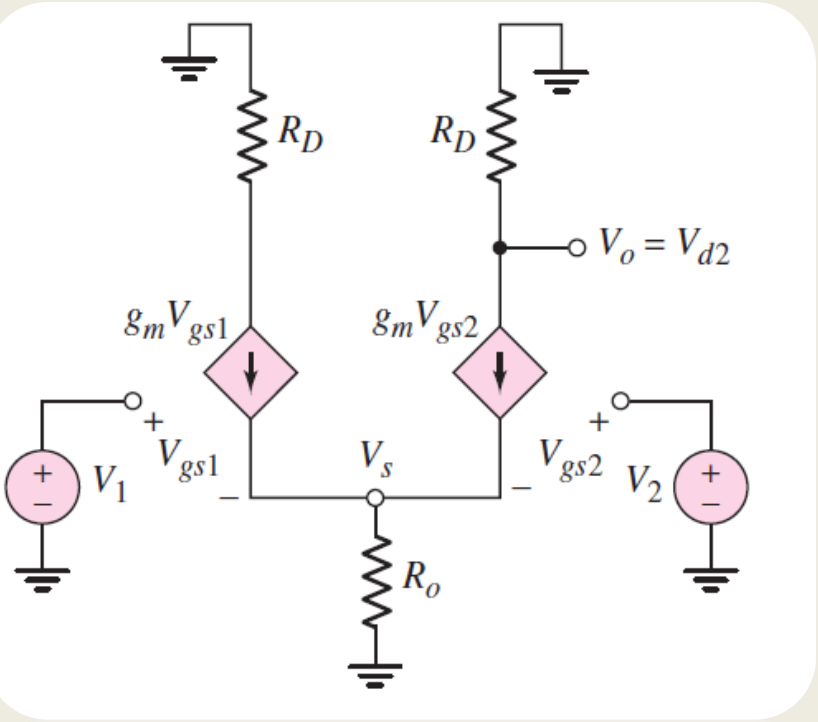
Then the differential voltage gain is

$$A_d = \frac{v_o}{v_d} = \frac{g_m R_D}{2} = \sqrt{\frac{K_n I_Q}{2}}.R_D$$


V+
iD1
RD
RD
iD2
vO
vG1
M1
M2
vG2
+
vGS1
–
–
+
vGS2
IQ
V–


RD
RD
Vo = Vd2
gmVgs1
gmVgs2
+
V1
–
+
Vgs1
–
Vs
–
Vgs2
+
V2
–
Ro

Small-Signal Equivalent Circuit Analysis



- We assume the transistors are matched, with $\lambda = 0$ for each transistor,
- CMRR
- The constant-current source is represented by a finite output resistance *Ro*.
- Transistor are biased at the same quiescent current, and *gm*1 = *gm*2 ≡ *gm*.

$$V_1 = V_{cm} + \frac{V_d}{2} \qquad V_{cm} = \frac{V_1 + V_2}{2}$$

$$V_2 = V_{cm} - \frac{V_d}{2} \qquad 2V_{cm} = V_1 + V_2$$

$$V_d = V_1 - V_2$$

from above equations

Writing a KCL equation at node V_s, we have

$$g_m V_{gs1} + g_m V_{gs2} = \frac{V_s}{R_o} \qquad 3$$

From the circuit, we see that $V_{gs1} = V_1 - V_s$ and $V_{gs2} = V_2 - V_s$

then becomes $g_m(V_1 + V_2 - 2V_s) = \frac{V_s}{R_o}$ 4

$$g_m(V_1 + V_2 - 2V_S) = \frac{V_S}{R_O}$$

$$g_m V_1 + g_m V_2 - 2g_m V_S = \frac{V_S}{R_O}$$

$$g_m(V_1 + V_2) = \frac{V_S}{R_O} + 2g_m V_S$$

$$V_S = \frac{g_m(V_1 + V_2)}{g_m\left(2 + \frac{1}{g_m R_O}\right)} = \frac{V_1 + V_2}{2 + \frac{1}{g_m R_O}}$$

For a one-sided output at the drain of M_2, we have

$$V_o = V_{d2} = -(g_m V_{gs2})R_D = -(g_m R_D)(V_2 - V_s)$$

$$V_o = V_{d2} = -(g_m R_D)\left[V_2 - \frac{V_1 + V_2}{2 + \frac{1}{g_m R_O}} \right]$$

$$V_o = V_{d2} = \frac{-(g_m R_D)\left[V_2\left[2 + \frac{1}{g_m R_O} \right] - (V_1 + V_2) \right]}{2 + \frac{1}{g_m R_O}} = \frac{-(g_m R_D)\left[V_2 + \frac{V_2}{g_m R_O} - V_1 \right]}{2 + \frac{1}{g_m R_O}}$$

$$V_o = -g_m R_D \left[\frac{V_2\left(1 + \frac{1}{g_m R_o} \right) - V_1}{2 + \frac{1}{g_m R_o}} \right]$$

$$V_{cm} = \frac{V_1 + V_2}{2}$$

$$2V_{cm} = V_1 + V_2$$

$$V_d = V_1 - V_2$$

Based on relationships between input voltages V_1 and V_2 and differential – and common – mode voltages,

from above equations

$$V_1 = V_{cm} + \frac{V_d}{2}$$

$$V_2 = V_{cm} - \frac{V_d}{2}$$

$$V_o = V_{d2} = \frac{-(g_m R_D)\left[\left(V_{cm} - \frac{V_d}{2}\right)\left(1 + \frac{1}{g_m R_O}\right) + \frac{V_2}{g_m R_O} - \left(V_{cm} + \frac{V_d}{2}\right)\right]}{2 + \frac{1}{g_m R_O}}$$

WKT :

$$V_o = A_{cm} V_{cm} + A_d V_d$$

Coefficients of A_{cm}

$$V_o = V_{d2} = \frac{-(g_m R_D)\left[V_{cm}\left(1 + \frac{1}{g_m R_O} - 1\right)\right]}{2 + \frac{1}{g_m R_O}} + A_d V_d$$

$$V_o = A_{cm}V_{cm} + A_dV_d$$

Coefficients of A_{cm}

$$V_o = V_{d2} = \frac{-(g_m R_D)\left[V_{cm}\left(1+\frac{1}{g_m R_O}-1\right)\right]}{2+\frac{1}{g_m R_O}} + A_dV_d$$

$$V_o = V_{d2} = \frac{\frac{-(g_m R_D)}{g_m R_O}.V_{cm}}{\frac{1+2g_m R_O}{g_m R_O}} + A_dV_d = \frac{-(g_m R_D)}{1+2g_m R_O}V_{cm} + A_dV_d$$

$$V_o = \frac{g_m R_D}{2}V_d - \frac{g_m R_D}{1+2g_m R_o}V_{cm}$$

The transconductance g_m of the MOSFET is

$$g_m = 2\sqrt{K_n I_{DQ}} = \sqrt{2K_n I_Q}$$

Differential-mode gain is

$$A_d = \frac{g_m R_D}{2} = \sqrt{2K_n I_Q}\left(\frac{R_D}{2}\right) = \sqrt{\frac{K_n I_Q}{2}}.R_D$$

Common-mode gain is

$$A_{cm} = \frac{-g_m R_D}{1+2g_m R_o} = \frac{-\sqrt{2K_n I_Q}.R_D}{1+2\sqrt{2K_n I_Q}.R_o}$$

We again see that for an ideal current source, the common-mode gain is zero since *Ro* =∞.

The common-mode rejection ratio, CMRR = $|A_d/A_{cm}|$, is found to be

$$A_d = \frac{g_m R_D}{2} = \sqrt{2K_n I_Q}\left(\frac{R_D}{2}\right) = \sqrt{\frac{K_n I_Q}{2}}.R_D$$

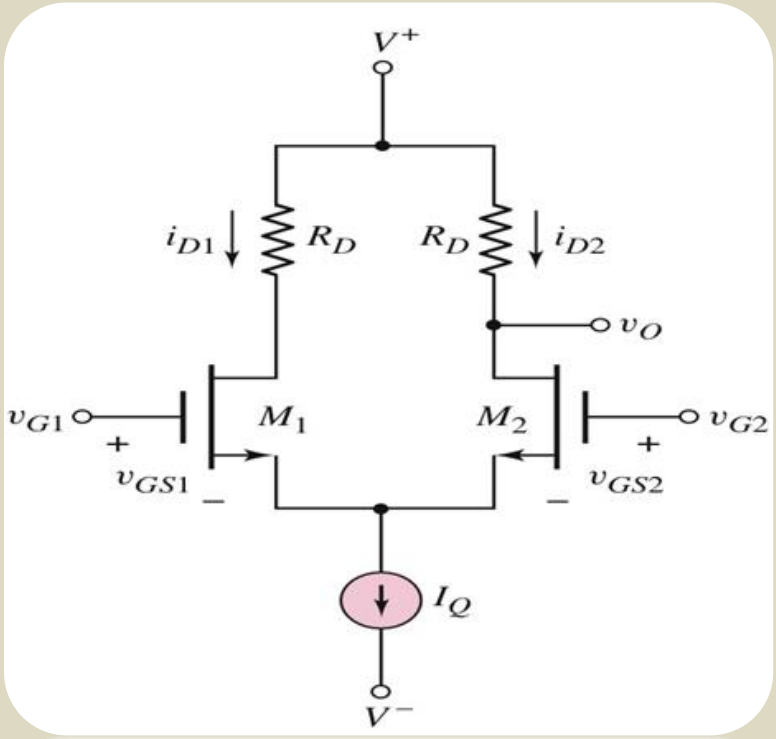
CMRR=

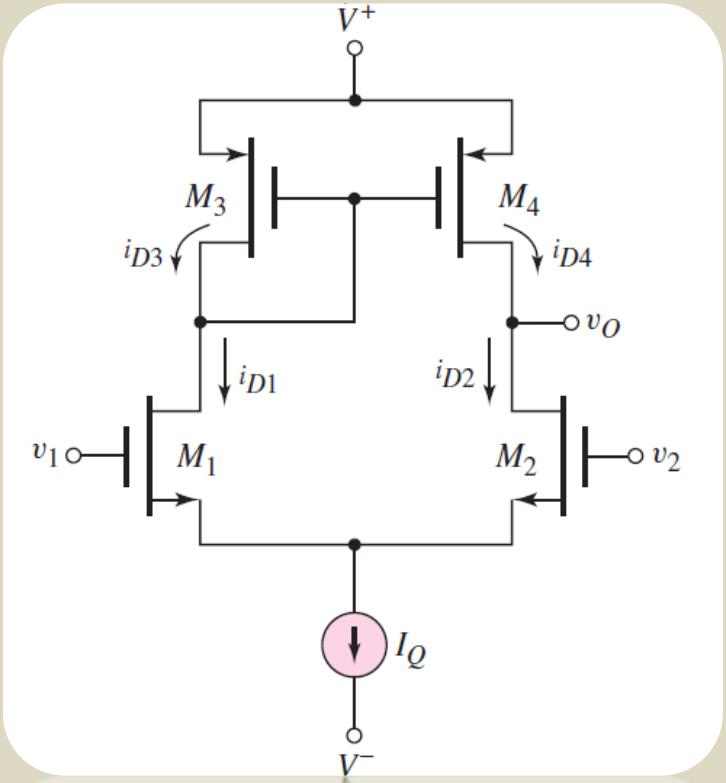
$$A_{cm} = \frac{-g_m R_D}{1+2g_m R_o} = \frac{-\sqrt{2K_n I_Q}.R_D}{1+2\sqrt{2K_n I_Q}.R_o}$$

$$CMRR = \frac{1}{2}\left[1+2\sqrt{2K_n I_Q}.R_o\right]$$

The value of CMRR can be increased by increasing the output resistance of the current source. The increase can be accomplished by using a more sophisticated current source circuit, such as the MOSFET cascode current mirror

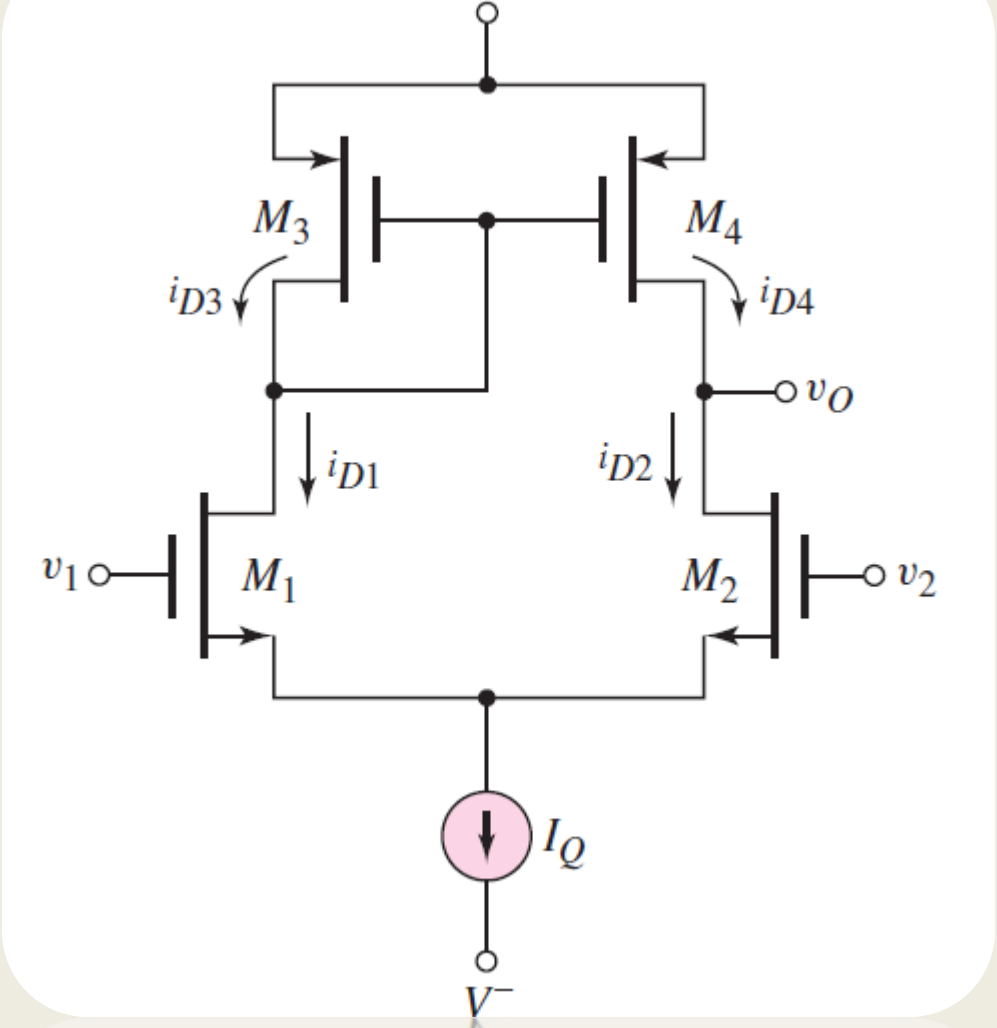
MOSFET differential amplifier with active load





Remember….

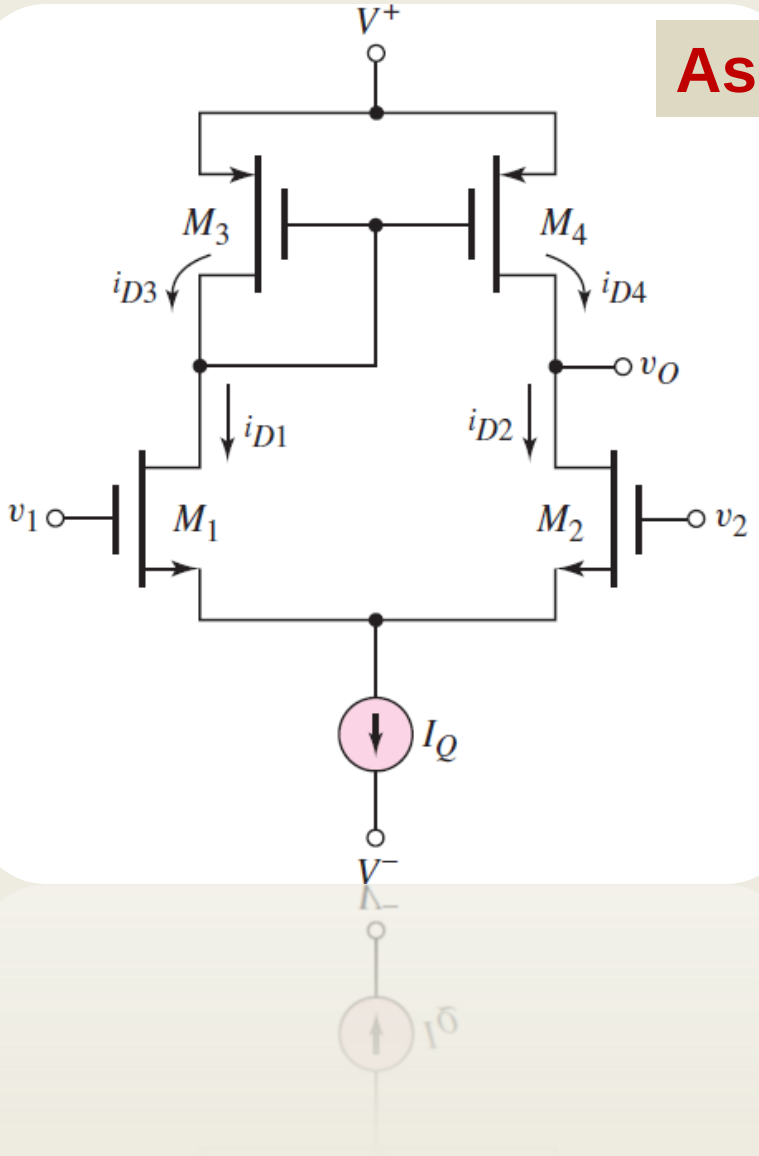
MOSFET differential amplifier with active load



M_1 and M_2 are n – channel devices and form the diff pair biased with

The load circuit consists of M_3 and M_4 , both p – channel devices, connected in a current – mirror configuration.

A one – sided output vO is taken from the common drains of M_2 and M



Assume Common Mode Signal

When a common – mode voltage $V_1 = V_2 = V_{CM}$ *is applied :*

the current I_Q *splits evenly*

between transistors M_1 *and* M_2 *,*

and $i_{D1} = i_{D2} = I_Q / 2.$ •

There are no gate currents,

therefore $i_{D3} = i_{D1}$ *and* $i_{D4} = i_{D2}$

Assume Difference Mode Signal

If a small diff – mode input voltage

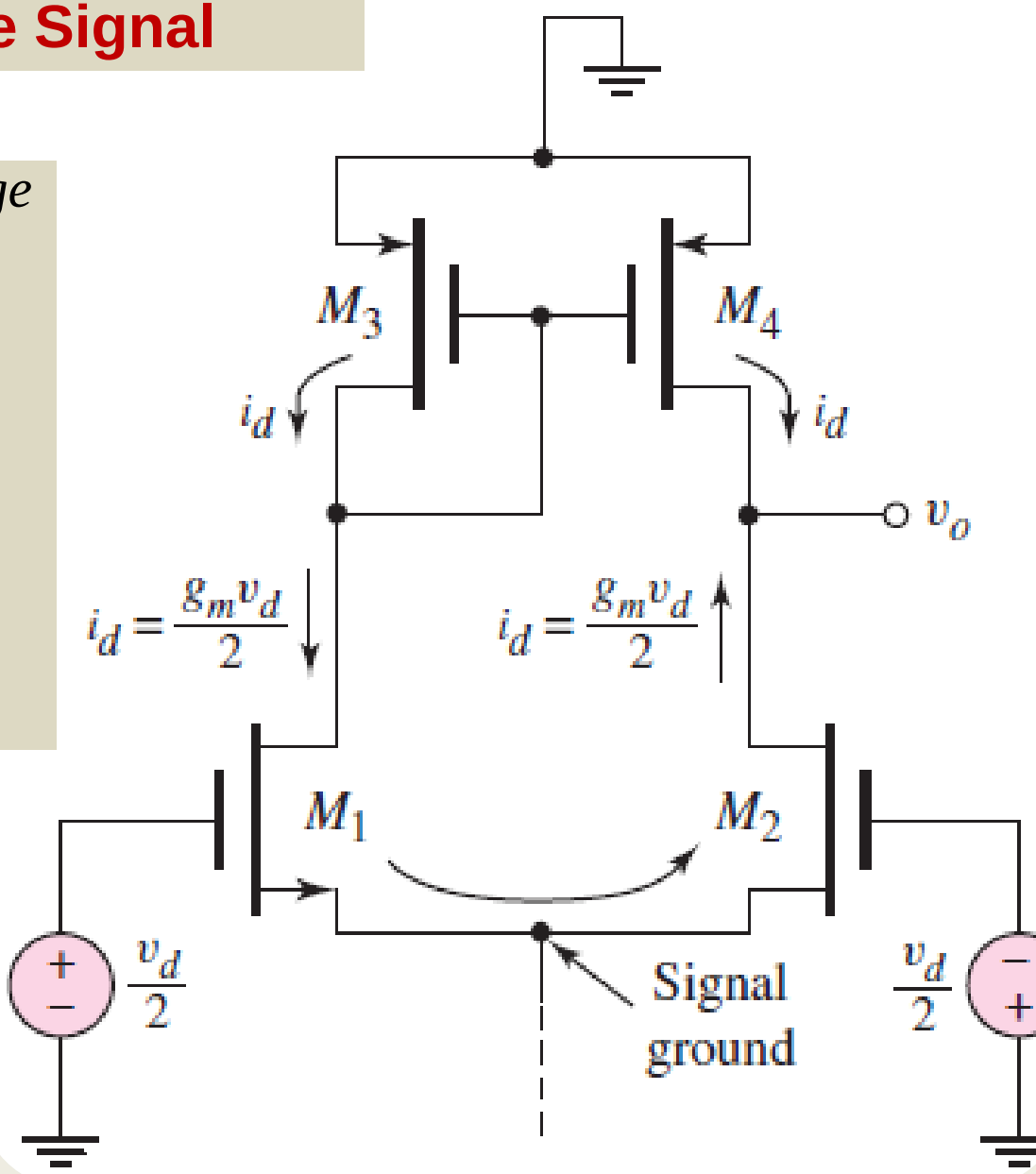
$V_d = V_1 - V_2$ *is applied,*

we can write

$$i_{D1} = \left(I_Q / 2\right) + i_d$$

$$i_{D2} = \left(I_Q / 2\right) - i_d$$

$$i_d = \frac{g_m v_d}{2}$$

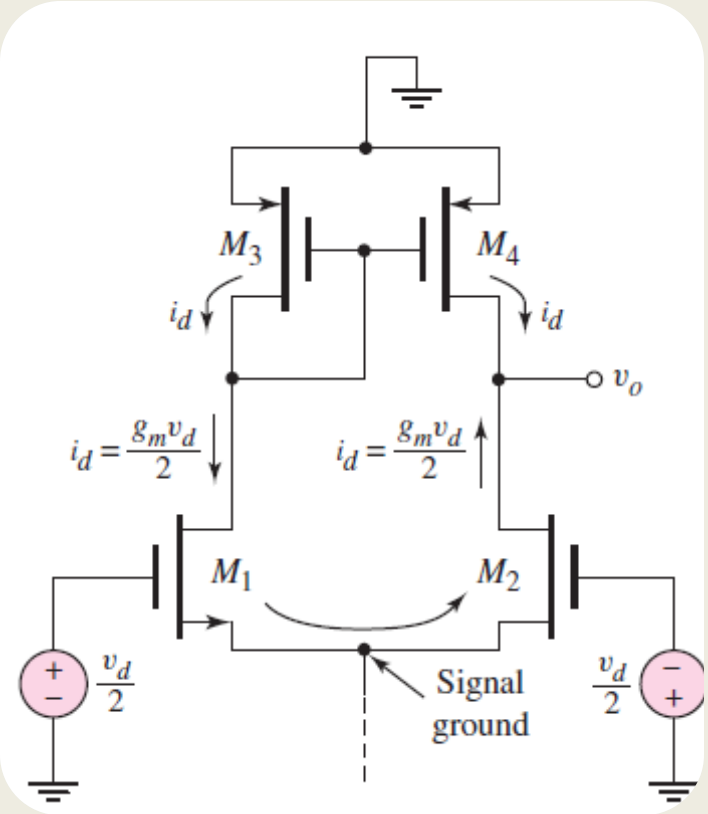


Since $M1$ *and* $M2$ *are in series,*

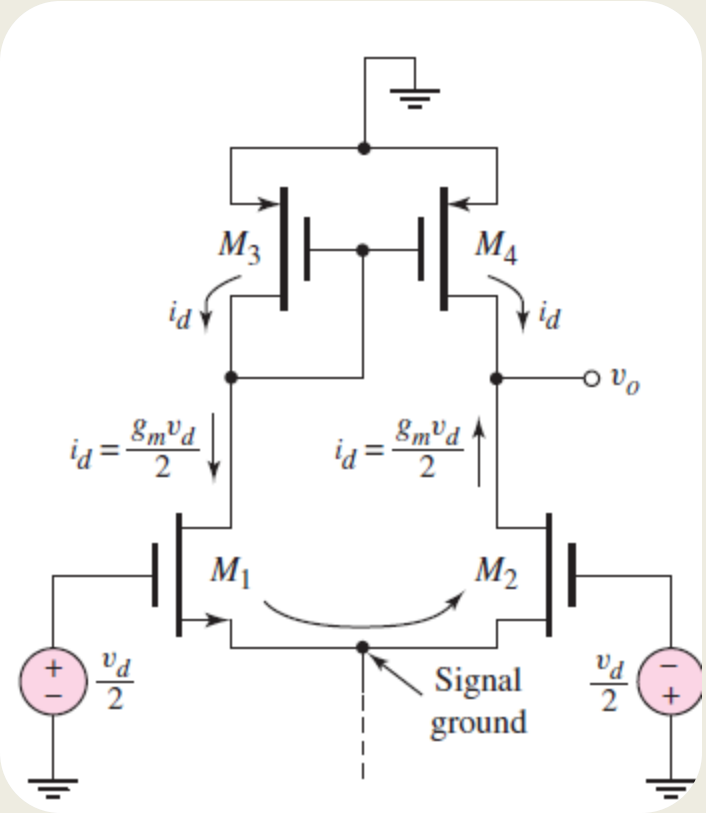
can be seen that $i_{D3} = i_{D1} = \left(I_Q / 2\right) + i_d$

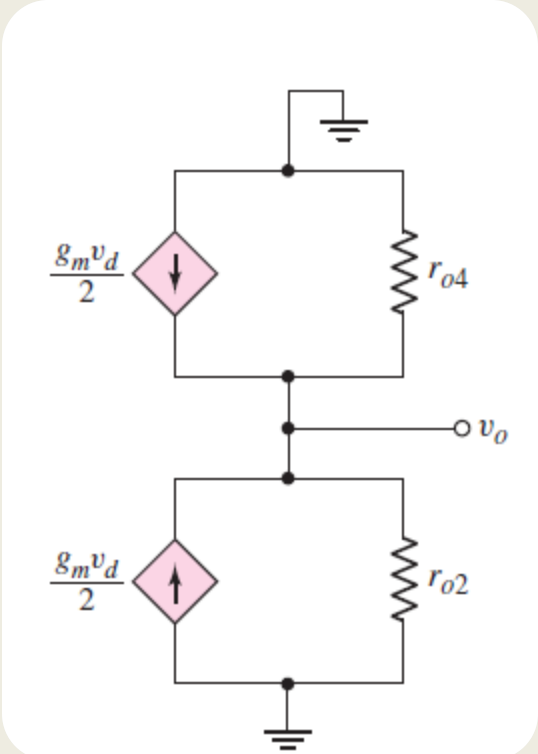
Finally, the current mirror consisting of

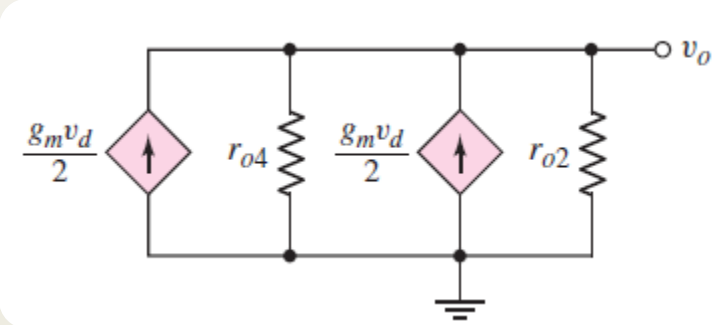
M_3 *and* M_4 *produces* $i_{D4} = i_{D3} = \left(I_Q / 2\right) + i_d$



Small Signal Equivalent Circuit







1.AC Equivalent Circuit
2.Small Signal Equivalent Circuit
3.Rearranged.

the Output Voltage is

$$v_o = 2\left(\frac{g_m v_d}{2}\right)\left(r_{o2} \| r_{o4}\right)$$

$$g_m = 2\sqrt{K_n I_D} = \sqrt{2K_n I_Q}$$

$$g_{o2} = \lambda_2 I_{DQ2} = (\lambda_2 I_Q)/2$$

$$g_{o4} = \lambda_4 I_{DQ4} = (\lambda_4 I_Q)/2$$

and the small-signal diff-mode voltage gain is

$$A_d = \frac{v_o}{v_d} = g_m\left(r_{o2} \| r_{o4}\right)$$

then Equation becomes

$$A_d = \frac{2\sqrt{2K_n I_Q}}{I_Q(\lambda_2 + \lambda_4)} = 2\sqrt{\frac{2K_n}{I_Q}} \cdot \frac{1}{\lambda_2 + \lambda_4}$$

can be rewritten in the form

$$A_d = \frac{g_m}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} = \frac{g_m}{g_{o2} + g_{o4}}$$

$$\frac{1}{R_0} = \frac{dI_D}{dV_{DS}} = \frac{1}{r_O} = \lambda I_D$$

Where

$$r_O = \frac{1}{g_0} = \frac{1}{\lambda I_D}$$

$$g_0 = \lambda I_D$$