5.2 COMPARATOR (No feed back loop) ($A_{OL} = \infty$)

A comparator is a circuit which compares a signal voltage applied at one input of an op-am with a known reference voltage at the other input. It is basically an open-loop op-amp wit output $\pm V_{sat}$ ($= V_{CC}$) as shown in the ideal transfer characteristics of Fig. 5.1 (a). Howeve a commercial op-amp has the transfer characteristics of Fig. 5.1 (b).

Comparator Low offset gain & High CMMR

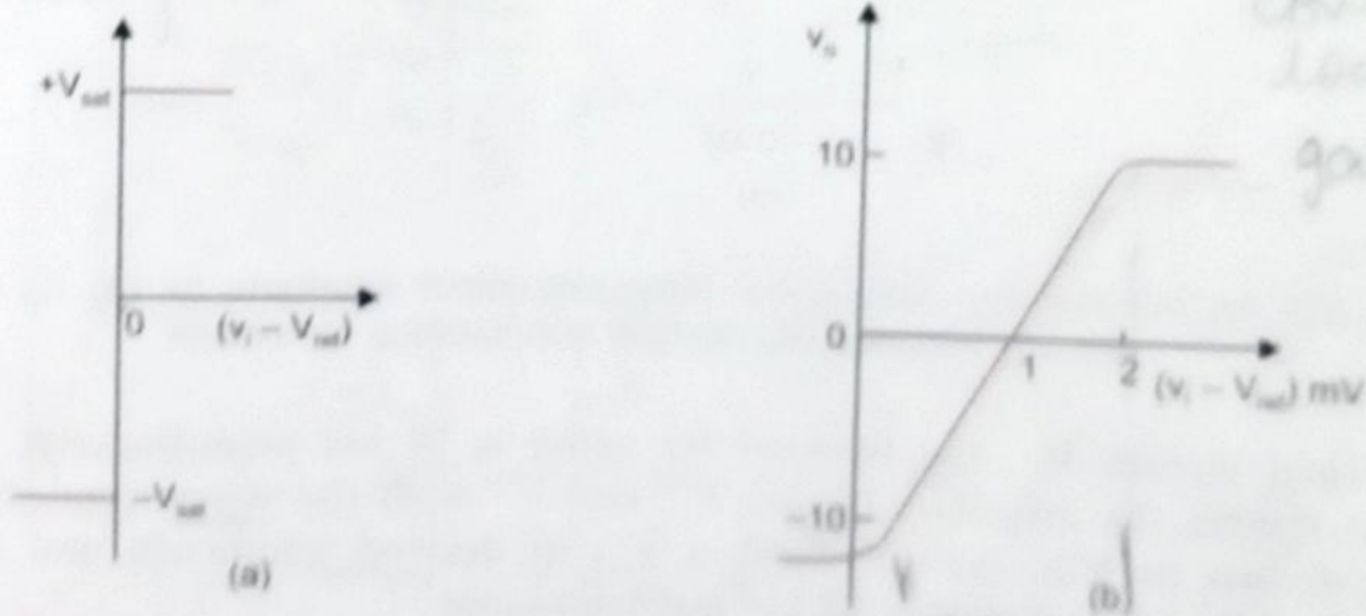

Fig. 5.1 The transfer characteristics (a) Ideal comparator (b) Practical comparator

It may be seen that the change in the output state takes place with an increment in input of only 2 mV. This is the uncertainty region where output cannot be directly defined. This region is due to input off-set voltage and off-set null compensating techniques can be used to eliminate this. There are basically two types of comparators.

5.2 COMPARATOR

(No feedback loop) ($A_{OL} = \infty$)

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output $\pm V_{sat}$ ($= V_{CC}$) as shown in the ideal transfer characteristics of Fig. 5.1 (a). However, a commercial op-amp has the transfer characteristics of Fig. 5.1 (b).

Comparator has low offset, high gain & High CMRR

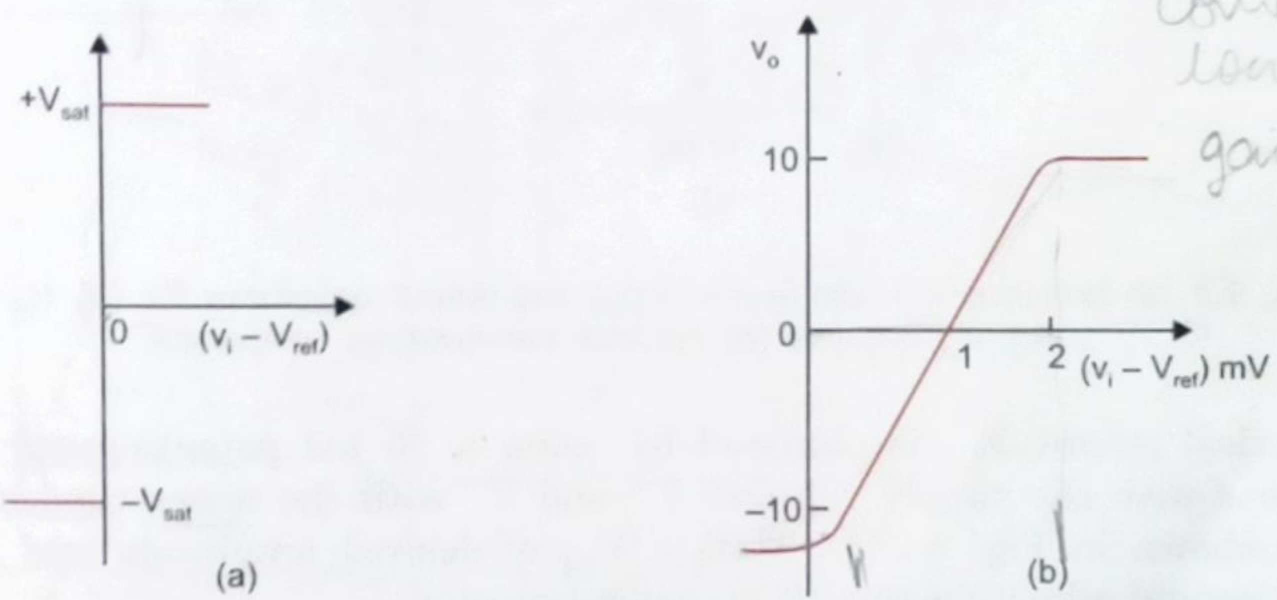

Fig. 5.1 The transfer characteristics (a) Ideal comparator (b) Practical comparator

It may be seen that the change in the output state takes place with an increment in input v_i of only 2 mV. This is the uncertainty region where output cannot be directly defined. This region is due to input off-set voltage and off-set null compensating techniques can be used to eliminate this. There are basically two types of comparators:

1. Non-inverting comparator
2. Inverting comparator.

The circuit of Fig. 5.2 (a) is called a non-inverting comparator. A fixed reference voltage V_{ref} is applied to (–) input and a time varying signal v_i is applied to (+) input. The output voltage is at $-V_{sat}$ for $v_i < V_{ref}$. And v_o goes to $+V_{sat}$ for $v_i > V_{ref}$. The output waveform for a sinusoidal input signal applied to the (+) input is shown in Figs. 5.2 (b and c) for positive and negative V_{ref} respectively.

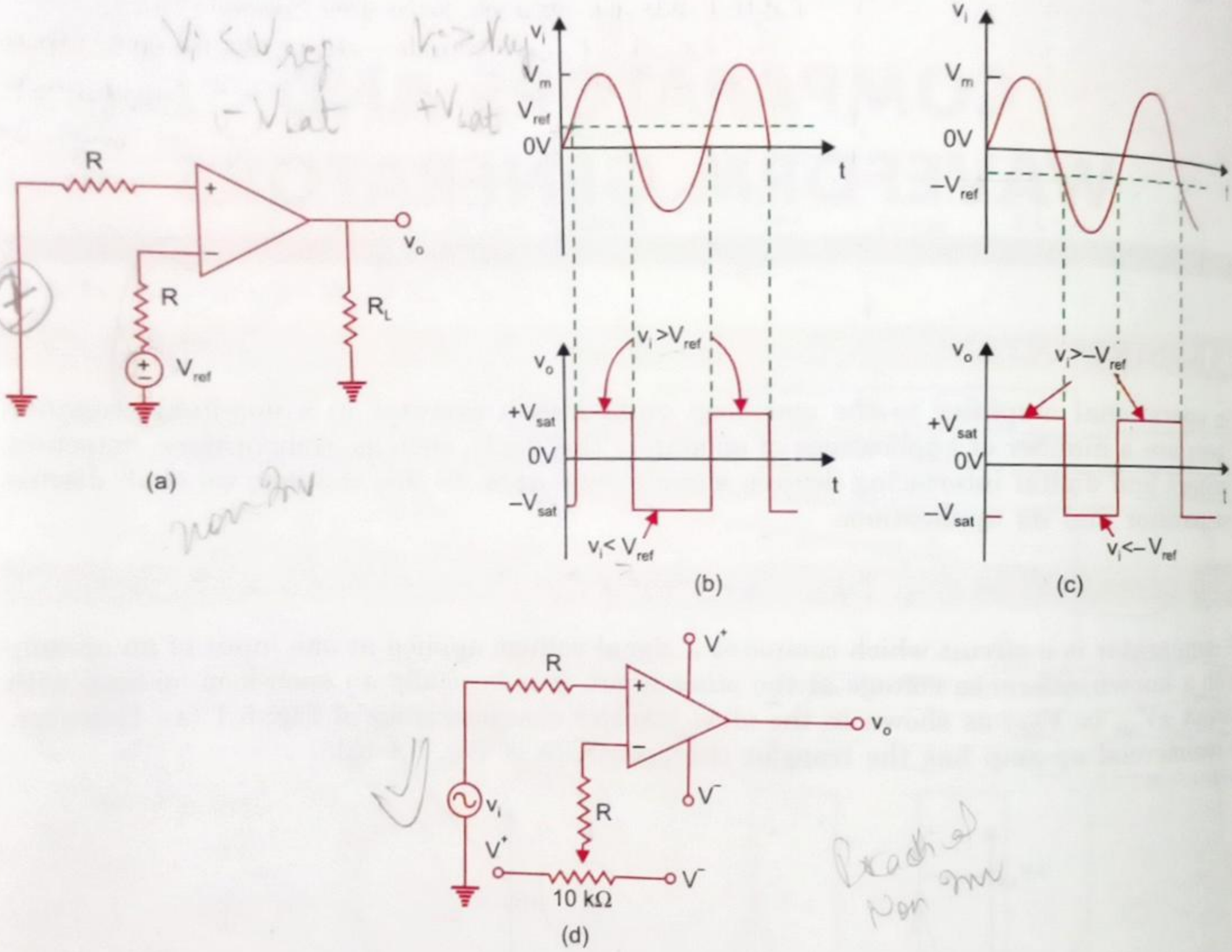

Fig. 5.2 (a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} positive (c) V_{ref} negative (d) Practical non-inverting comparator

In a practical circuit V_{ref} is obtained by using a 10 kΩ potentiometer which forms a voltage divider with the supply voltages V^+ and V^- with the wiper connected to (–) input terminal as shown in Fig. 5.2 (d). Thus a V_{ref} of desired amplitude and polarity can be obtained by simply adjusting the 10 kΩ potentiometer.

Figure 5.3 (a) shows a practical inverting comparator in which the reference voltage V_{ref} is applied to the (+) input and v_i is applied to (–) input. For a sinusoidal input signal, the output waveform is shown in Fig. 5.3 (b) and (c) for V_{ref} positive and negative respectively. Output voltage levels independent of power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp as shown in

Fig. 5.3 (d). The value of resistance R is chosen so that the zener diodes operate at the recommended current. It can be seen that the limiting voltages of v_o are $(V_{Z1} + V_D)$ and $-(V_{Z2} + V_D)$ where V_D (~0.7 V) is the diode forward voltage.

In the waveforms of Figs. 5.2 and 5.3, the output transitions are shown as taking place instantaneously. Practical circuits, however, take a certain amount of time to switch from one voltage level to another. The actual waveform will therefore exhibit slanted edges as well as delays at the points of input threshold crossing. These effects are more noticeable at high frequencies where the output switching times are comparable or even longer than the input period itself. Thus there is an upper limit to the operating frequency of any comparator. If 741, the internally compensated op-amp is used as comparator, the primary limitation is the slew rate. Since 741C has slew rate equal to 0.5 V/μs, it takes $2 \times 13/0.5 = 50$ μs ($V_{sat} = \pm 13$ V for 741) to swing from one saturation level to the other. In many applications, this

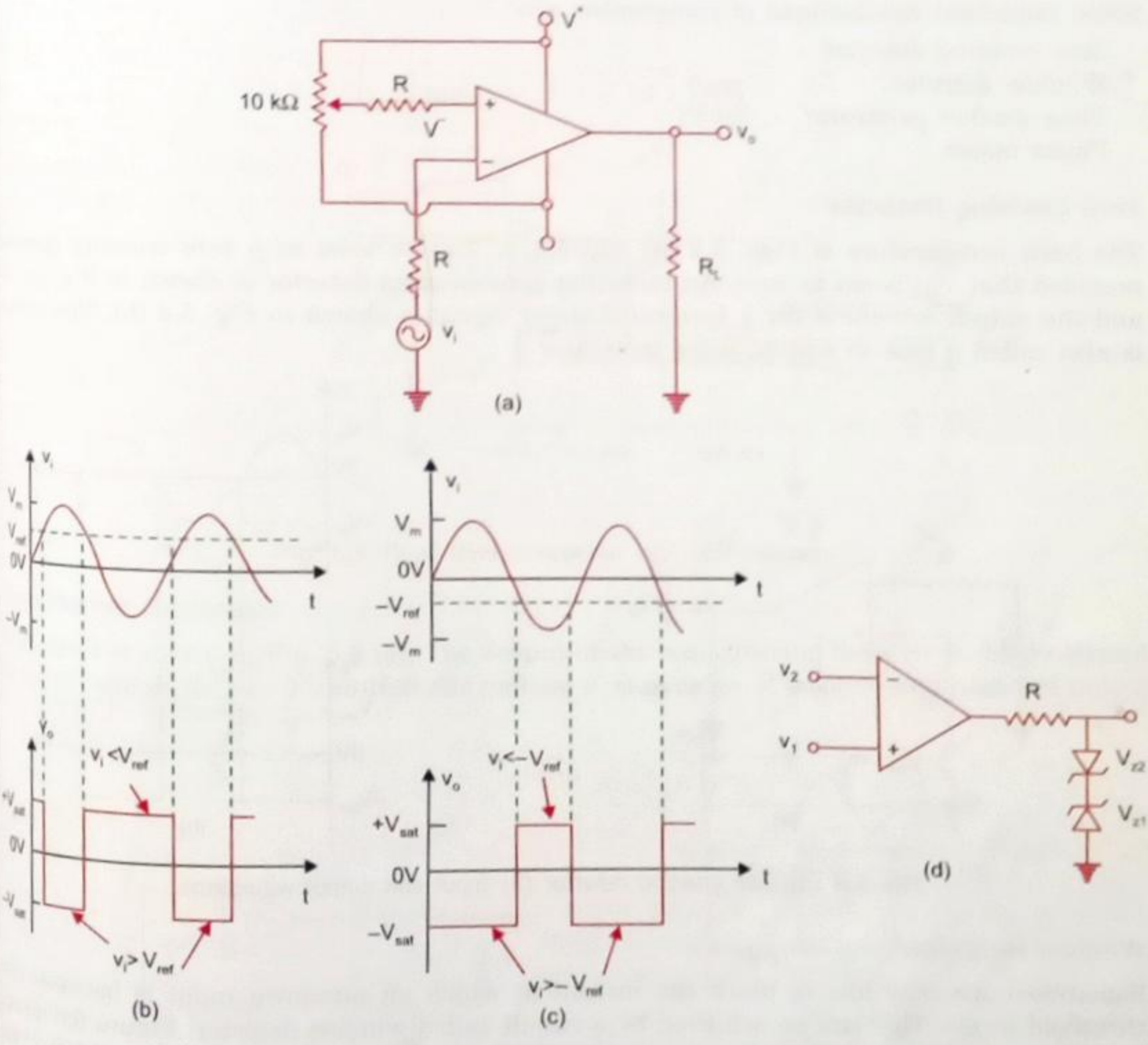

Fig. 5.3 (a) Inverting comparator. Input and output waveforms (b) $V_{ref} > 0$ (c) $V_{ref} < 0$ (d) Comparator with zener diode at the output

is too long. To decrease the response time, it is possible to use uncompensated op-amps such as 301, for comparator applications.

Although uncompensated op-amps make faster comparators than compensated op-amps, there are applications where even higher speeds are required. Also, for interfacing, it is often desired that the output logic levels be compatible with standard logic families such as TTL, CMOS, ECL. To accommodate these needs, monolithic voltage comparators are available. Some of the comparator chips available are the Fairchild μA710 and 760, the National LM 111, 160 and 311. The response time for 311 is 200 ns whereas 710 is a high speed comparator with a response time of 40 ns. CMOS comparators are also available. Some examples are TLC 372 dual, TLC 374 quad (Texas Instruments), MC 14574 quad (Motorola).

5.3 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

If positive feedback is added to the comparator circuit, gain can be increased greatly. Consequently, the transfer curve of comparator becomes more close to ideal curve. Theoretically if the loop gain $-\beta A_{OL}$ is adjusted to unity, then the gain with feedback, A_{Vf} becomes infinite. This results in an abrupt (zero rise time) transition between the extreme values of output voltage. In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations. So a value greater than unity is chosen. This also gives an output waveform virtually discontinu

...s at the comparison voltage. This circuit, however, now exhibits a phenomenon called ...ysteresis or backlash.

...igure 5.8 (a) shows such a regenerative comparator. The circuit is also known as Schmitt ...rigger. The input voltage is applied to the (−) input terminal and feedback voltage to the (+) ...nput terminal. The input voltage v_i triggers the output v_o every time it exceeds certain ...oltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold ...oltage (V_{LT}). The hysteresis width is the difference between these two threshold voltages i.e. $V_{UT} - V_{LT}$. These threshold voltages are calculated as follows.

Suppose the output $v_o = +V_{sat}$. The voltage at (+) input terminal can be obtained by using ...uperposition

$$V_{UT} = \frac{V_{ref}R_1}{R_1 + R_2} + \frac{R_2 V_{sat}}{R_1 + R_2} \tag{5.1}$$

This voltage is called upper threshold voltage V_{UT}. As long as v_i is less than V_{UT}, the ...utput v_o remains constant at $+V_{sat}$. When v_i is just greater than V_{UT}, the output regeneratively ...witches to $-V_{sat}$ and remains at this level as long as $v_i > V_{UT}$ as shown in Fig. 5.8 (b).

For $v_o = -V_{sat}$, the voltage at the (+) input terminal is,

$$V_{LT} = \frac{V_{ref}R_1}{R_1 + R_2} - \frac{R_2 V_{sat}}{R_1 + R_2} \tag{5.2}$$

This voltage is referred to as lower threshold voltage V_{LT}. The input voltage v_i must ...ecome lesser than V_{LT} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$. A regenerative ...ransition takes place as shown in Fig. 5.8 (c) and the output v_o returns from $-V_{sat}$ to $+V_{sat}$ ...lmost instantaneously. The complete transfer characteristics are shown in Fig. 5.8 (d).

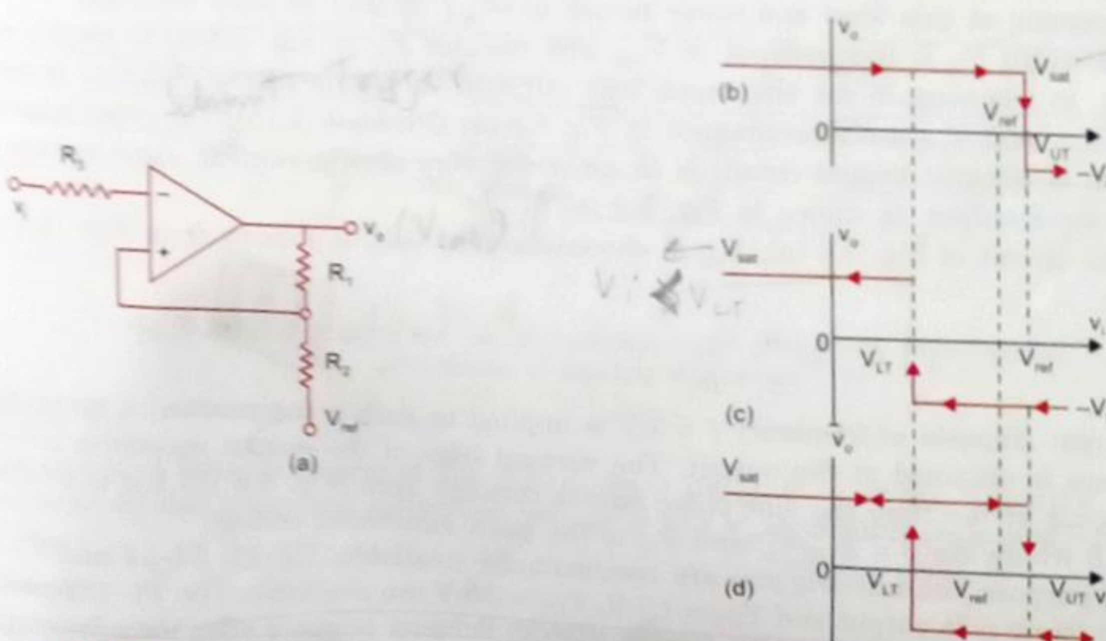

Fig. 5.8 (a) An inverting Schmitt Trigger (b, c) Transfer characteristics for v_i increasing and v_i decreasing (d) Composite input-output curve

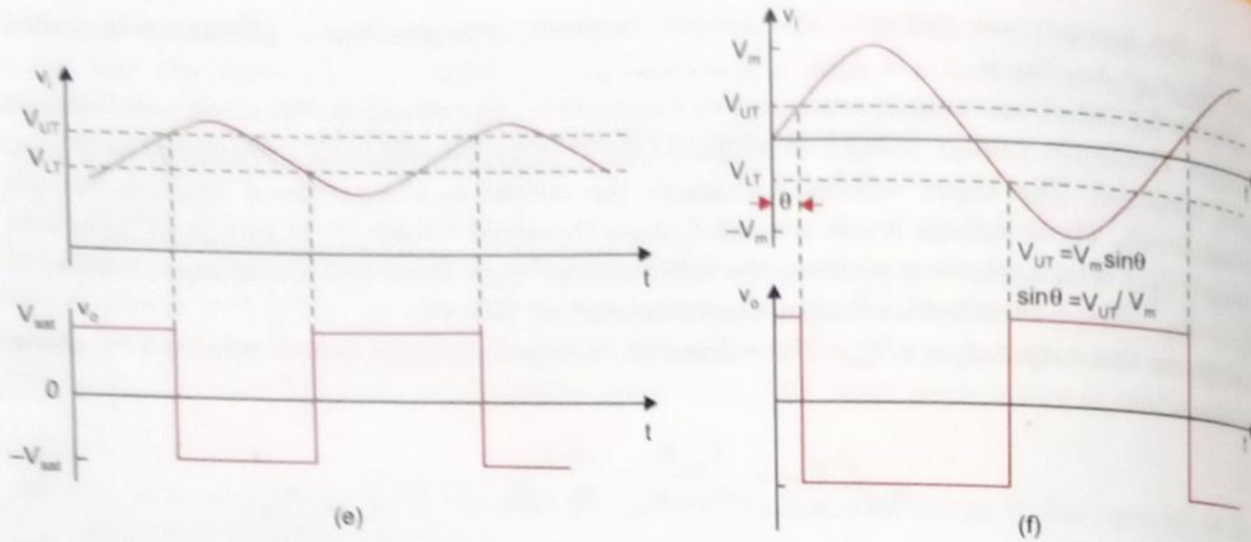

Fig. 5.8 (e) Schmitt Trigger used as a squarer (f) Shift θ in the output waveform for $V_{UT} = -V_{LT}$

Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2\,R_2 V_{sat}}{R_1 + R_2} \tag{5.3}$$

Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones. Further, note that if peak-to-peak input signal v_i were smaller than V_H then the Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction would never reset itself, that is, once the output has jumped to, say, $+V_{sat}$ it would remain at this level and never return to $-V_{sat}$. It may be seen from Eq. (5.3) that hysteresis width V_H is independent of V_{ref}. The resistor R_3 in Fig. 5.8 (a) is chosen equal to $R_1 \| R_2$ to compensate for the input bias current. A non-inverting Schmitt trigger is obtained if v_i and V_{ref} are interchanged in Fig. 5.8 (a) (Problem 5.10). The most important application of Schmitt trigger circuit is to convert a very slowly varying input voltage into a square wave output as shown in Fig. 5.8 (e).

If in the circuit of Fig. 5.8 (a), V_{ref} is chosen as zero volt, it follows from Eqs. (5.1) and (5.2) that

$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

$R_3 = R_1 \| R_2$

If an input sinusoid of frequency $f = 1/T$ is applied to such a comparator, a symmetrical square wave is obtained at the output. The vertical edge of the output waveform however will not occur at the time the sine wave passes through zero [Fig. 5.8 (f)] but is shifted in phase by θ where $\sin\theta = V_{UT}/V_m$ and V_m is the peak sinusoidal voltage.

Special purpose Schmitt triggers are commercially available. T1–13, T1–14 and T1–132 chips with totem pole output and $V_{UT} = 1.7$ V, $V_{LT} = 0.9$ V are available. The T1–132 package is a quad two-input NAND Schmitt trigger. CMOS Schmitt triggers offer the advantage of high input impedance and low power consumption. Examples of CMOS inverting Schmitt trigger are the CD40106B and 744C14.

An interesting application of hysteresis is in the detection and counting of the zero-crossings of an arbitrary waveform if it is superimposed with interference say of a frequency much higher than the signal.

Consider the Fig. 5.8(g) where the clean signal crosses the zero axis a number of times when corrupted with noise interference around each of the zero crossing points we are trying to detect. A simple comparator would change state at each of the zero crossings. If, however, we know the expected peak-to peak amplitude of the interference, the problem is solved by introducing hysteresis of appropriate width in the circuit as shown by V_{UT} and V_{LT} in Fig. 5.8 (g). The hysteresis in the comparator characteristics thus provides an effective means of rejecting interference.

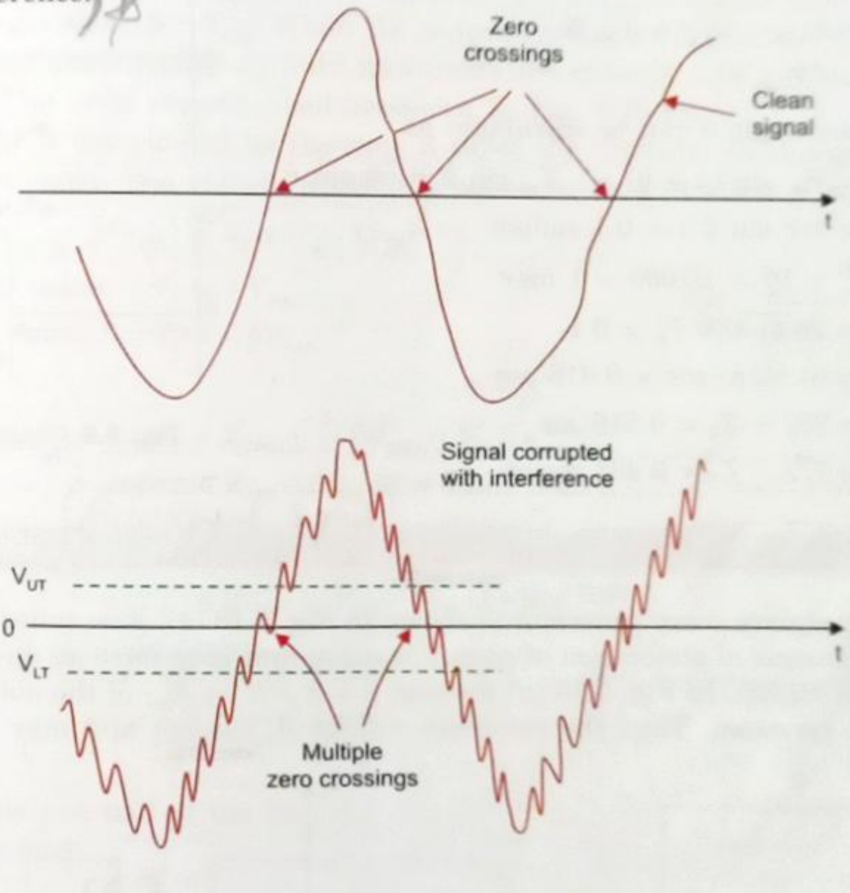

Fig. 5.8 (g) Illustrating the use of hysteresis in the comparator characteristics as a means of rejecting interference

Example 5.2

In the circuit of Schmitt trigger of Fig. 5.8 (a), $R_2 = 100\,\Omega$, $R_1 = 50\ \text{k}\Omega$, $V_{ref} = 0$ V, $v_i = 1\ V_{pp}$ (peak-to-peak) sine wave and saturation voltage = ±14 V. Determine threshold voltages V_{UT} and V_{LT}.

Solution

From Eqs. (5.1) and (5.2)

$$V_{UT} = \frac{100}{50100} \times 14 = 28 \text{ mV}$$

$$V_{LT} = \frac{100}{50100} \times (-14) = -28 \text{ mV}$$

Example 5.3

A Schmitt trigger with the upper threshold level $V_{UT} = 0$ V and hysteresis width $V_H = 0.2$ V converts a 1 kHz sine wave of amplitude $4V_{pp}$ into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

Solution

$$V_{UT} = 0$$

$$V_H = V_{UT} - V_{LT} = 0.2 \text{ V}$$

So, $\boxed{V_{LT} = -0.2 \text{ V}}$

$\sin\theta = \frac{V_{LT}}{V_m}$

In Fig. 5.9, the angle θ can be calculated as

$-V_{LT} = \sin\theta \cdot V_m$

$$-0.2 = V_m \sin(\pi + \theta) = -V_m \sin\theta = -2 \sin\theta$$

$$\theta = \text{arc} \sin 0.1 = 0.1 \text{ radian}$$

The period, $T = 1/f = 1/1000 = 1$ ms

$$wT_\theta = 2\pi\,(1000)\,T_\theta = 0.1$$

$$T_\theta = (0.1/2\pi) \text{ ms} = 0.016 \text{ ms}$$

So, $T_1 = T/2 + T_\theta = 0.516$ ms

and $T_2 = T/2 - T_\theta = 0.484$ ms

(free running)

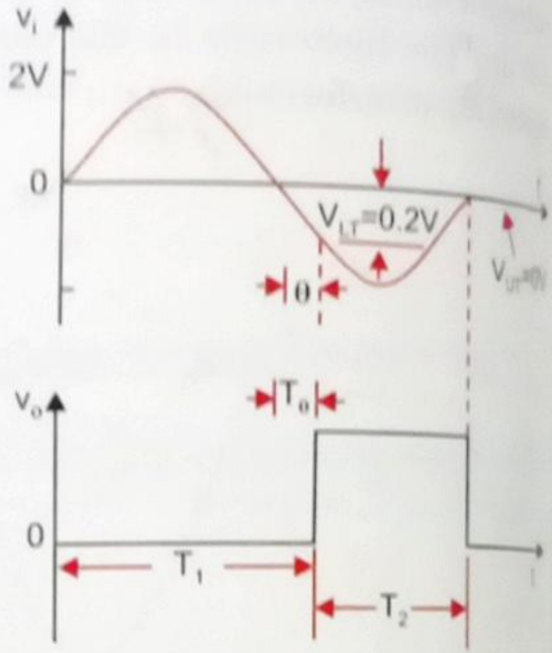

Fig. 5.9 Circuit for Example 5.3

5.5 MONOSTABLE MULTIVIBRATOR (one shot)

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The circuit shown in Fig. 5.11(a) is a modified form of the astable multivibrator

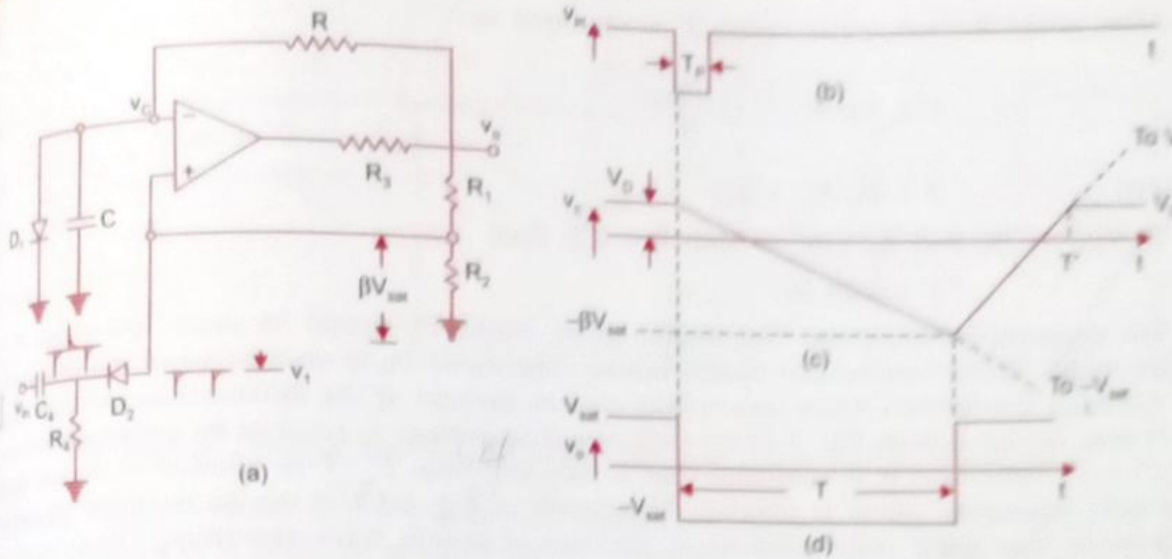

Fig. 5.11 (a) Monostable multivibrator (b) Negative going triggering signal (c) Capacitor waveform (d) Output voltage waveform

diode D_1 clamps the capacitor voltage to 0.7 V when the output is at $+V_{sat}$. A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative going triggering impulse and is applied to the (+) input terminal.

To analyse the circuit, let us assume that in the stable state, the output v_o is at $+V_{sat}$. The diode D_1 conducts and v_c the voltage across the capacitor C gets clamped to +0.7 V. The voltage at the (+) input terminal through R_1R_2 potentiometric divider is $+\beta V_{sat}$. Now, if negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7 V, i.e. ($[\beta V_{sat} + (-V_1)] < 0.7$ V), the output of the op-amp will switch from $+V_{sat}$ to $-V_{sat}$. The diode will now get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$. When the capacitor voltage v_c becomes just slightly more negative than $-\beta V_{sat}$, the output of the op-amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until v_c is 0.7V as capacitor C gets clamped to the voltage. Various waveforms are shown in Fig. 5.11 (b, c, d).

The pulse width T of monostable multivibrator is calculated as follows:

The general solution for a single time constant low pass RC circuit with V_i and V_f as initial and final values is,

$$v_o = V_f + (V_i - V_f)e^{-t/RC} \tag{5.13}$$

For the circuit, $V_f = -V_{sat}$ and $V_i = V_D$ (diode forward voltage).

The output v_c is,

$$v_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC} \tag{5.14}$$

at $t = T$,

$$v_c = -\beta V_{sat} \tag{5.15}$$

Therefore,

$$-\beta\, V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-T/RC}$$

After simplification, pulse width T is obtained as

$$T = RC \ln \frac{(1 + V_D V_{sat})}{1 - \beta} \quad (5.16)$$

where $\beta = R_2/(R_1 + R_2)$

If, $V_{sat} >> V_D$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$T = 0.69\ RC \quad (5.17)$$

For monostable operation, the trigger pulse width T_p should be much less than T, the pulse width of the monostable multivibrator. The diode D_2 is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

It may be noted from Fig. 5.11 (b) that capacitor voltage v_c reaches its quiescent value V_1 at $T' > T$. Therefore, it is essential that a recovery time $T' - T$ be allowed to elapse before the next triggering signal is applied. The circuit of Fig. 5.11 (a) can be modified to achieve voltage to time delay conversion as in the case of square wave generator. The monostable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a predetermined time T after the application of input trigger. It is also called a gating circuit as it generates a rectangular waveform at a definite time and thus could be used to gate parts of a system.

5.6 TRIANGULAR WAVE GENERATOR

A triangular wave can be simply obtained by integrating a square wave as shown in Fig. 5.12 (a). It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig. 5.12 (b). Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases. This is because the reactance of the capacitor C_2 in the feedback circuit decreases at high frequencies. A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of practical integrator.

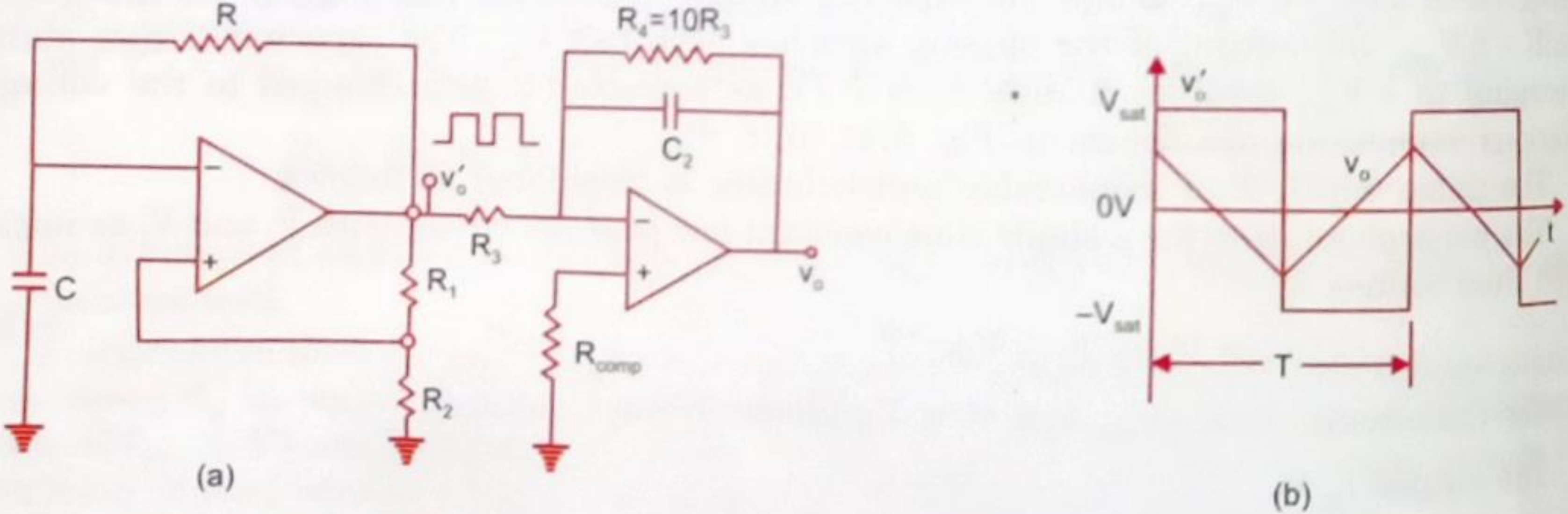

Fig. 5.12 (a) Triangular waveform generator (b) Output waveform

Another triangular wave generator using lesser number of components is shown in Fig. 5.13 (a). It basically consists of a two level comparator followed by an integrator. The output of the comparator A_1 is a square wave of amplitude $\pm V_{sat}$ and is applied to the (–) input terminal of the integrator A_2 producing a triangular wave. This triangular wave is fed back as input to the comparator A_1 through a voltage divider R_2R_3.

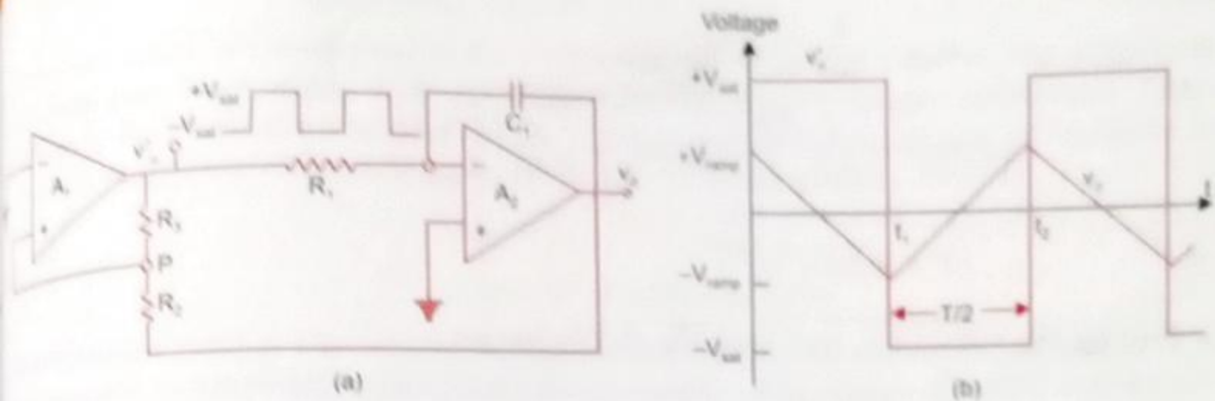

Fig. 5.13 (a) Triangular waveform generator using lesser components (b) Waveforms

Initially, let us consider that the output of comparator A_1 is at $+V_{sat}$. The output of the integrator A_2 will be a negative going ramp as shown in Fig. 5.13 (b). Thus one end of the voltage divider R_2R_3 is at a voltage $+V_{sat}$ and the other at the negative going ramp of A_2. At time $t = t_1$, when the negative going ramp attains a value of $-V_{ramp}$, the effective voltage at point P becomes slightly less than 0 V. This switches the output of A_1 from positive saturation to negative saturation level $-V_{sat}$. During the time when the output of A_1 is at $-V_{sat}$, the output of A_2 increases in the positive direction. And at the instant $t = t_2$, the voltage at point P becomes just above 0 V, thereby switching the output of A_1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular waveform. It can be seen that the frequency of the square wave and triangular wave will be the same. However, the amplitude of the triangular wave depends upon the RC value of the integrator A_2 and the output voltage level of A_1. The output voltage of A_1 can be set to desired level by using appropriate zener diodes. The frequency of the triangular waveform can be calculated as follows:

The effective voltage at point P during the time when output of A_1 is at $+V_{sat}$ level is given by

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right] \tag{5.18}$$

At $t = t_1$, the voltage at point P becomes equal to zero. Therefore, from Eq. (5.18),

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat}) \tag{5.19}$$

Similarly, at $t = t_2$, when the output of A_1 switches from $-V_{sat}$ to $+V_{sat}$,

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat}) = \frac{R_2}{R_3}(V_{sat}) \tag{5.20}$$

Therefore, peak to peak amplitude of the triangular wave is,

$$v_o\,(\text{pp}) = +V_{ramp} - (-V_{ramp}) = 2\frac{R_2}{R_3}V_{sat} \tag{5.21}$$

The output switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$. Putting the values in the basic integrator equation

Chapter 5

$$v_o = -\frac{1}{RC}\int v_i \, dt$$

$$v_o(\text{pp}) = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{\text{sat}})dt = \frac{V_{\text{sat}}}{R_1C_1}\left(\frac{T}{2}\right)$$

or,

$$\boxed{T = 2\,R_1C_1\frac{v_o\,(\text{pp})}{V_{\text{sat}}}}$$ (5.2

Putting the value of v_o (pp) from Eq. (5.21), we get

$$\boxed{T = \frac{4R_1C_1R_2}{R_3}}$$

Hence the frequency of oscillation f_o is,

$$\boxed{f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2}}$$ (5.2

RC-Phase Shift Oscillator

The circuit of an RC-phase shift oscillator is shown in Fig. 5.16 (a). The op-amp is used in the inverting mode and therefore provides 180° phase shift. The additional phase of 180° is provided by the RC feedback network to obtain a total phase shift of 360°. The feedback network consists of three identical RC stages. Each of the RC stage provides a 60° phase shift so that the total phase shift due to feedback network is 180°. It is not necessary that all the three RC sections are identical so long the total phase shift is 180°. However, if we use non-identical stages, it is possible that the total phase shift is 180° for more than one frequency. This phenomenon can lead to undesirable inter-modal oscillations.

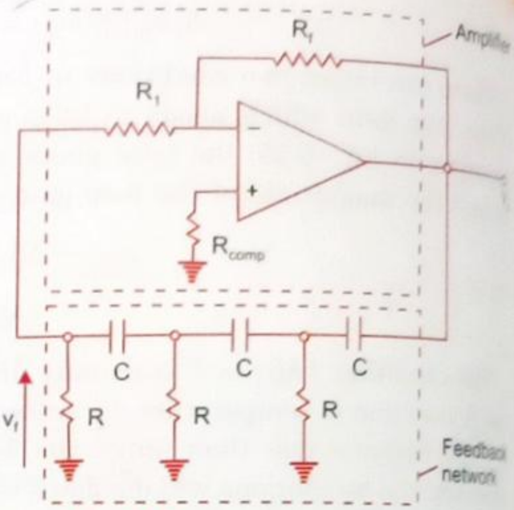

Fig. 5.16 (a) Phase shift oscillator

The feedback factor β of the RC network can be calculated by writing the KVL equations from Fig. 5.16 (b).

$$I_1\left(R+\frac{1}{sC}\right)-I_2R = V_o \qquad (5.28)$$

$$-I_1R+I_2\left(2R+\frac{1}{sC}\right)-I_3R = 0 \qquad (5.29)$$

$$0-I_2R+I_3\left(2R+\frac{1}{sC}\right) = 6 \qquad (5.30)$$

and $$V_f = I_3R \qquad (5.31)$$

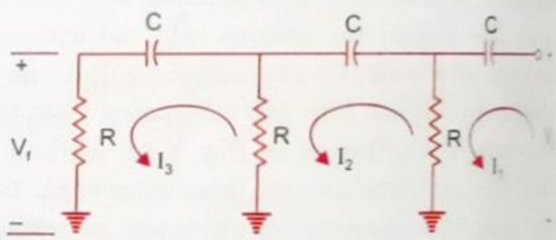

Fig. 5.16 (b) Calculating β from the phase shift network

Solving Eqs. (5.28), (5.29) and (5.30) for I_3, we get

$$I_3 = \frac{V_oR^2s^3C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \qquad (5.32)$$

and $$V_f = I_3R = \frac{V_oR^3s^3C^3}{1+5sRC+6s^2C^2R^2+s^3C^3R^3} \qquad (5.33)$$

$$= \frac{1}{1+\dfrac{6}{sRC}+\dfrac{5}{s^2C^2R^2}+\dfrac{1}{s^3C^3R^3}} \qquad (5.34)$$

$\beta = \frac{V_f}{V_o}$

Replacing $s = j\omega$, $s^2 = -\omega^2$ and $s^3 = -j\omega^3$, we get

$$\beta = \frac{1}{1-\dfrac{6}{j\omega RC}-\dfrac{5}{\omega^2R^2C^2}+\dfrac{1}{j\omega^3R^3C^3}} \qquad (5.35)$$

$$= \frac{1}{(1-5\alpha^2)+j\alpha(6-\alpha^2)} \qquad (5.36)$$

where

$$\alpha = \frac{1}{\omega RC} \tag{5.37}$$

For $A\beta = 1$, β should be real, that is the imaginary term in Eq. (5.36) must be zero. Thus

$$\alpha\,(6 - \alpha^2) = 0 \tag{5.38}$$

$$\alpha^2 = 6$$

$$\alpha = \sqrt{6}$$

That is,

$$\frac{1}{\omega RC} = \sqrt{6}$$

$X_C = \frac{1}{2\pi f_0 C}$ $R = R_1$

$Z = \sqrt{R^2 + X_C^2}$

The frequency of oscillation, f_o, is therefore given by

$$f_o = \frac{1}{2\pi\, RC\, \sqrt{6}} \tag{5.39}$$

$\phi = \tan^{-1} \frac{X_C}{R}$

Putting $\alpha^2 = 6$ in Eq. (5.36), we get

$$\beta = -\frac{1}{29} \tag{5.40}$$

The negative sign indicates that the feedback network produces a phase shift of 180°.

So, $$|\beta| = \frac{1}{29}$$

Since $$|A\beta| \geq 1$$

Therefore, for sustained oscillations,

$$|A| \geq 29 \tag{5.41}$$

That is the gain of the inverting op-amp should be atleast 29, or $R_f = 29\, R_1$. The gain A_v is kept greater than 29 to ensure that variations in circuit parameters will not make $|A_v \beta| < 1$, otherwise oscillations will die out.

For low frequencies (< 1 kHz), op-amp 741 may be used, however, for high frequencies, LM 318 or LF 351 should be used.

$\beta = \frac{V_f}{V_0}$

Example 5.4

Design a phase shift oscillator of Fig. 5.15 to oscillate at 100 Hz.

$f = 100$

Solution

Let $C = 0.1\ \mu$F. Then from Eq. (5.25)

$$R = \frac{1}{\sqrt{6}\, 2\pi (10^{-7})(100)} = 6.49\ \text{k}\Omega$$

Use $R = 6.5$ kΩ

To prevent loading of the amplifier by RC network, $R_1 \leq 10\, R$

Therefore, let $R_1 = 10\, R = 65$ kΩ

Since $R_f = 29\, R_1$

$R_f = 1885$ kΩ