Module:7 Special Function ICs

Course: BECE206L – Analog Circuits

Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

Module:7   Special Function ICs

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- **IC 555 timer**, Astable and **Monostable operations, and applications**. IC voltage regulator - LM317.

1. Introduction

- IC 555 timer – highly stable device for generating accurate time delay and oscillations
- Either as 14 pin DIP with two 555 timers
  or as single 8 pin DIP with one 555 timer
- Supply voltage: +5V to +18V
- Can drive a load upto 220mA
- Compatible with both Transistor Transistor Logic (TTL) or CMOS(complementary MOSFET) logic circuits
- Applications: oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor, etc

2. PIN Diagram and Functional diagram

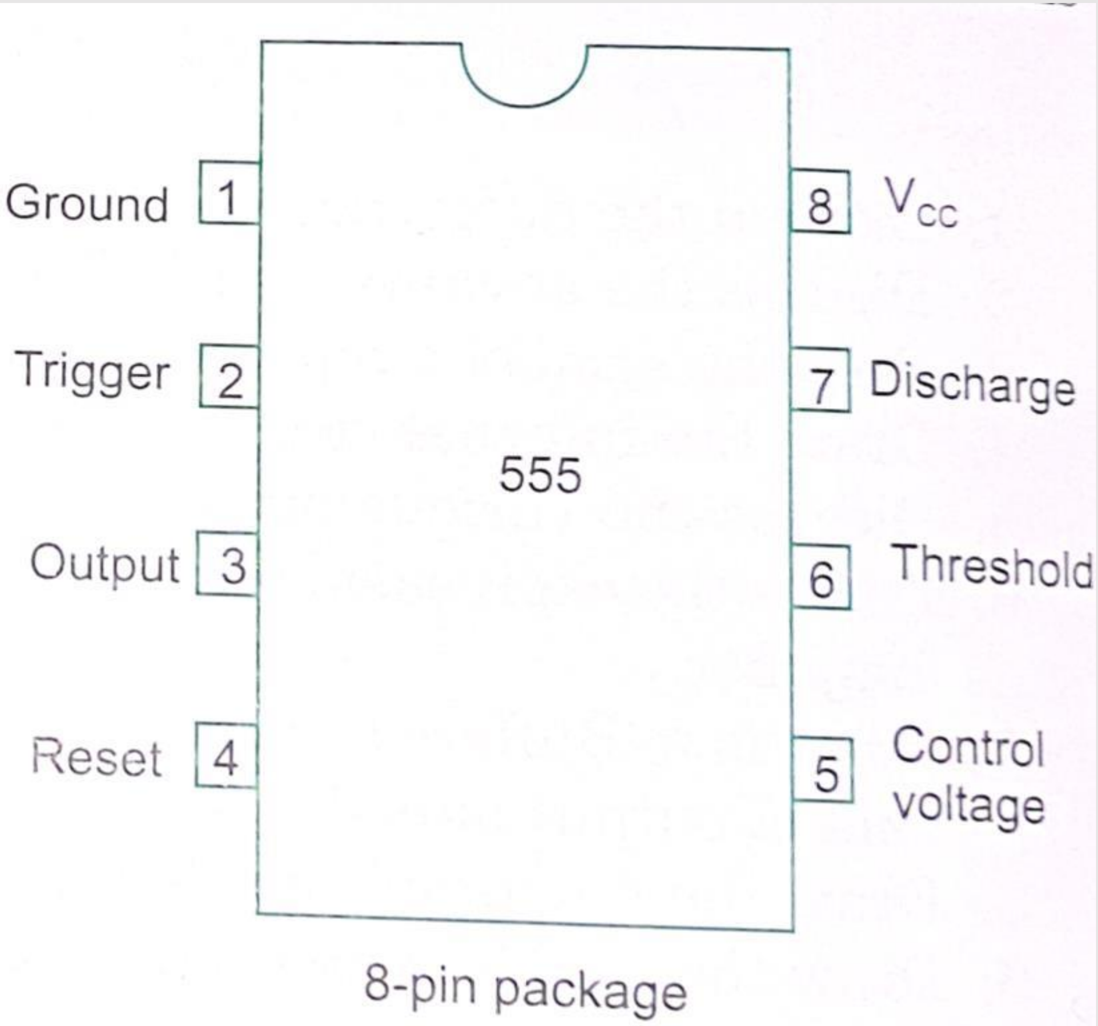
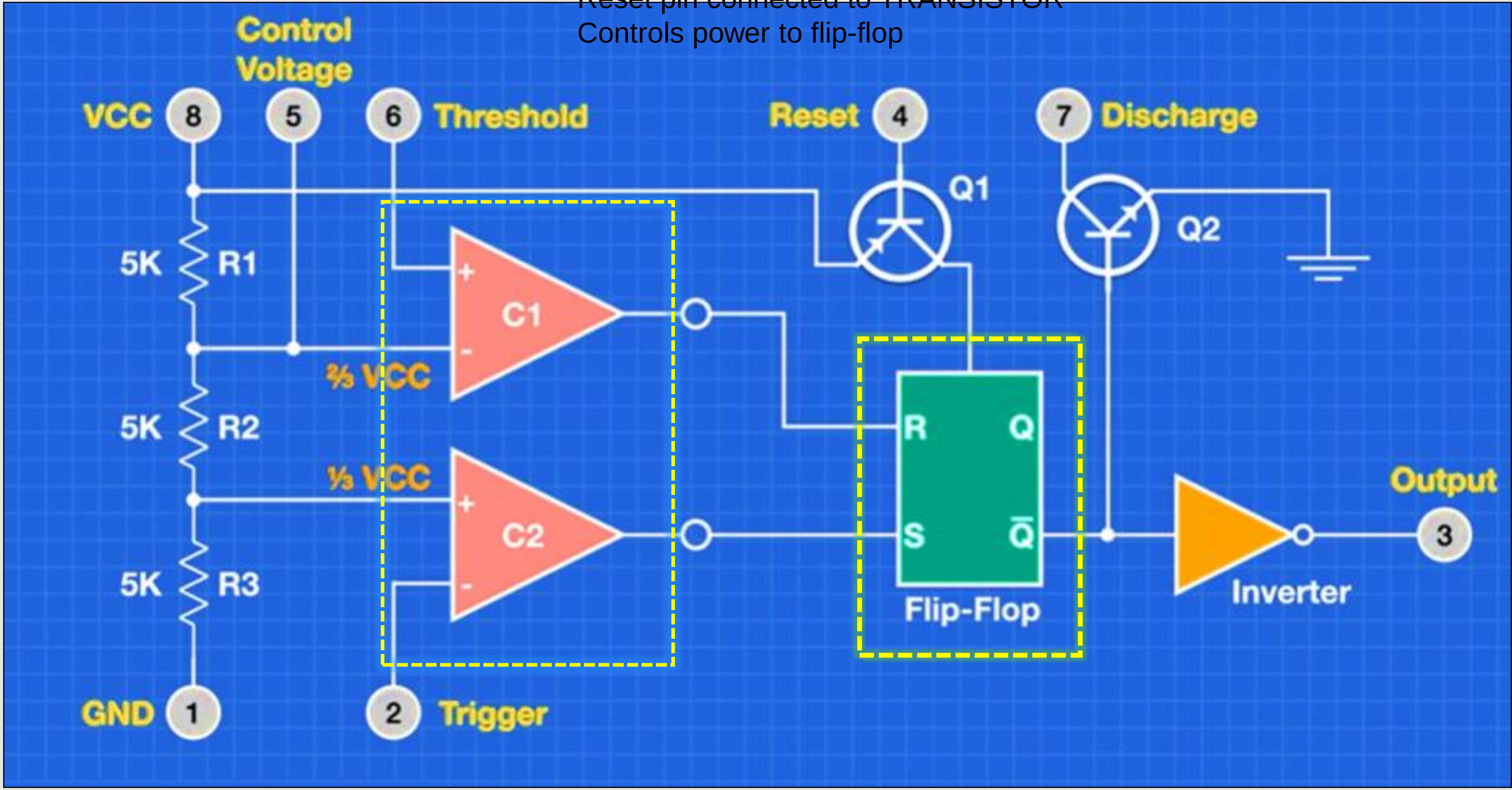


Fig. 9.1 Pin diagram

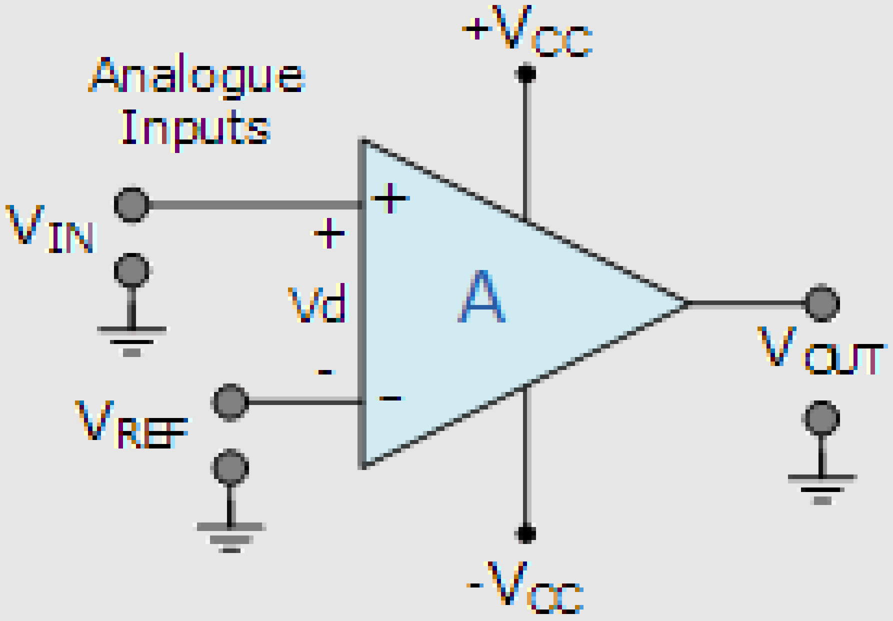
Reset pin connected to TRANSISTOR
Controls power to flip-flop

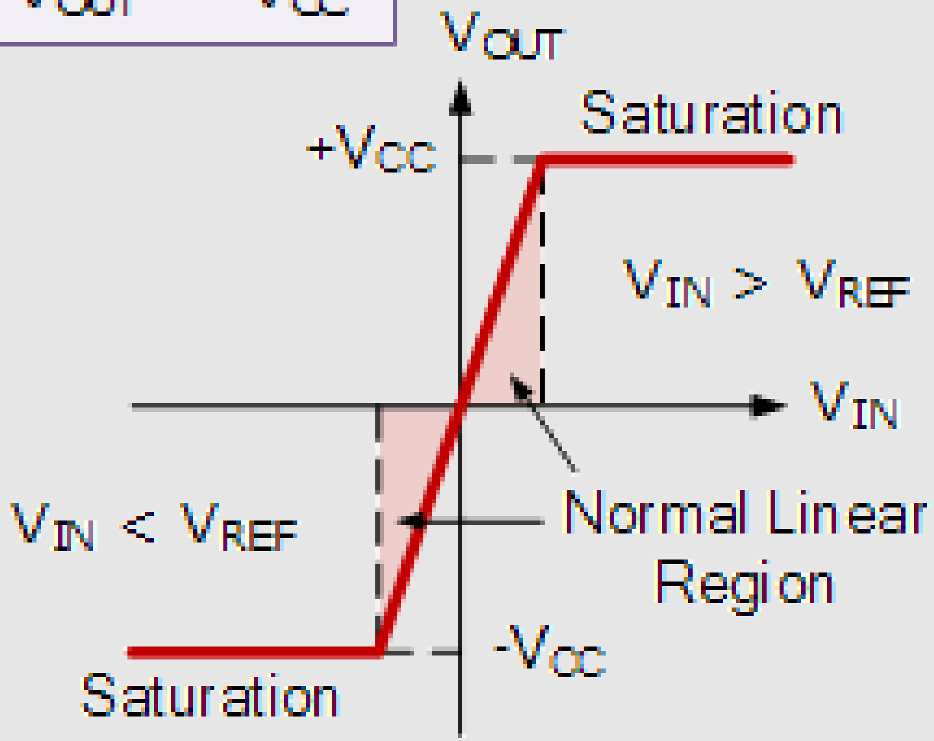


Comparator

As v_1 and v_2 are applied at terminals:
non-inverting(+) and inverting(-)
For infinite gain: v_0 will be in
positive saturation ($+V_{sat}$) if $v_1 > v_2$
negative saturation ($-V_{sat}$) if $v_2 > v_1$

If $V_{IN} > V_{REF}$ then $V_{OUT} = +V_{CC}$
If $V_{IN} < V_{REF}$ then $V_{OUT} = -V_{CC}$





Flip Flop

Threshold	Trigger	R	S	NOT Q
LOW	LOW	LOW	HIGH	LOW
LOW	HIGH	LOW	LOW	LOW
HIGH	HIGH	HIGH	LOW	HIGH
HIGH	LOW	HIGH	HIGH	INVALID

- Set/Reset with Inverted Inputs
- Set and Reset
- Q and Not Q
- Flip-flops and latches are used as data storage elements. A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero".

INPUTS			OUTPUT	STATE
CLK	S	R	Q	
X	0	0	No Change	Previous
↑	0	$\boxed{1}$	0	Reset
↑	$\boxed{1}$	0	1	Set
↑	1	1	-	Forbidden

2. PIN Diagram and Functional diagram

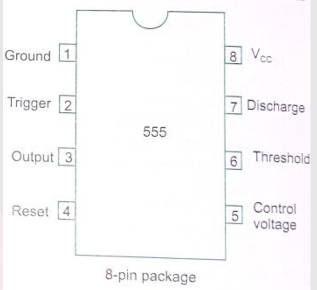


Fig. 9.1 Pin diagram

- **5$k\Omega$ internal resistors**: act as voltage dividers
  Provides bias of $2V_{cc}/3$ to **upper comparator** (UC)
  and Bias of $1V_{cc}/3$ to **lower comparator** (LC)
- These voltage levels are thresholds for comparator and fix timing interval
- **By providing modulation to control voltage at pin 5, time can be varied electronically**
- When no control is needed, connect 0.01μF capacitor between 5 and ground, to bypass noise, ripples.

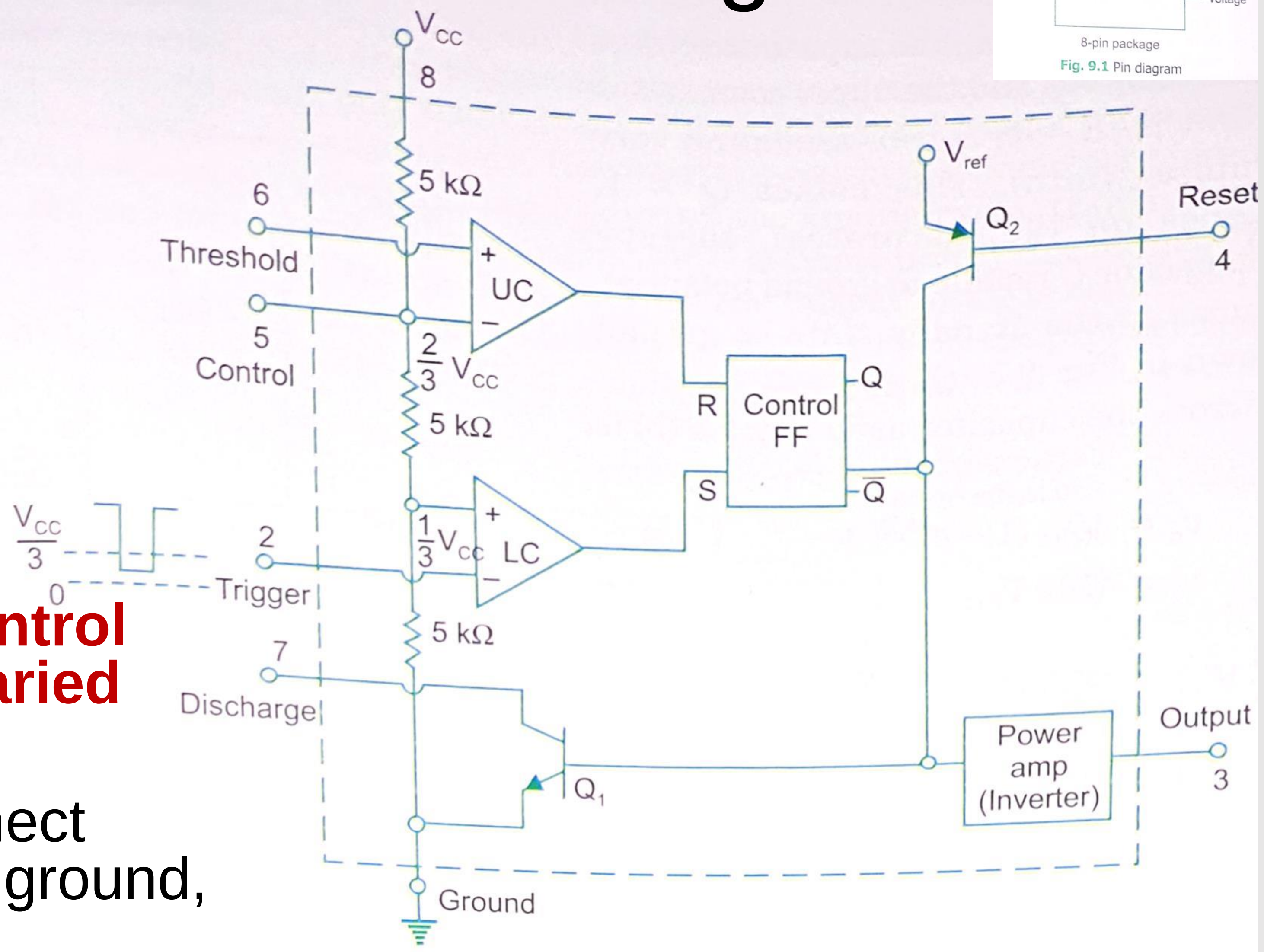


Fig. 9.2 Functional diagram of 555 timer

2. PIN Diagram and Functional diagram

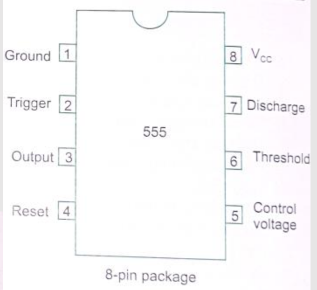


Fig. 9.1 Pin diagram

- In standby(stable state), output $\bar{Q}$ of flipflop (FF) is HIGH, which makes power amp(inverter) output to LOW.
- When negative going trigger (which goes from value above $V_{cc}/3$ to below $V_{cc}/3$) is given to pin 2, output of the comparator LC goes HIGH, Sets flipflop FF: **output Q goes HIGH, $\bar{Q}$ goes LOW,**
- When positive going signal at threshold (pin 6) goes above $2V_{cc}/3$, Output of UC comparator goes HIGH, Resets the flipflop, $\boldsymbol{Q \rightarrow LOW, \bar{Q} \rightarrow HIGH}$

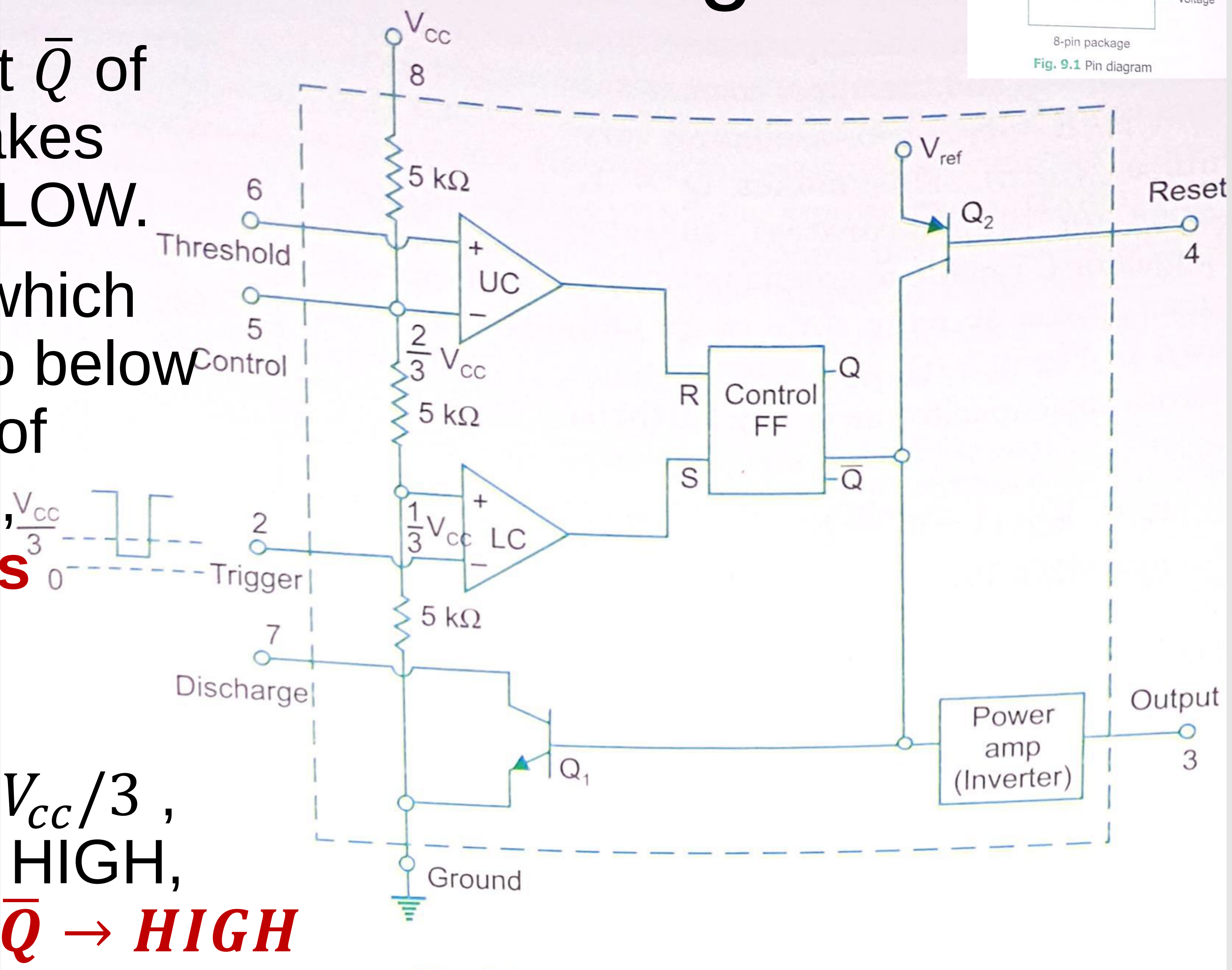


Fig. 9.2 Functional diagram of 555 timer

2. PIN Diagram and Functional diagram

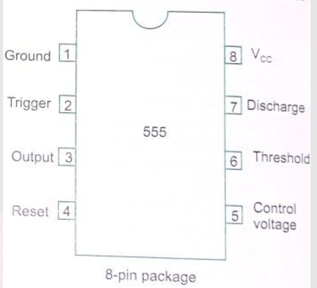


Fig. 9.1 Pin diagram

- RESET pin (4) when enabled(LOW or less than 0.4V for Q2’s PN voltage), this overrides any instruction coming from lower comparator to FF.
- RESET pin(4) when unused, is returned to V_{CC}.
- Q_2 serves as buffer to isolate reset input from FF and transistor Q_1
- Q_2 transistor is driven by V_{ref} (internal reference voltage) which is derived from V_{CC}

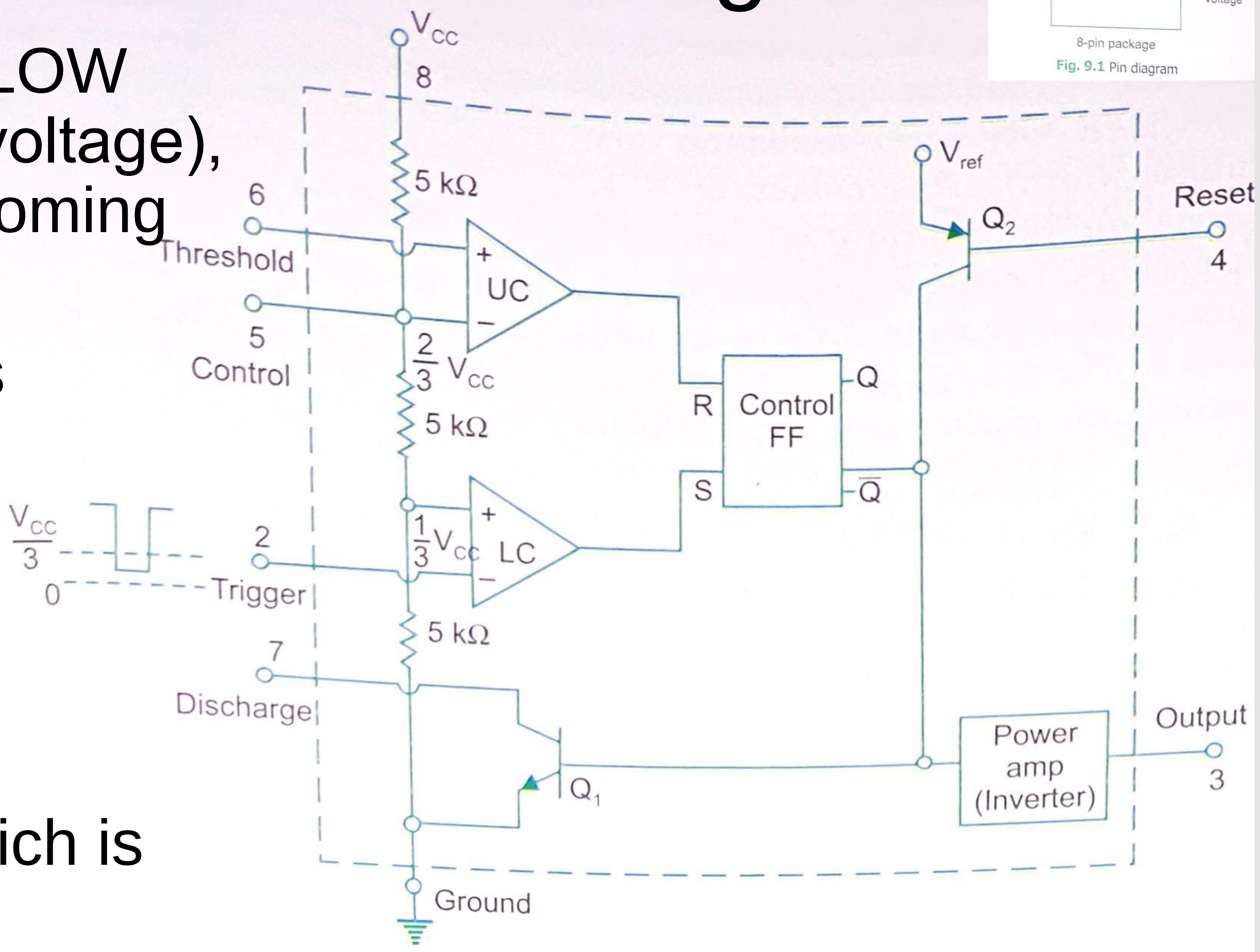


Fig. 9.2 Functional diagram of 555 timer

3. Monostable Operation

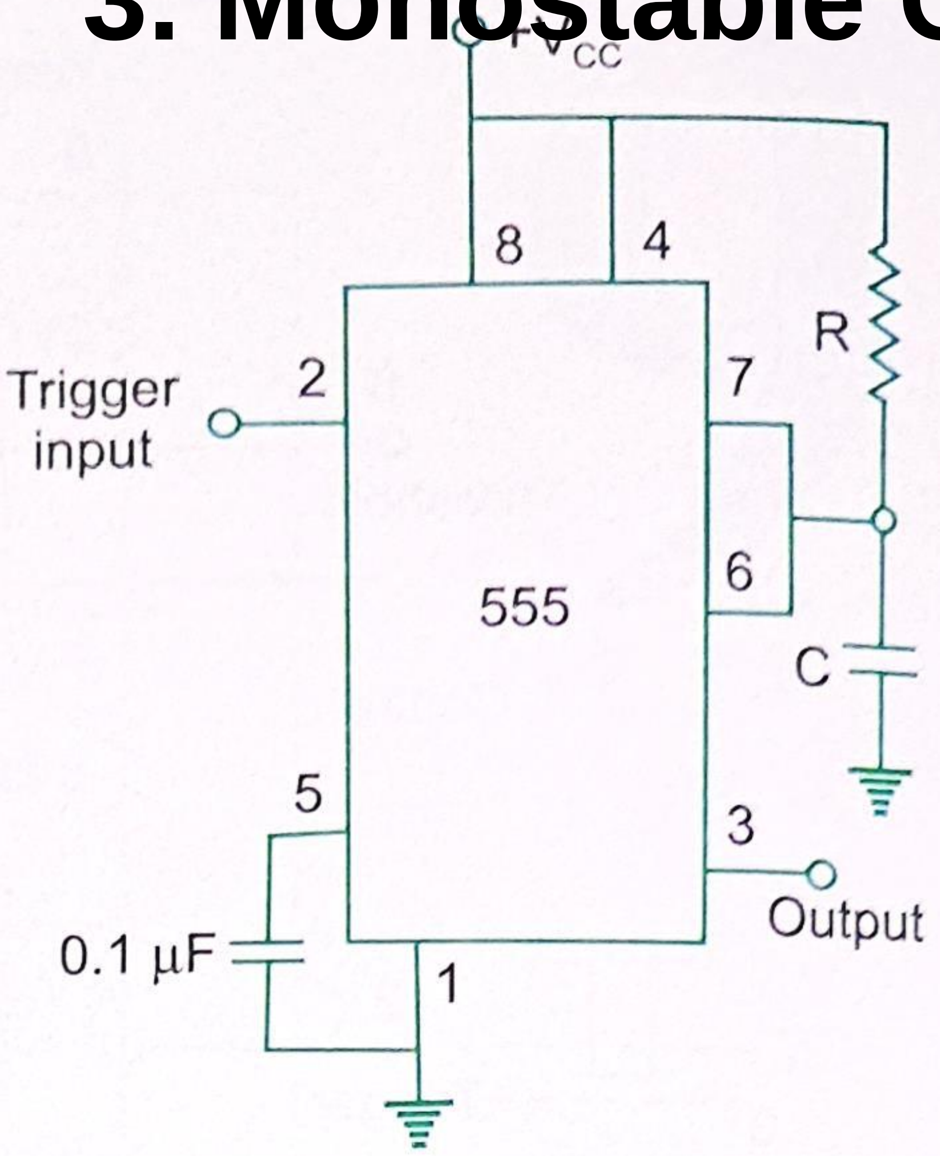
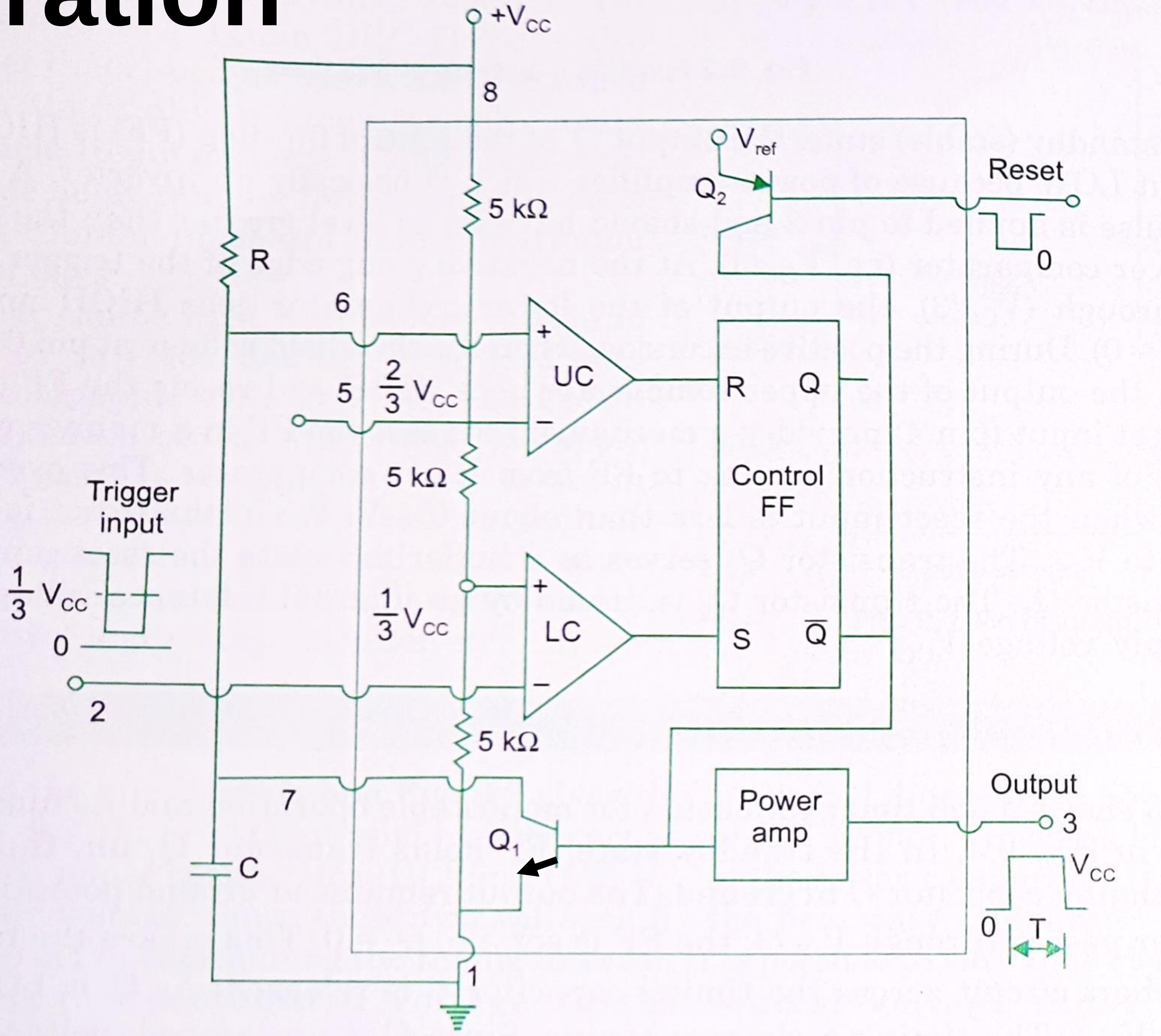


Fig. 9.3 Monostable multivibrator



3. Monostable Operation

- **<u>1. In standby state</u>**:
  ***FF* holds transistor Q_1 on.**
  Thus clamping the external timing capacitor C to ground. Output remains at ground potential (LOW)

<u>2, As trigger passes through</u>
$V_{CC}/3$, FF is set, $Q = 1; \overline{Q} = 0$:
This makes transistor Q_1 off, **previous short circuit across timing capacitor C is removed.**
C is unclamped, voltage across it rises exponentially **through R towards V_{CC} with time constant RC**.

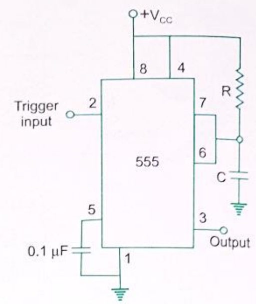
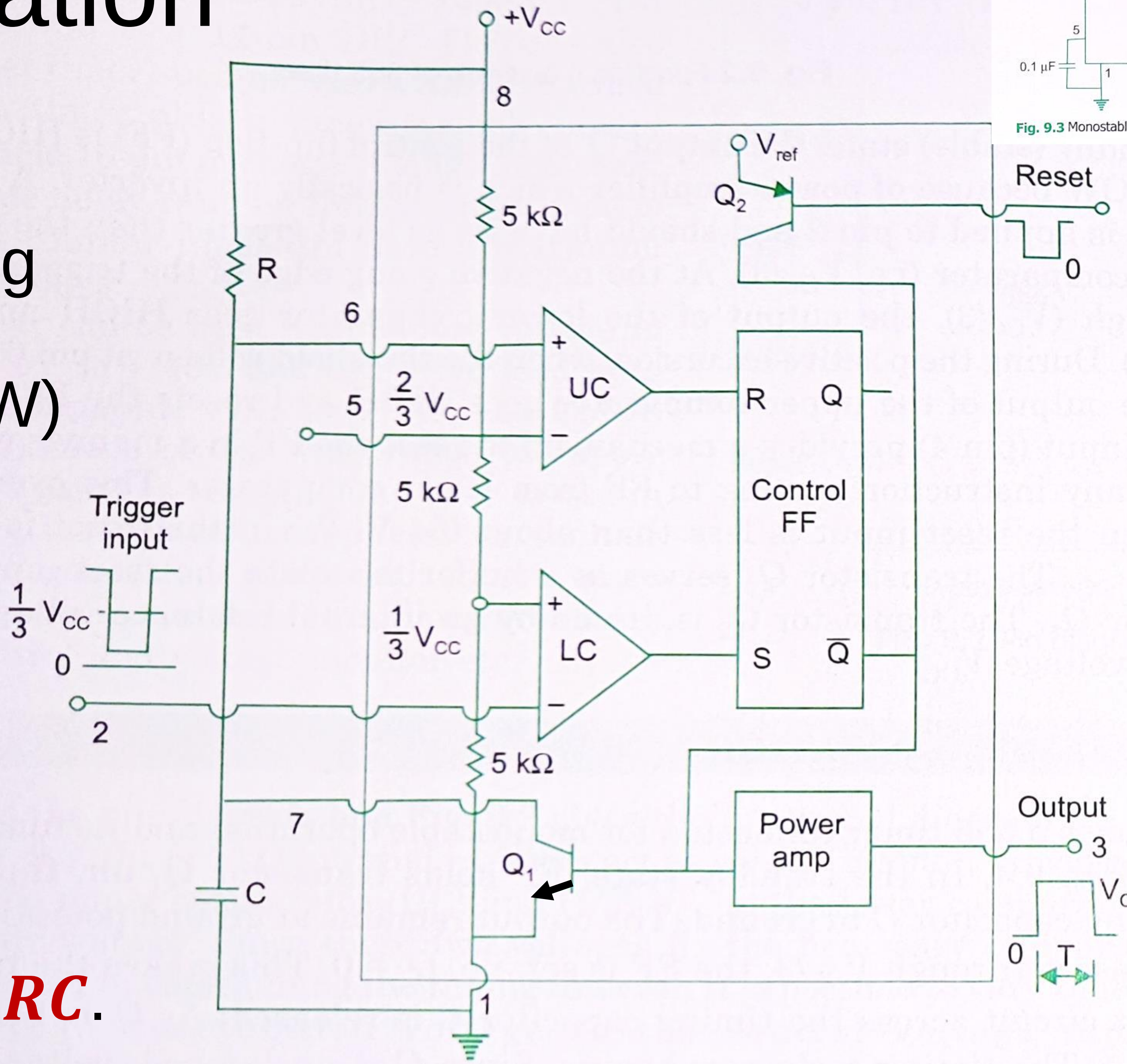
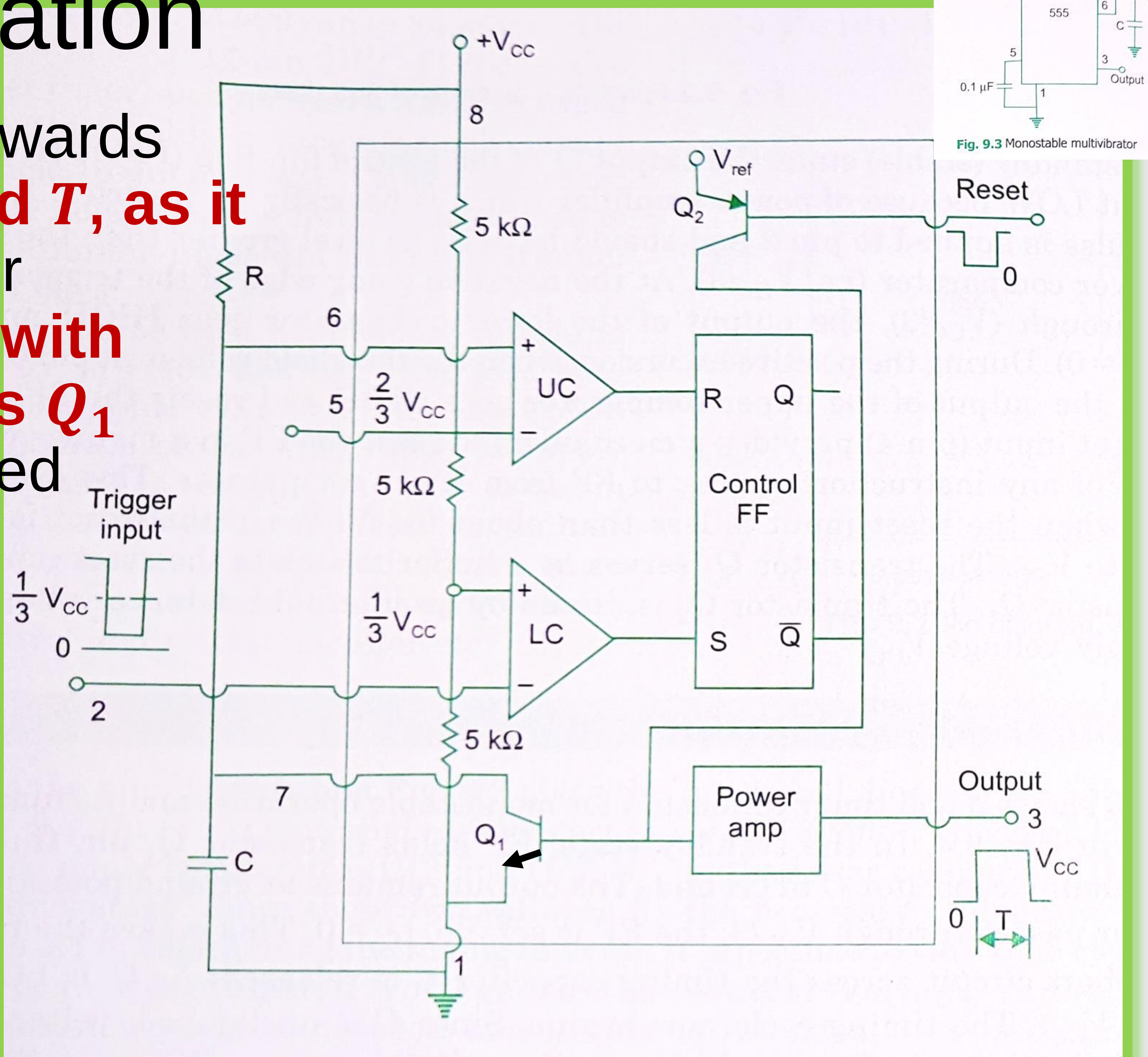


Fig. 9.3 Monostable multivibrator



3. Monostable Operation

- **<u>As capacitor tries to charge</u>** towards **V_{CC}, through R with time period T, as it reaches $2V_{CC}/3$**, UC comparator output is HIGH, and **FF is reset with $Q = 0$ and $\bar{Q} = 1$.** This **saturates Q_1 to be ON**, and capacitor is shorted to ground(discharges) through transistor.
- **The output returns to standby**



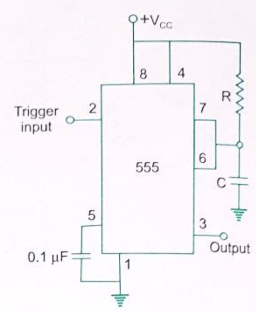


Fig. 9.3 Monostable multivibrator

3. Monostable Operation

- Voltage across capacitor:

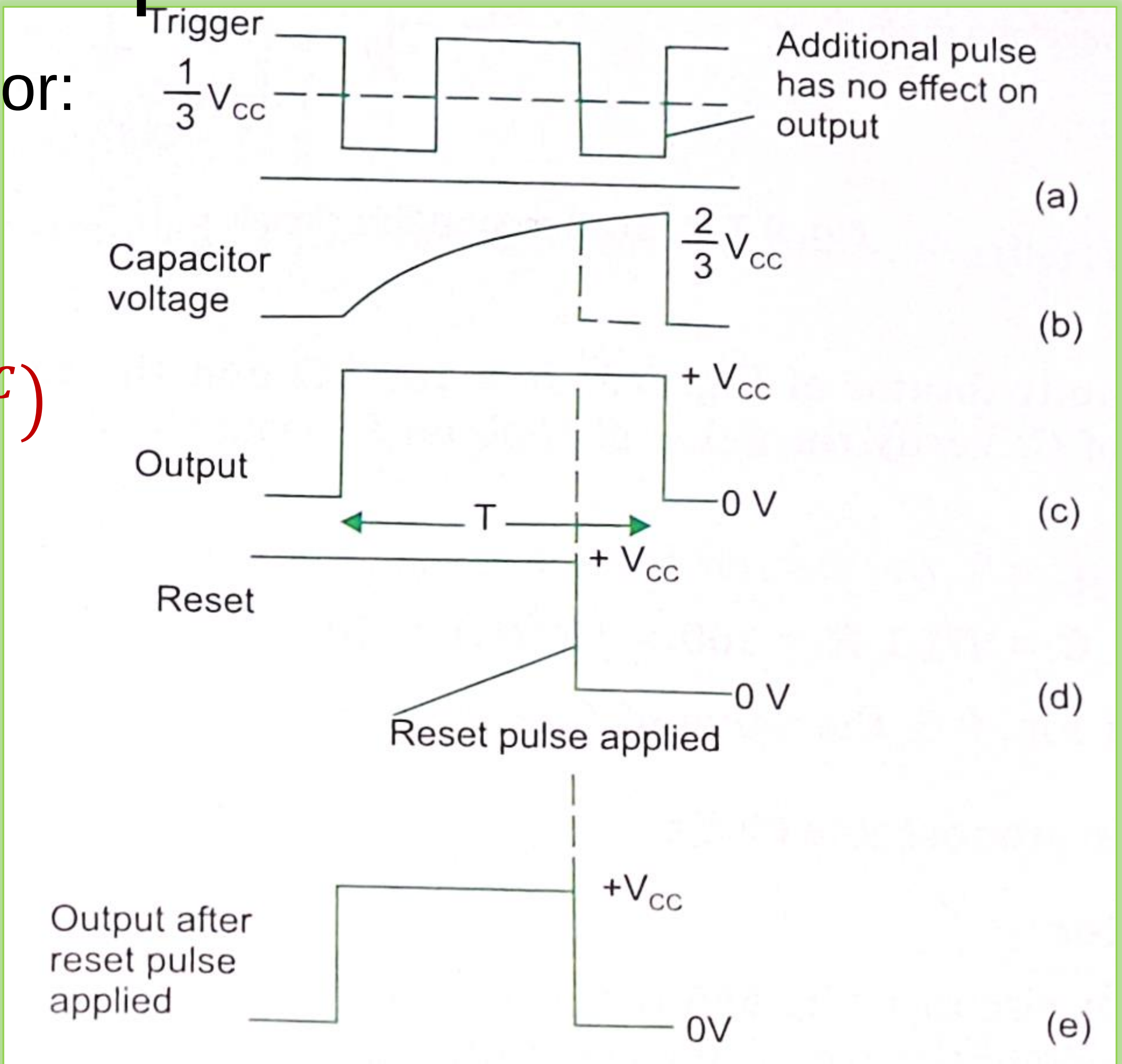
$$v_C = V_{CC}\left(1 - e^{-t/RC}\right)$$

- At $t = T$, $v_C = \frac{2}{3}V_{CC}$

$$\boldsymbol{\frac{2}{3}V_{CC} = V_{CC}\left(1 - e^{-t/RC}\right)}$$

$$\boldsymbol{T = RC\ln(1/3)}$$

$$\boldsymbol{T = 1.1\,RC\ (seconds)}$$



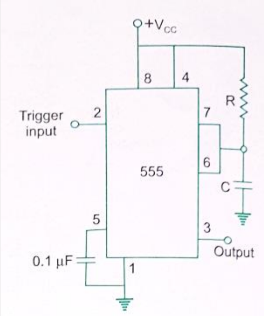


Fig. 9.3 Monostable multivibrator

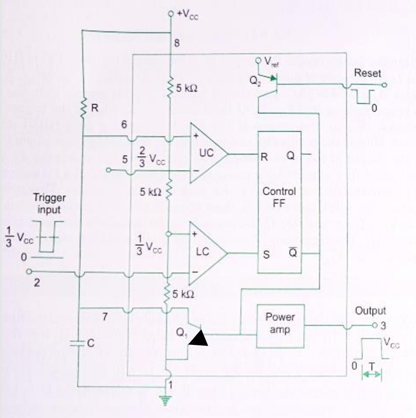


Fig. 9.4 Timer in monostable operation with functional diagram

3. Monostable Operation

- But, **when negative RESET input is given, Q_2 is ON**,
  This saturates Q_1 and output will remain low until RESET is removed.
- When **RESET input goes high, until a negative trigger is initiated, Capacitor will not initiate charging and output remains low until the negative trigger input is given at pin 2**.

- then output will go to LOW

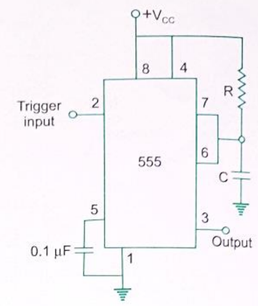
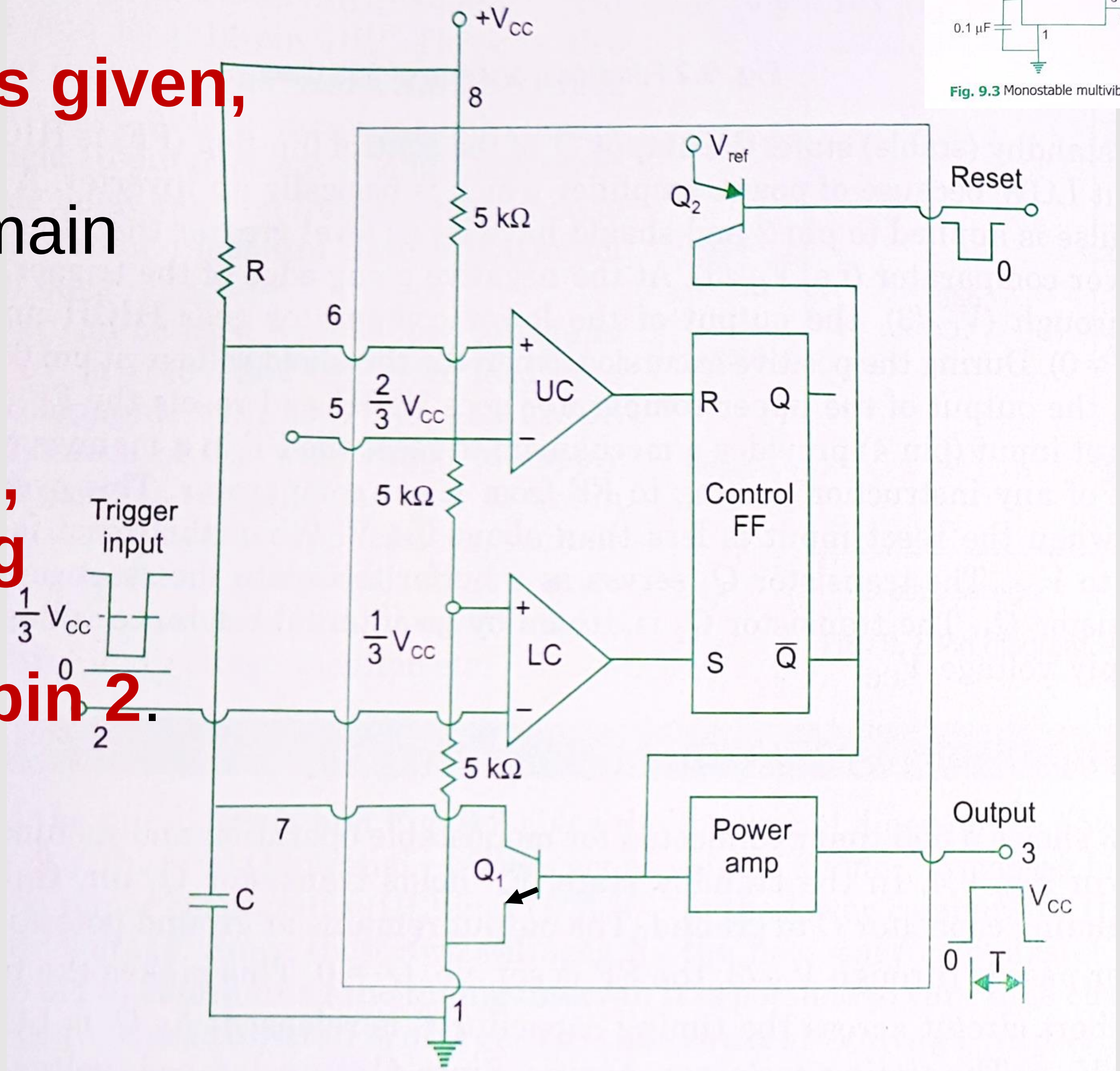


Fig. 9.3 Monostable multivibrator



3.2 Problem

- In monostable multivibrator, $R = 100k\Omega$, $T = 100\ ms$. Calculate the value of C.
- $T = 1.1\ RC$

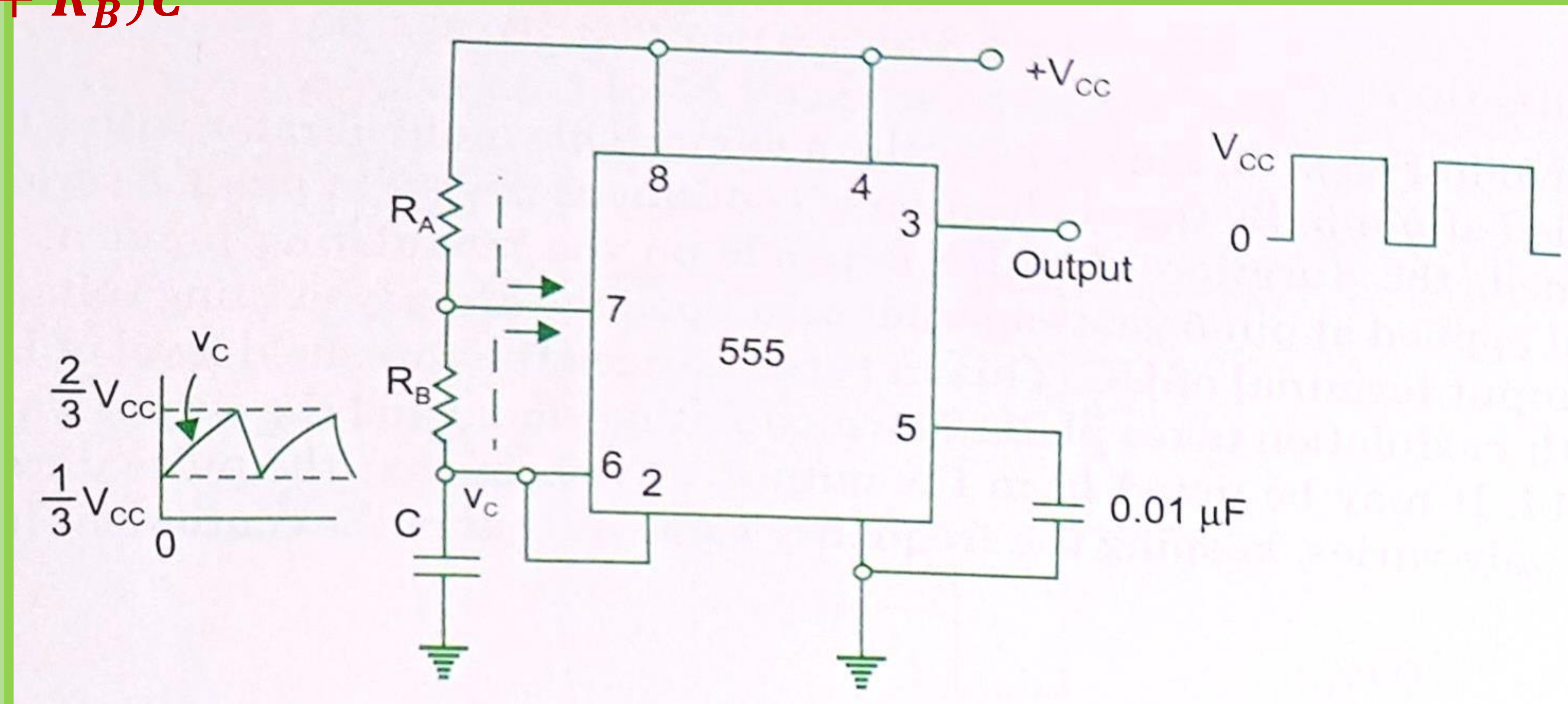
$$C = \frac{\boldsymbol{T}}{\boldsymbol{1.1R}} = \frac{\boldsymbol{100 \times 10^{-3}}}{\boldsymbol{1.1 \times 100 \times 10^{3}}} = \boldsymbol{0.9\mu F}$$

4. Applications of Monostable mode:

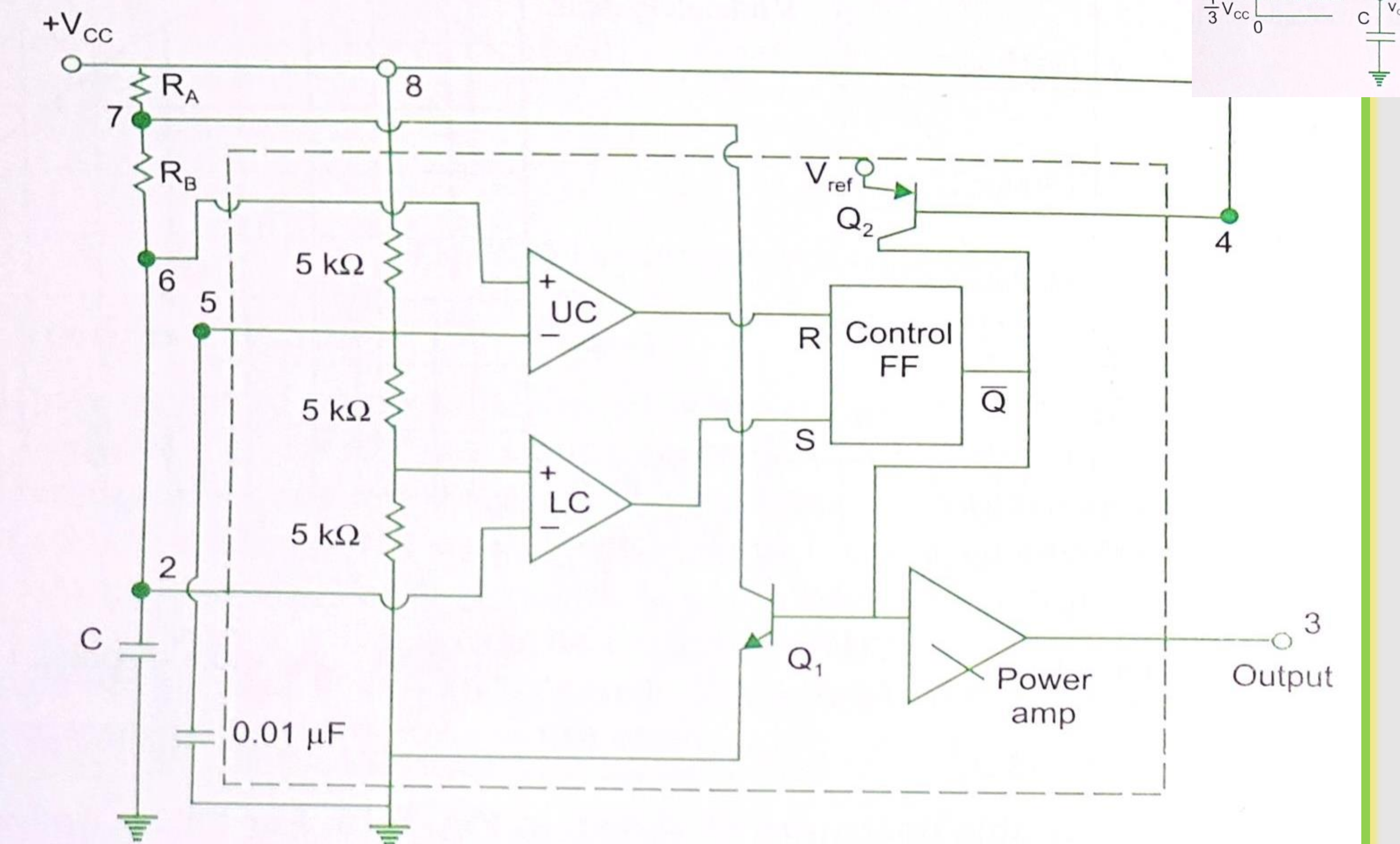
- Missing pulse detector
- Linear ramp generator
- Frequency divider
- Pulse width modulator

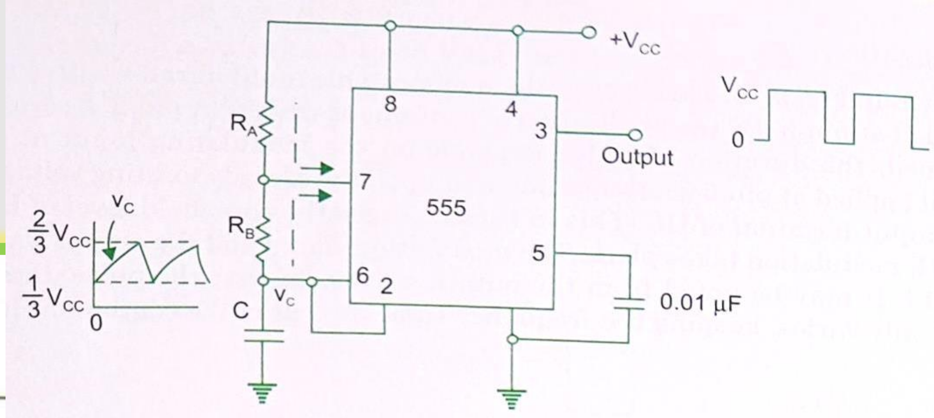
Astable Multivibrator

- **Timing resistor is split into two (R_A and R_B)**
  Pin 7(discharging transistor path) is connected between R_A and R_B
- When V_{CC} is connected, **Capacitor charges towards V_{CC} with time constant $(R_A + R_B)C$**



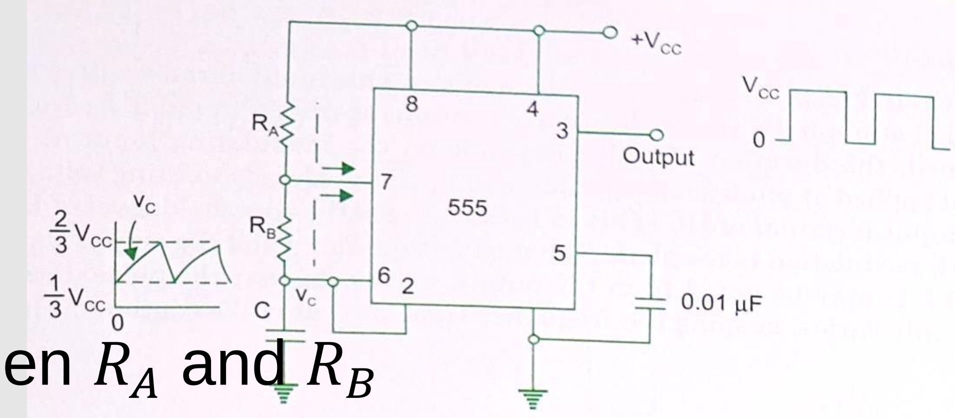
1. Astable Multivibrator



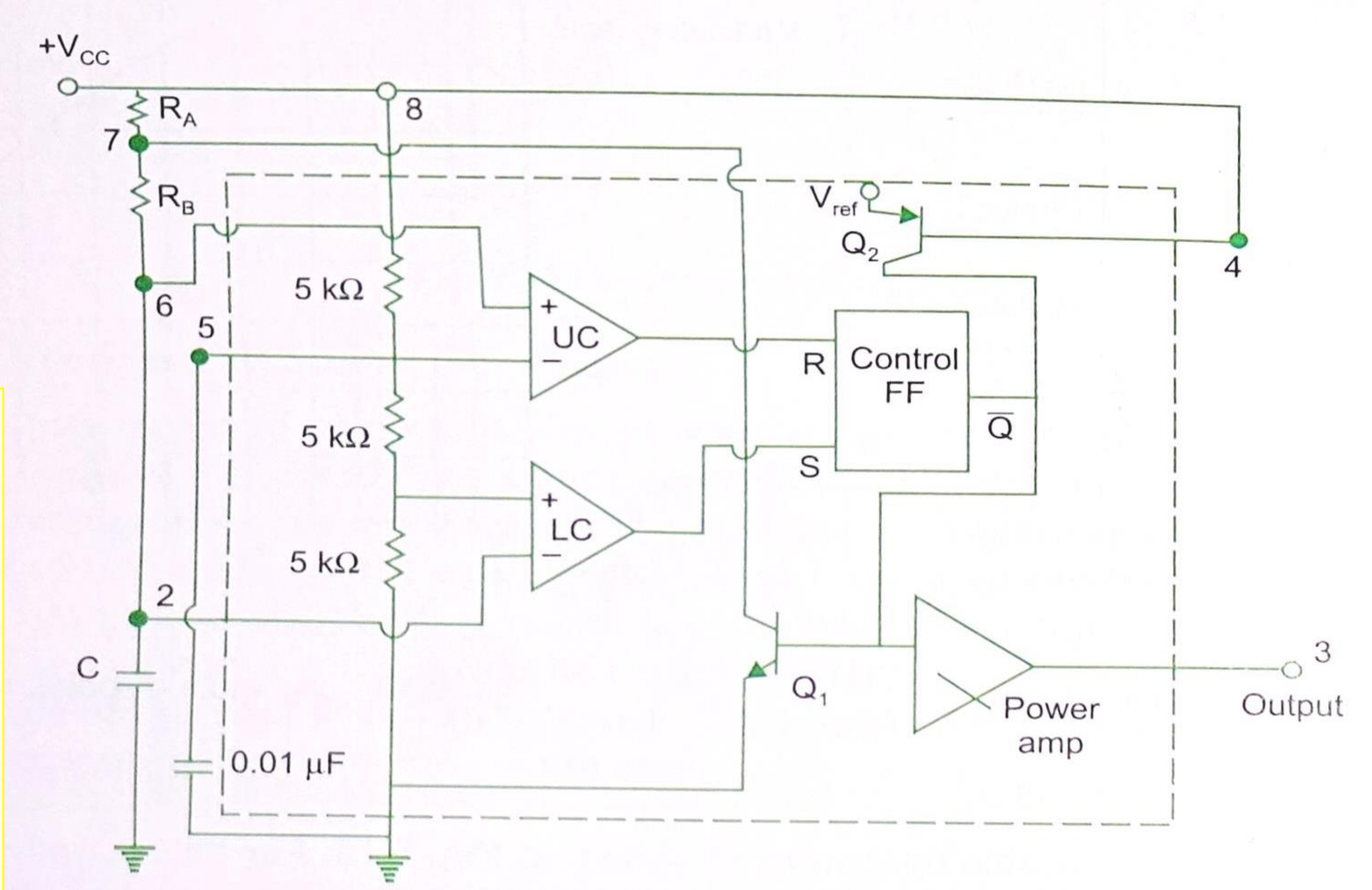


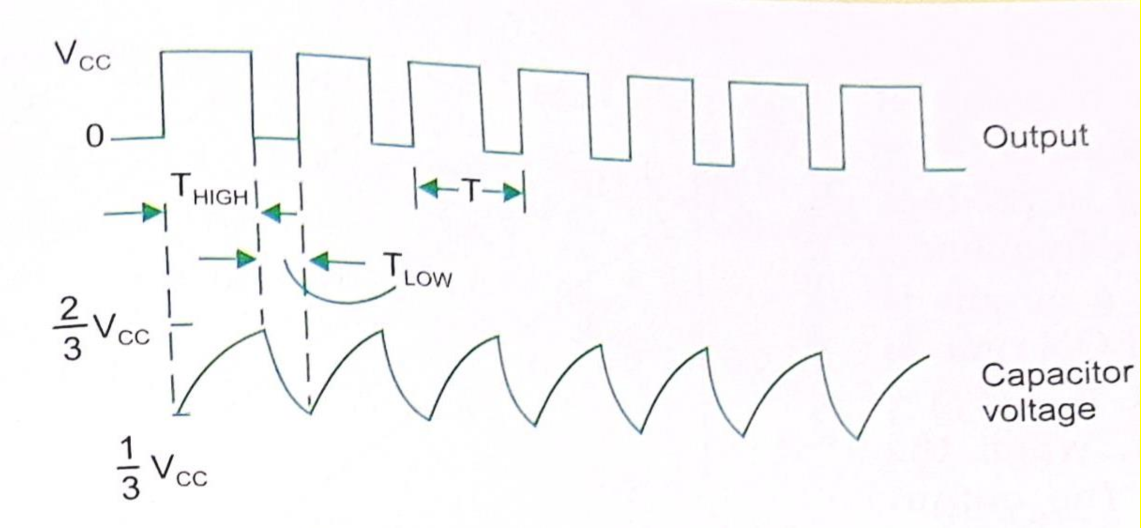
Courtesy:Roy Choudhury et al.

1. Astable Multivibrator



- Timing resistor is split into two (R_A and R_B)
  Pin 7(discharging transistor path) is connected between R_A and R_B
- When V_{CC} is connected, Capacitor charges towards V_{CC} with time constant $(R_A + R_B)C$. While charging, output pin 3 is HIGH, since $R = 0, S = 1, \bar{Q} = 0$, unclamped capacitor C
  (Q1 transistor not operational)





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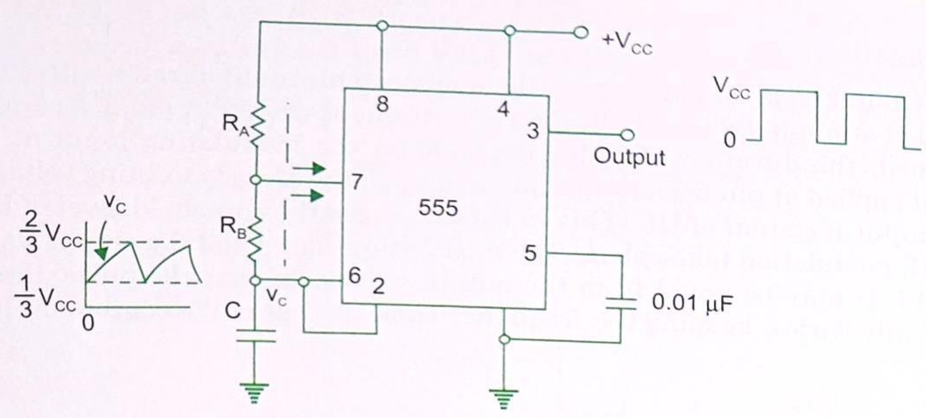
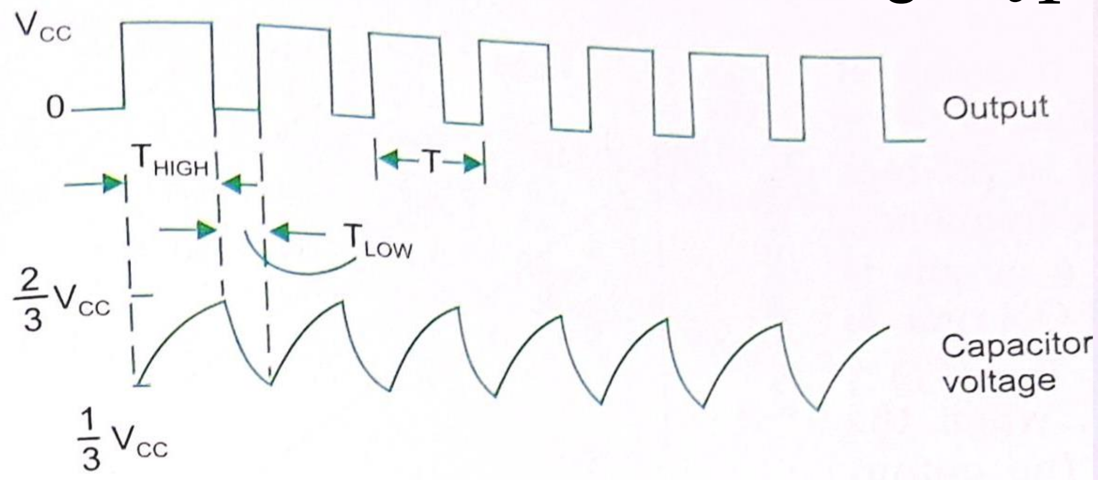
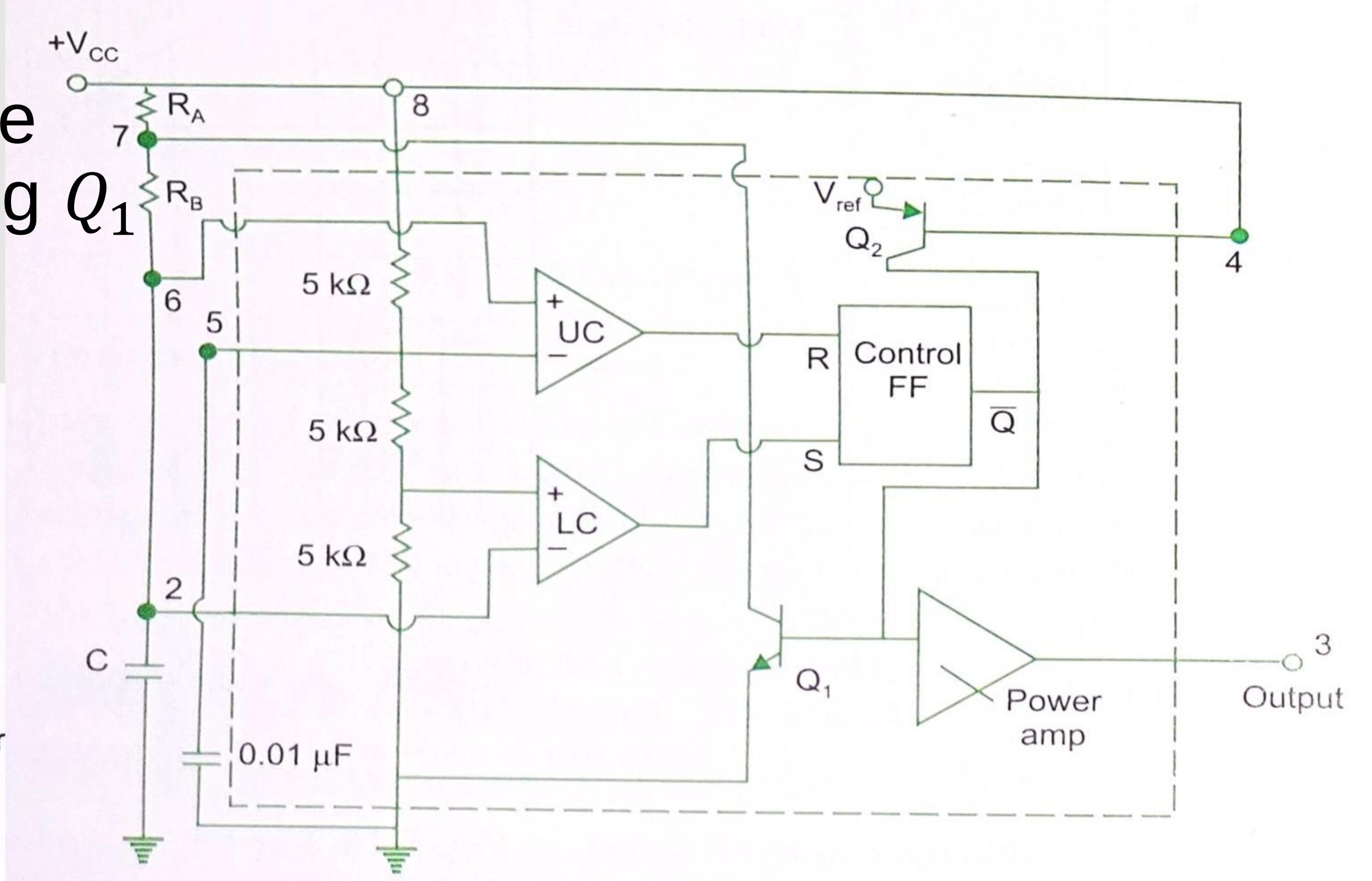


- When Capacitor voltage equals $2V_{CC}/3$, upper comparator triggers control **FF $\bar{Q} = 1$**
  Transistor Q_1 will be ON, capacitor will discharge through R_B, Q_1 with time constant $R_B C$
- R_A, R_B are large values to reduce discharge current from damaging Q_1
- Min value of $R_A = V_{CC}/0.2\text{A}$
  0.2 A is max current through Q_1





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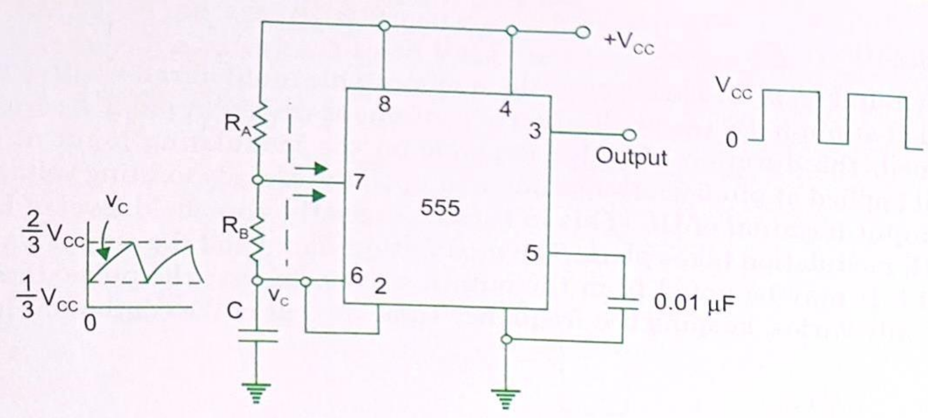
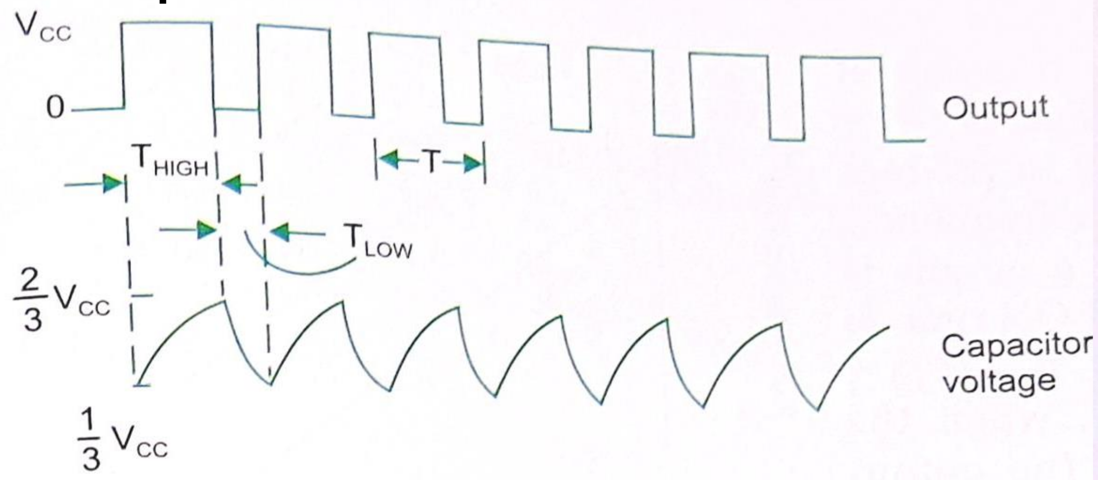
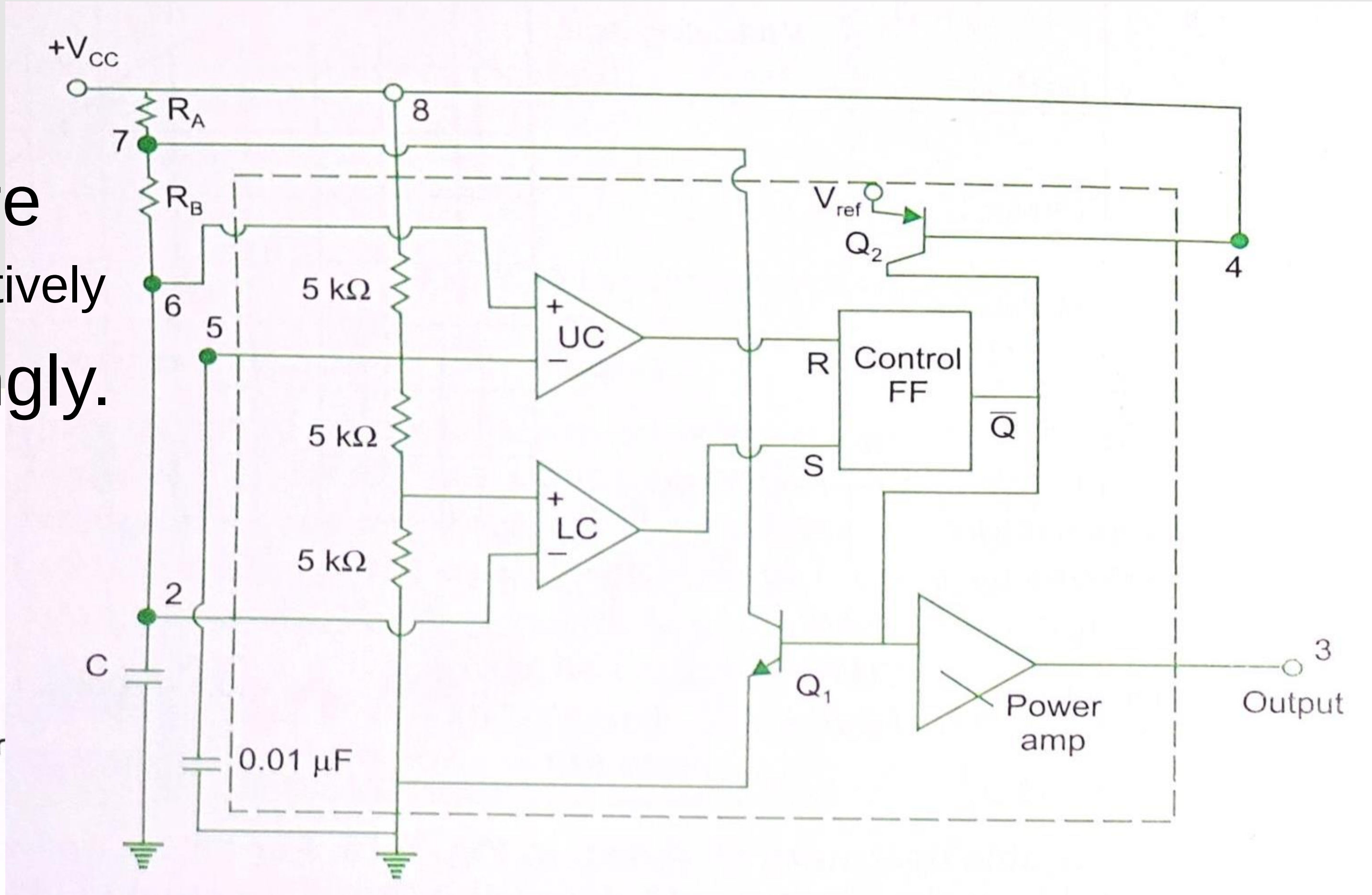


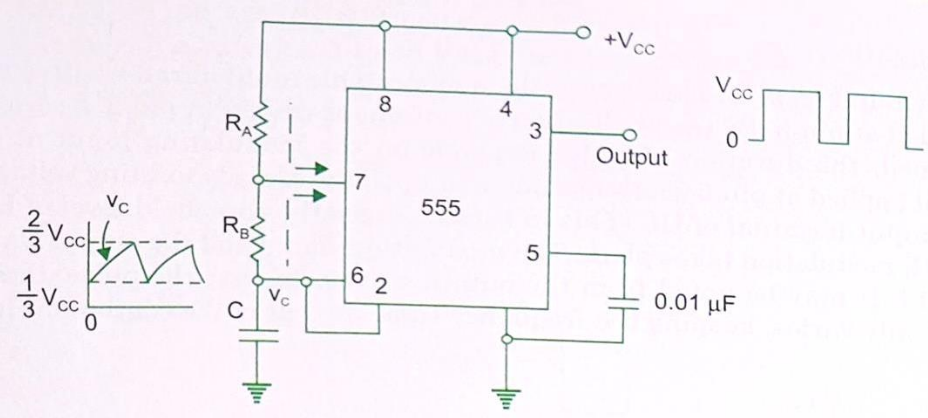
- During discharge of timing capacitor, when voltage of capacitor reaches $V_{CC}/3$, Lower comparator is triggered, S=1, R=0, $\bar{Q} = 0$, transistor Q_1 OFF. Stops discharge as external timing capacitor is unclamped.
- Capacitor now charges as before and discharges as above, Alternatively
- Output hence switches accordingly.

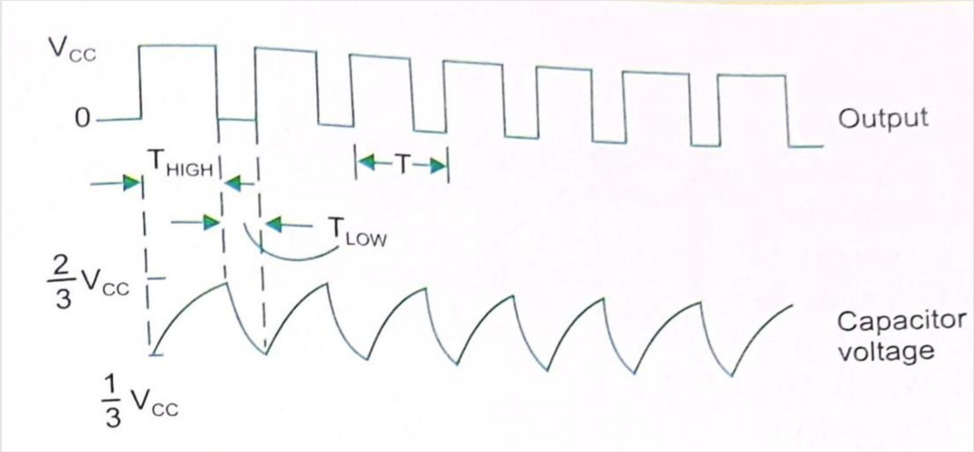


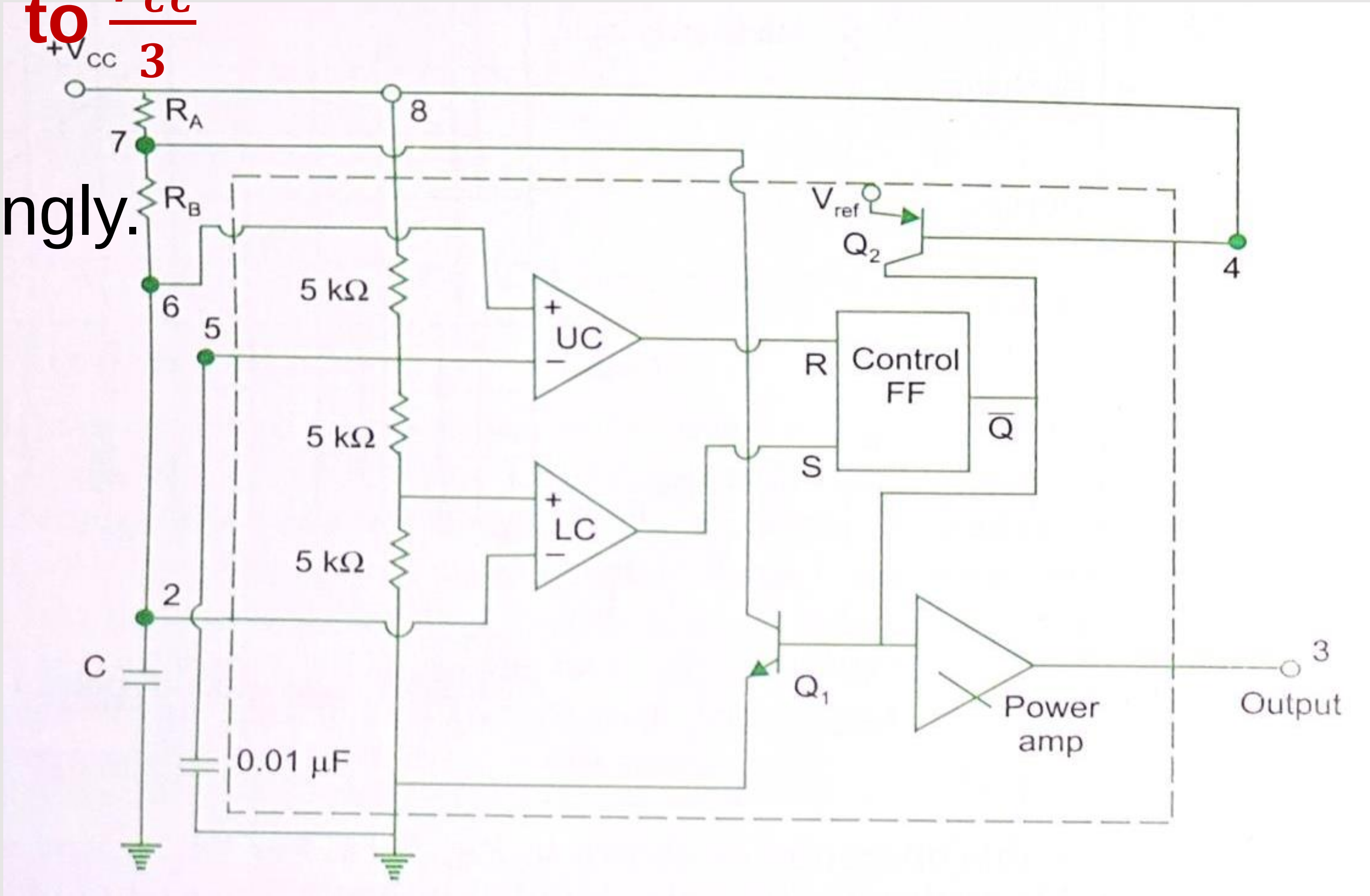


1. Astable Multivibrator

- **Capacitor charges from $V_{CC}/3$ to $\frac{2V_{CC}}{3}$ through $R_A + R_B$ and discharges from $2V_{CC}/3$ to $\frac{V_{CC}}{3}$ through R_B**
- Output hence switches accordingly. (ON while charging, OFF when discharging)







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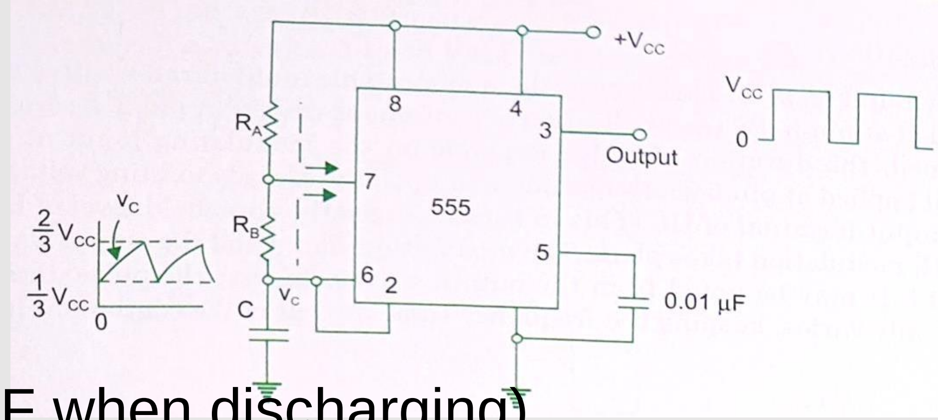
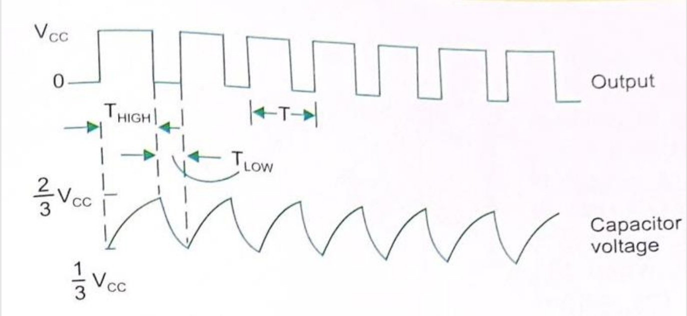
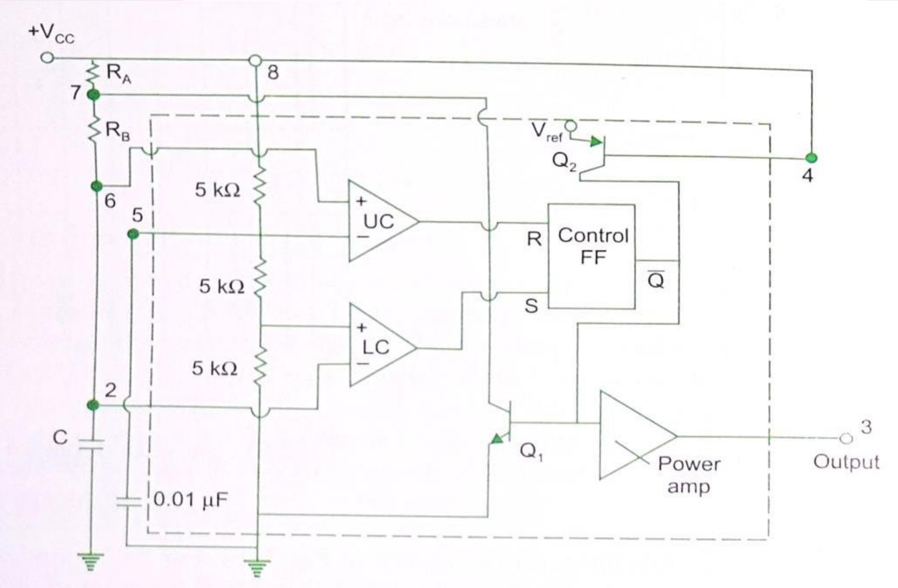


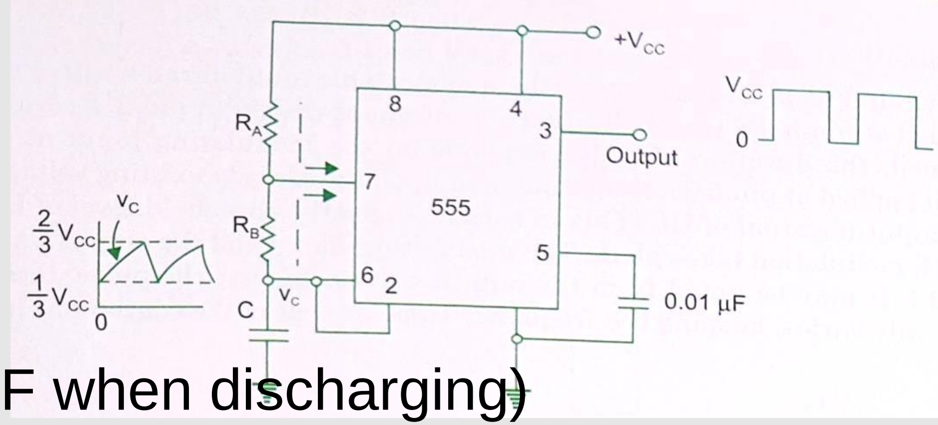
- Capacitor charges from $V_{CC}/3$ to $2V_{CC}/3$ through $R_A + R_B$ and discharges from $2V_{CC}/3$ to $V_{CC}/3$ through R_B
- Output hence switches accordingly. (ON while charging, OFF when discharging)
- **Charging capacitor voltage $v_o = V_{CC}\left(1 - e^{-t/RC}\right)$**
- **t_1: Time to charge from 0 upto $2V_{CC}/3$,**
  t_2: Time to charge from 0 upto $V_{CC}/3$,



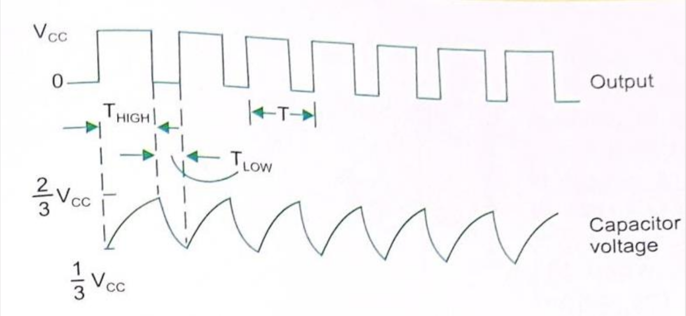
- $v_c(t_1) = \frac{2V_{cc}}{3} = V_{CC}\left(1 - e^{-t_1/RC}\right) \quad t_1 = 1.09RC$
  $v_c(t_2) = \frac{V_{cc}}{3} = V_{CC}\left(1 - e^{-t_2/RC}\right) \quad t_2 = 0.405\,RC$
- $t_{HIGH} = t_1 - t_2$: Time to charge from $\frac{V_{CC}}{3}$ upto $2\frac{V_{CC}}{3}$,
  $= RC(1.09 - 0.405)$
  $= 0.69RC = 0.69(R_A + R_B)C$



1. Astable Multivibrator

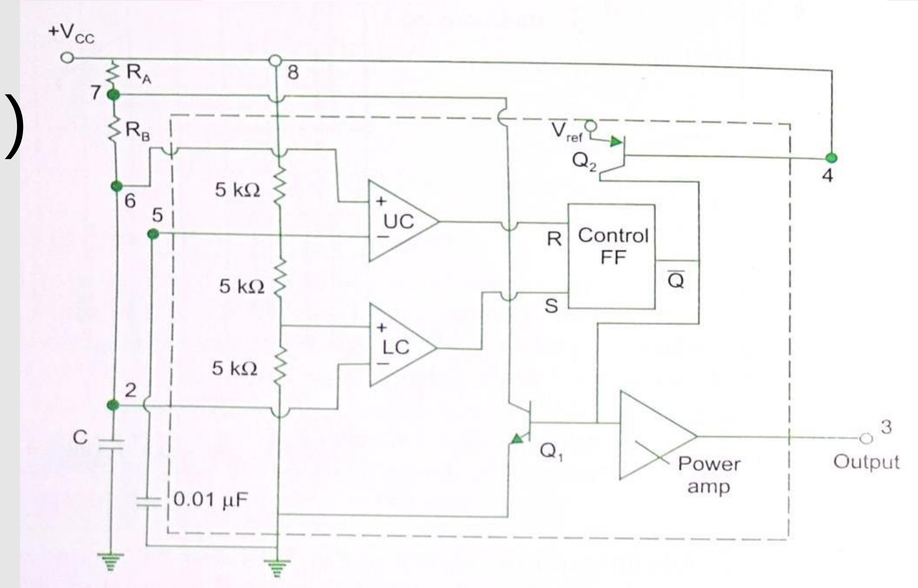


- Capacitor charges from $V_{CC}/3$ to $2V_{CC}/3$ through $R_A + R_B$ and discharges from $2V_{CC}/3$ to $V_{CC}/3$ through R_B
- Output hence switches accordingly. (ON while charging, OFF when discharging)
- $\boldsymbol{t_{HIGH} = 0.69(R_A + R_B)C}$
- Discharging capacitor voltage $v_c = V_{initial}\left(e^{-t/RC}\right)$
- t_{LOW}: Time to discharge from $2V_{CC}/3$ upto $V_{CC}/3$,

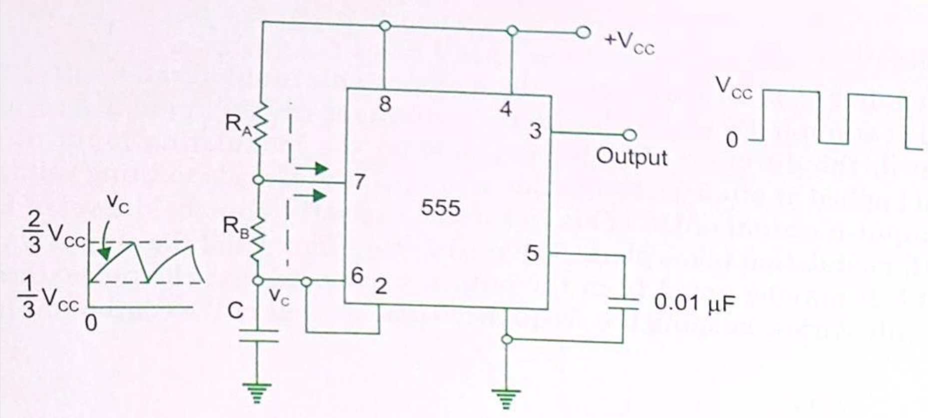


- $v_c(t_{LOW}) = \frac{V_{CC}}{3} = \frac{2V_{CC}}{3}\left(e^{-t_{LOW}/RC}\right)$

  $\boldsymbol{t_{LOW} = 0.69RC = 0.69R_BC}$
- Time period (one cycle of charging and discharging) = Time period of output voltage
- $T = t_{HIGH} + t_{LOW} = 0.69(R_A + 2R_B)C$
- Frequency of oscillation $f = \frac{1}{T} = \frac{1.45}{(R_A+2R_B)C}$

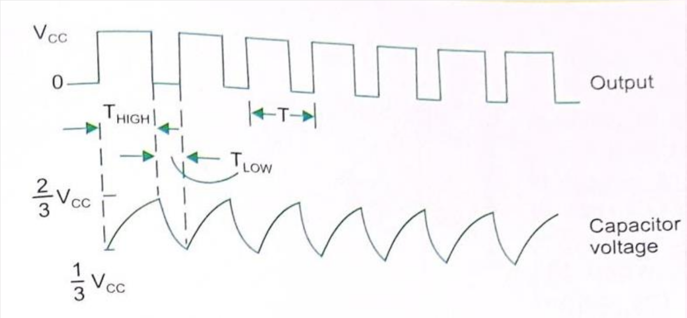


1. Astable Multivibrator



- $t_{HIGH} = 0.69(R_A + R_B)C$
- $t_{LOW} = 0.69 R_B C$
- $T = t_{HIGH} + t_{LOW} = 0.69(R_A + 2R_B)C$
- $f = \frac{1}{T} = \frac{1.45}{(R_A+2R_B)C}$
- Wrt transistor Q_1, when ON, output goes low
- **Duty cycle $D\% = \frac{t_{LOW}}{T} \times 100\%$**

$$D\% = \frac{R_B}{(R_A+2R_B)} \times 100\%$$



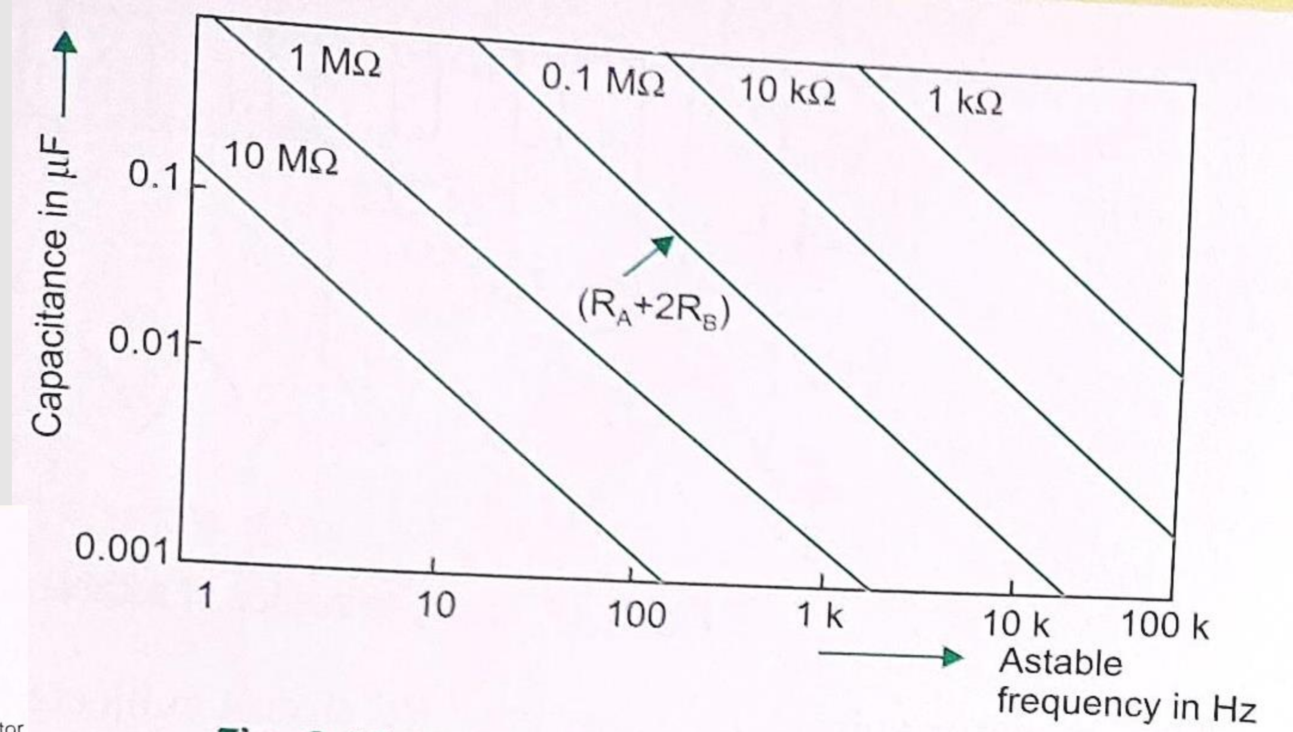


Fig. 9.18 Frequency dependence of R_A, R_B and C

2. Astable with adjustable duty cycle

- With this circuit $t_{HIGH} = 0.69 R_A C$
- $t_{LOW} = 0.69 R_B C$
- $T = t_{HIGH} + t_{LOW} = 0.69(R_A + R_B)C$
- $f = \frac{1.45}{(R_A + R_B)C}$
- Duty cycle $D\% = \frac{R_B}{R_A + R_B} \times 100\%$

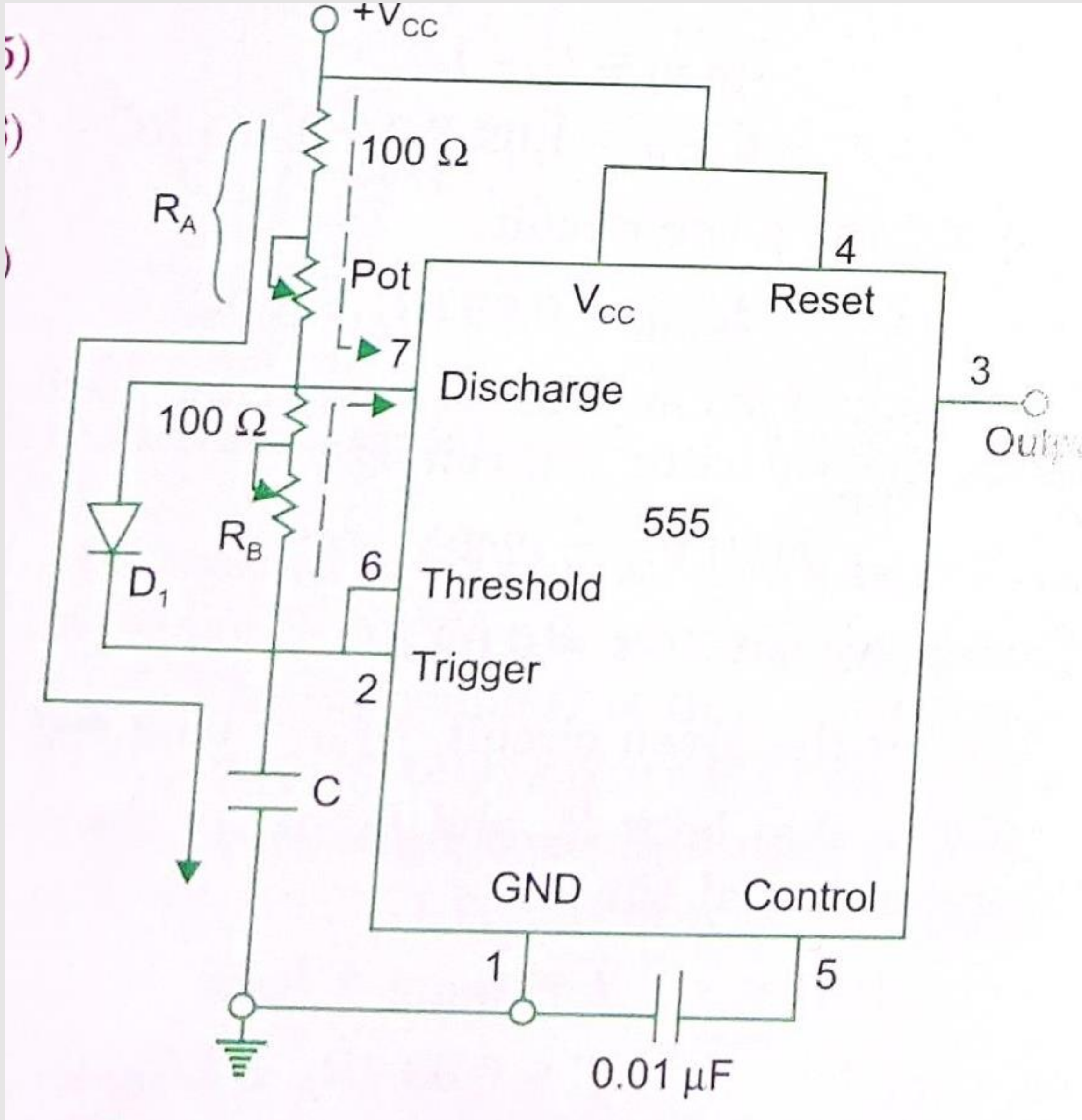


Fig. 9.19 Adjustable duty cycle rectangular wave generator

3.4 Applications of Astable operations

- Schmitt trigger

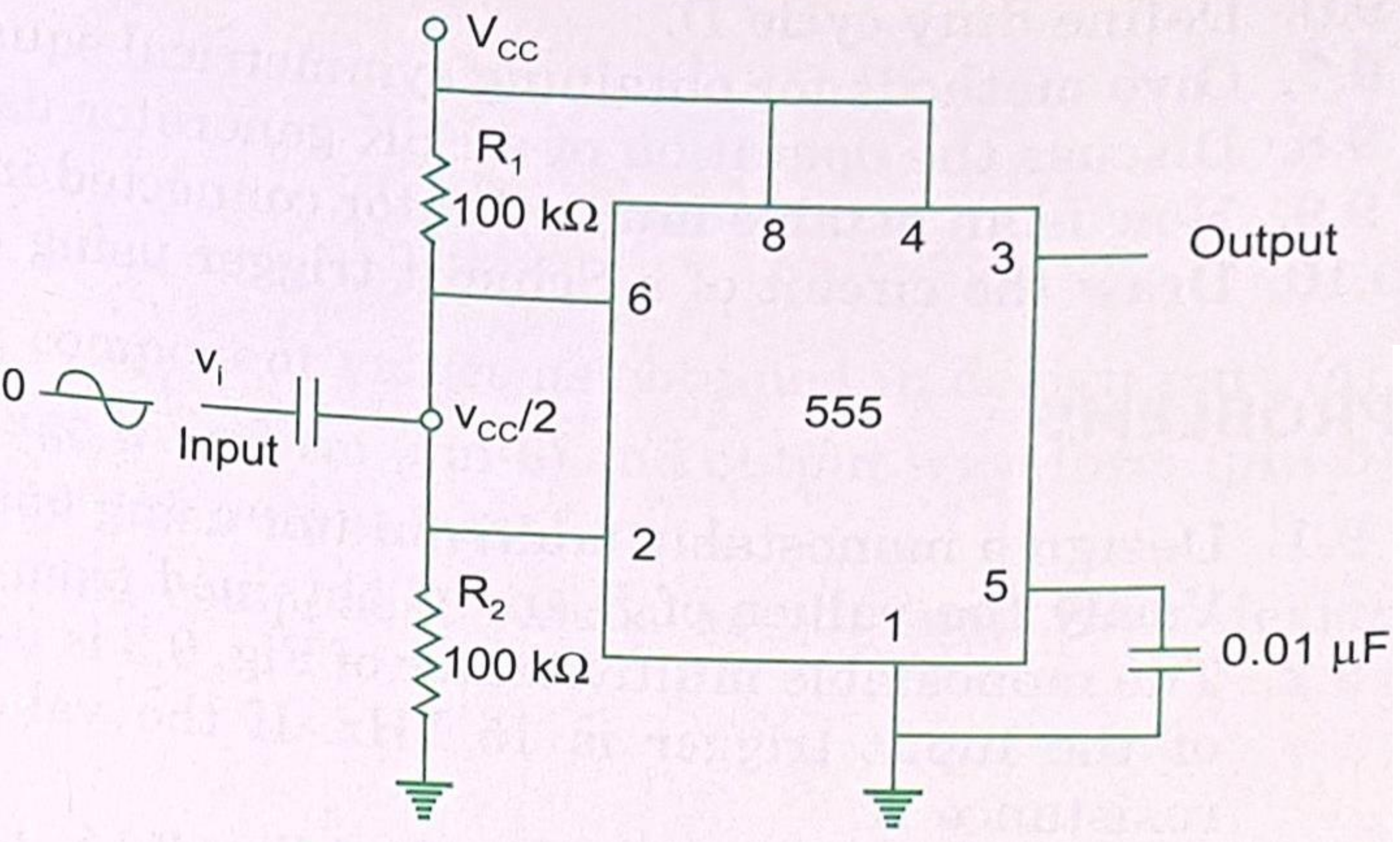


Fig. 9.24 Timer in Schmitt Trigger Operation

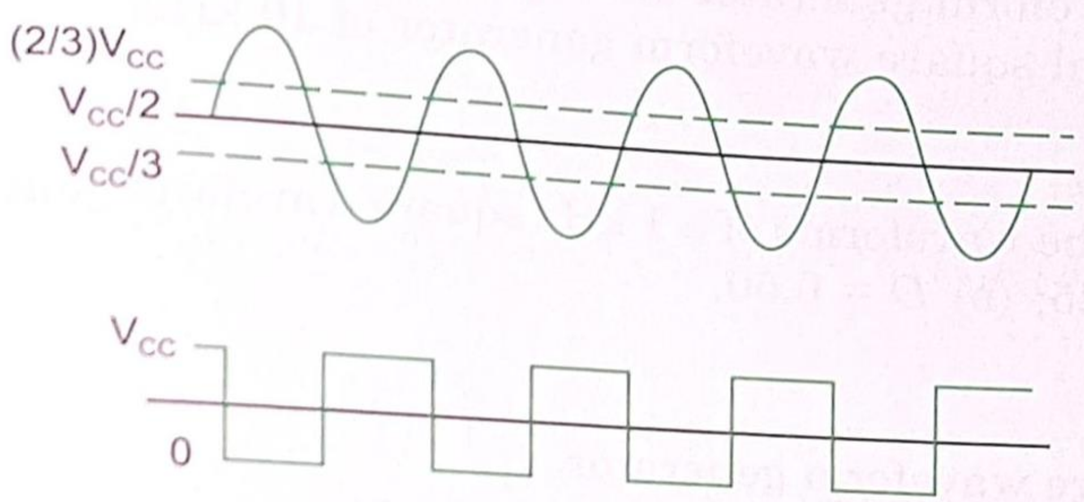


Fig. 9.25 Input output waveforms of Schmitt Trigger