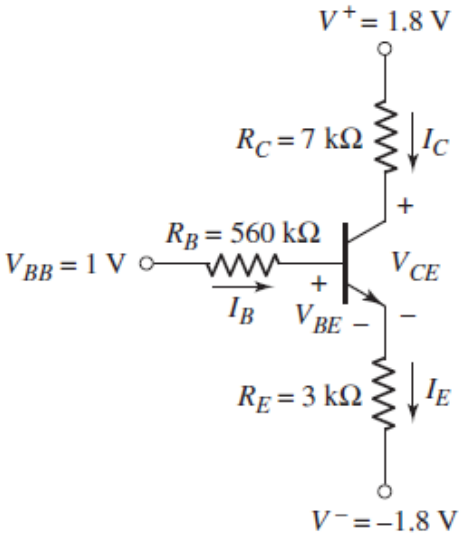
Practice Questions (Module 01- Module 04)

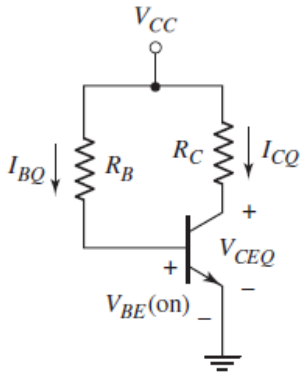
Problem 01

Calculate the characteristics of a circuit containing an emitter resistor. For the circuit shown in Figure, let V_{BE}(on) = 0.7 V and β = 75. Note that the circuit has both positive and negative power supply voltages



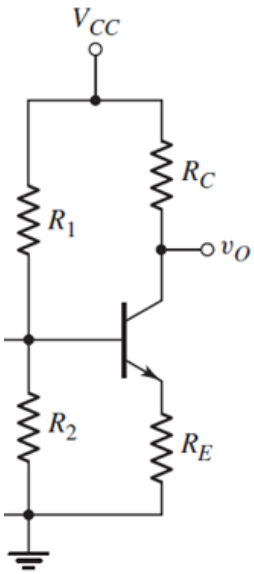
Problem 02

The circuit configuration to be designed is shown in Figure. The circuit is to be biased with V_{CC} = +12 V. The transistor quiescent values are to be I_{CQ} = 1 mA and V_{CEQ} = 6 V.



Problem 03

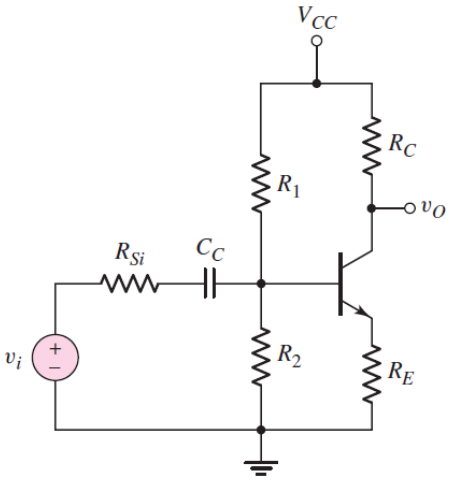
Analyze a circuit using a voltage divider bias circuit, and determine the change in the *Q*-point with a variation in when the circuit contains an emitter resistor. For the circuit given in Figure, let R_1 = 56 k, R_2 = 12.2 k, R_C = 2 k, R_E = 0.4 k, V_{CC} = 10 V, V_{BE}(on) = 0.7 V, and β= 100



Problem 04

Calculate the corner frequency and maximum gain of a bipolar common emitter circuit with a coupling capacitor.

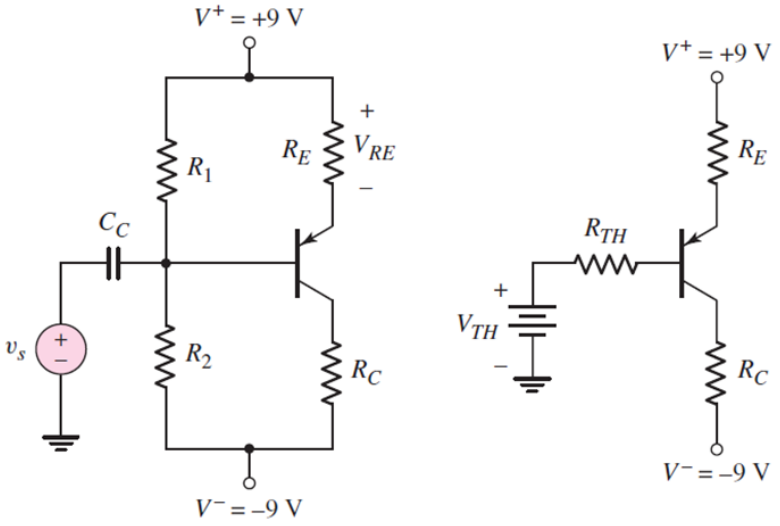
The parameters are: R_1 = 51.2 k, R_2 = 9.6 k, R_C = 2 k, R_E = 0.4 k, R_{Si} = 0.1 k, C_C = 1 μF, and V_{CC} = 10 V. The transistor parameters are: V_{BE}(on) = 0.7 V, β= 100, and V_A = ∞.



Problem 05

Problem: Design a bias-stable pnp transistor circuit to meet a set of specifications

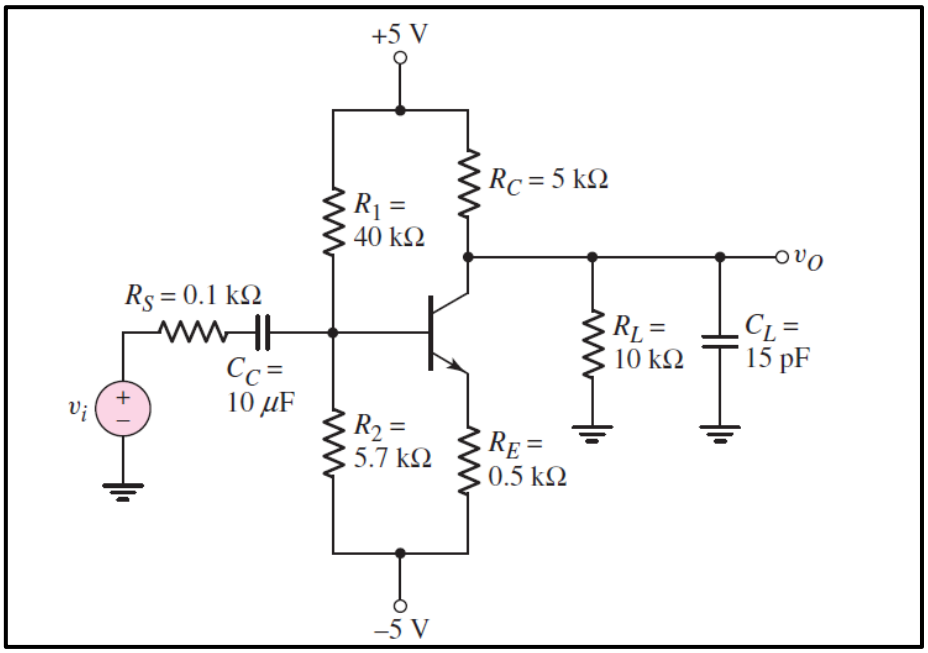
The transistor Q-point values are to be: $V_{ECQ} = 7$ V, $I_{CQ} \cong 0.5$ mA, and $V_{RE} \cong 1$ V.



Assume transistor parameters of $\beta = 80$ and $V_{BE}(\text{on}) = 0.7$ V. Standard resistor values are to be used in the final design.

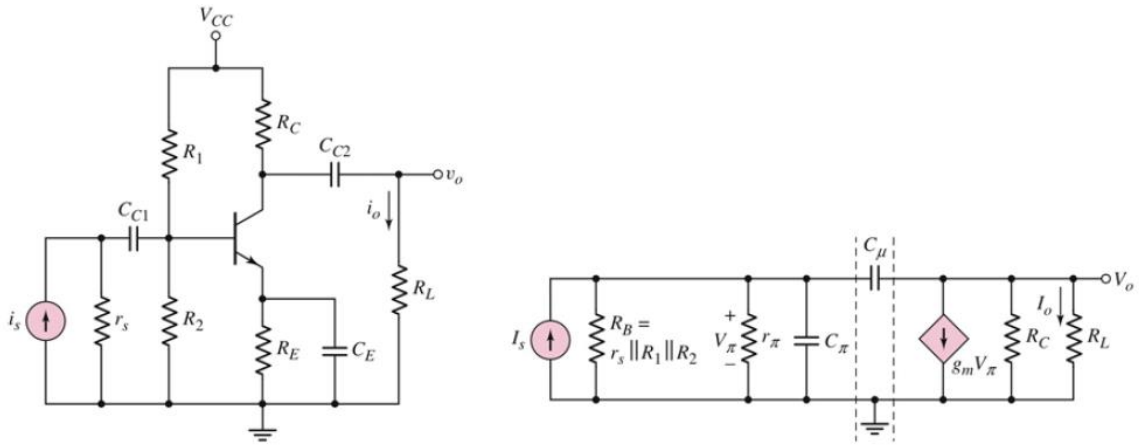
Problem 06

Determine the midband gain, corner frequencies, and bandwidth of a circuit containing both a coupling capacitor and a load capacitor. Consider the circuit shown in Figure with transistor parameters *VBE*(on) = 0.7 V, $\beta = 100$, and *VA* =∞.



Problem 07

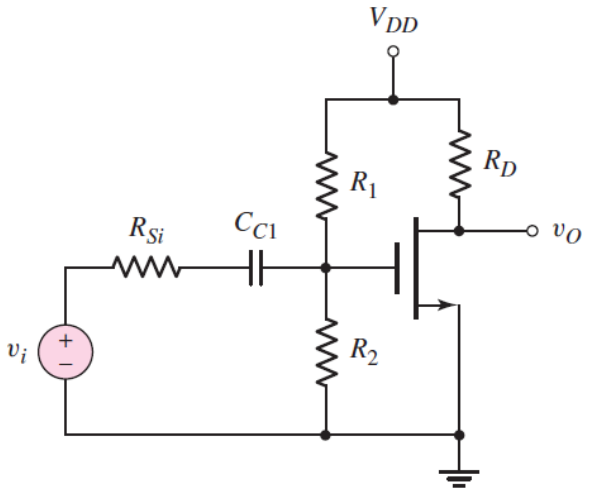
For the circuit in Figure the parameters are: $R_1 = 200\ \text{k}\Omega$, $R_2 = 220\ \text{k}\Omega$, $R_C = 2.2\ \text{k}\Omega$, $R_L = 4.7\ \text{k}\Omega$, $R_E = 1\ \text{k}\Omega$, $r_s = 100\ \text{k}\Omega$, and $V_{CC} = 5\ \text{V}$. The transistor parameters are: $\beta_o = 100$, $V_{BE}(\text{on}) = 0.7\ \text{V}$, $V_A = \infty$, $C_\pi = 10\ \text{pF}$, and $C_\mu = 2\ \text{pF}$. Using the simplified hybrid-π model shown in Figure 7.47, calculate: (a) the Miller capacitance, and (b) the 3 dB frequency.



Problem 08

Determine the small-signal voltage gain and input and output resistances of a common-source amplifier. The parameters are:

$R_D = 10\,\text{k}\Omega$, $R_1 = 140\,\text{k}\Omega$, $R_2 = 60\,\text{k}\Omega$, and $R_{\text{Si}} = 4\,\text{k}\Omega$. The transistor parameters are: $V_{TN} = 0.4\,\text{V}$, $K_n = 0.5\,\text{mA/V}^2$, and $\lambda = 0.02\,\text{V}^{-1}$.



Problem 09

Determine the unity-gain bandwidth of an MOSFET.

Consider an n-channel MOSFET with parameters $K_n = 1.5\,\text{mA/V}^2$, $V_{TN} = 0.4\,\text{V}$, $\lambda = 0$, $C_{gd} = 10\,\text{fF}$, and $C_{gs} = 50\,\text{fF}$. Assume the transistor is biased at $V_{GS} = 0.8\,\text{V}$.

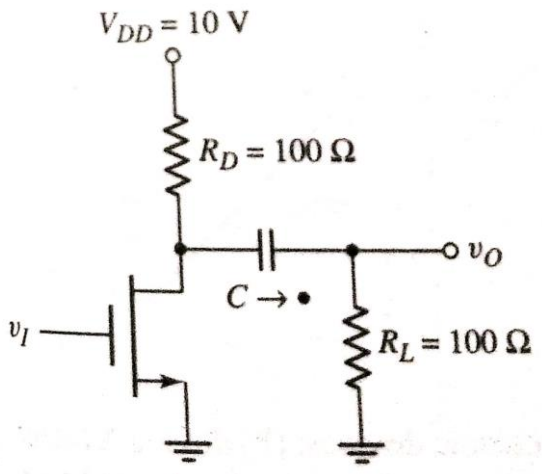
Problem 10

Determine the Miller capacitance and cutoff frequency of an MOSFET circuit.

Consider an n-channel MOSFET with parameters $K_n = 1.5\,\text{mA/V}^2$, $V_{TN} = 0.4\,\text{V}$, $\lambda = 0$, $C_{gd} = 10\,\text{fF}$, and $C_{gs} = 50\,\text{fF}$. Assume the transistor is biased at $V_{GS} = 0.8\,\text{V}$. a 10 kΩ load is connected to the output.

Problem 11

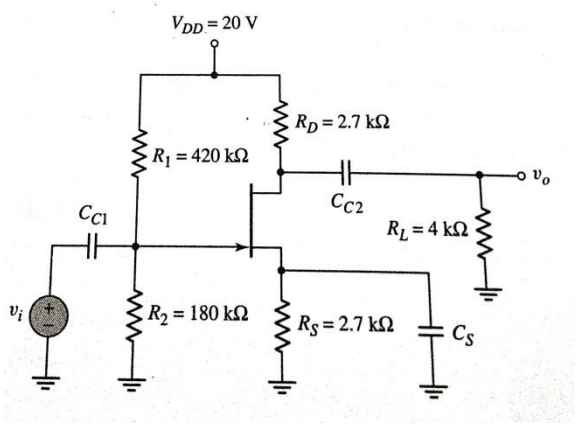
For the common source circuit shown in Figure the Q-point is $V_{DSQ} = 4\,V$. (a) Find I_{DQ} (b) The minimum value of the instantaneous drain current must be no less than $\frac{1}{10} I_{DQ}$, and the minimum value of the instantaneous drain to source voltage must be no less than $v_{DS} = 1.5\,V$. Determine the maximum peak to peak amplitude of a symmetrical sinusoidal output voltage. (c) For the conditions of part (b), calculate the power conversion efficiency, where the signal power is the power delivered to R_L.



Problem 12

Determine the small signal voltage gain of a JFET amplifier

Consider the circuit shown in Figure with transistor parameters $I_{DSS} = 12\ mA$, $V_p = -4V$, and $\lambda = 0.008\ V^{-1}$. Determine the small signal voltage gain $A_v = v_o/v_i$

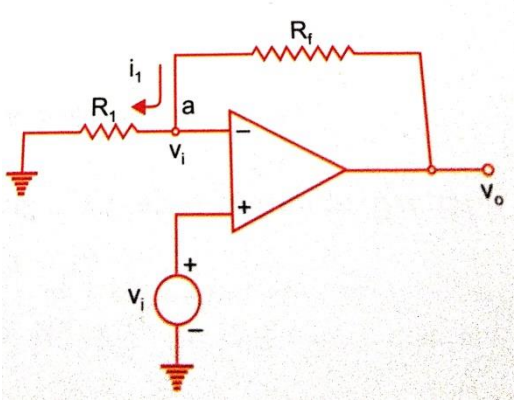


Problem 13

Design an amplifier with a gain of +5 using one op-amp.

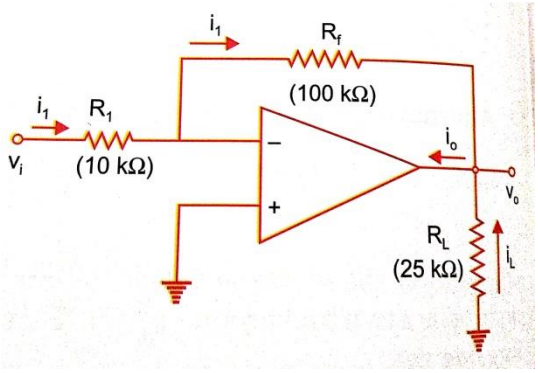
Problem 14

In the circuit of Figure, let $R_1 = 5\ k\Omega$, $R_f = 20\ k\Omega$ and $v_i = 1V$. A load resistor $R_L = 5\ k\Omega$ is connected at the output. Calculate (i) v_o (ii) A_{CL} (iii) i_L (iv) output current i_o



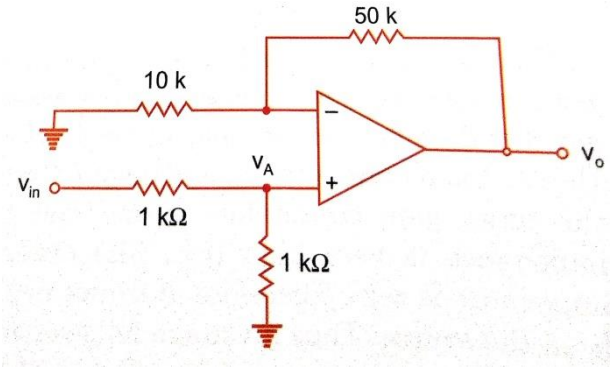
Problem 15

In the circuit of Figure, let $R_1 = 10\ k\Omega$, $R_f = 100\ k\Omega$ and $v_i = 1V$. A load resistor $R_L = 25\ k\Omega$ is connected at the output. Calculate (i) v_o (ii) A_{CL} (iii) i_L (iv) output current i_o



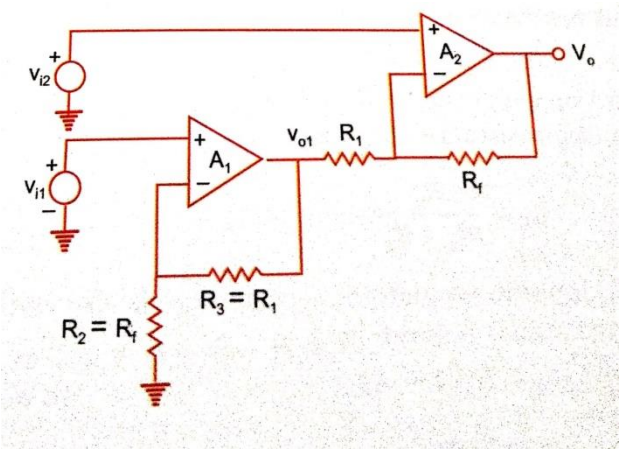
Problem 16

Calculate v_o if $v_i = 1V$.



Problem 17

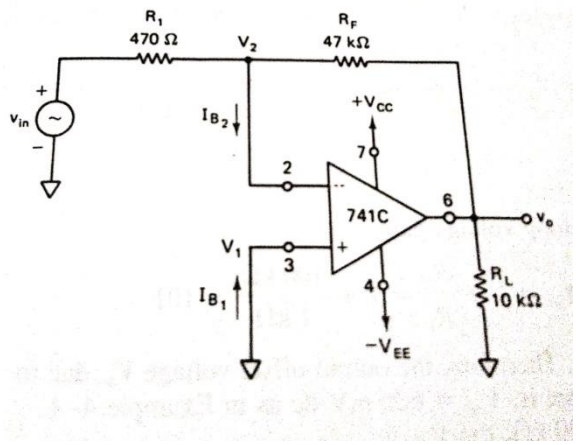
In Figure, given that $R_1 = R_3 = 560\Omega$, $R_f = R_2 = 5.6\ k\Omega$ and $V_{01} = 2V$ (peak to peak), $V_{01} = 2V$(peak to peak), $R_i = 2\ M\Omega$ and open loop gain $A_{OL} = 2 \times 10^5$. Calculate (i) voltage gain (ii) input resistance (iii) output voltage of the differential amplifier.



Problem 18

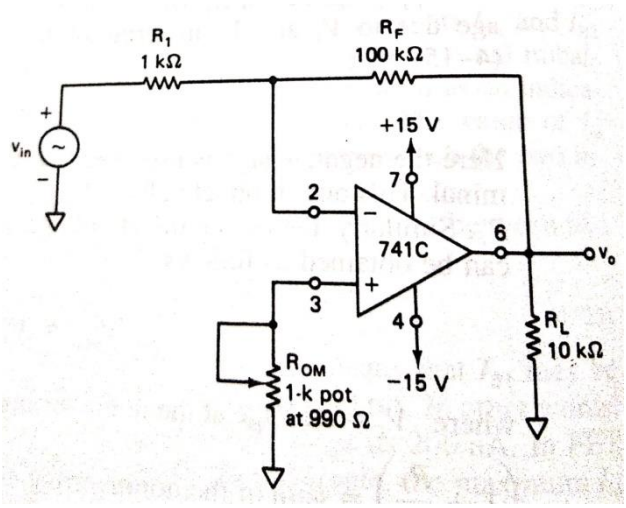
a) For the inverting amplifier of figure, determine the maximum possible output voltage due to (i) Input offset voltage V_{io} and (ii) Input bias current I_B. The op-amp is a type 741.

b) What value of R_{COM} is needed to reduce the effect of input bias current I_B?



Problem 19

For the inverting amplifier in Figure , determine the maximum output offset voltage $V_{o_{I_{io}}}$ caused by the input offset current I_{io}. The op-amp is a type 741.



Problem 20

(a) Design an op-amp differentiator that will differentiate an input signal with $f_{max} = 100Hz$

(b) Draw the output waveform for a sine wave of 1 V peak at 100Hz applied to the differentiator.

(c) Repeat part (b) for a square wave input.

Problem 21

For the component values $R_1 = 10\ k\Omega$, $R_F = 100k\Omega$ and $C_F = 10\ nF$, determine the lower frequency limit of integration and study the response for the inputs (i) sine wave (ii) step input (iii) square wave.

Problem 22

Find V_o for the adder-subtractor shown in Figure.