Module:6 Active filters and Data Converters

Course: BECE206L – Analog Circuits

DA3 Quiz

11.11.2022, 8:30 pm – 8:50 pm

Module 4,5,6 (Filters)

Talk Title: Automotive MIMO RADAR

Time: 6:30 pm-7:30 pm

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Module:6 Active filters and Data Converters

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- **Filter classifications: First and second order Low-pass and High pass filter designs, Band-pass filter, Notch filter**. Sample-and-hold circuits, DAC characteristics, D/A conversion techniques, A/D characteristics, A/D conversion techniques.

1. Introduction

- Electric Filters – In circuits requiring separation of signals according to **frequency of operations**
- Almost used in all sophisticated electronic instruments
- Consists of : a) Passive RLC components
  b) Crystals
  c) Resistors, capacitors, Op-amps(active filters)

2. RC active filters

- Electric filter:A frequency **selective electric circuit**
  Passes electric signals of **specified band of frequencies**
  Attenuates signals of frequencies outside this band
- Filters can be analog or digital.
- Passive filters **use R, L, C components**.
  High frequencies, works well
  Low frequencies, **Inductors require more turns, which add series resistance(coil resistance) which results in high power dissipation**
- Active filters overcome these problems.
  Op-amp will be active element (Can provide gain if necessary)
  RC will be passive elements
  Inductors are avoided by enclosing capacitors in feedback loop

2. RC active filters

- Active filters
  Op-amp will be active element (Can provide gain if necessary)
  Op-amp – Non inverting configuration – offers high input impedance and low output impedance
  Load is isolated from filter circuit
- Limitations of Active filters
  High frequency response is limited by
  a) gain bandwidth product (GBW)
  b) slew rate (response time)
  High frequency active filters are expensive than passive filters

2. RC active filters

- Common filters

a) Low pass filter(LPF)
b) High pass filter (HPF)
c) Band pass filter (BPF)
d) Band reject filter or
Band stop filter (BSF)

Frequency response
Dashed curve – ideal
Solid curve – practical

Impossible for ideal
Can achieve close to ideal with special design

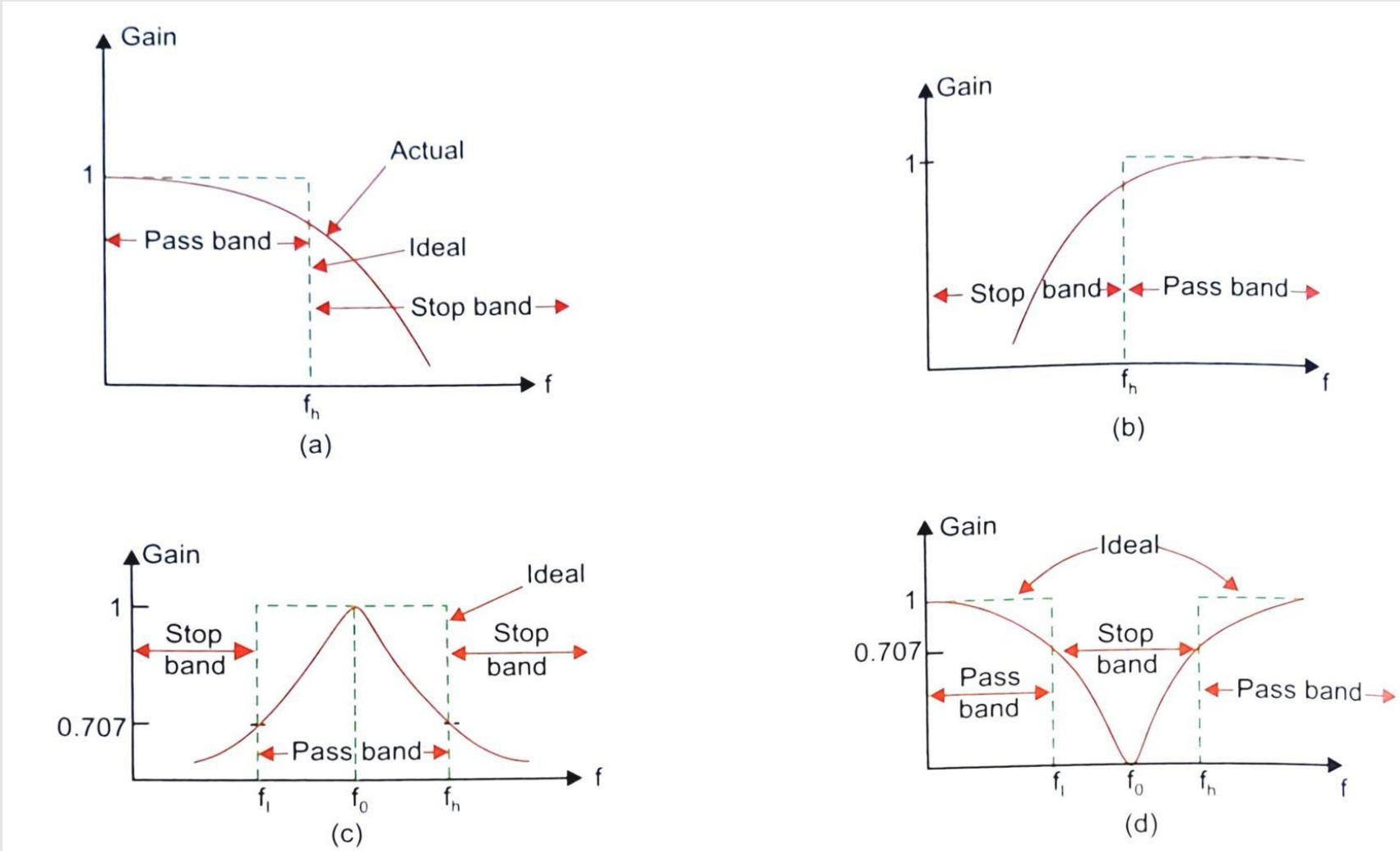


Fig. 7.1 Frequency response of filters, (a) Low-pass, (b) High-pass, (c) Band-pass, (d) Band-reject

2. RC active filters

- Active filters are specified by voltage transfer function

$$H(s) = \frac{V_0(s)}{V_i(s)}$$

- Under steady state conditions $s = j\omega$

$$H(j\omega) = |H(j\omega)|e^{j\phi(\omega)}$$

- Where $|H(j\omega)|$ is magnitude or gain function and $\phi(\omega)$ is the phase function
- Usually, magnitude response is given in dB as

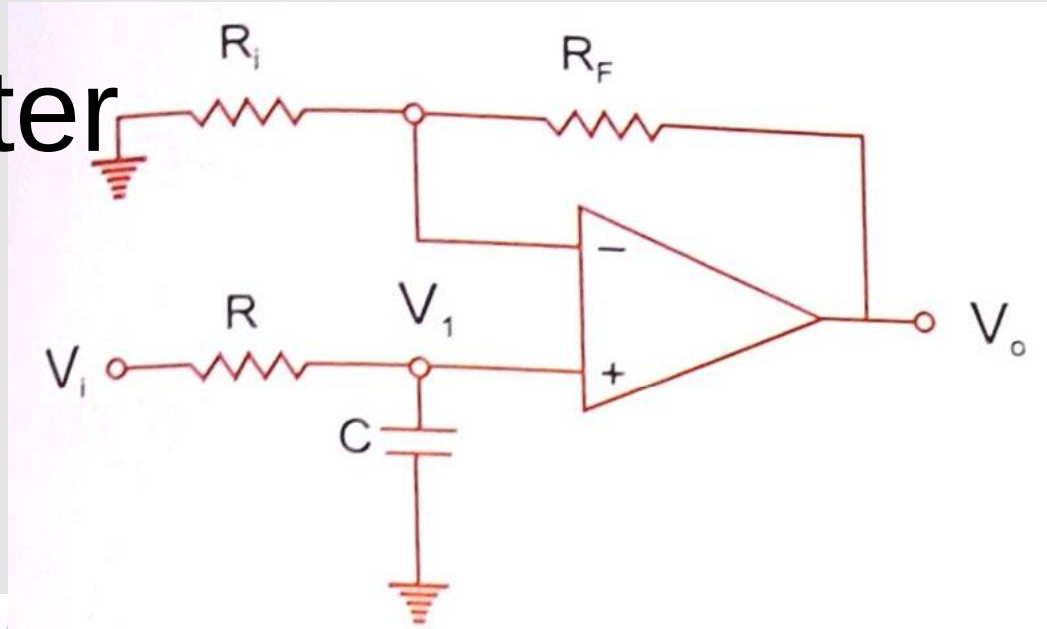
$$20\log_{10}|H(j\omega)|$$

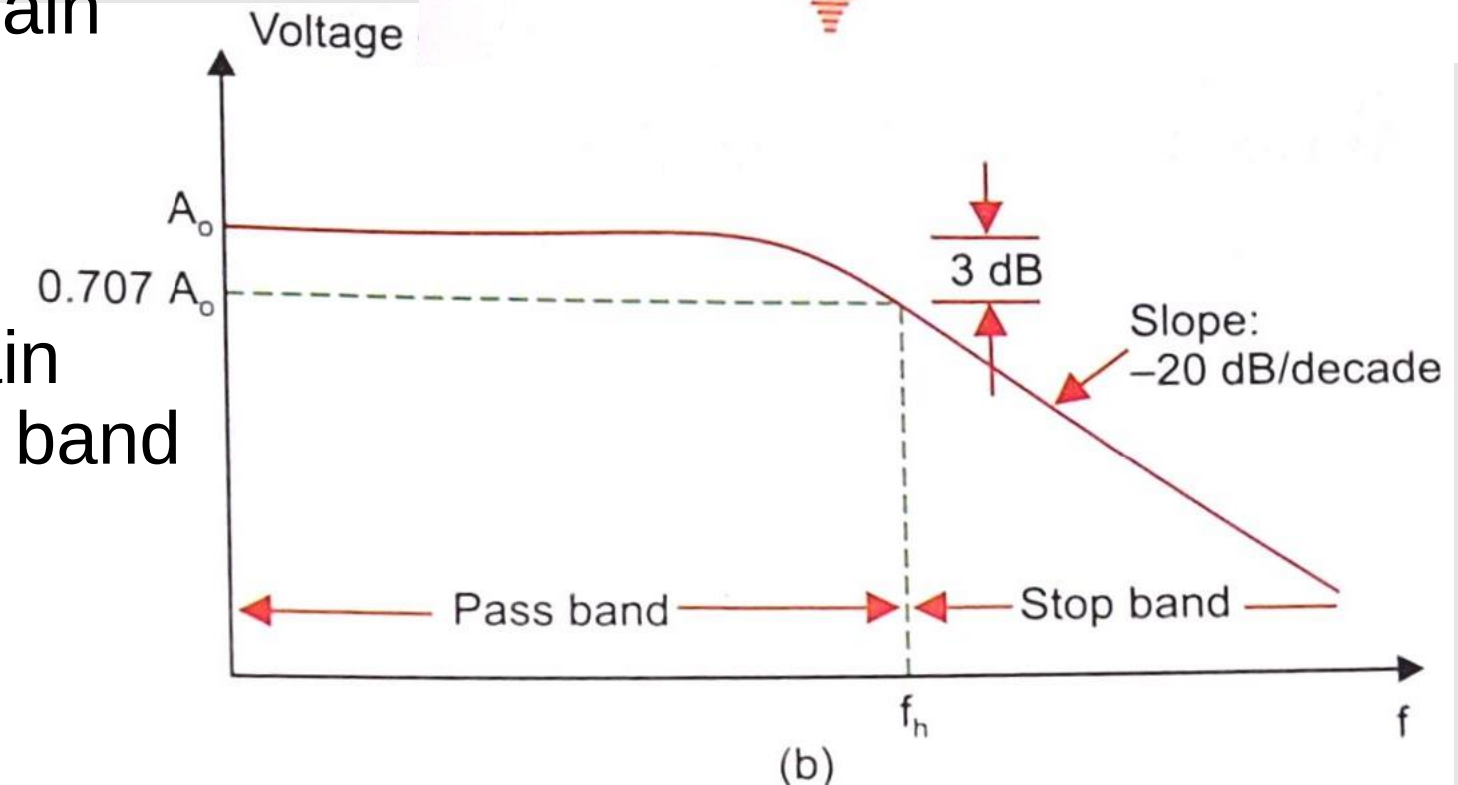
  And phase response in degrees as

$$-\phi(\omega) \times \frac{180}{\pi} \text{degrees}$$

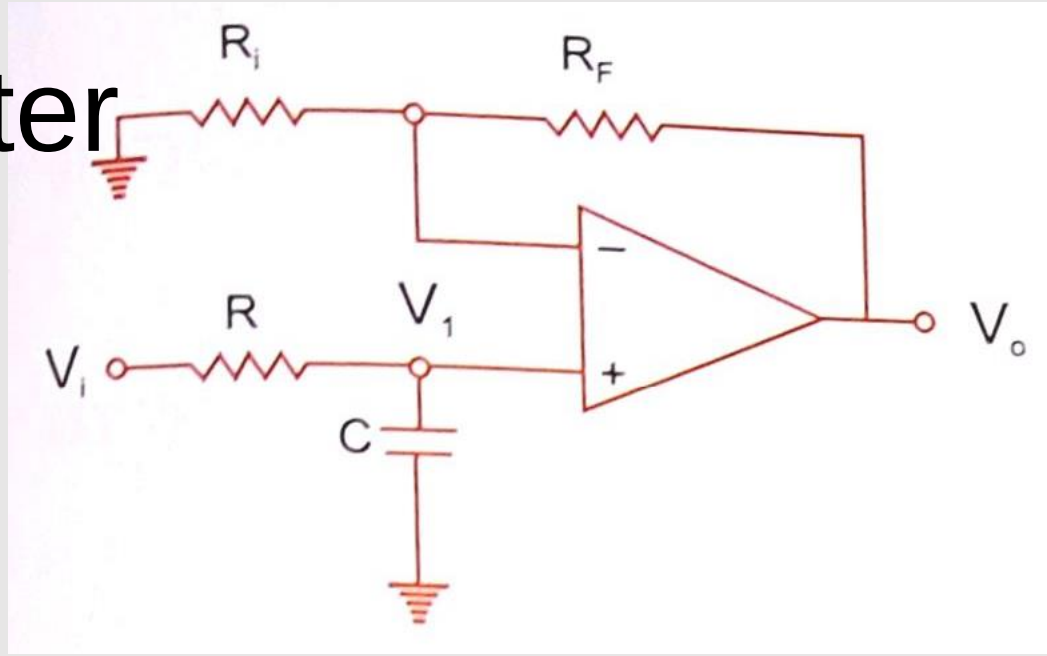
3. First order Low Pass Filter

- First order LPF:
  Single RC network connected to (+) input terminal of non-inverting op-amp.
- Pass band: Gain : from max gain until -3dB from max gain.
- Stop band:
  Gain below -3dB from max gain
  Slope: -20dB / decade in stop band





3. First order Low Pass Filter

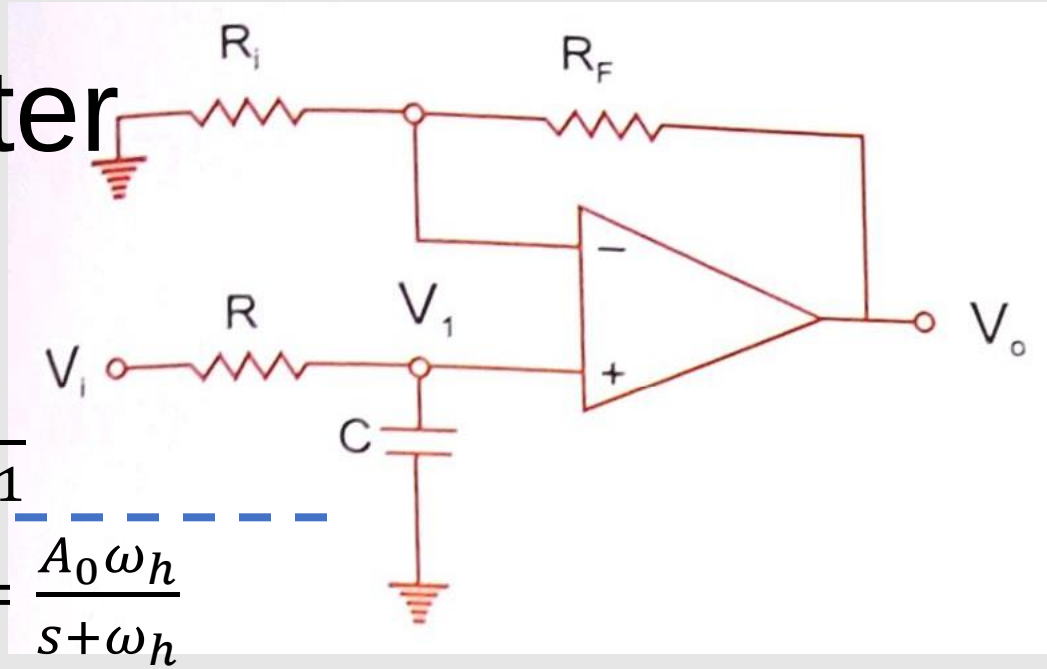


- If V is in time domain,
  $V(s)$ is Laplace transform in freq domain.
- Voltage V_1 across capacitor C in s-domain

$$V_1(s) = \frac{\frac{1}{sc}}{R+\frac{1}{sc}} V_i(s)$$

- $$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs+1}$$
- Closed loop gain $A_0 = \frac{V_0(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_1}\right)$
- Overall transfer function: $H_{LP}(s) = \frac{V_0(s)}{V_i(s)} = \frac{V_0(s)}{V_1(s)} . \frac{V_1(s)}{V_i(s)} = \frac{A_0}{RCs+1}$

3. First order Low Pass Filter

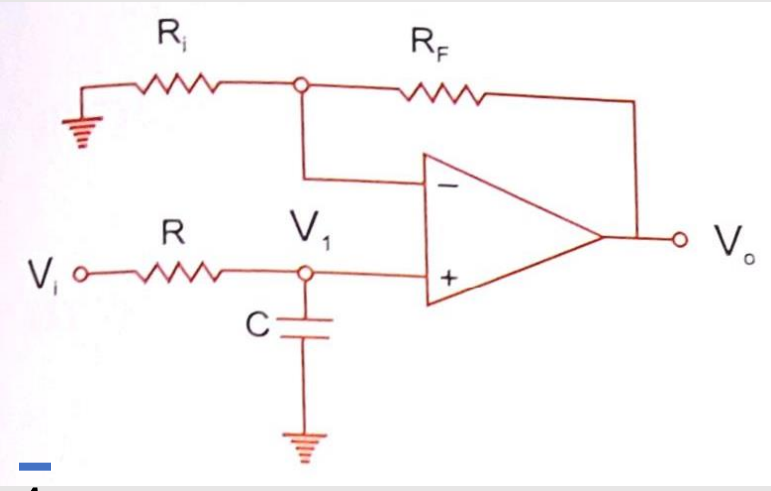


- Closed loop gain $A_0 = \frac{V_0(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_1}\right)$
- Overall transfer function: $H_{LP}(s) = \frac{V_0(s)}{V_i(s)} = \frac{A_0}{RCs+1}$
- Let $\omega_h = 1/RC$: $H_{LP}(s) = \frac{V_0(s)}{V_i(s)} = \frac{A_0}{\frac{s}{\omega_h}+1} = \frac{A_0\omega_h}{s+\omega_h}$
- This is standard form of transfer function of first order low pass system
- To determine, put $s = j\omega$

$$H_{LP}(j\omega) = \frac{A_0}{RCs+1} = \frac{A_0}{1+j\omega\,RC} = \frac{A_0}{1+j\omega/\omega_h} = \frac{A_0}{1+j(f/f_h)}$$

- Where $f_h = \frac{1}{2\pi RC}$ and $f = \frac{\omega}{2\pi}$

3. First order Low Pass Filter



- $A_0 = \frac{V_0(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_1}\right)$ $H_{LP}(s) = \frac{A_0}{RCs+1}$

  $H_{LP}(j\omega) = \frac{A_0}{1+j(f/f_h)}$ $f_h = \frac{1}{2\pi RC}$ and $f = \frac{\omega}{2\pi}$

- At very low frequencies: $f \ll f_h$: $|H_{LP}(j\omega)| \approx \frac{A_0}{1+j(0)} \approx A_0$

- At $f = f_h$: $|H_{LP}(j\omega)| = \left|\frac{A_0}{1+j(f_h/f_h)}\right| = \left|\frac{A_0}{1+j}\right| = \frac{A_0}{\sqrt{2}} = 0.707A_0$

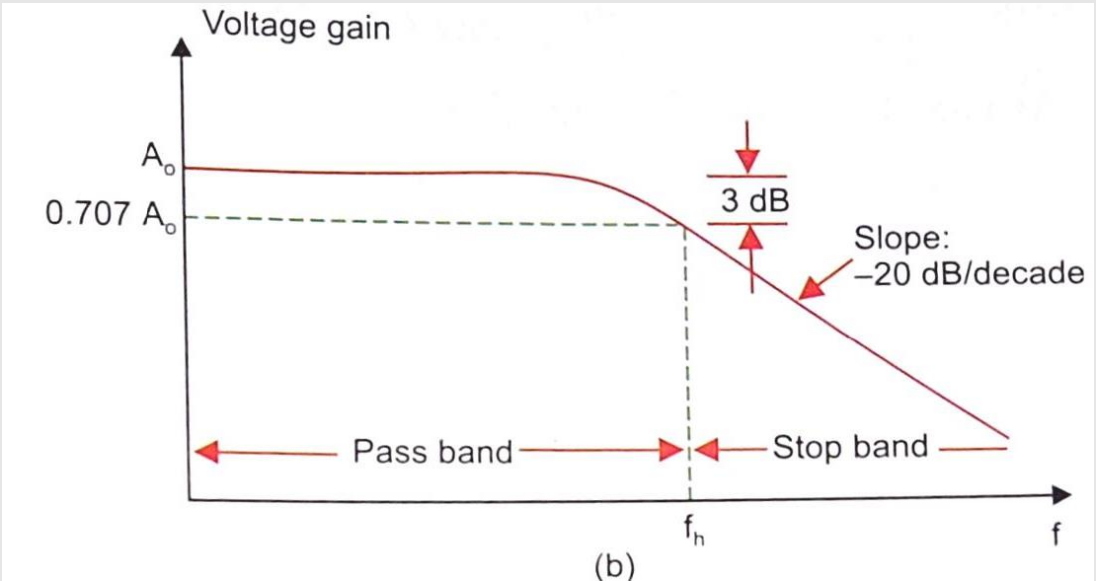
  (Log scale: -3dB below max gain)

  Pass band: Max gain A_0 to $0.707A_0$

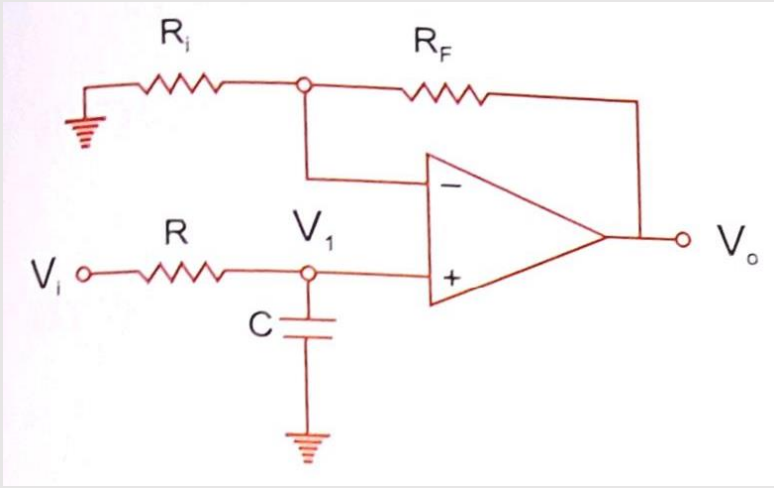
- At $f \gg f_h$: $|H_{LP}(j\omega)| \to \frac{A_0}{1+j(\infty)} \to 0$ $(\ll A_0)$

  Log scale: $-\infty$

  Stop band: $0.707\ A_0$ to 0 gain region



3. First order Low Pass Filter

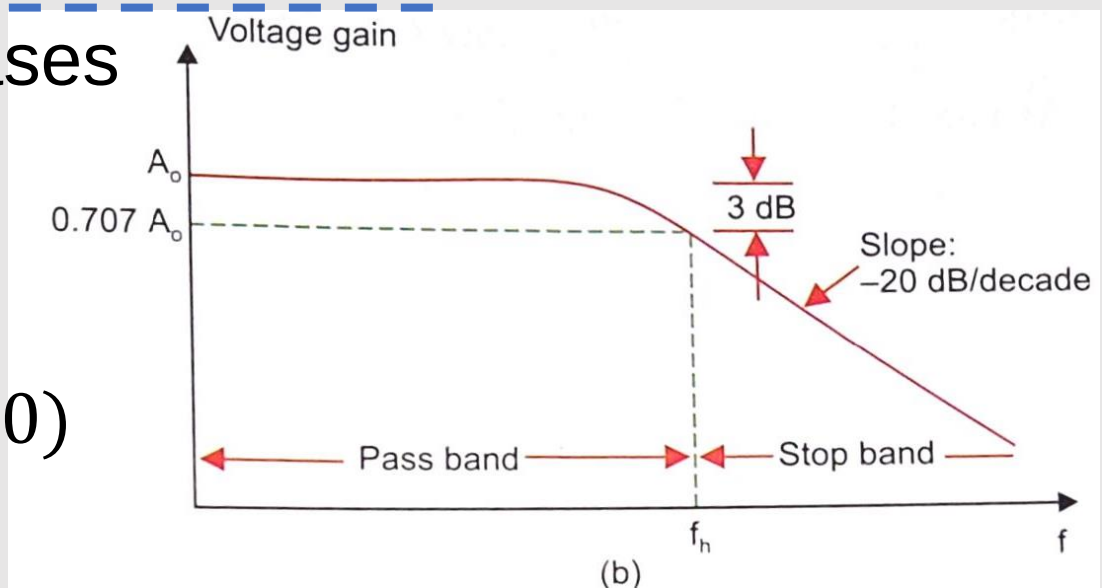


- $A_0 = \frac{V_0(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_1}\right)$ $H_{LP}(s) = \frac{A_0}{RCs+1}$

  $H_{LP}(j\omega) = \frac{A_0}{1+j(f/f_h)}$ $f_h = \frac{1}{2\pi RC}$ and $f = \frac{\omega}{2\pi}$
- At very low frequencies: $f \ll f_h$ $|H_{LP}(j\omega)| \approx A_0$
- At $f = f_h$: $|H_{LP}(j\omega)| = 0.707A_0$ (Log scale: -3dB below max gain)
- At $f \gg f_h$: $|H_{LP}(j\omega)| \to 0$ $(\ll A_0)$

- When f increases above f_h, gain decreases constantly at $-\frac{20dB}{decade}$ (Roll off rate)

  When frequency is increased 10 times
  Gain drops 10 times
  or $-20dB$ (in dB scale $20\log(1/10)$)



4. Second order active LPF

- Two RC pairs
- Roll off: $-40dB/decade$
- $A_0 = (1 + R_F/R_1)$ (Gain)
- $H(s) = \dfrac{A_0}{(sCR)^2 + sCR(3 - A_o) + 1}$
- $H_{LP}(s) = \dfrac{A_0\omega_h^2}{s^2 + \alpha\omega_h s + \omega_h^2}$

  ω_h: upper cutoff frequency (radians/second)

  α =damping coefficient= $3 - A_0$

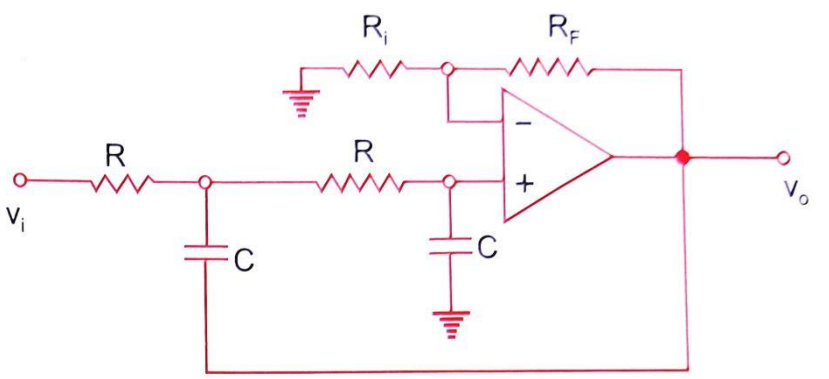


Fig. 7.4 Second order low-pass filter

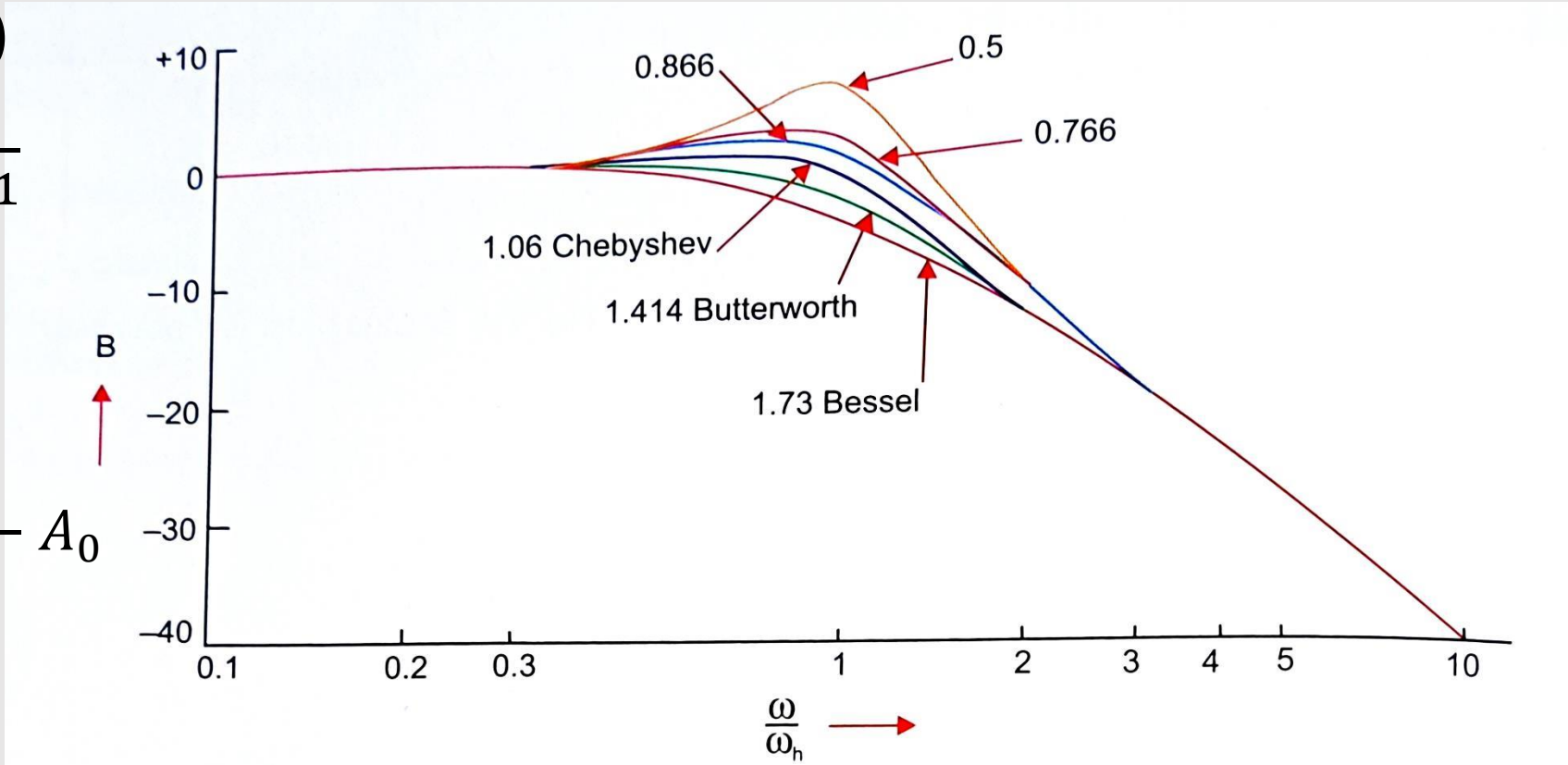


Fig. 7.5 Second order low-pass active filter response for different damping (unity gain $A_o = 1$)

5. Higher order LPF

- With $s_n = j\,\omega/\omega_h$
- $Normalized$ transfer function of nth order generalized low pass (maximally flat)

$$\left|\frac{H_{LP}(j\omega)}{A_0}\right| = \frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^{2n}}}$$

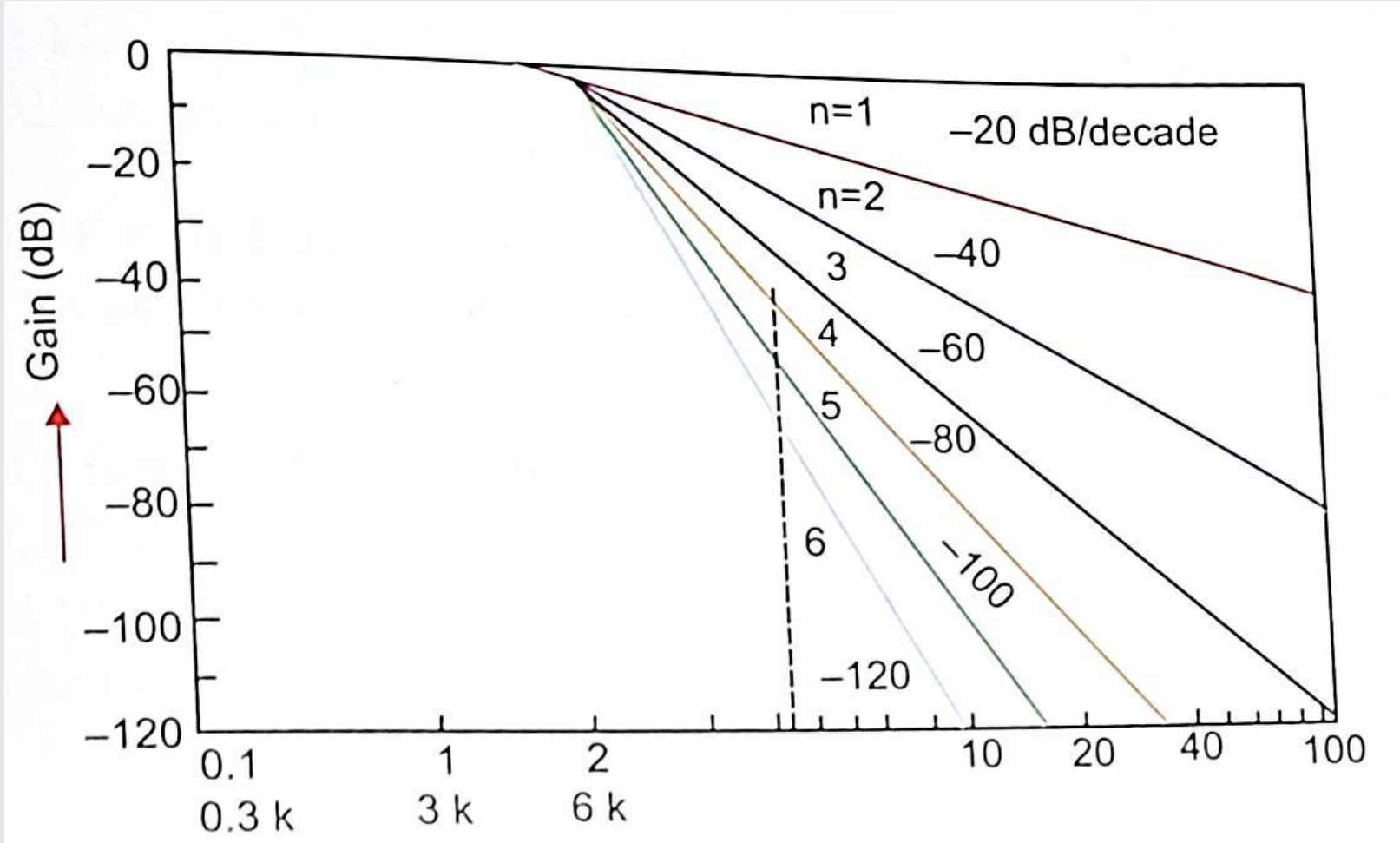


Fig. 7.6 Roll-off rate for different values of *n*

6. First order High pass active filter

- Complement of Low pass filter (Obtained by interchanging R and C)
- Single RC network to non-inverting terminal
  Gain is controlled by $R_i R_F$ in inverting configuration
- V_1 at non-inverting terminal is $V_1(s) = \frac{R}{R+1/sc} V_i(s)$

$$\frac{V_1(s)}{V_i(s)} = \frac{RCs}{1+RCs}$$

- $V_0(s) = \left(1 + \frac{R_F}{R_1}\right) V_1(s)$

CL gain:

$$A_0 = \frac{V_0(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_1}\right)$$

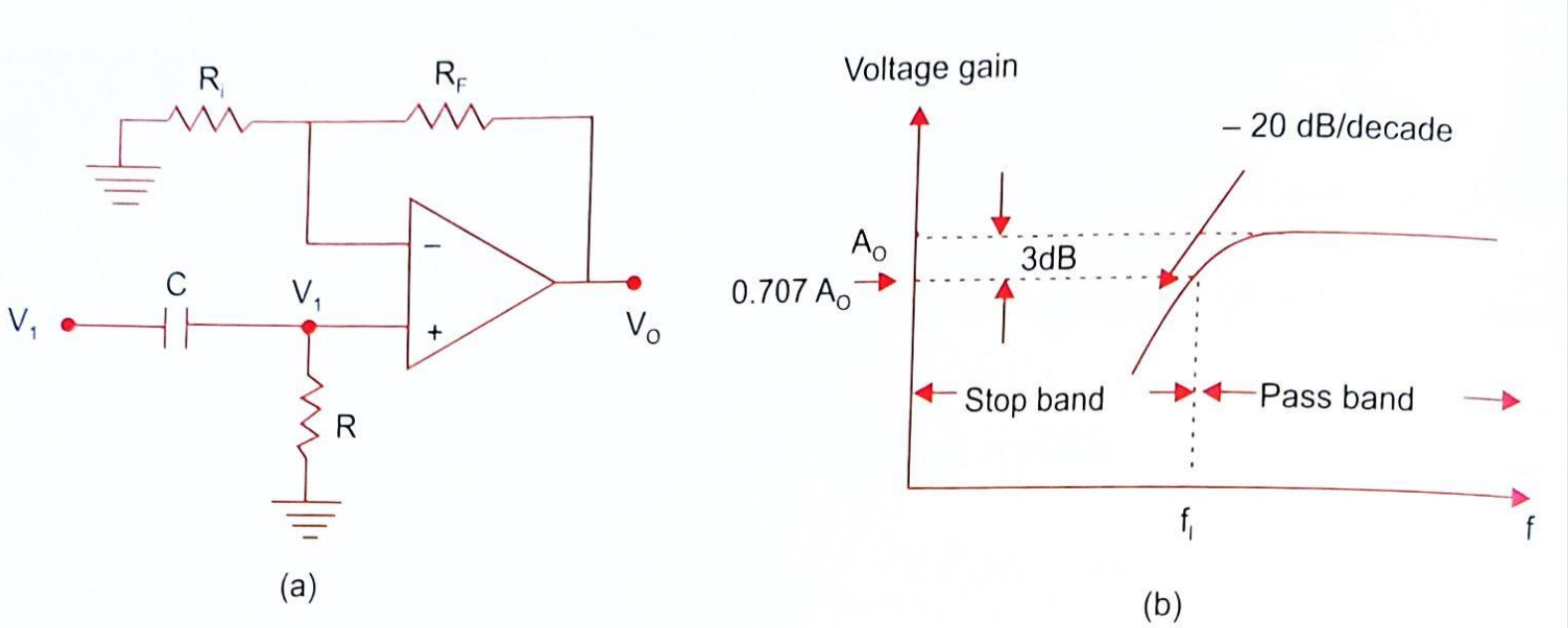


Fig 7.8 (a) First order high-pass filter. (b) Frequency response

6. First order High pass active filter

$$\frac{V_1(s)}{V_i(s)} = \frac{RCs}{1+RCs} \qquad A_0 = \frac{V_0(s)}{V_1(s)} = \left(1 + \frac{R_F}{R_1}\right)$$

Overall Transfer function $H_{HP}(s) = \frac{V_0(s)}{V_i(s)} = \frac{V_0(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)} = \frac{A_0\, RCs}{1+RCs}$

With $s = j\omega \quad and\ \omega_l = 1/RC \qquad RCs = \frac{j\omega}{\omega_l} = j\frac{2\pi f}{2\pi f_l} = j\frac{f}{f_l}$,

$$H_{HP}(j\omega) = A_0 \frac{\left(j\frac{f}{f_l}\right)}{1+j\frac{f}{f_l}}$$

Frequency response:

$$|H_{HP}(j\omega)| = \left|\frac{V_0}{V_i}\right|$$

$$= A_0 \frac{f/f_l}{\sqrt{1+(f/f_l)^2}} = \frac{A_0}{\sqrt{1+(f_l/f)^2}}$$

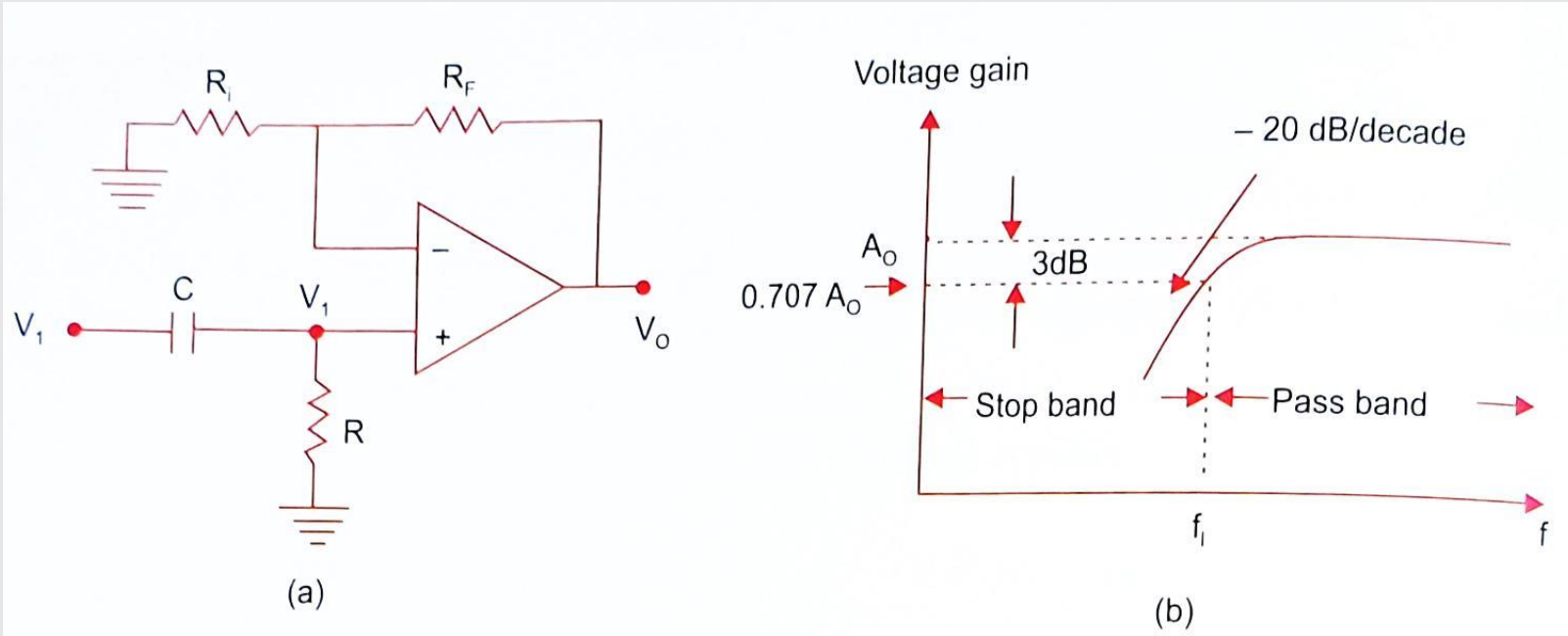


Fig 7.8 (a) First order high-pass filter. (b) Frequency response

6. First order High pass active filter

Frequency response: $|H_{HP}(j\omega)| = \left|\frac{V_0}{V_i}\right| = \frac{A_0}{\sqrt{1+(f_l/f)^2}}$

Pass band: very high frequency $f > f_l$: Gain is constant = A_0 (as$(f_l/f)^2$<<1)

Stop band: At $f < f_l$, gain rolls off at -20dB/decade

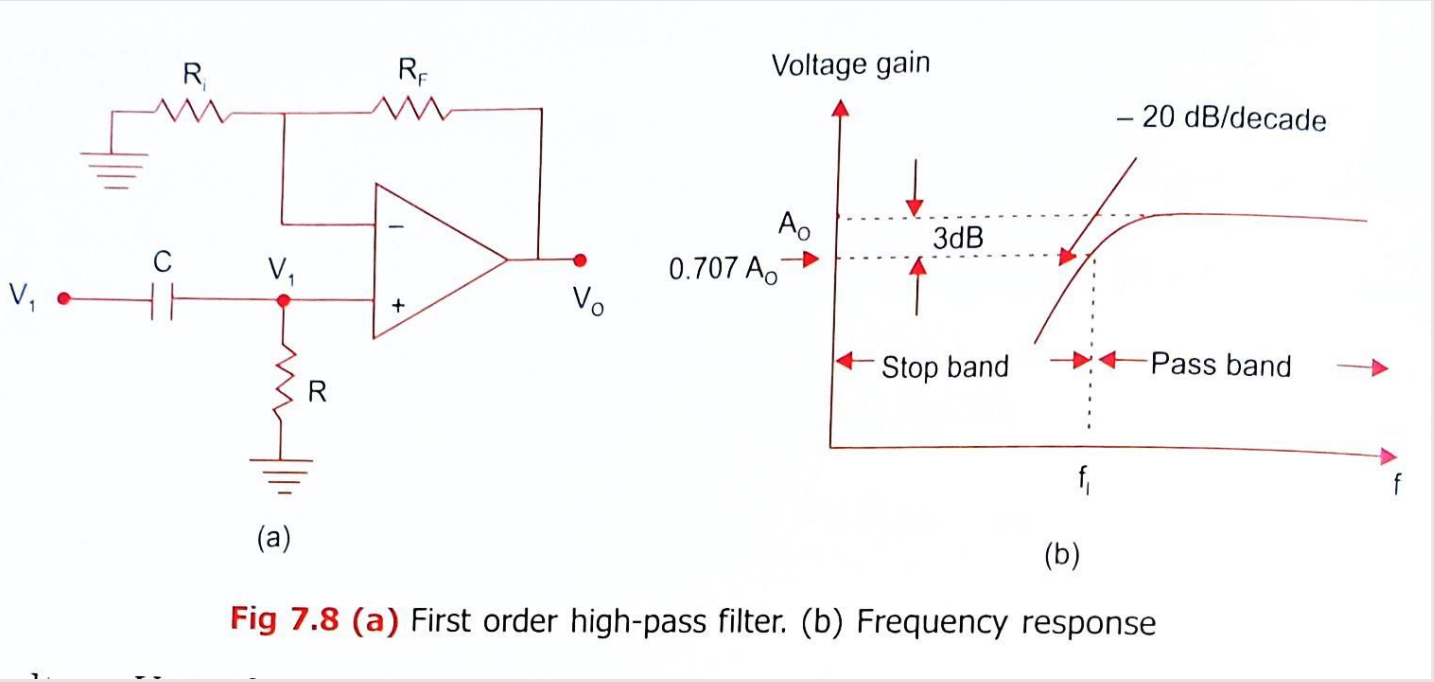


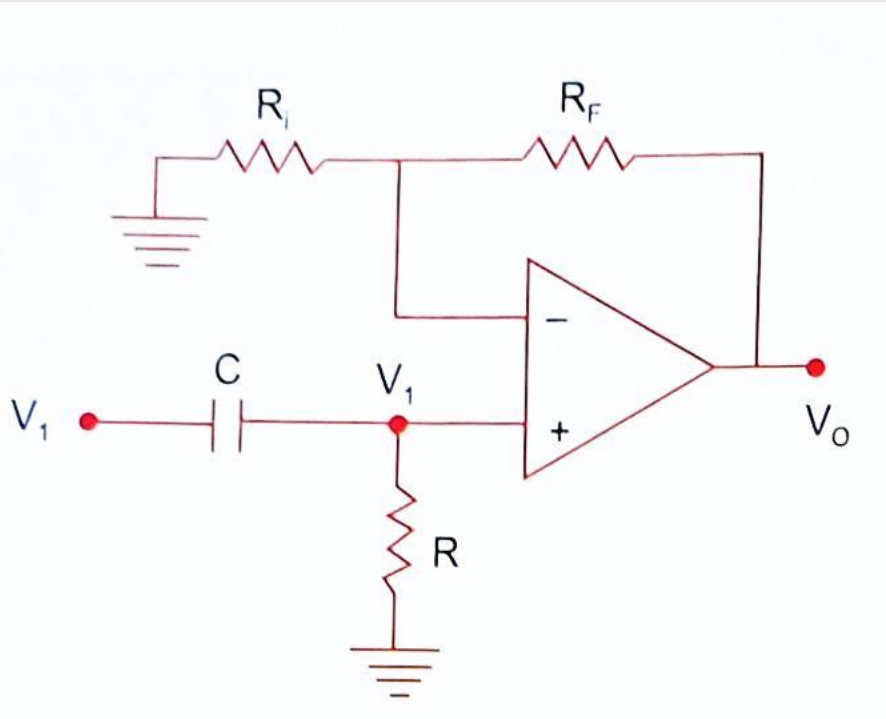
Fig 7.8 (a) First order high-pass filter. (b) Frequency response

Problem 2: Design a first-order high pass filter at a cut-off frequency of 2 kHz with a pass band gain of 2

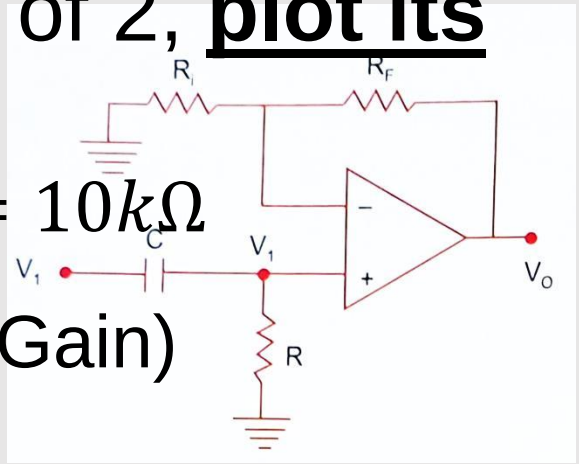
- $f_l = 2kHz$ and $C = 0.01\mu F$
- $\omega_l = \frac{1}{RC}$ $f_l = \frac{1}{2\pi RC}$ $R = \frac{1}{2\pi f C} = \frac{1}{2\pi(2k)(0.01\mu F)} = 7.95k\Omega$
- To obtain pass band gain of 2

$$A_0 = 2 = 1 + \frac{R_F}{R_1}$$

$$\frac{R_F}{R_1} = 1 \quad R_F = R_1 = 10k\Omega$$



Problem 3: For the designed first-order high pass filter at a cut-off frequency of 2 kHz with a pass band gain of 2, **plot its frequency response**



- $f_l = 2kHz$ and $C = 0.01\mu F$ $R = 7.95k\Omega$ $R_F = R_1 = 10k\Omega$

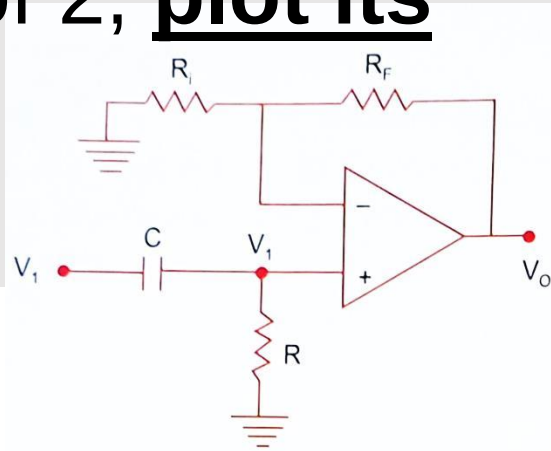
For frequency response: $|H_{HP}(j\omega)| = \left|\frac{V_0}{V_i}\right| = \frac{A_0}{\sqrt{1+(f_l/f)^2}}$ (Gain)

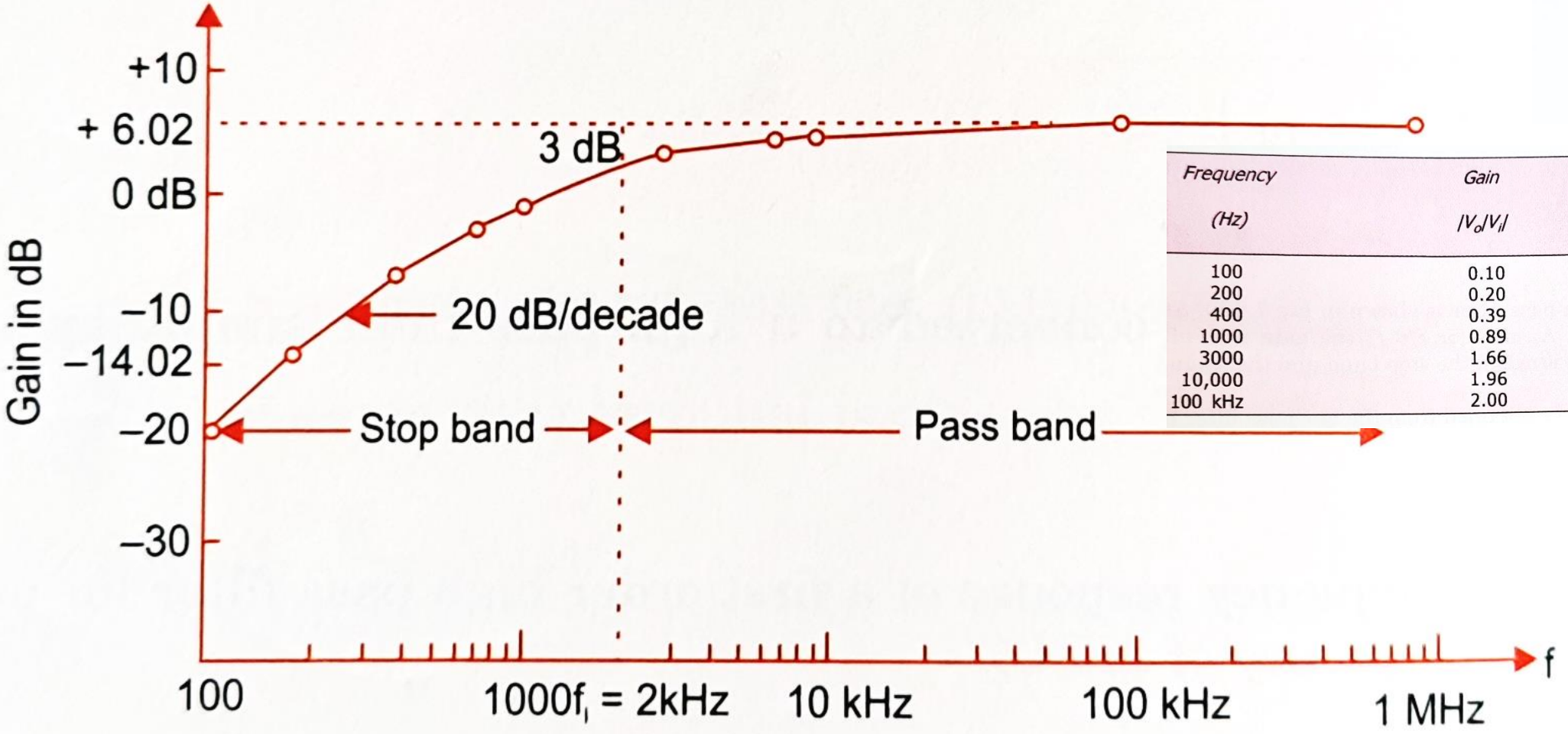
$|H_{HP}(j\omega)|_{dB} = 20\log_{10}\left(\frac{A_0}{1+(f_l/f)^2}\right)$ (Gain in dB)

Frequency (Hz)	Gain $\lvert V_o/V_i \rvert$	Gain in dB $20 \log \frac{V_o}{V_i}$
100	0.10	− 20.01
200	0.20	− 14.02
400	0.39	− 8.13
1000	0.89	− 0.97
3000	1.66	4.42
10,000	1.96	5.85
100 kHz	2.00	6.02

Problem 3: For the designed first-order high pass filter at a cut-off frequency of 2 kHz with a pass band gain of 2, **plot its frequency response**

$$|H_{HP}(j\omega)|_{dB} = 20\log_{10}\left(\frac{A_0}{1+(f_l/f)^2}\right)$$ (Gain in dB)





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1000	0.89	− 0.97
3000	1.66	4.42
10,000	1.96	5.85
100 kHz	2.00	6.02

7. Second order high pass filter

- Two pairs of RC with feedback to RC
- $H_{HP} = \frac{A_0}{1+\frac{\omega_l}{s}(3-A_0)+\left(\frac{\omega_l}{s}\right)^2}$
- Denominator has second power of $\left(\frac{\omega_l}{s}\right)$ as highest power

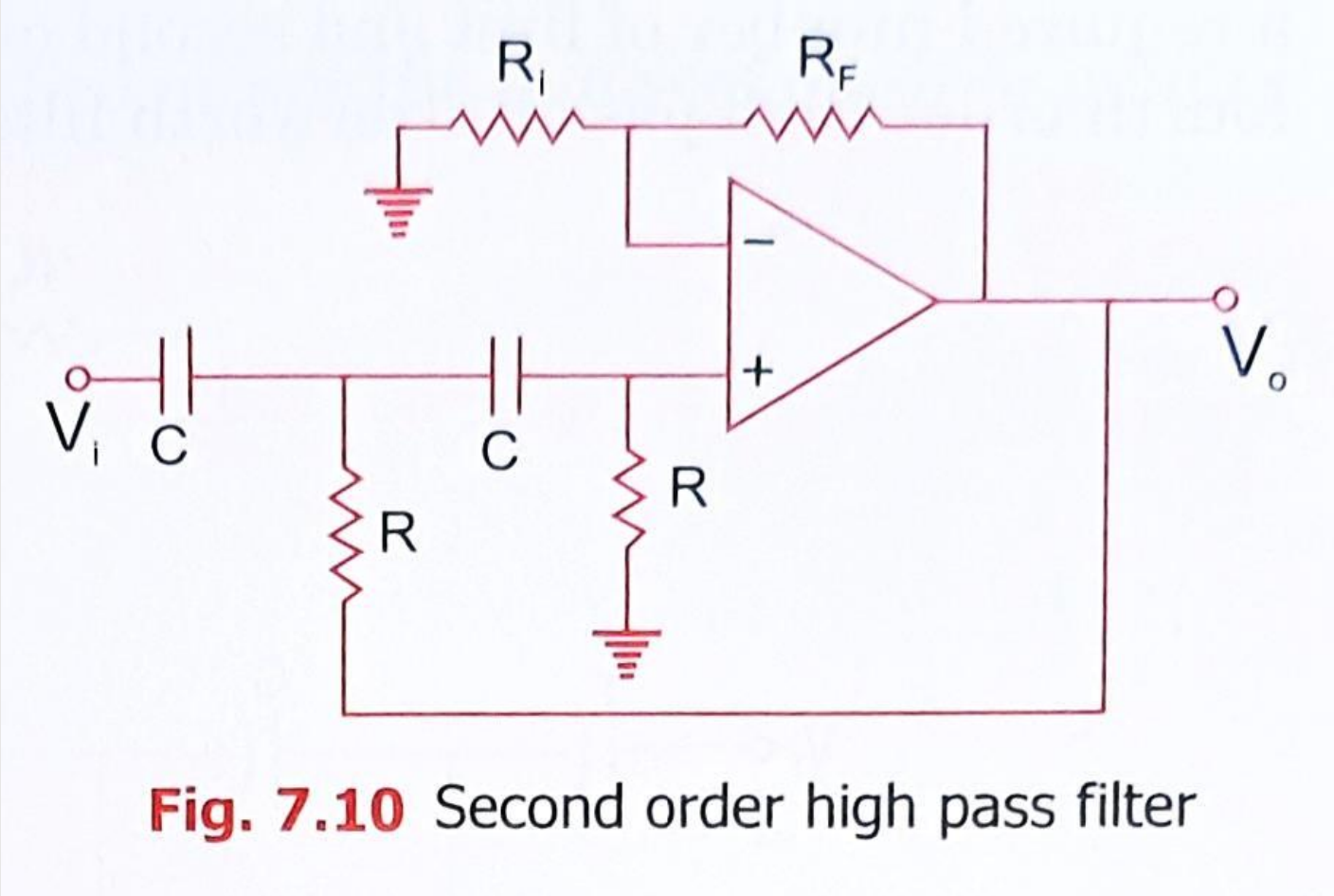
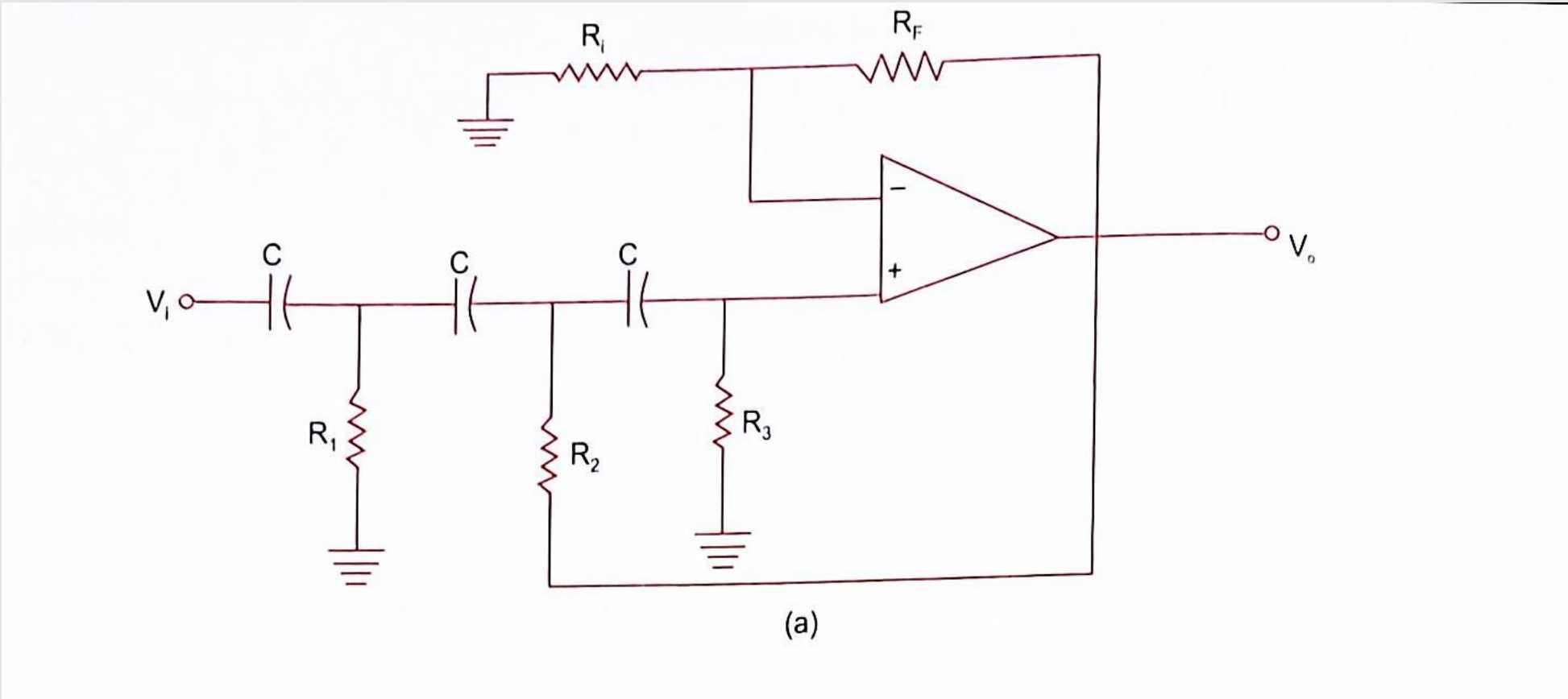


Fig. 7.10 Second order high pass filter

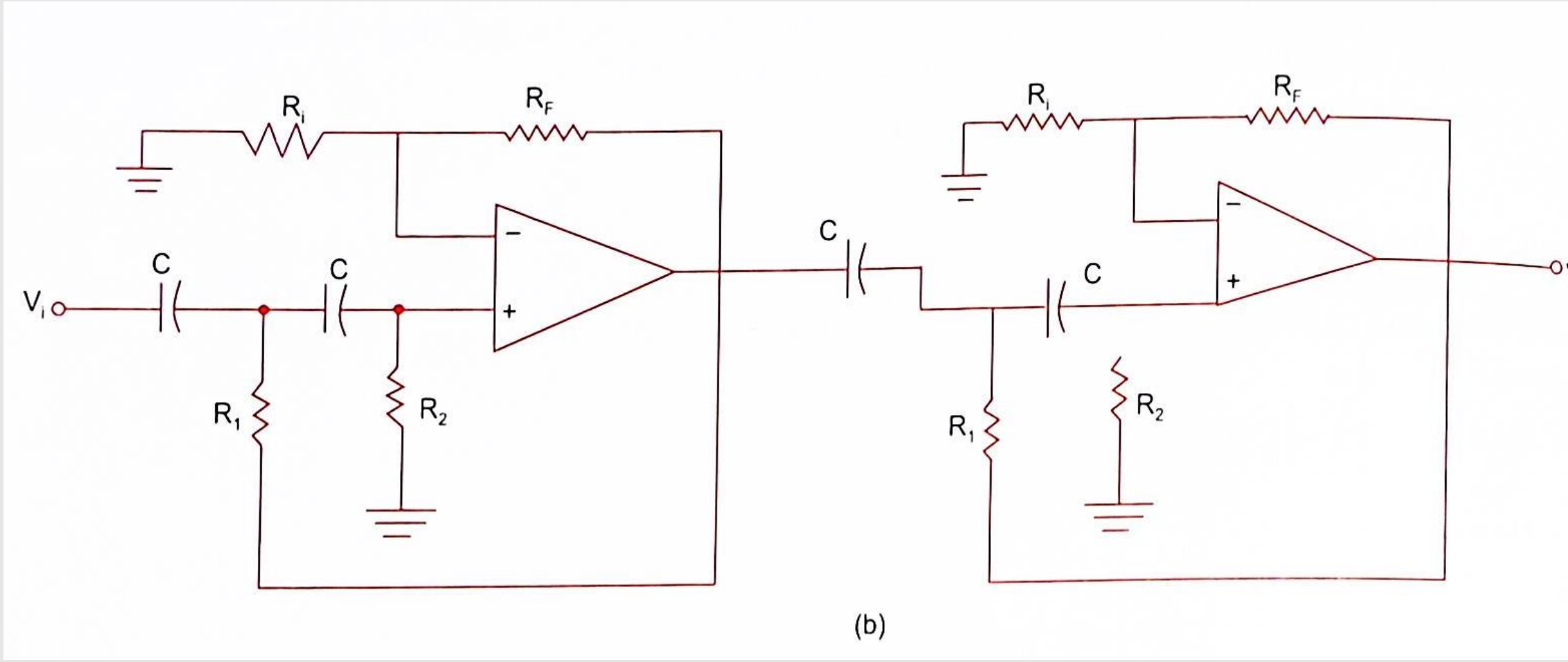
8. Higher order high pass filter

- Third order HPF



8. Higher order high pass filter

- Fourth Order HPF



1. Application of A/D and D/A convertors

- Most of real world quantities: Analog form (Continuous)
  Example: Voltage, current, temperature, pressure, time, etc
- Signal processing – difficult to store or transmit analog:
  if amplitude modulation – noise gets superimposed
- For processing, transmission and storage – Digital form is preferred
- Digital – More accuracy and less noise
-

1. Application of A/D and D/A convertors

- Analog from Sensor – Antialiasing filter limits bandwidth – Sample & hold (S/H) samples the analog signal at twice the maximum frequency and holds for A/D conversion to complete – ADC output is sequence of binary digits - Computer performs signal processing on binary digits and has output as digital binary signal.

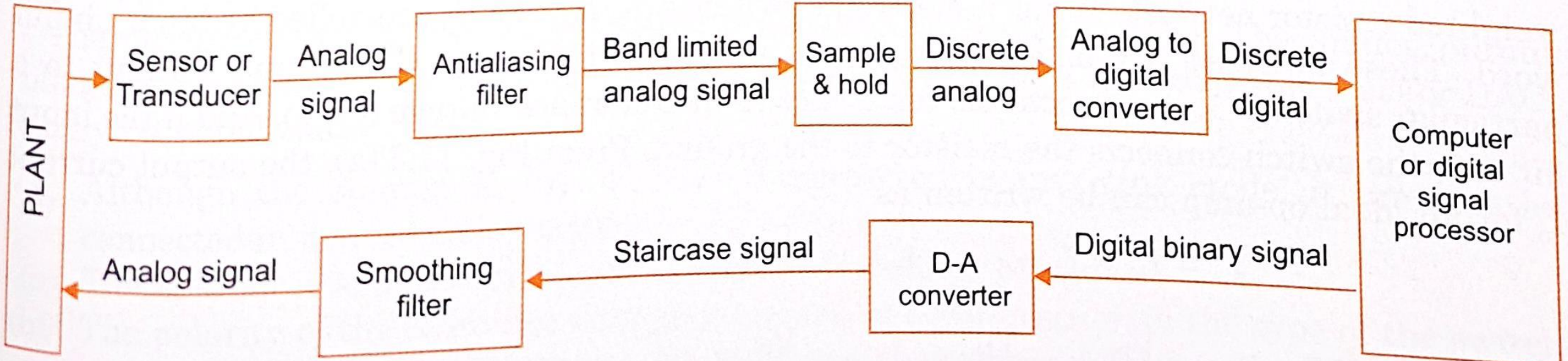


Fig. 11.1 Circuit showing application of A/D and D/A converter

1. Application of A/D and D/A convertors

- Output digital binary signal of Computer(or digital signal processor) – converted to staircase signal using D-A converter (digital to continuous) – Smoothing filter converts staircase signal to analog signal reducing quantization noise.

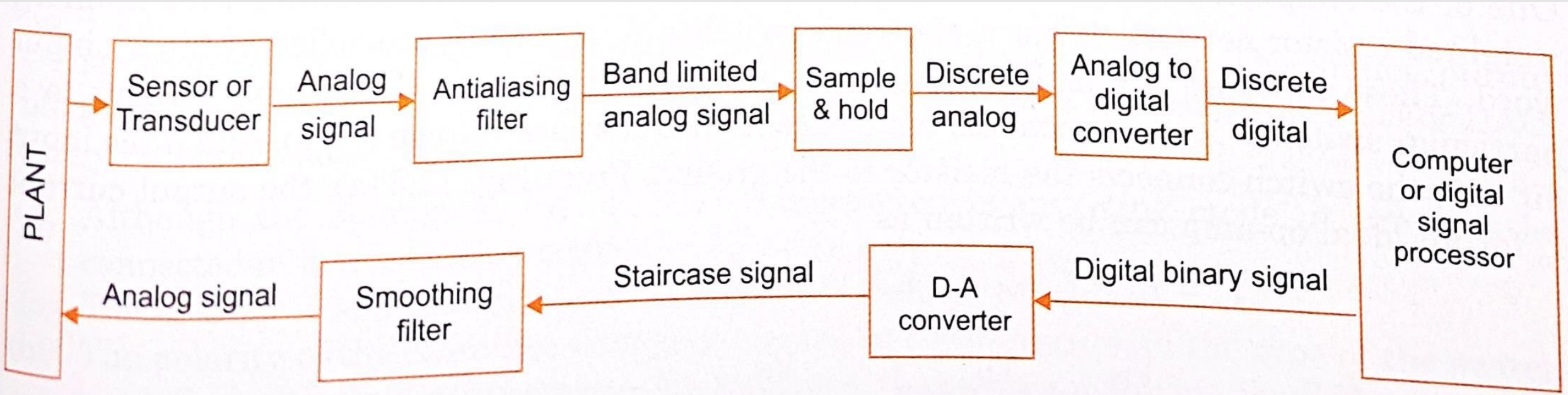


Fig. 11.1 Circuit showing application of A/D and D/A converter

1. Application of A/D and D/A convertors

- Used in either full or part in many applications: Digital audio recording and playback, computer, music synthesis, music and video synthesis, pulse code modulation transmission, data acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

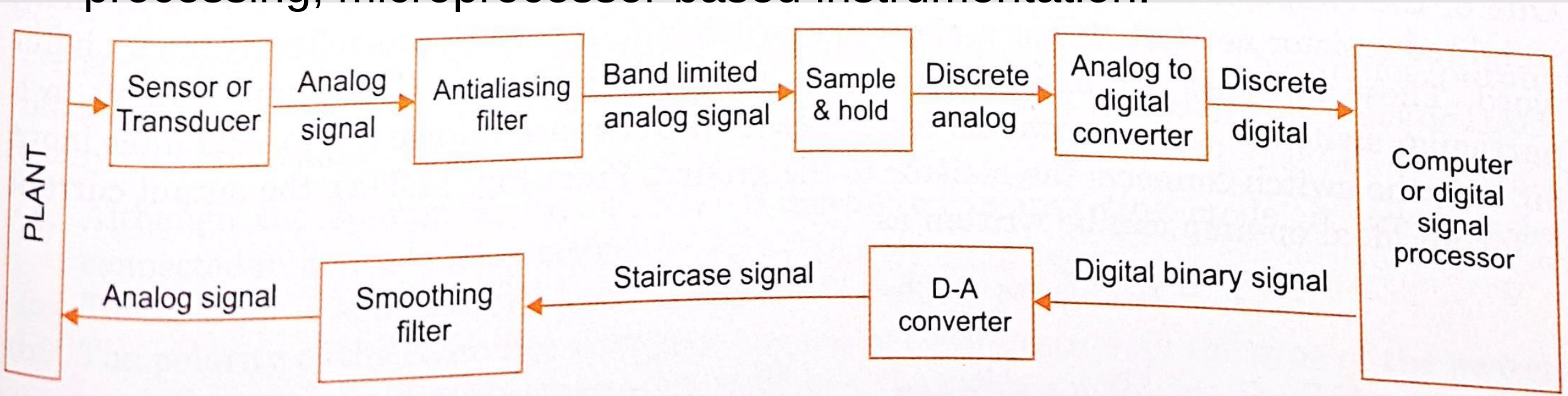


Fig. 11.1 Circuit showing application of A/D and D/A converter

1. Application of A/D and D/A convertors

- Some cases, S/H may be avoided without considerable error
- ADC(Analog to digital converter) and DAC(Digital to analog converter) are data converters and are available in IC form

2. Basic DAC techniques

- Input to DAC is n-bit binary word D and is combined with a reference voltage V_R to give analog output signal
- Output of DAC – either voltage or current
- For voltage output DAC: $V_0 = K\,V_{FS}\,(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$

V_0: Output voltage

V_{FS}: Full scale output voltage

K: Scaling factor (usually 1)

$d_1, d_2, \ldots, d_n$: n bit binary functional word with decimal point located at left

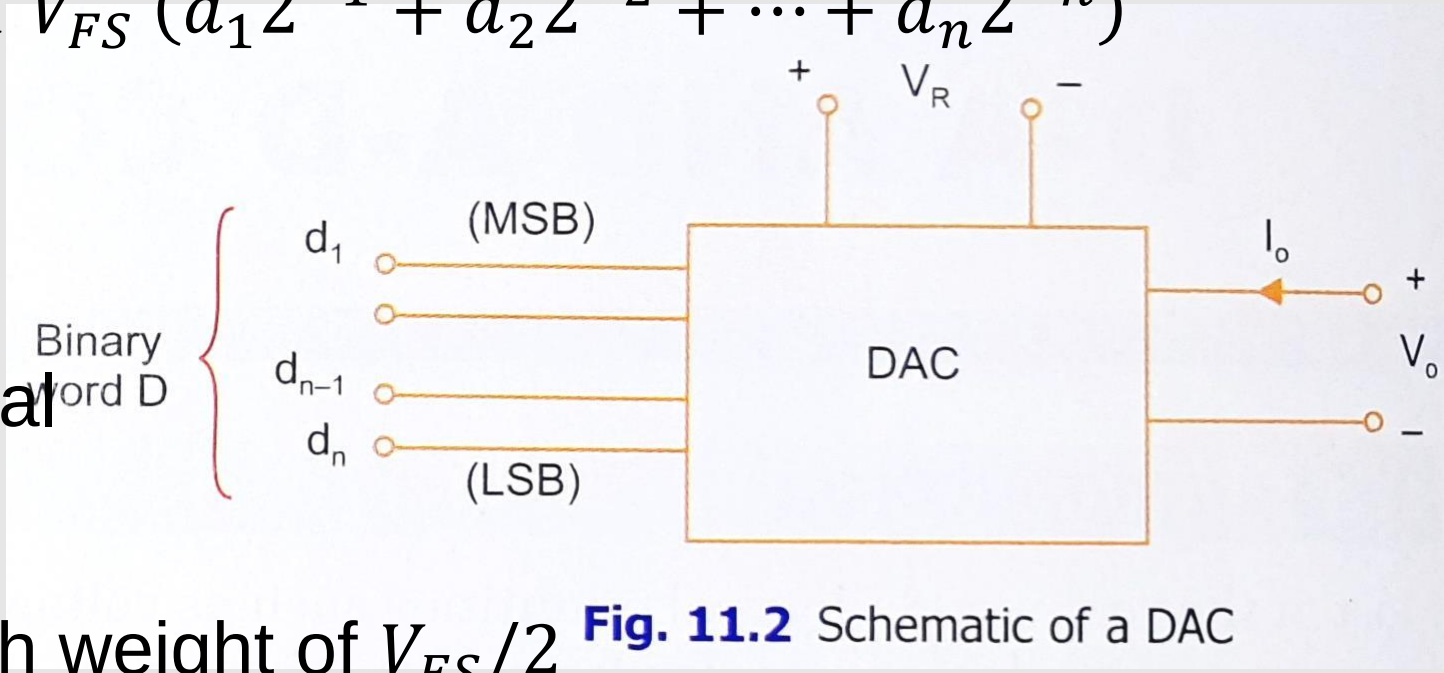


Fig. 11.2 Schematic of a DAC

d_1: most significant bit (MSB) with weight of $V_{FS}/2$

d_2: least significant bit (LSB) with weight of $V_{FS}/2^n$

2. Basic DAC techniques

- Various methods are available.
- Methods involving resistors:
  Weighted resistor DAC

  R-2R ladder

  Inverted R-2R ladder

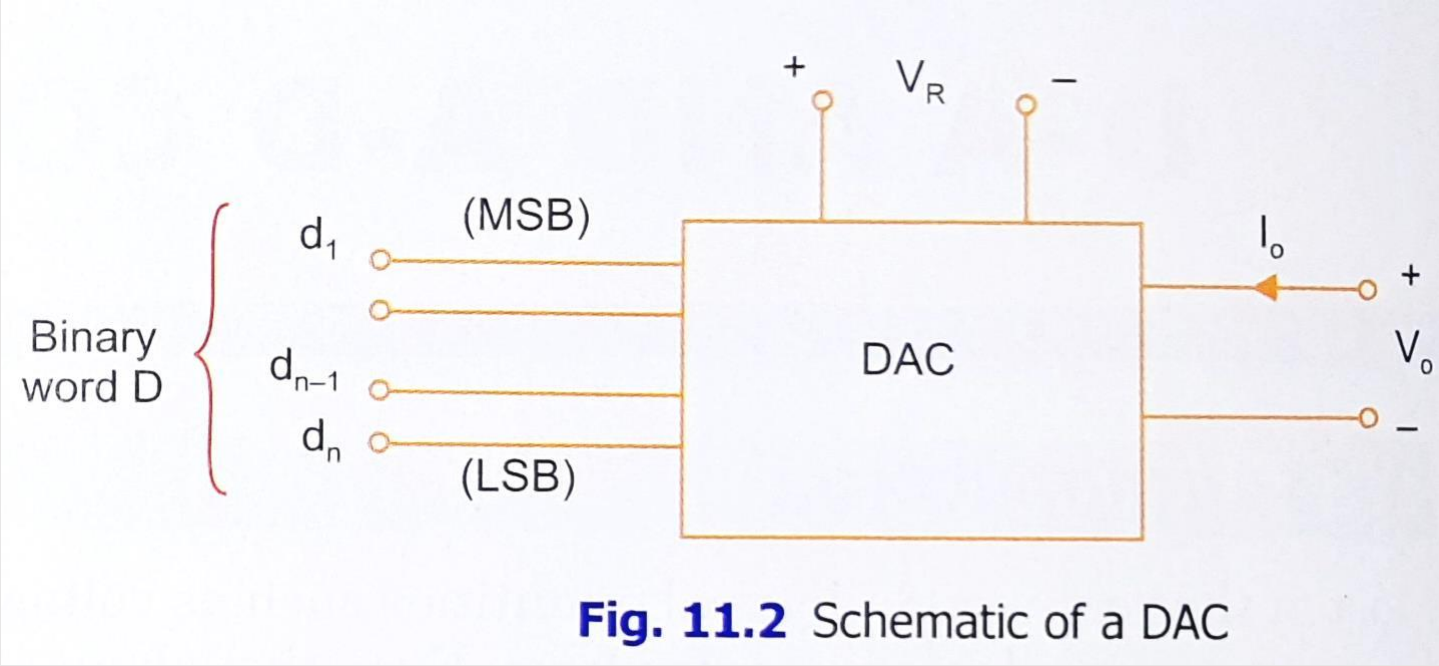
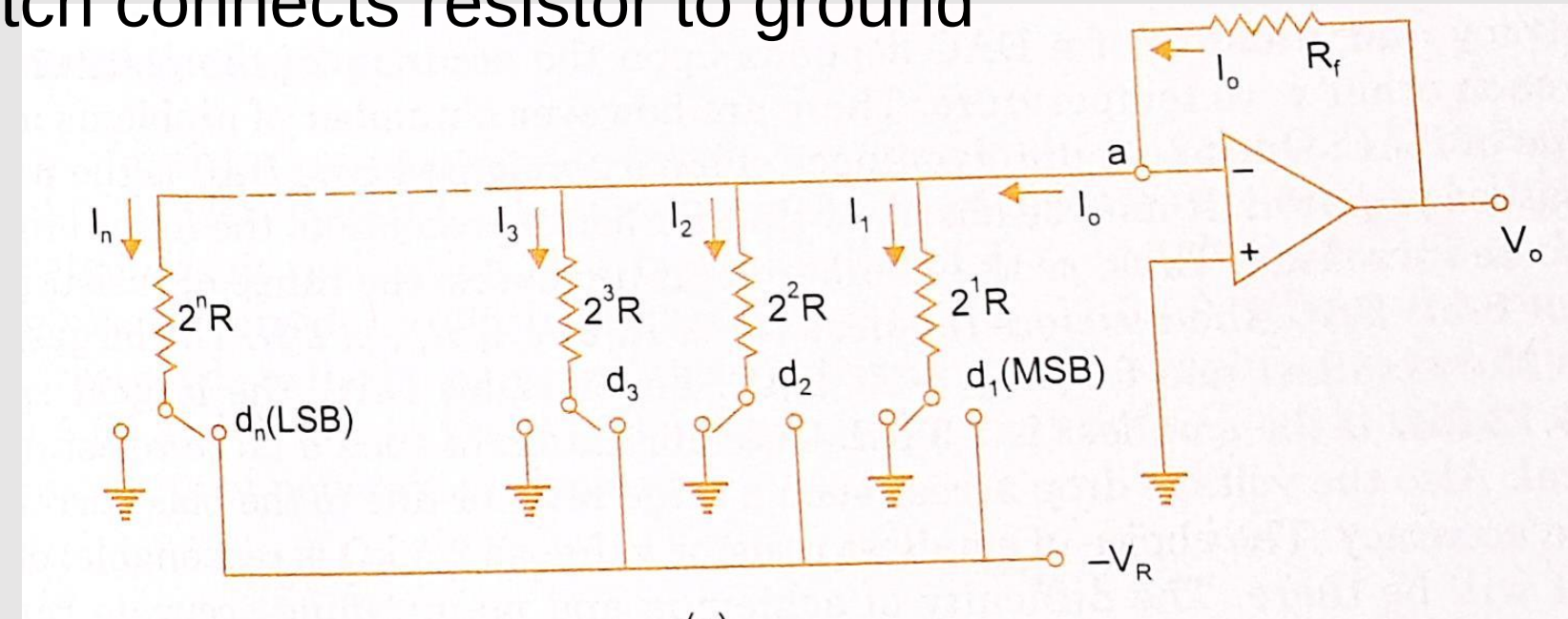


Fig. 11.2 Schematic of a DAC

3. Weighted Resistor DAC

For voltage output DAC:
$V_0 = K\,V_{FS}\,(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$

- Simplest: Uses summing amplifier with binary weighted resistors
- N electronic switches, d_1, d_2,…, d_n controlled by binary input word
- Single pole double throw (SPDT) type switches
- If a binary input to particular switch is 1, connects resistance to reference voltage $-V_R$
  If a binary input is 0, switch connects resistor to ground



3. Weighted Resistor DAC

For voltage output DAC:
$V_0 = K\,V_{FS}\,(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$

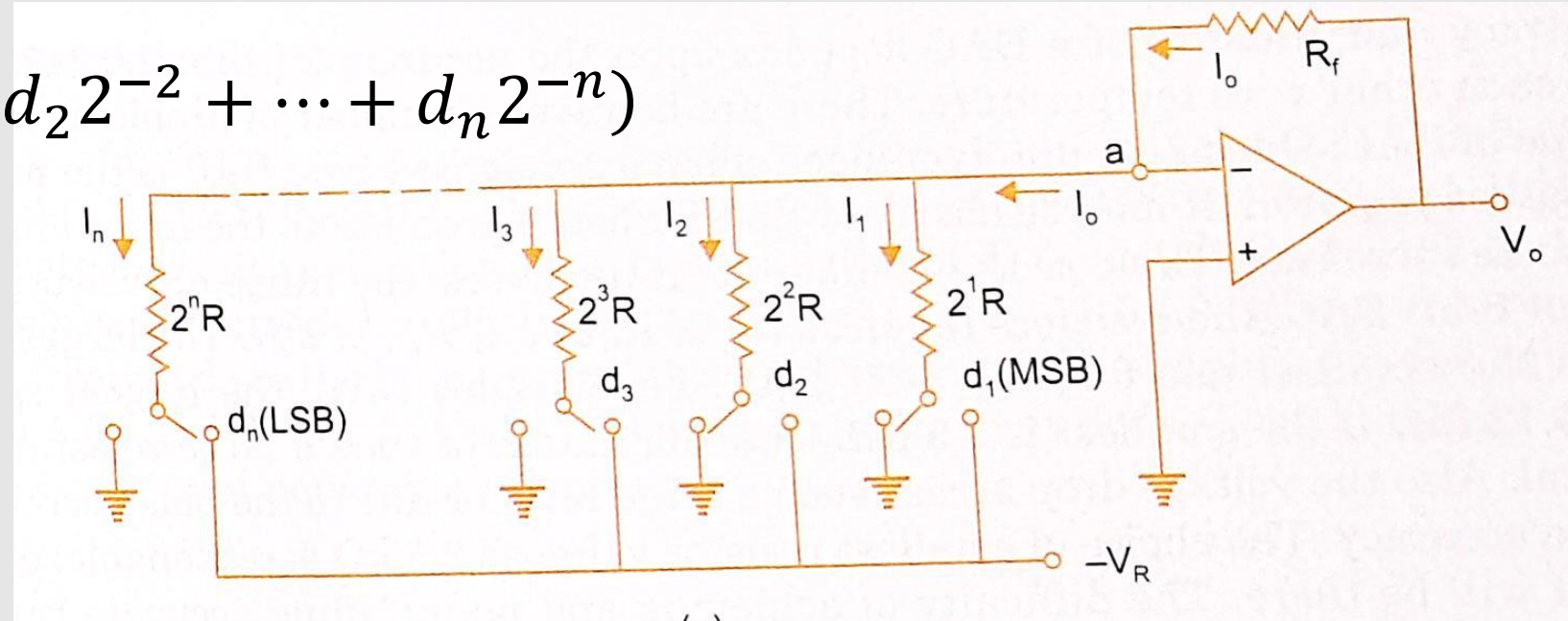
- Output current for ideal Op-amp

$$I_0 = I_1 + I_2 + \cdots + I_n$$
$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2R^2} d_2 + \cdots + \frac{V_R}{2R^n} d_n$$
$$= \frac{V_R}{R}(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$$

Output voltage:

$$V_0 = I_0 R_f = V_R \frac{R_f}{R}(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$$

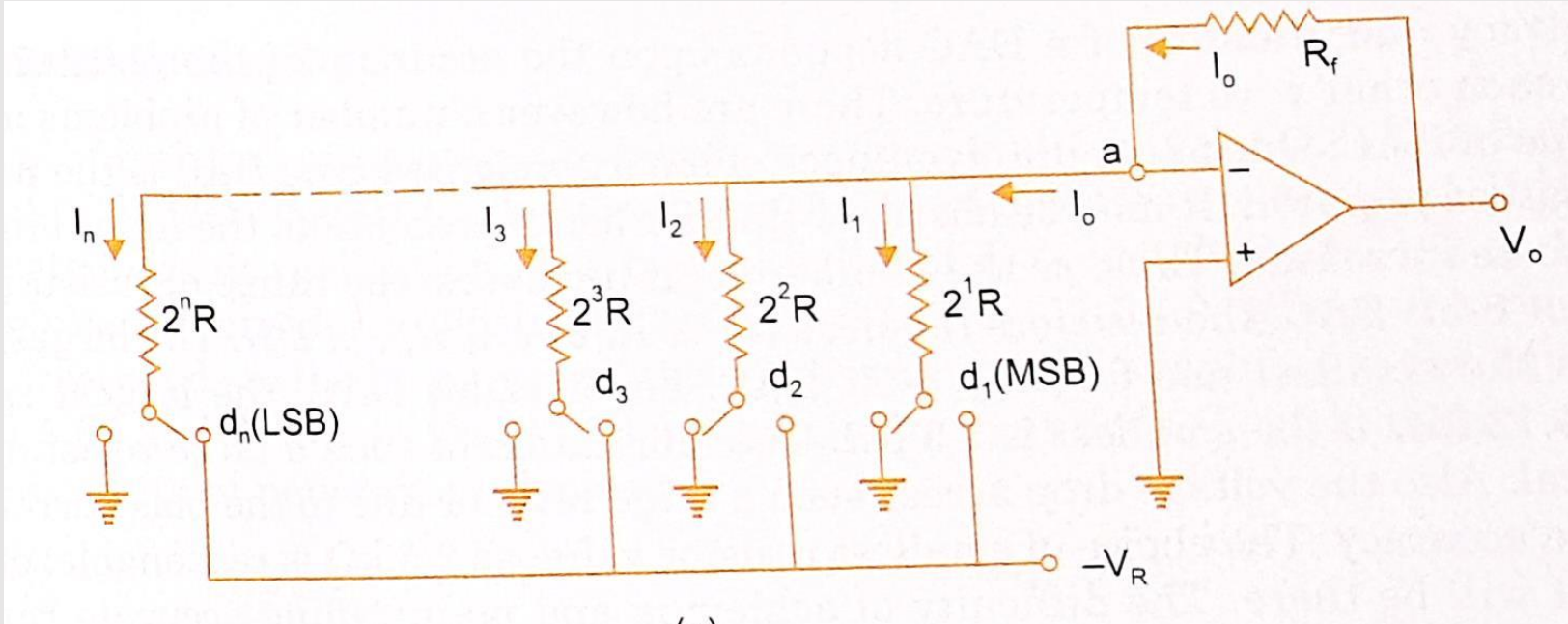
If $R_f = R$, then $K = 1$
and $V_{FS} = V_R$



3. Weighted Resistor DAC

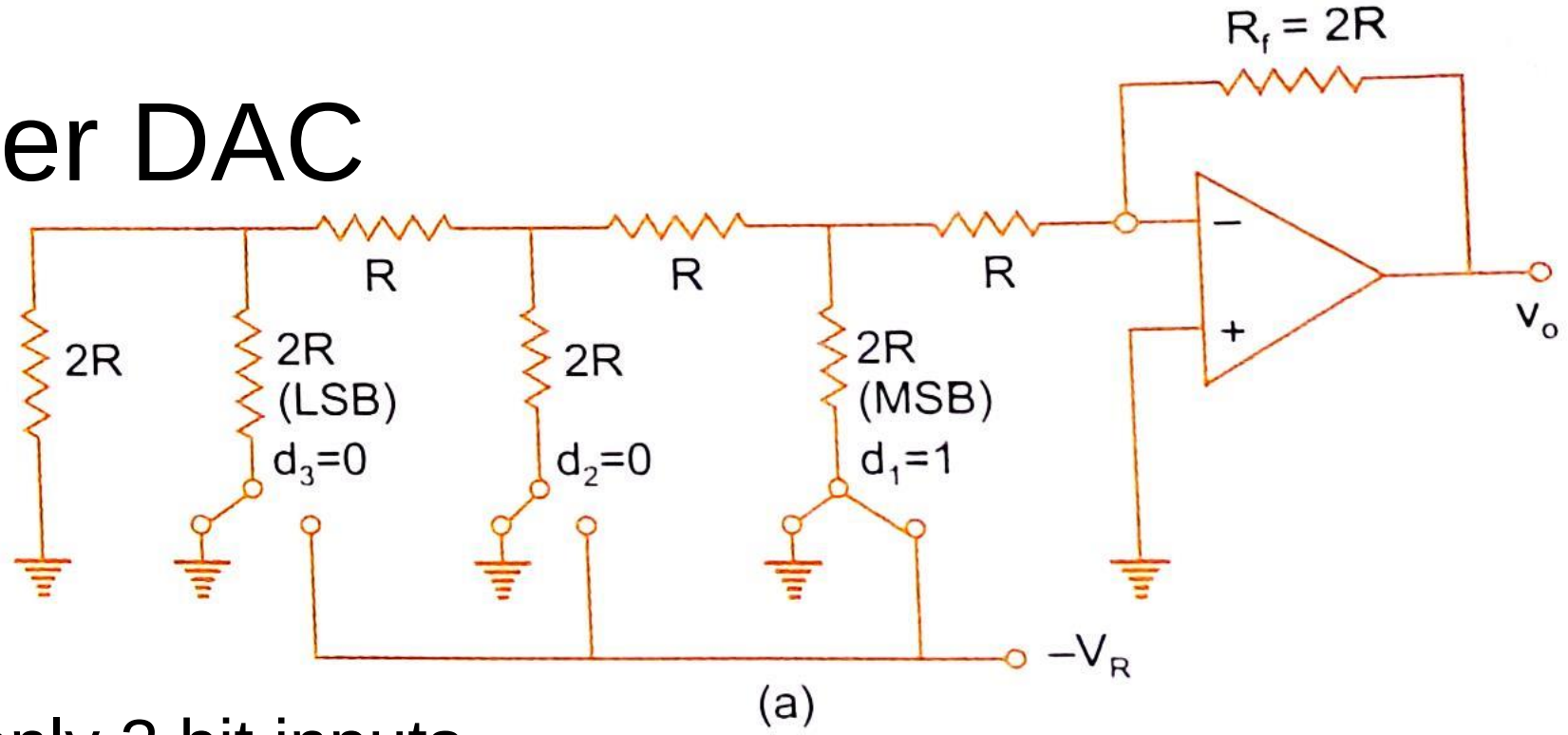
For voltage output DAC:
$V_0 = K\,V_{FS}\,(d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n})$

- Disadvantage:
  Resistor range increases for better resolution
  Difficult to fabricate different and large resistor values
- Accuracy is low

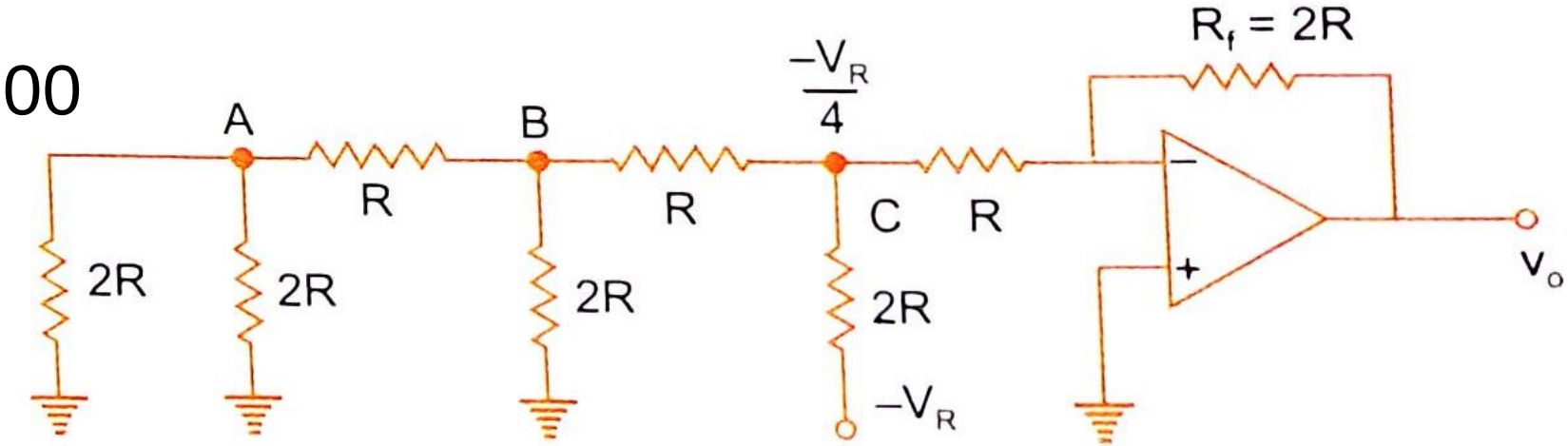


4. R-2R Ladder DAC

- Only 2 resistor values are used
- Well suitable for ICs
- Typical ranges of R: 2.5kΩ to 10kΩ
- For example(simple) only 3 bit inputs are present
- $d_1 d_2 d_3$: binary word = 100
- Simplified circuit is:



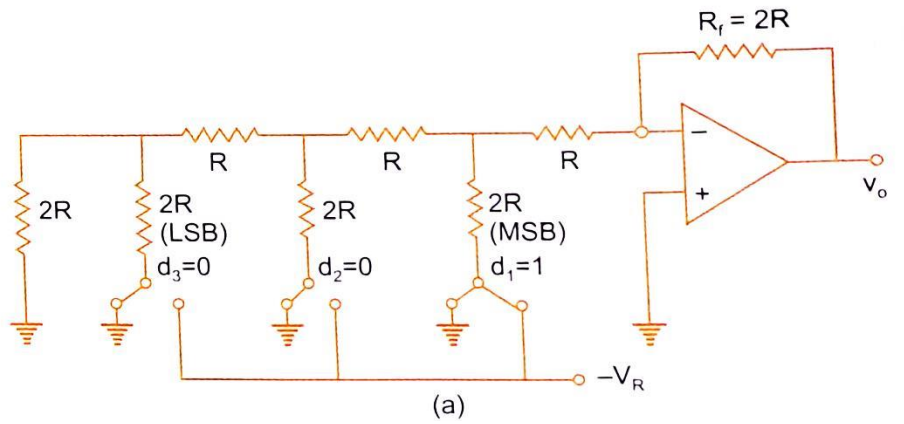
(a)



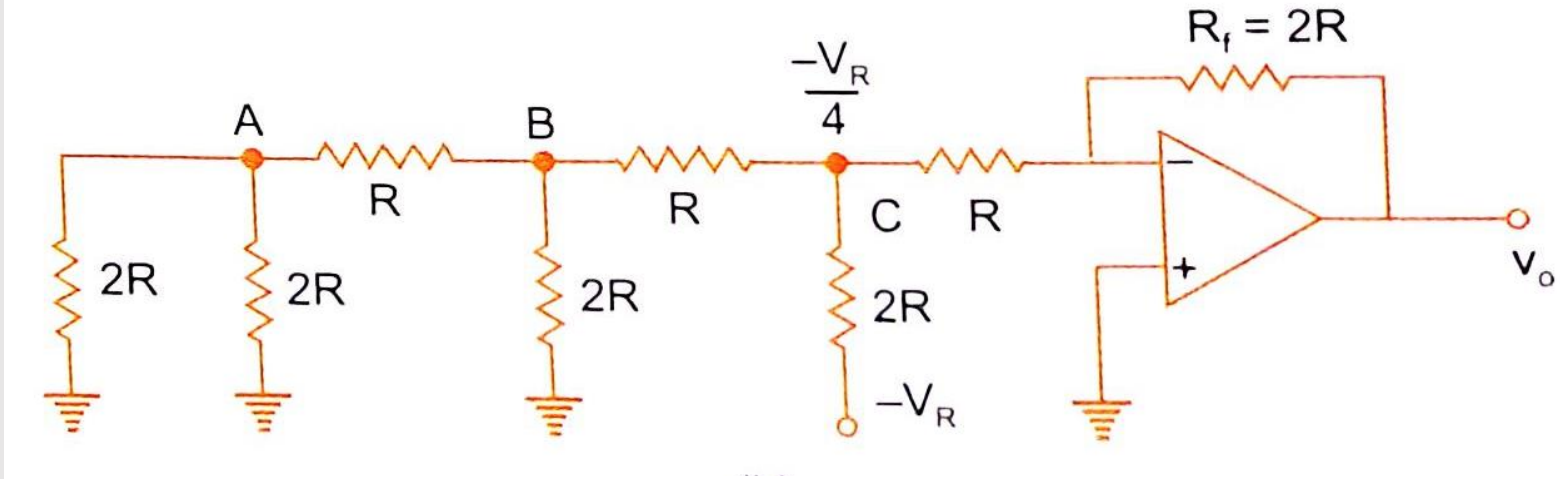
(b)

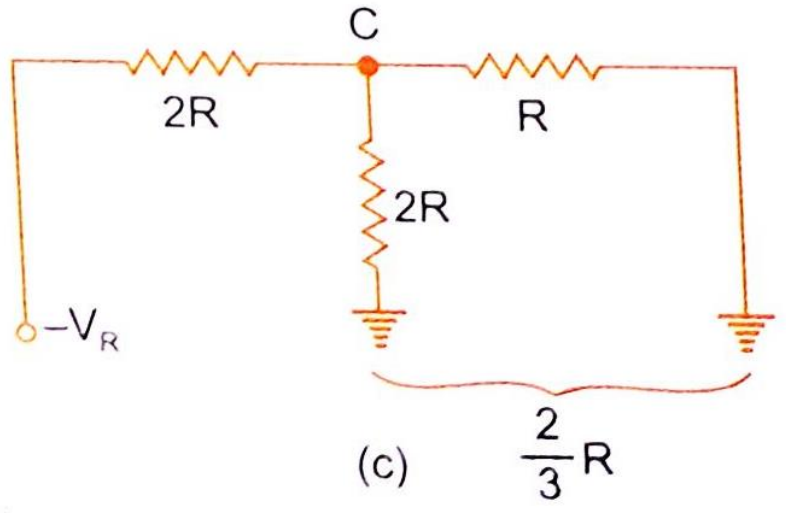
4. R-2R Ladder DAC

- Only 2 resistor values are used
- Well suitable for ICs
- Typical ranges of R: 2.5kΩ to 10kΩ
- For example(simple) only 3 bit inputs are present
- $d_1 d_2 d_3$: binary word = 100
- Simplified circuit is:
  It has effective vales at C node as shown here:



(a)





(c)

4. R-2R Ladder DAC

- $d_1d_2d_3$: **binary word = 100**
- Voltage at Node C using Network analysis:

$$= -V_R\left(\frac{2R\|R}{2R+(2R\|R)}\right)$$

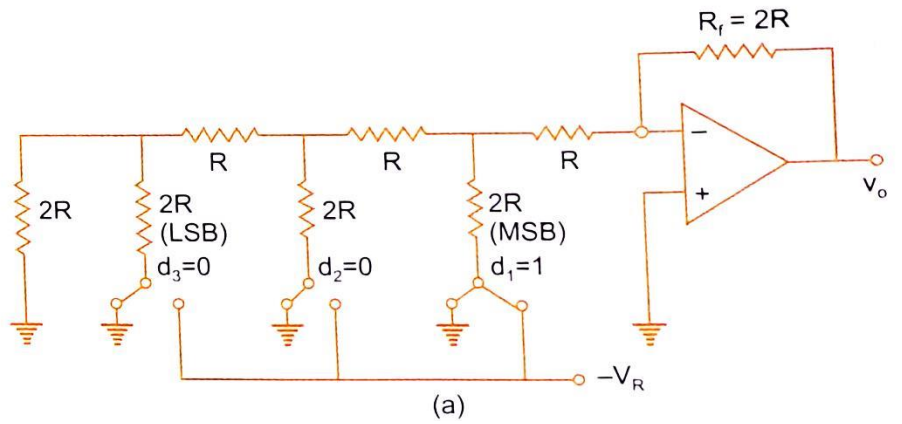
$$= -V_R\left(\frac{2R/3}{2R+2R/3}\right)$$

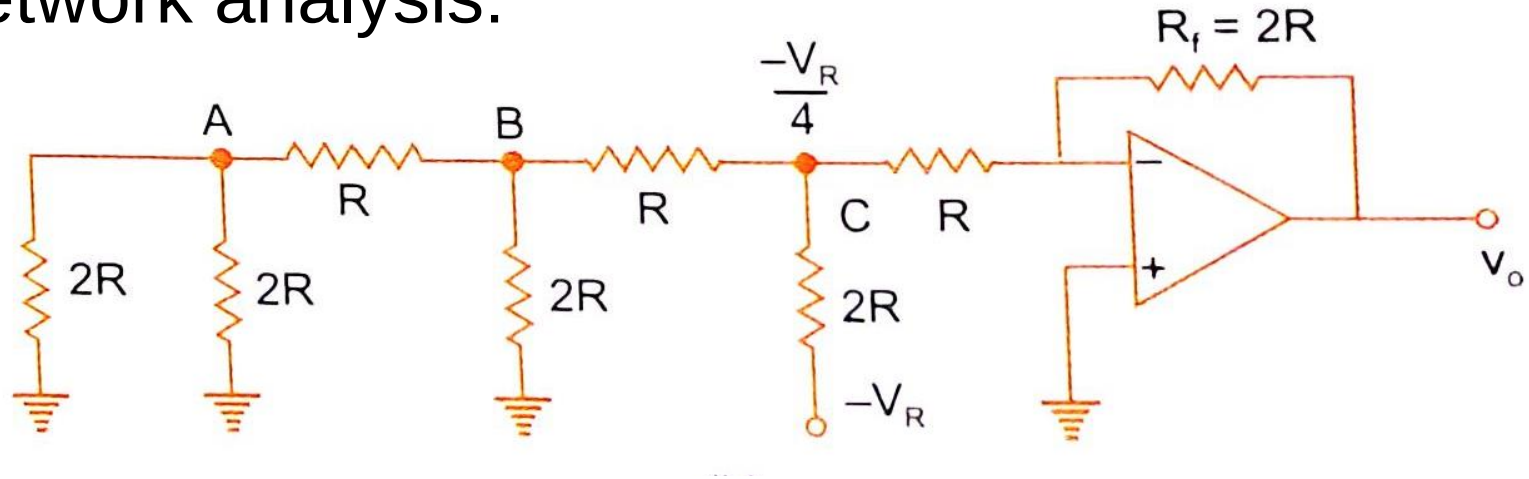
$$= -V_R/4$$

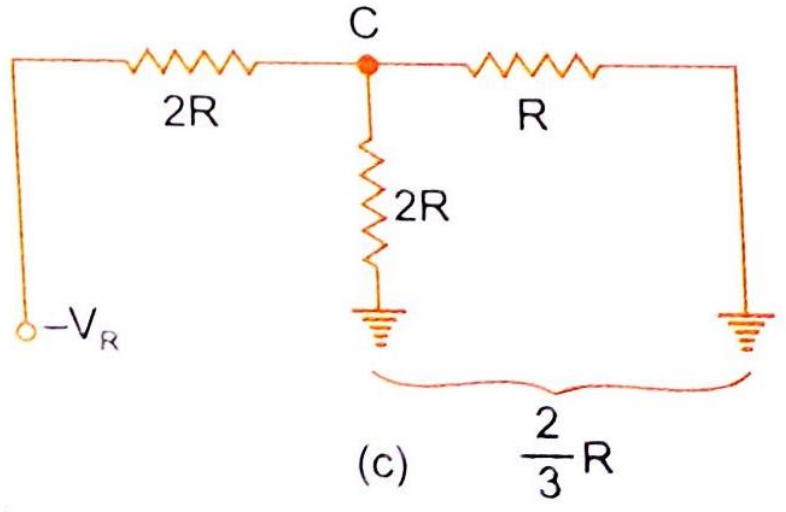
with input as $-V_R/4$

Output voltage of inverting configuration:

$$V_0 = -\frac{R_f}{R}\left(-\frac{V_R}{4}\right) = -\frac{2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

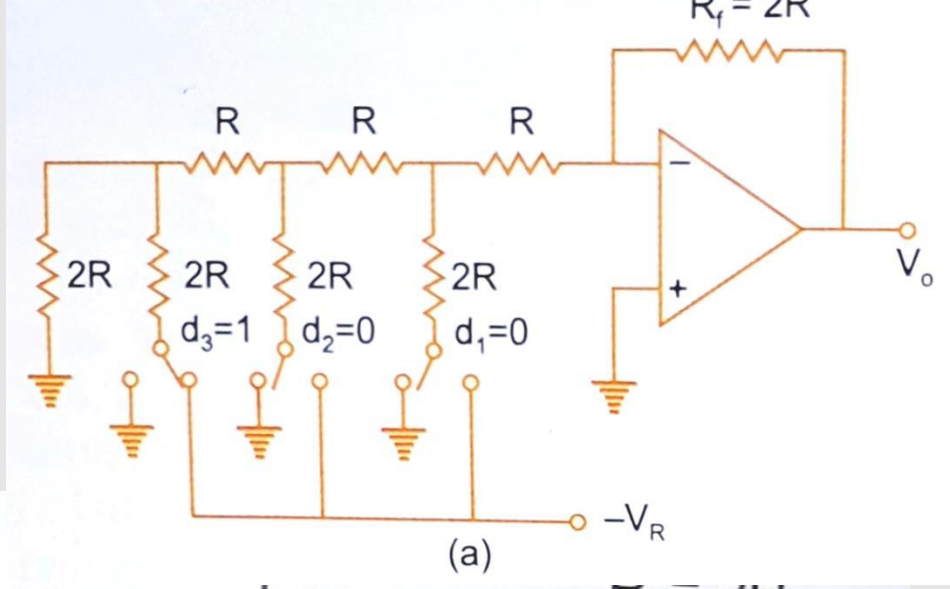




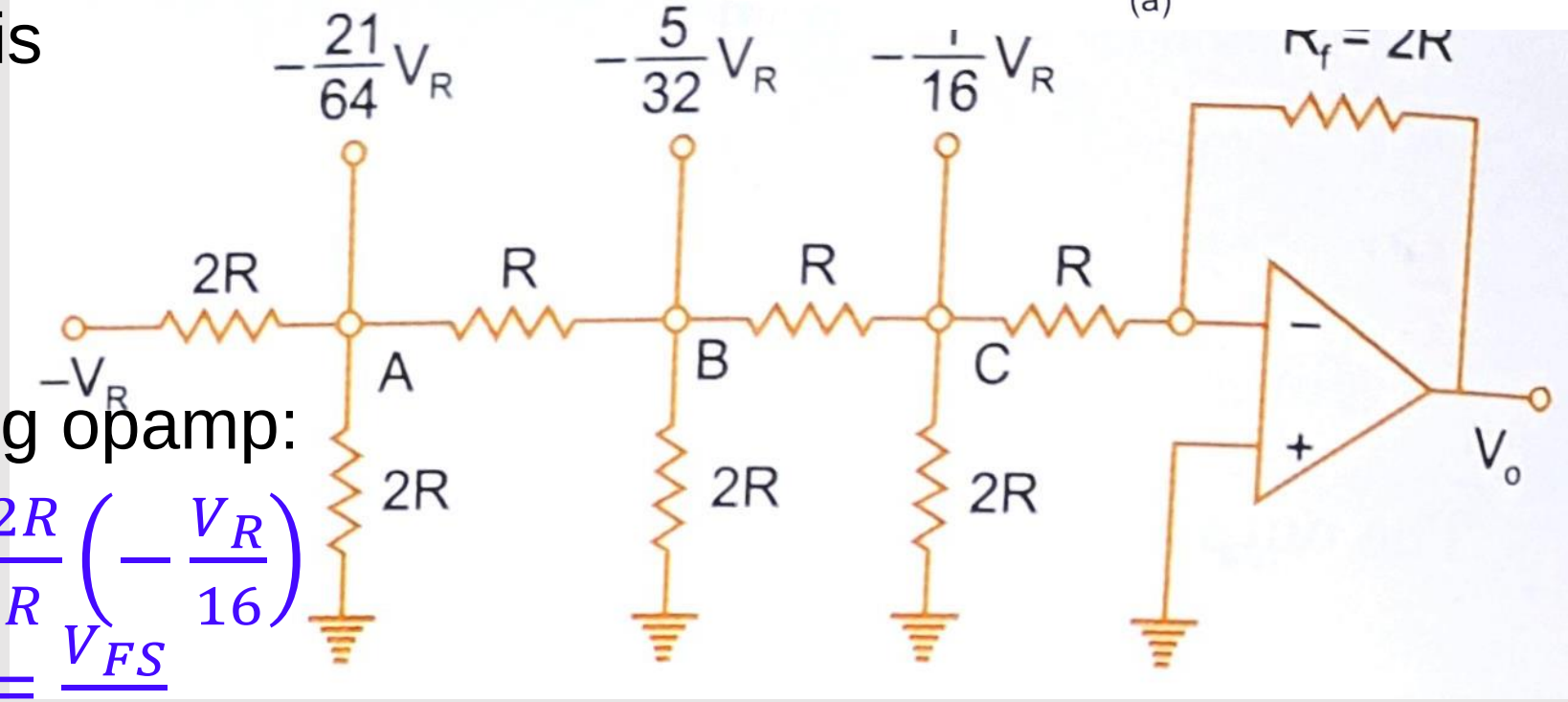


4. R-2R Ladder DAC

- $d_1 d_2 d_3$: **binary word = 100**
- Similarly redraw circuit:



And apply nodal analysis



with input as $-V_R/8$ at C

Output voltage of inverting opamp:

$$V_0 = -\frac{R_f}{R}\left(-\frac{V_R}{16}\right) = -\frac{2R}{R}\left(-\frac{V_R}{16}\right)$$

$$= \frac{V_R}{8} = \frac{V_{FS}}{8}$$

4. R-2R Ladder DAC

- Similarly, in the R-2R ladder type, output voltages of other 3bit binary words which are the DAC input can be calculated

1. Analog to digital converter

- Accepts analog input voltage V_a and produces output binary word $d_1 d_2 \ldots d_n$ with functional value $D = d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}$
- MSB: d_1
- LSB: d_n
- Two control lines: START (when to start) and EOC: End of conversion)
- ADCs may give digital output to Microprocessors(interfacing) or Digital dive LCD or LED displays

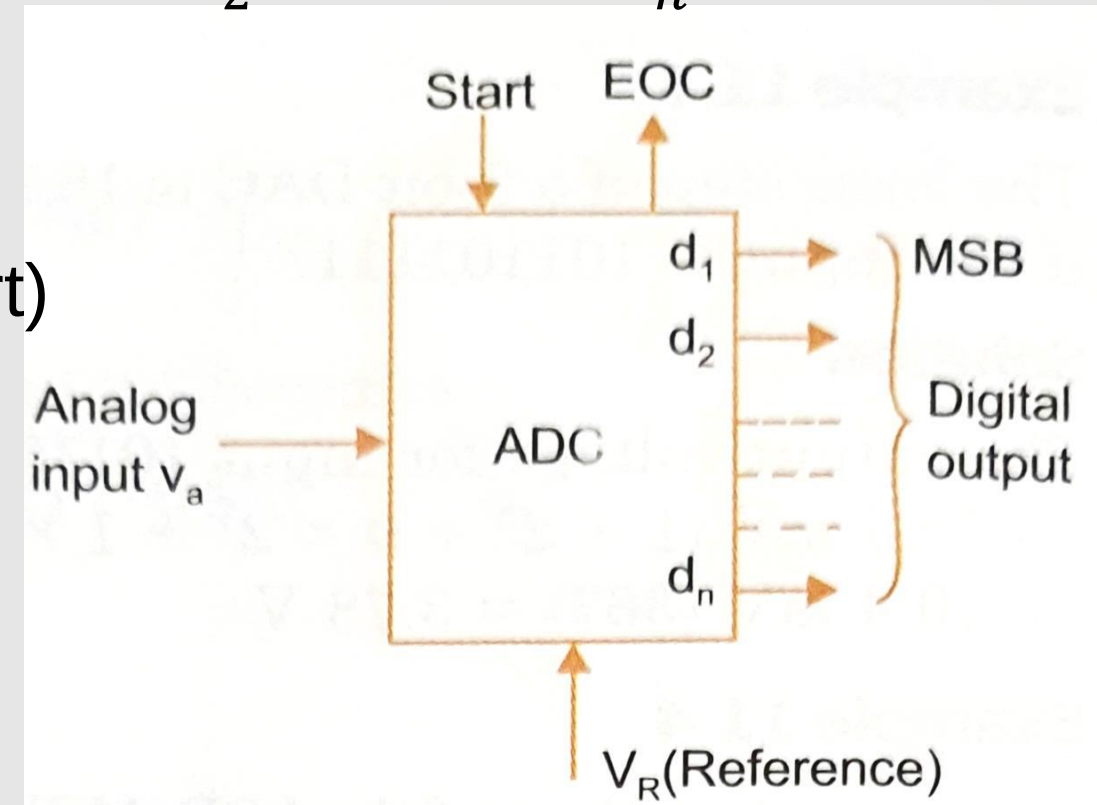


Fig. 11.9 Functional diagram of ADC

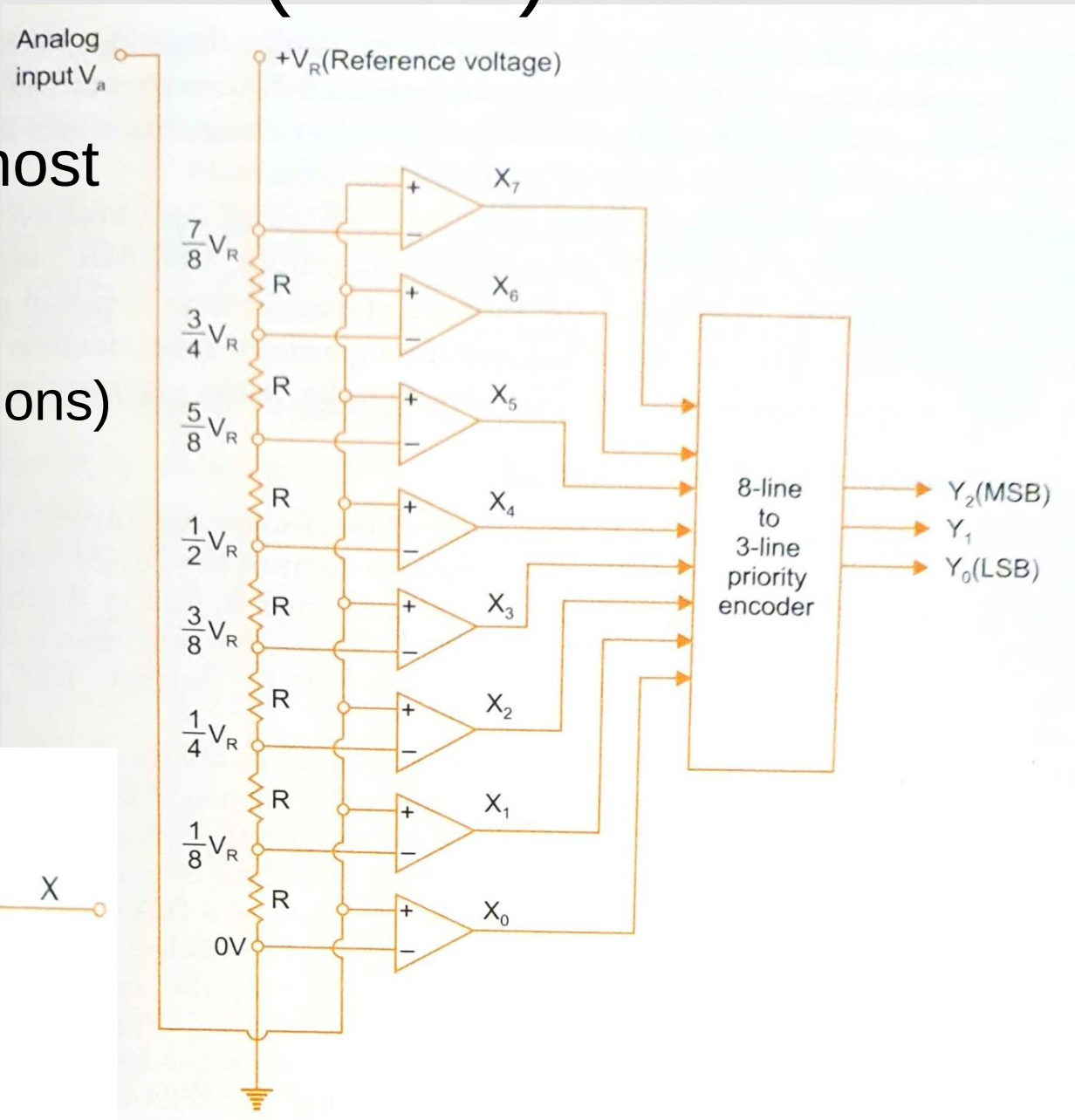
1. Analog to digital converter

ADCs classification

- Direct type ADC
  (Compare given analog signal with internally generated equivalent signal)
  - **Flash (comparator) type converter**
  - Counter type converter
  - Tracking or servo converter
  - Successive approximation type converter (Most commonly used)
- Integrating type ADC
  (first changes analog input to linear function of time and frequency, and then to digital code) – Most commonly used
  - Charge balancing ADC
  - Dual slope ADC

2.1 Direct: Parallel Comparator (Flash) A/D Converter

- Simplest A/D converter, fastest and most expensive technique
- 3Bit A/D converter:
  Resistive divider (equal R for equal divisions)
  8 op-amp comparators
  8-line to 3 line encoder (3 bit priority encoder)



Voltage input	*Logic output X*
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

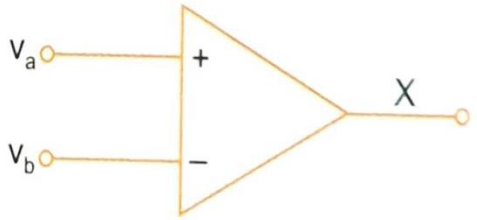


Fig. 11.10 (b) Comparator and its truth table

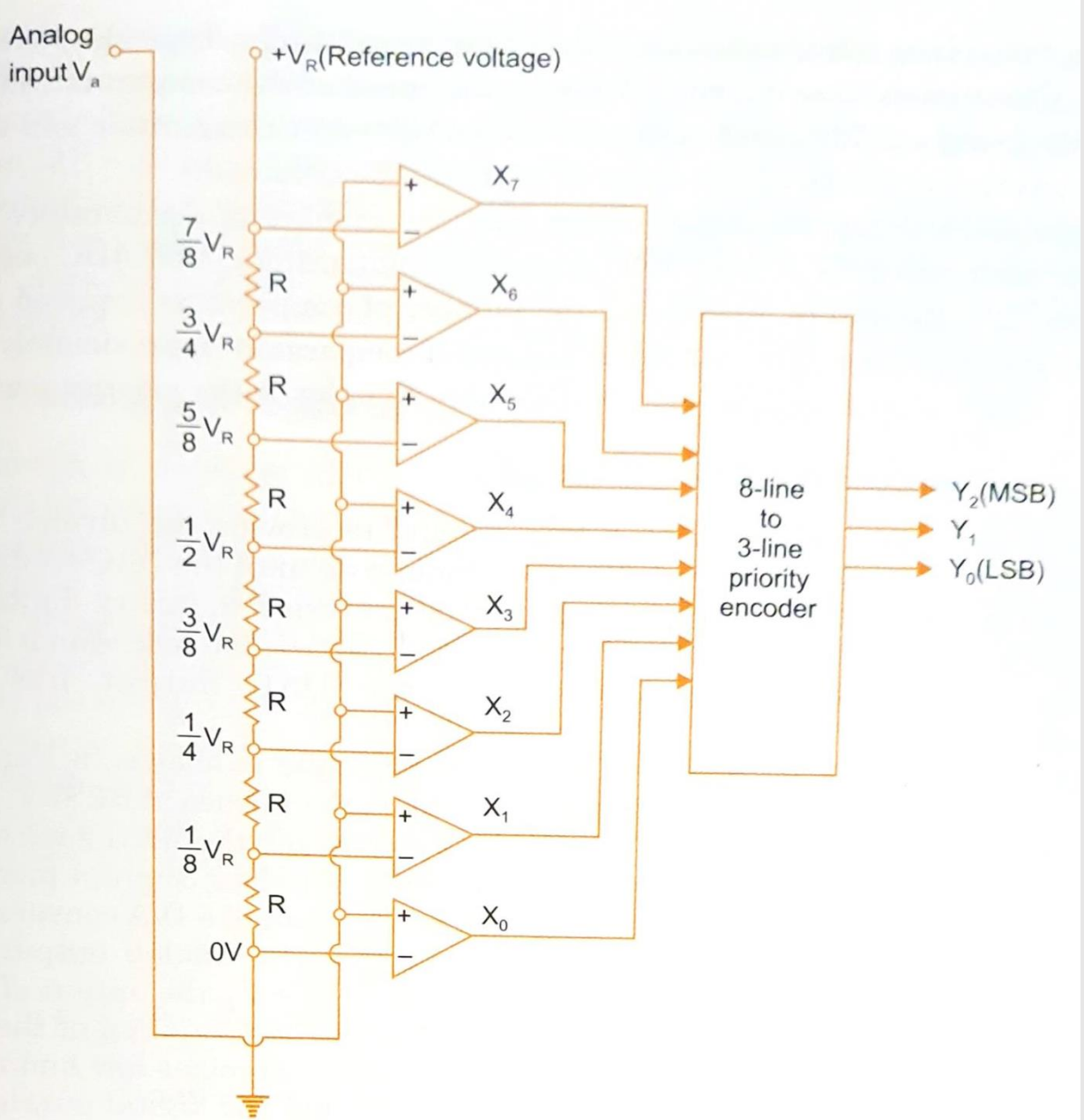
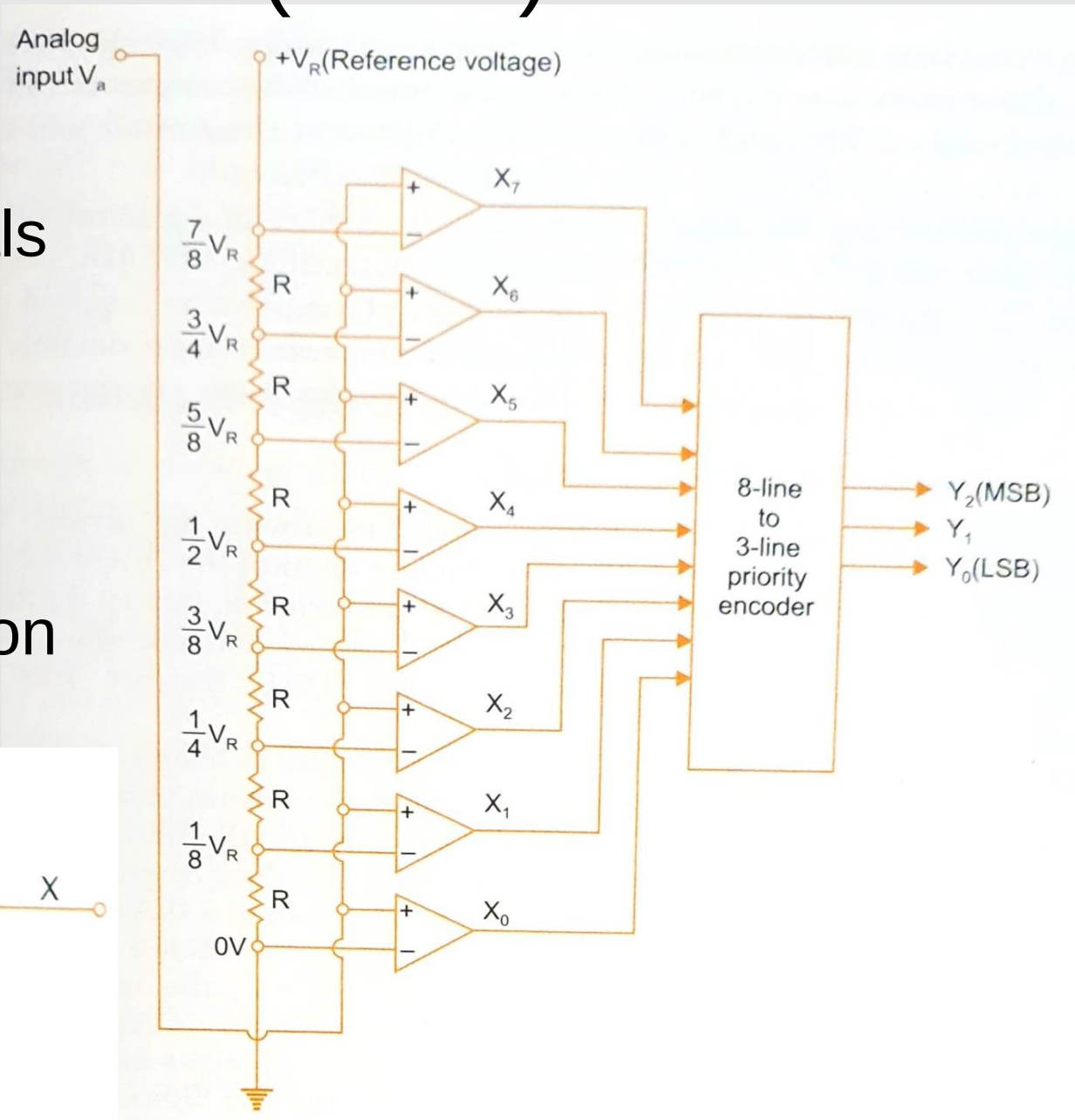


Fig. 11.10 (a) Basic circuit of a flash type A/D converter

2.1 Direct: Parallel Comparator (Flash) A/D Converter

- Circuit compares: Voltage levels are available at non-inverting terminals and divided between VR (reference voltage) and ground
- Circuit compares analog input V_a with each node voltages
- High speed conversion with conversion time less than 100ns



Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

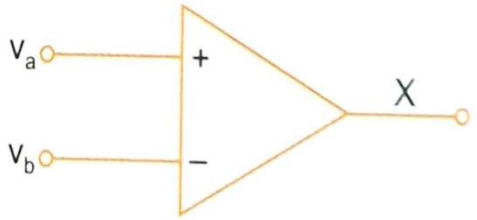


Fig. 11.10 (b) Comparator and its truth table

2.1 Direct: Parallel Comparator (Flash) A/D Converter

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

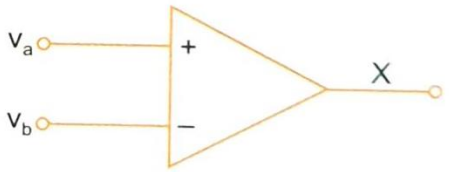
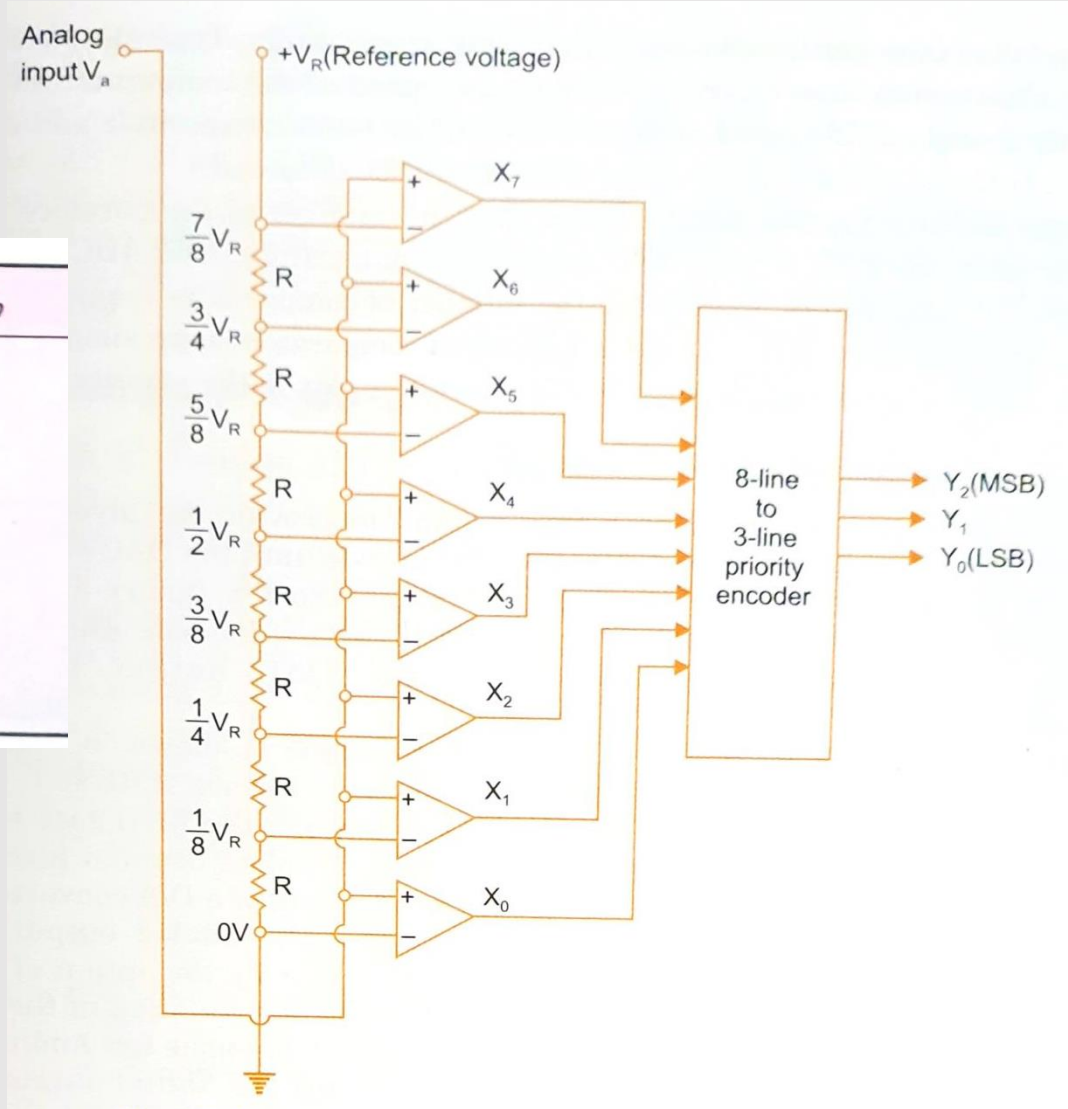


Fig. 11.10 (b) Comparator and its truth table



2.1 Direct: Parallel Comparator (Flash) A/D Converter

- Disadvantage: Number of comparators double for each bit increase ($2^n - 1$ comparators for n bit)

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value

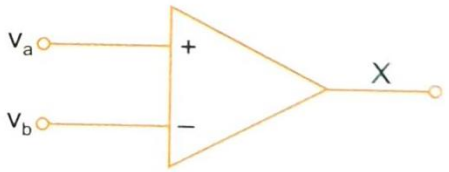


Fig. 11.10 (b) Comparator and its truth table