Reg. No.:

Name :

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act 1956)

Continuous Assessment Test 2 – June 2023

Programme	:	B.Tech (ECE/ECM)	Semester	:	FIS 2023-24
Course	:	VLSI System Design	Code	:	BECE303L
			Class Nbr	:	CH2022232500114, CH2022232500316, CH2022232500116, CH2022232500115, CH2022232500117
Faculty	:	Sakthivel S M, Ravi Shankar A, Biswajit Jena, Prashanth Kumar B, Sridhar C	Slot	:	A2+TA2
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		A depletion-type NMOS transistor realized using a metal-gate process is shown in the figure 1 below. With neat cross-sectional sketches, explain the fabrication flow diagram of the transistor. How many masks are required to realize this transistor? Neatly draw all the masks used for fabrication. Assume a positive photoresist for the metallization process step and a negative photoresist for all other process steps. Considering the time constraint, limit the number of process steps to ten. **(8 marks)**	[8]

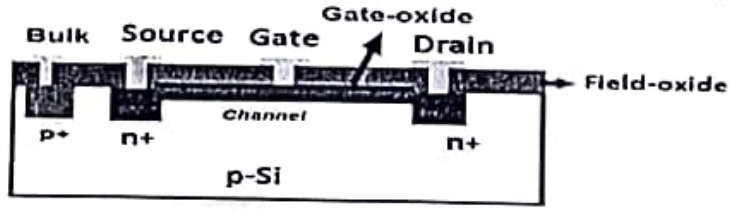

Figure 1

2.		Sketch a color-coded stick diagram and Euler path for the function **(7 Marks)** $F = \overline{(RG+V+H).WF}$	[7]
3.		Calculate the minimum delay for the path from A to B in the circuit illustrated in figure 2. Size the gates (X, Y, Z, W) accordingly to achieve this delay for a load capacitance of $C_L = 75$. **(10 Marks)**	[15]
		Determine the ratio of NMOS to PMOS in each stage, relative to their (W/L) ratios, for the load capacitance mentioned in (a). **(5 Marks)**	

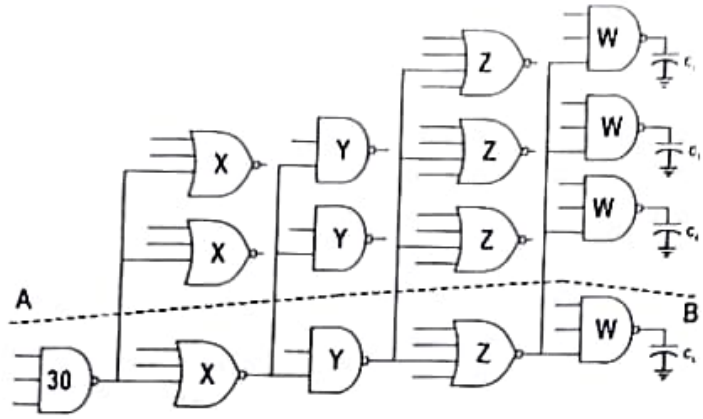

Figure 2

Evaluate the voltages at all the nodes of the pass-transistor circuit shown in figure 3. Assume that the threshold voltage of all the transistors is 0.45 V. Ignore the body effect. **(4 marks)**

4. [4]

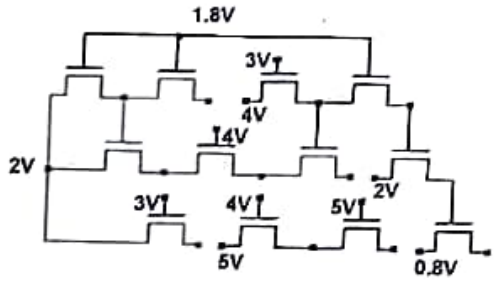

Figure 3

Construct a truth table and evaluate the OUT signal of the following circuit diagram as shown in figure 4. For the eight input combinations, mention the ON/OFF condition of all the transmission gates in the truth table. **(6 marks)**

5. [6]

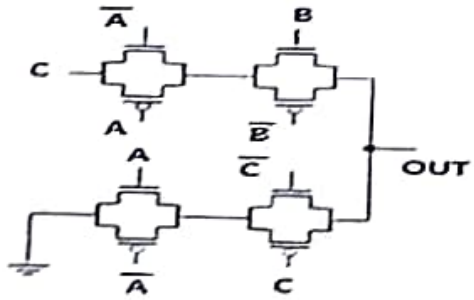

Figure 4

(a) Sketch pseudo-nMOS gate that implement the function
$F=\overline{X.(A+B+C)+(Y.Z)}$ **(4 marks)**

(b) Draw a 3-input XOR/XNOR based CVSL circuit where P pull-up devices are cross-coupled to latch output. **(6 marks)** [10]