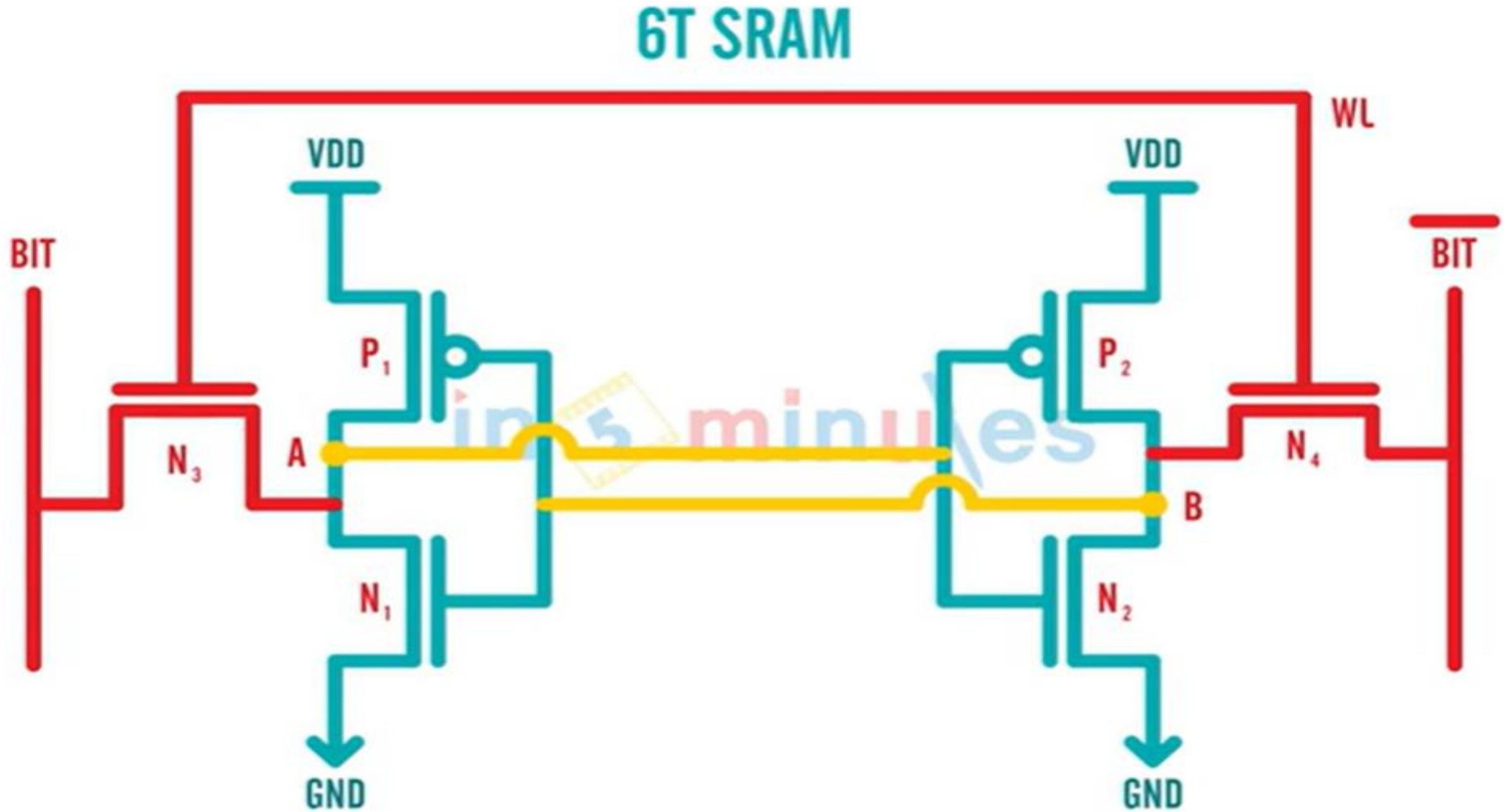
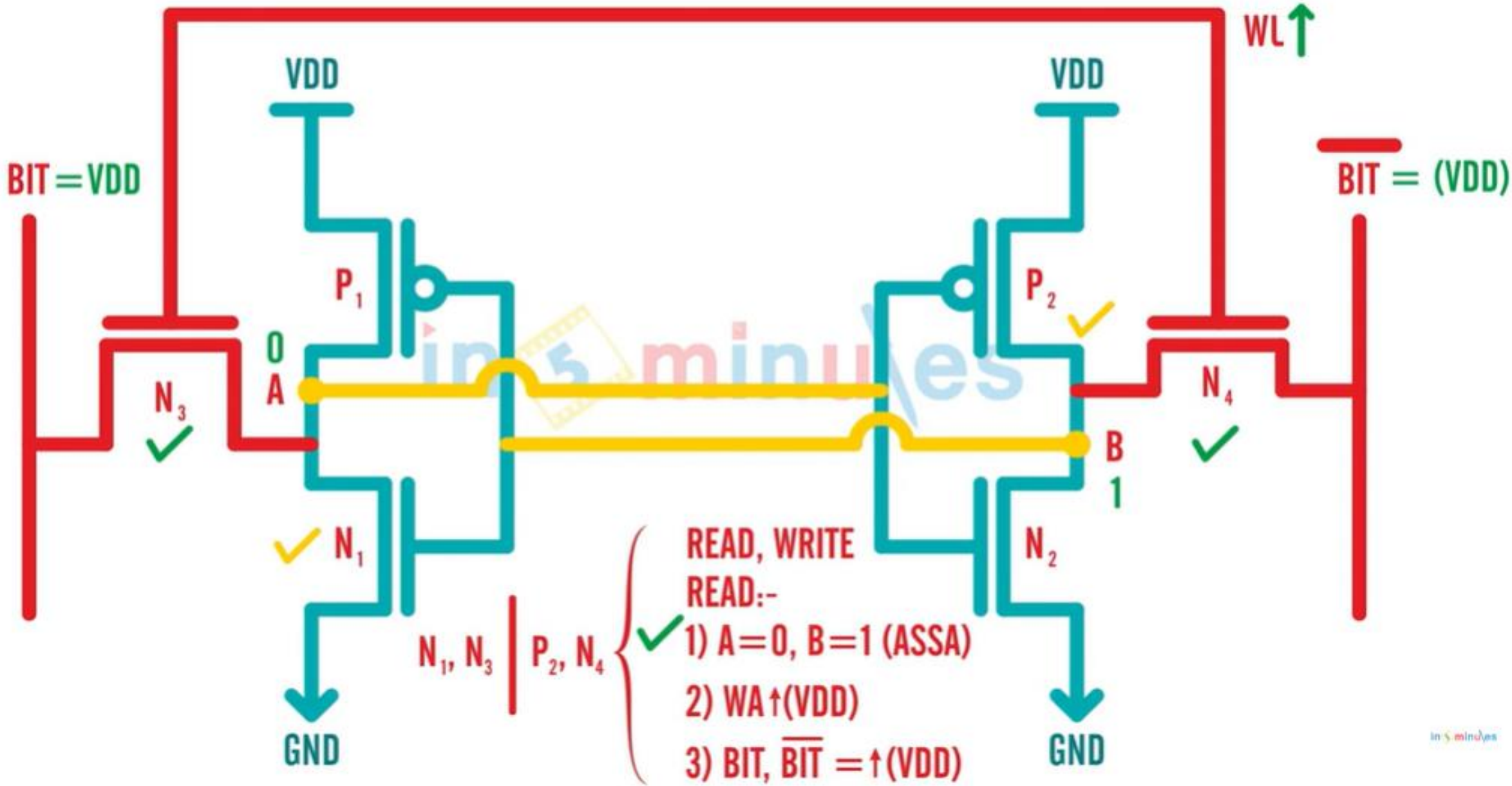
Semiconductor Memory Design

Unit -7

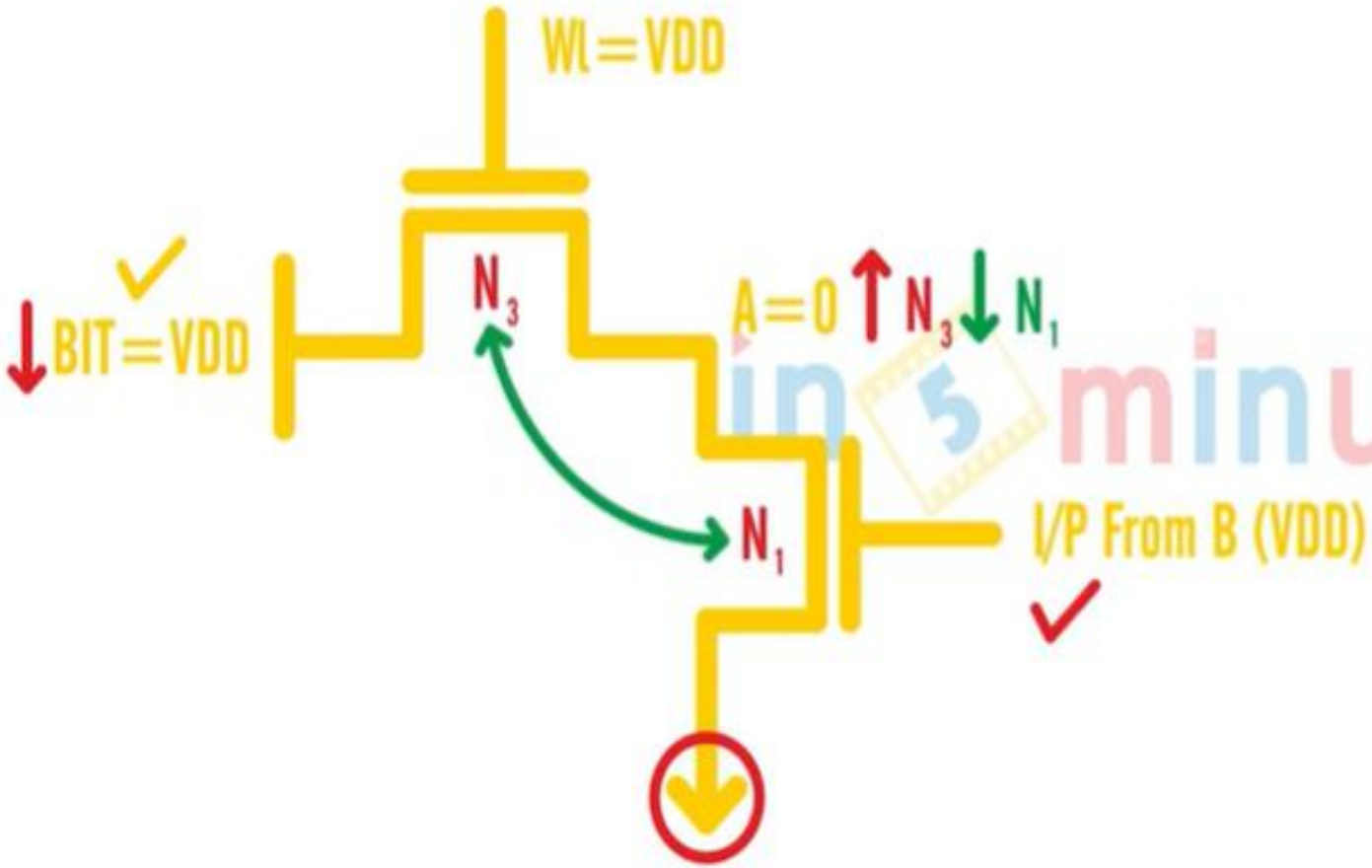
by
Dr. SAKTHIVEL.S.M

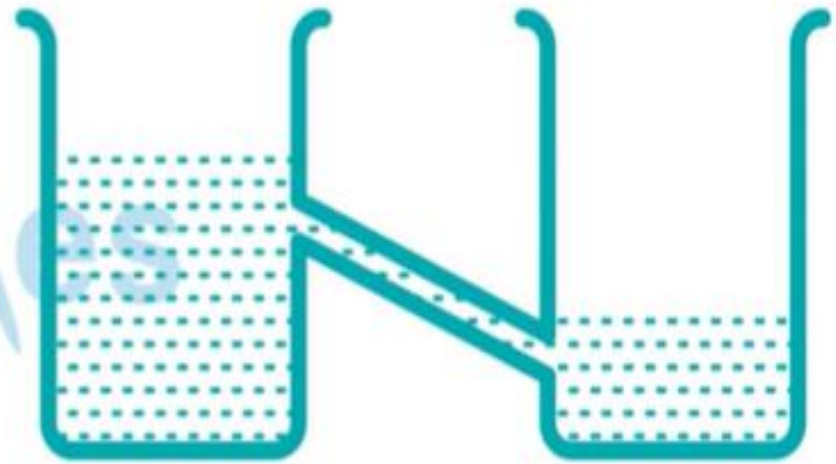

6T SRAM
WL
VDD
VDD
BIT
BIT
P1
P2
N3
A
N4
B
N1
N2
GND
GND

6T SRAM


WL ↑
VDD
VDD
BIT = VDD
BIT = (VDD)
P1
P2
N3
N4
A
0
B
1
N1
N2
GND
GND
N1, N3 | P2, N4
READ, WRITE
READ:-
1) A = 0, B = 1 (ASSA)
2) WA ↑ (VDD)
3) BIT, BIT = ↑ (VDD)

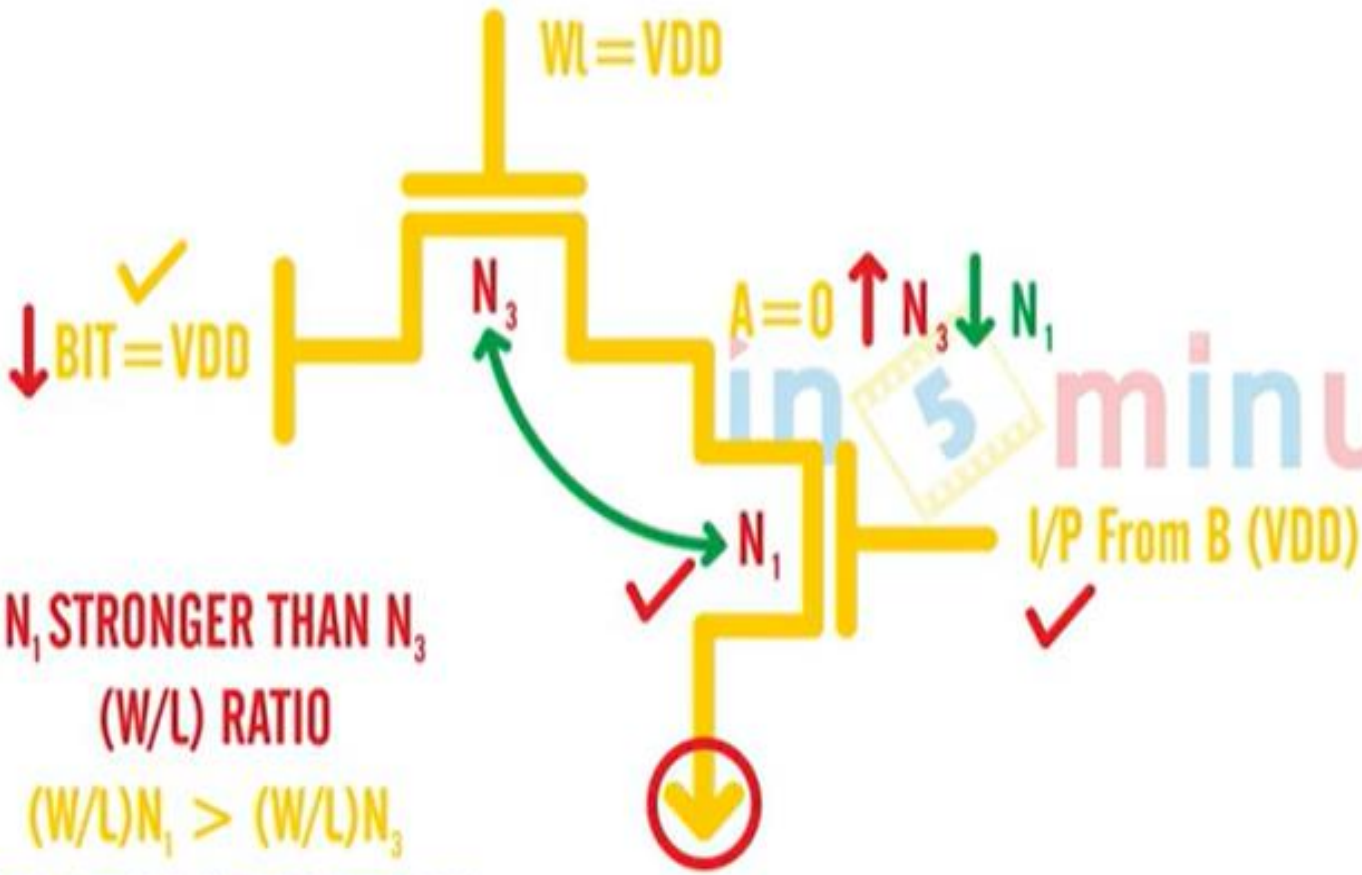
6T SRAM





TILL TIME
BOTH EQUAL!

6T SRAM

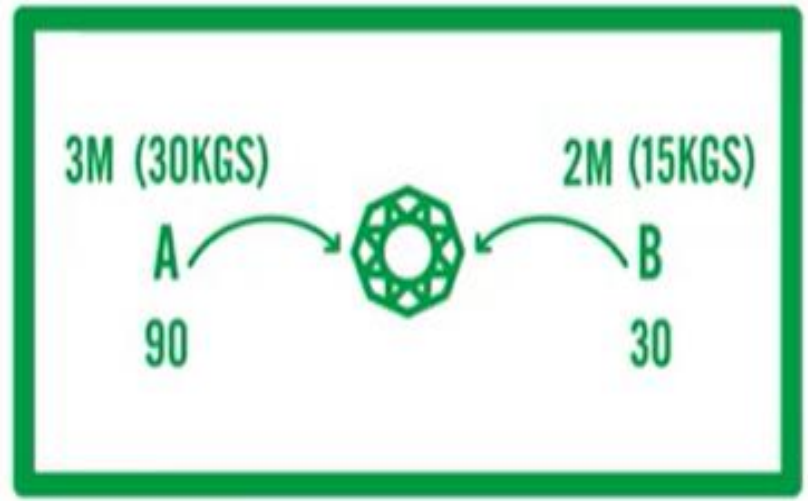


N_1 STRONGER THAN N_3

(W/L) RATIO

$(W/L)N_1 > (W/L)N_3$

(READ STABILITY CRITERIA)



$V = IR$; $I \alpha I/R$ (V CONST)

$ID \alpha (W/L) \alpha I/R$

$(W/L)_{N_1} > (W/L)_{N_3}$

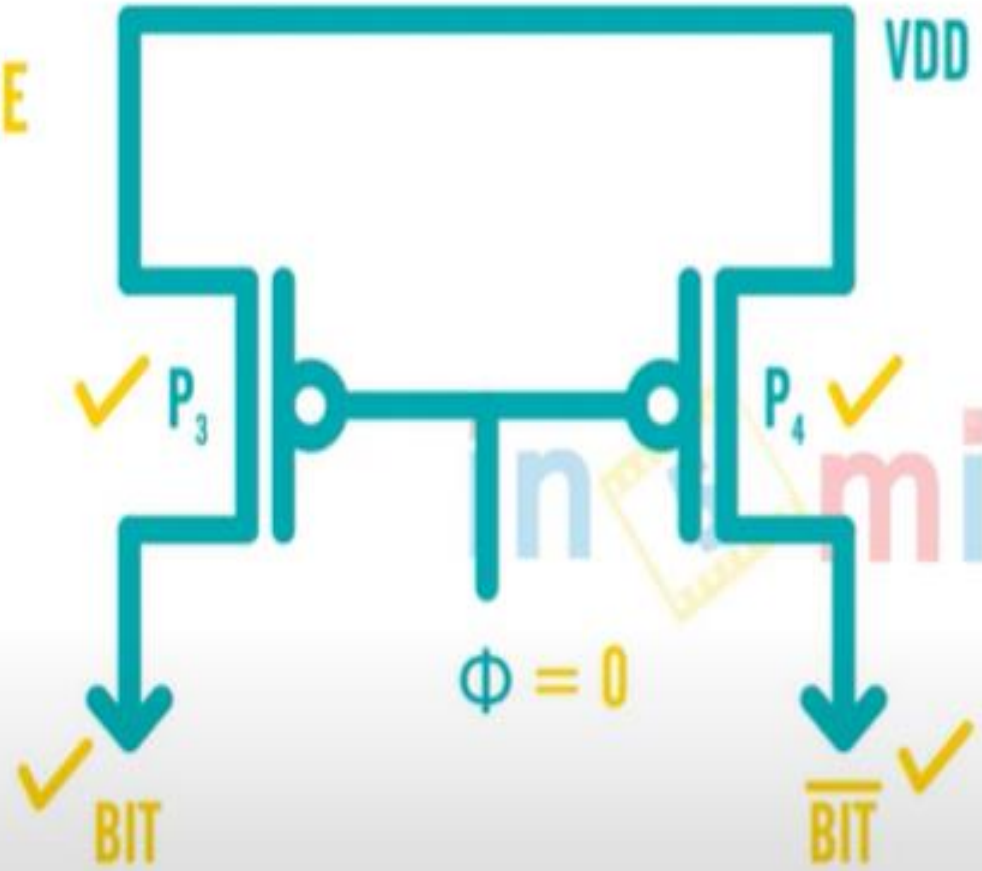
$R_{N_1} < R_{N_3}$

} READ STABILITY CRITERIA

in 5 minutes

6T SRAM

PRE - CHARGE CIRCUIT

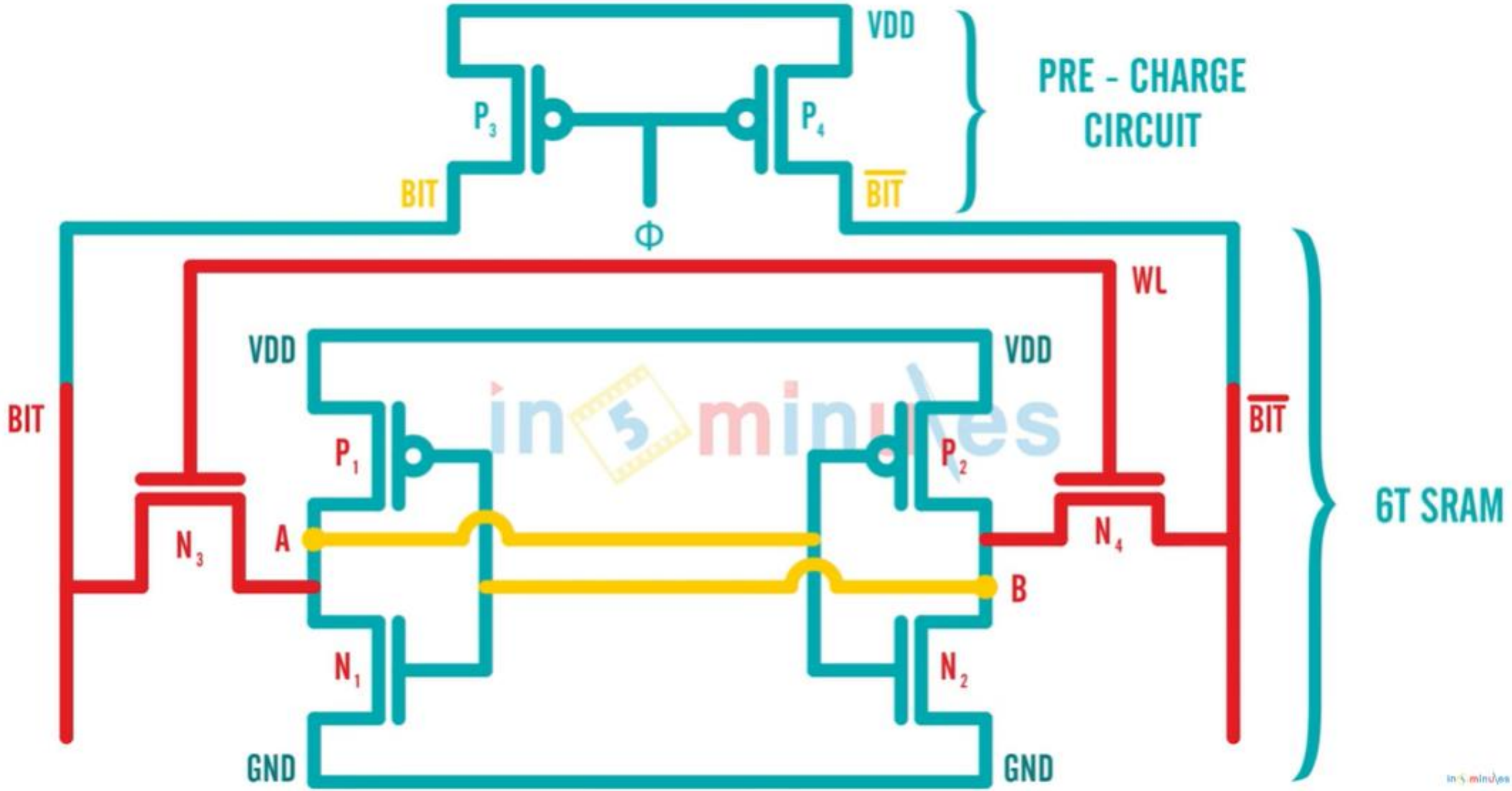


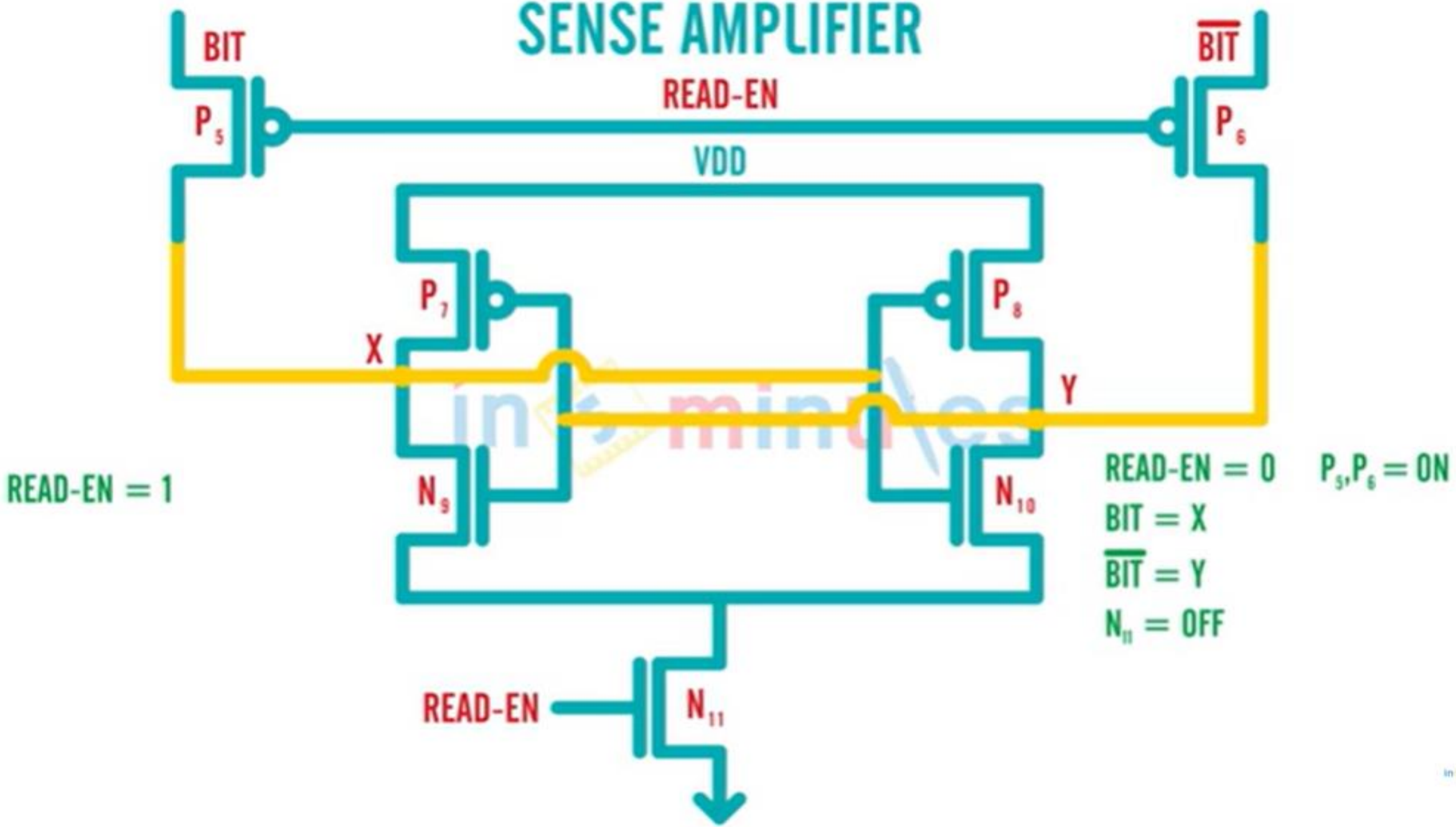
READ OPERATION :

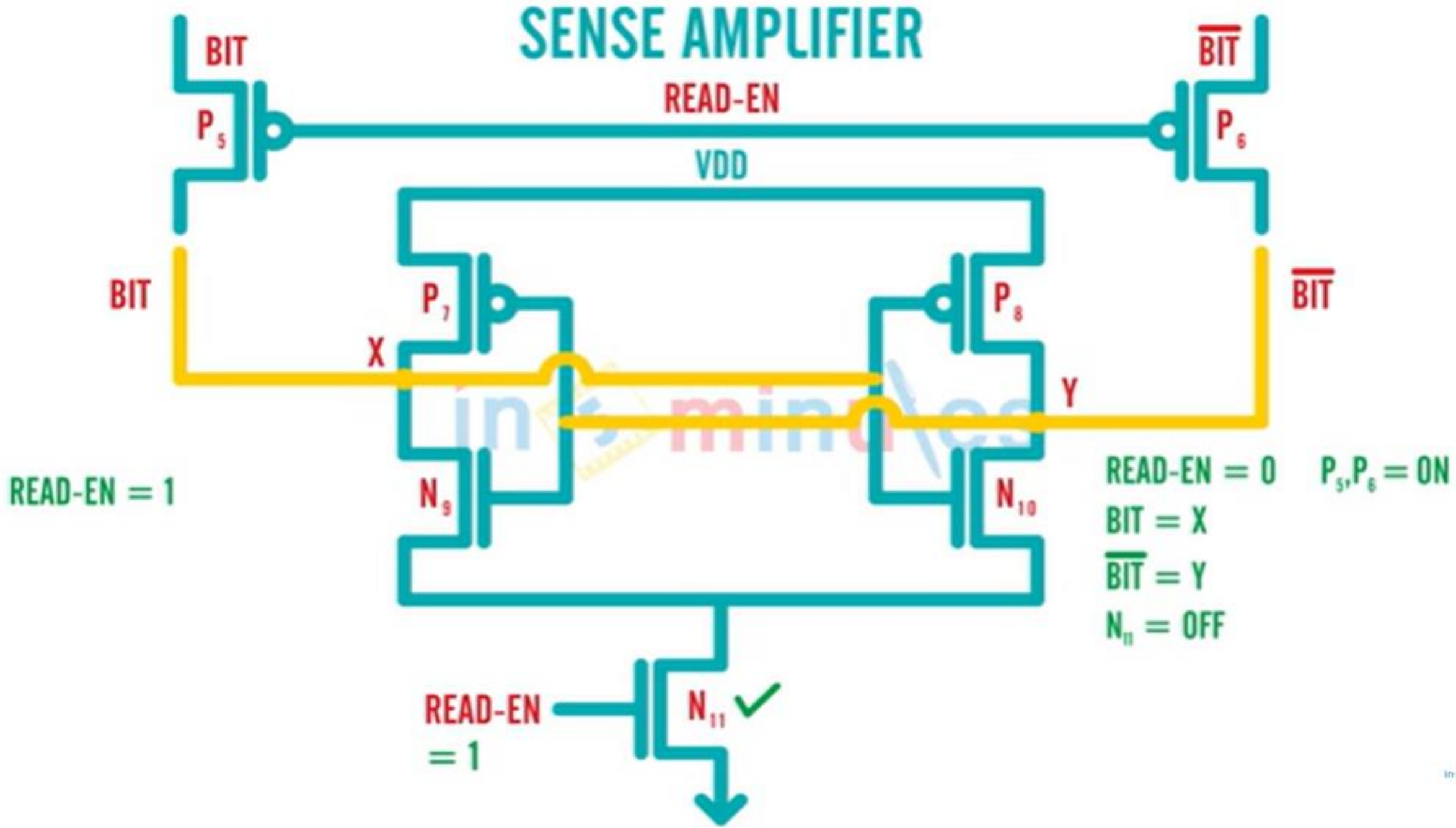
1) WL = VDD
2) BIT, $\overline{BIT}$ = VDD

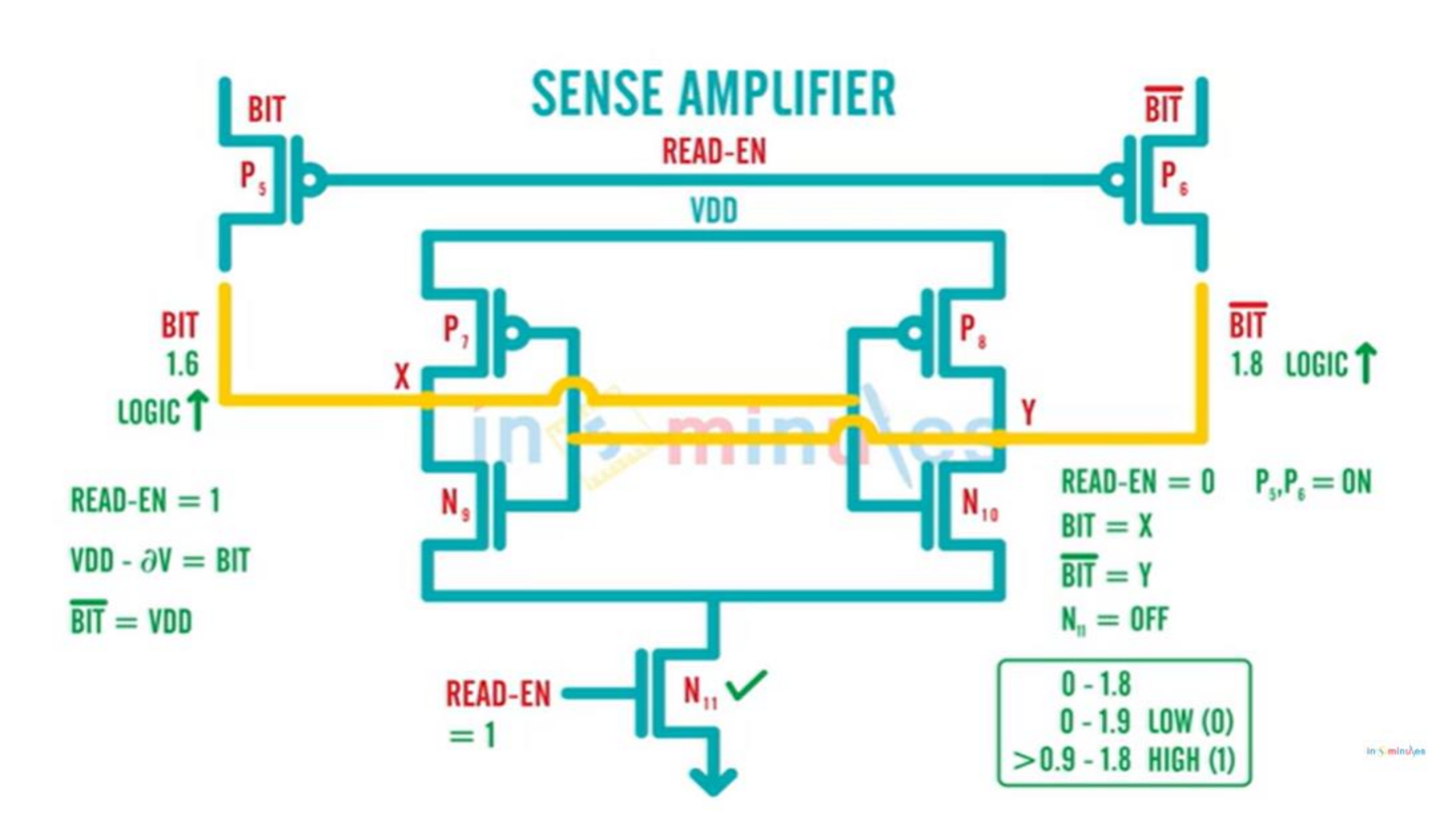
Φ = 0 P_3, P_4 = ON

Φ = 1 P_3, P_4 = OFF

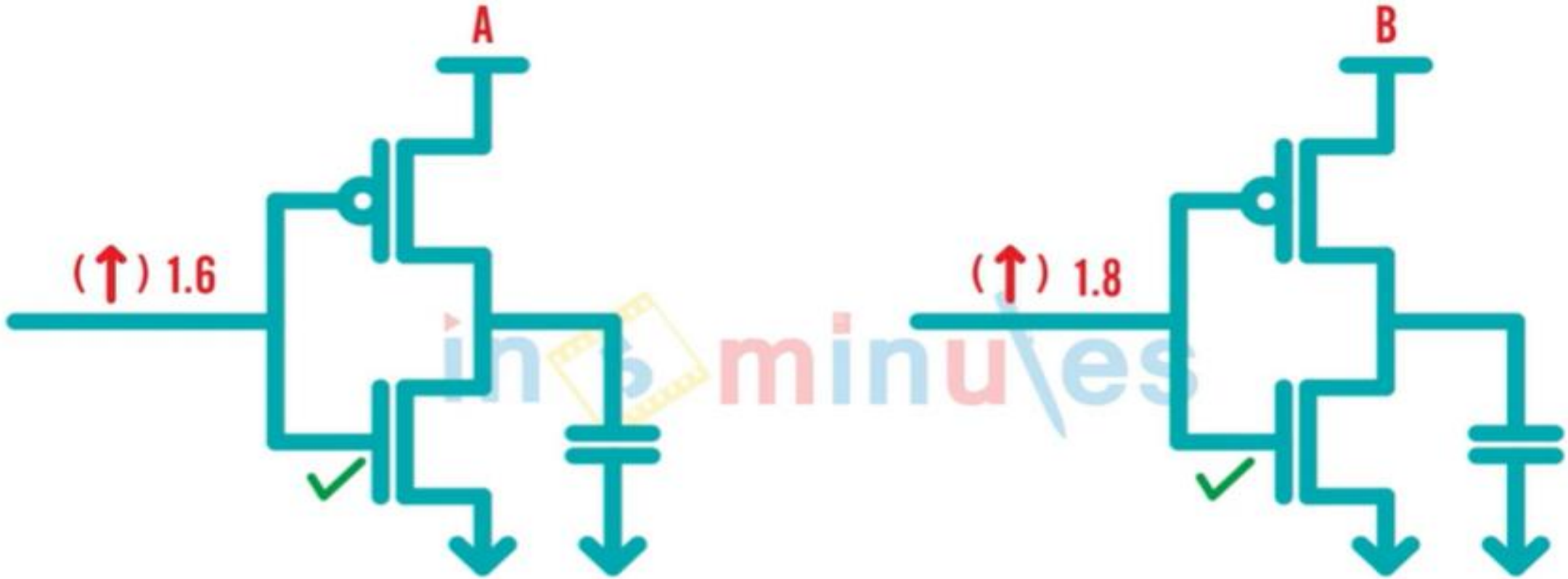

VDD
PRE - CHARGE CIRCUIT
P3
P4
BIT
BIT
Φ
WL
VDD
VDD
BIT
BIT
P1
P2
N3
A
N4
B
N1
N2
GND
GND
6T SRAM


SENSE AMPLIFIER
BIT
$\overline{BIT}$
READ-EN
P_5
P_6
VDD
P_7
P_8
X
Y
N_9
N_{10}
READ-EN = 1
READ-EN = 0
P_5,P_6 = ON
BIT = X
$\overline{BIT}$ = Y
N_{11} = OFF
READ-EN
N_{11}


SENSE AMPLIFIER
BIT
$\overline{BIT}$
READ-EN
P_5
P_6
VDD
BIT
$\overline{BIT}$
P_7
P_8
X
Y
READ-EN = 1
N_9
N_{10}
READ-EN = 0
P_5, P_6 = ON
BIT = X
$\overline{BIT}$ = Y
N_{11} = OFF
READ-EN
= 1
N_{11}


SENSE AMPLIFIER
BIT
$\overline{BIT}$
READ-EN
P_5
P_6
VDD
BIT
1.6
LOGIC
P_7
P_8
X
Y
$\overline{BIT}$
1.8 LOGIC
N_9
N_{10}
READ-EN = 1
VDD - ∂V = BIT
$\overline{BIT}$ = VDD
READ-EN = 0
P_5,P_6 = ON
BIT = X
$\overline{BIT}$ = Y
N_{11} = OFF
READ-EN
= 1
N_{11}
0 - 1.8
0 - 1.9 LOW (0)
>0.9 - 1.8 HIGH (1)

SENSE AMPLIFIER

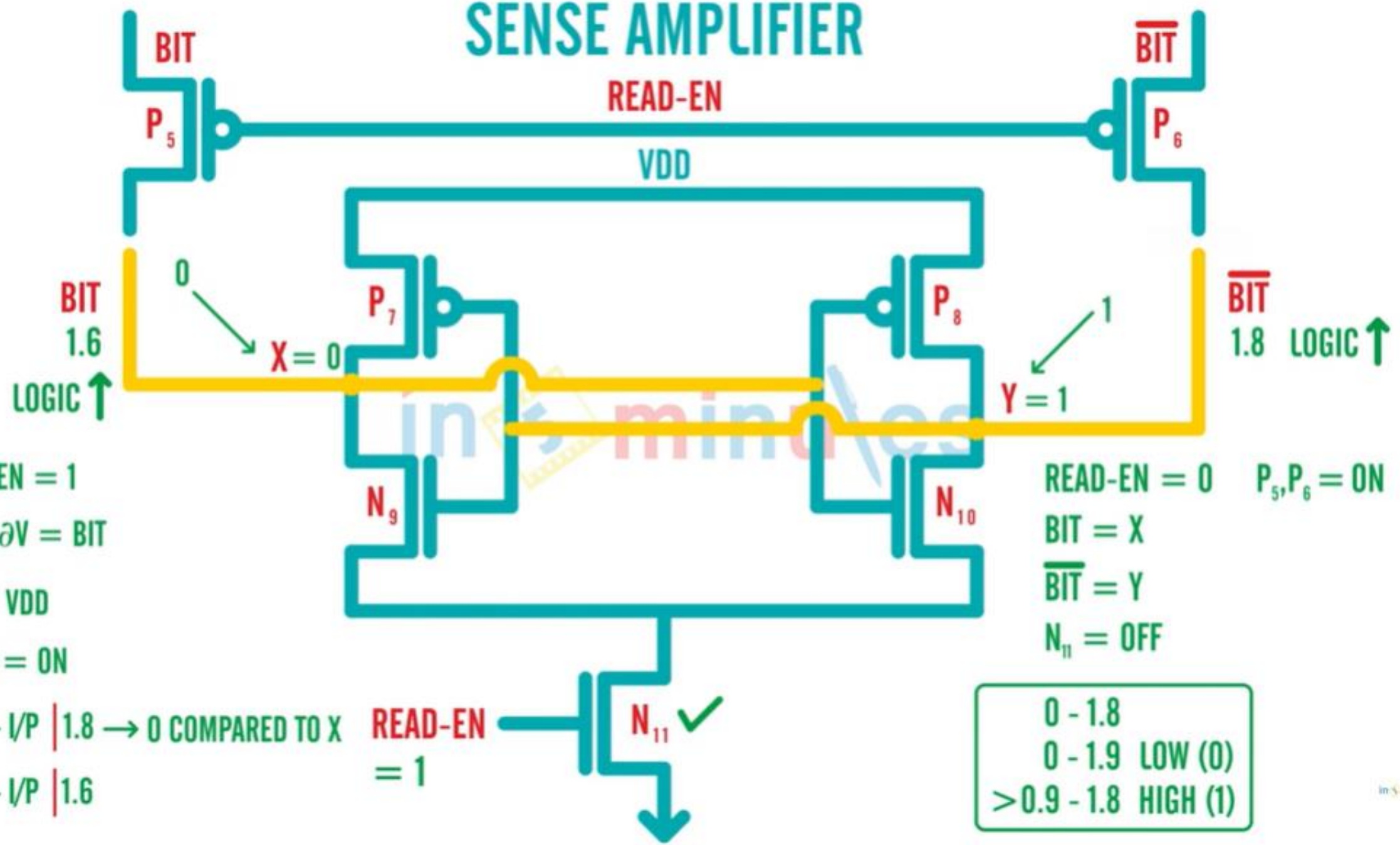


ID, A ? ID, B ?

ID, B > ID, A

ID α VGS
ID α VG

SENSE AMPLIFIER



READ-EN = 1

VDD - ∂V = BIT

$\overline{BIT}$ = VDD

N_9, N_{10} = ON

N_9 : Y - I/P | 1.8 → 0 COMPARED TO X

N_{10} : X - I/P | 1.6

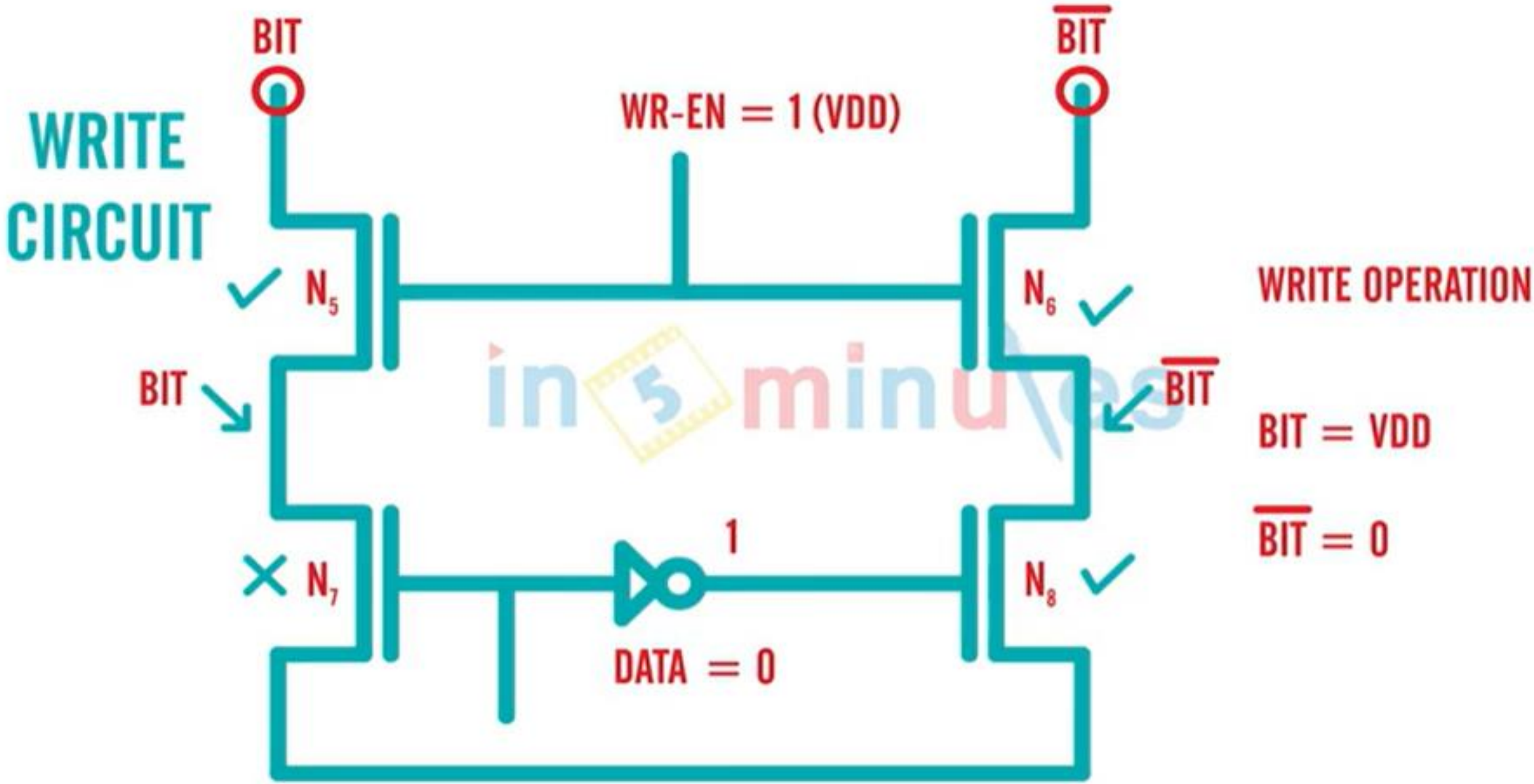
READ-EN = 0 P_5,P_6 = ON

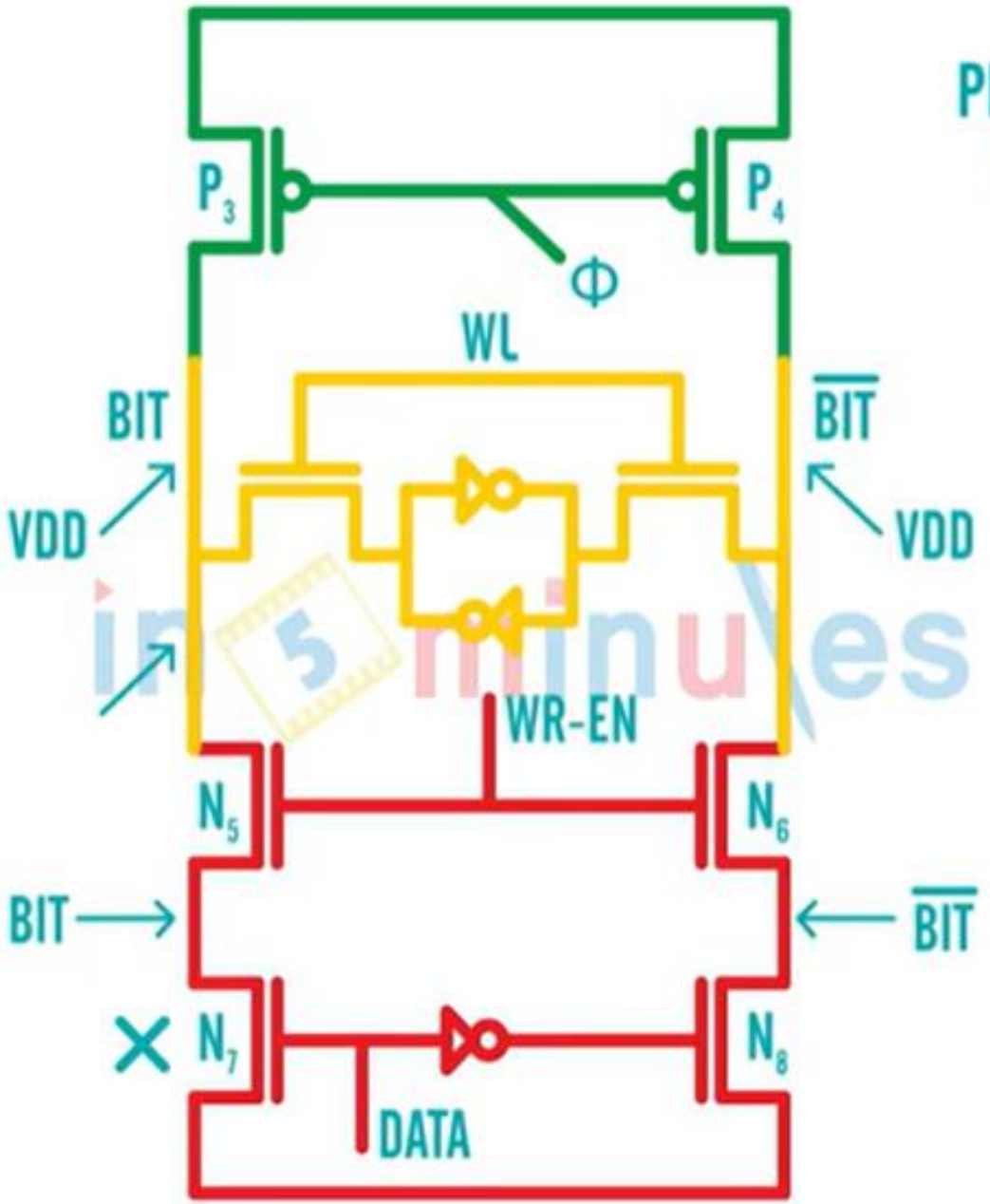
BIT = X

$\overline{BIT}$ = Y

N_{11} = OFF

0 - 1.8	
0 - 1.9	LOW (0)
>0.9 - 1.8	HIGH (1)


WRITE CIRCUIT
BIT
$\overline{BIT}$
WR-EN = 1 (VDD)
N_5
N_6
BIT
$\overline{BIT}$
N_7
1
N_8
DATA = 0
WRITE OPERATION
BIT = VDD
$\overline{BIT}$ = 0



PRE CHARGE CIRCUIT

READ OPERATION :

BIT, $\overline{BIT}$ = VDD

Φ = 0, (P_3, P_4)

WRITE OPERATION

WR-EN = 1

(N_5, N_6) = ON

DATA = 0

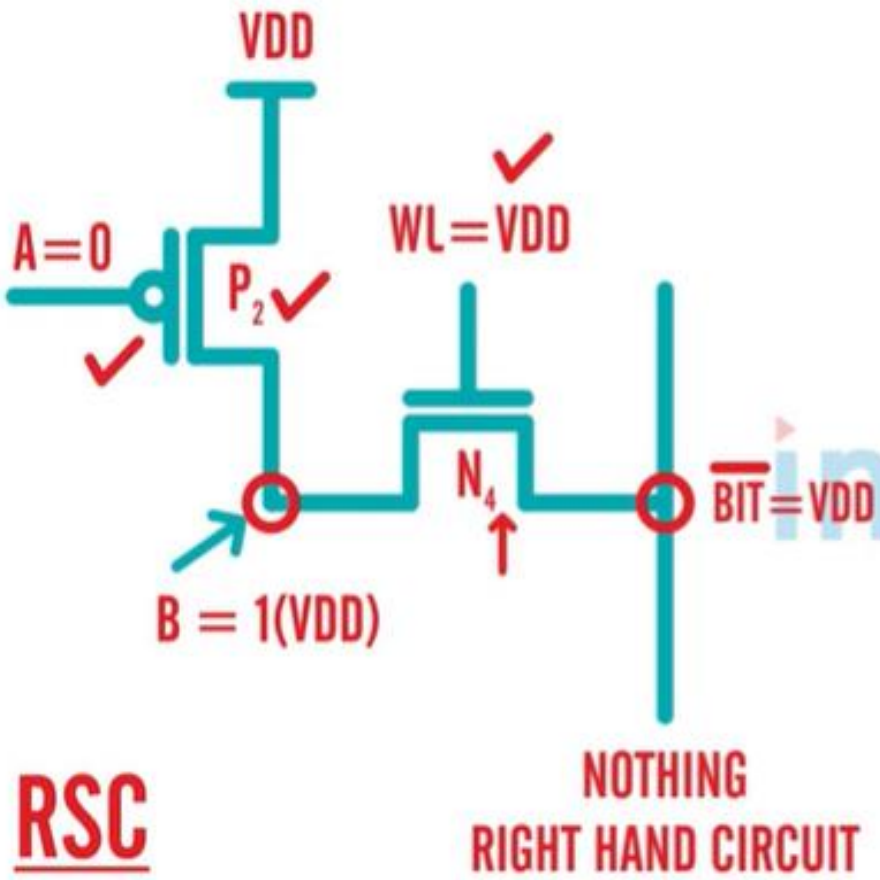
N_7 = OFF

N_8 = ON

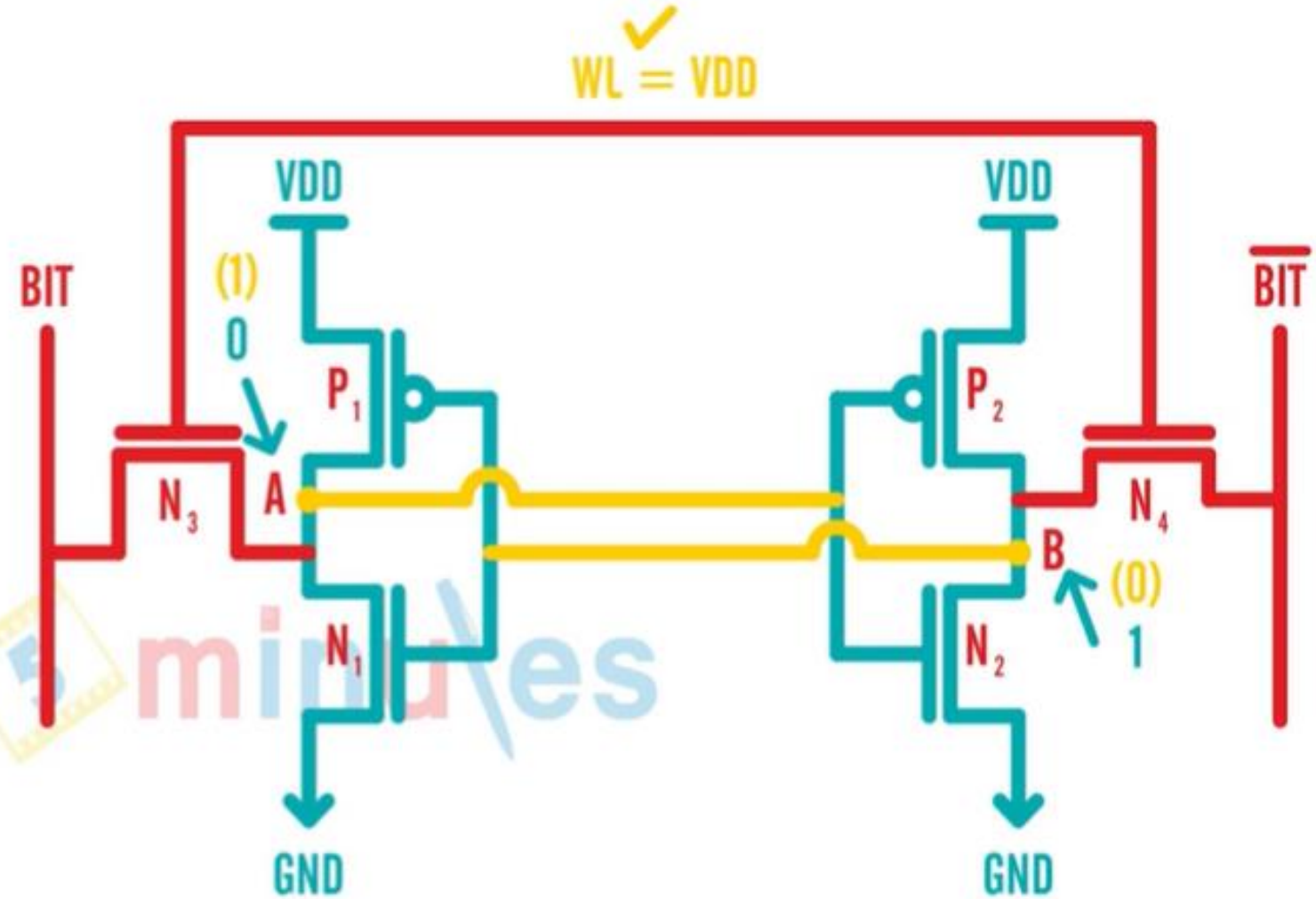
BIT = VDD

$\overline{BIT}$ = 0

in 5 minutes



RSC



WRITE :

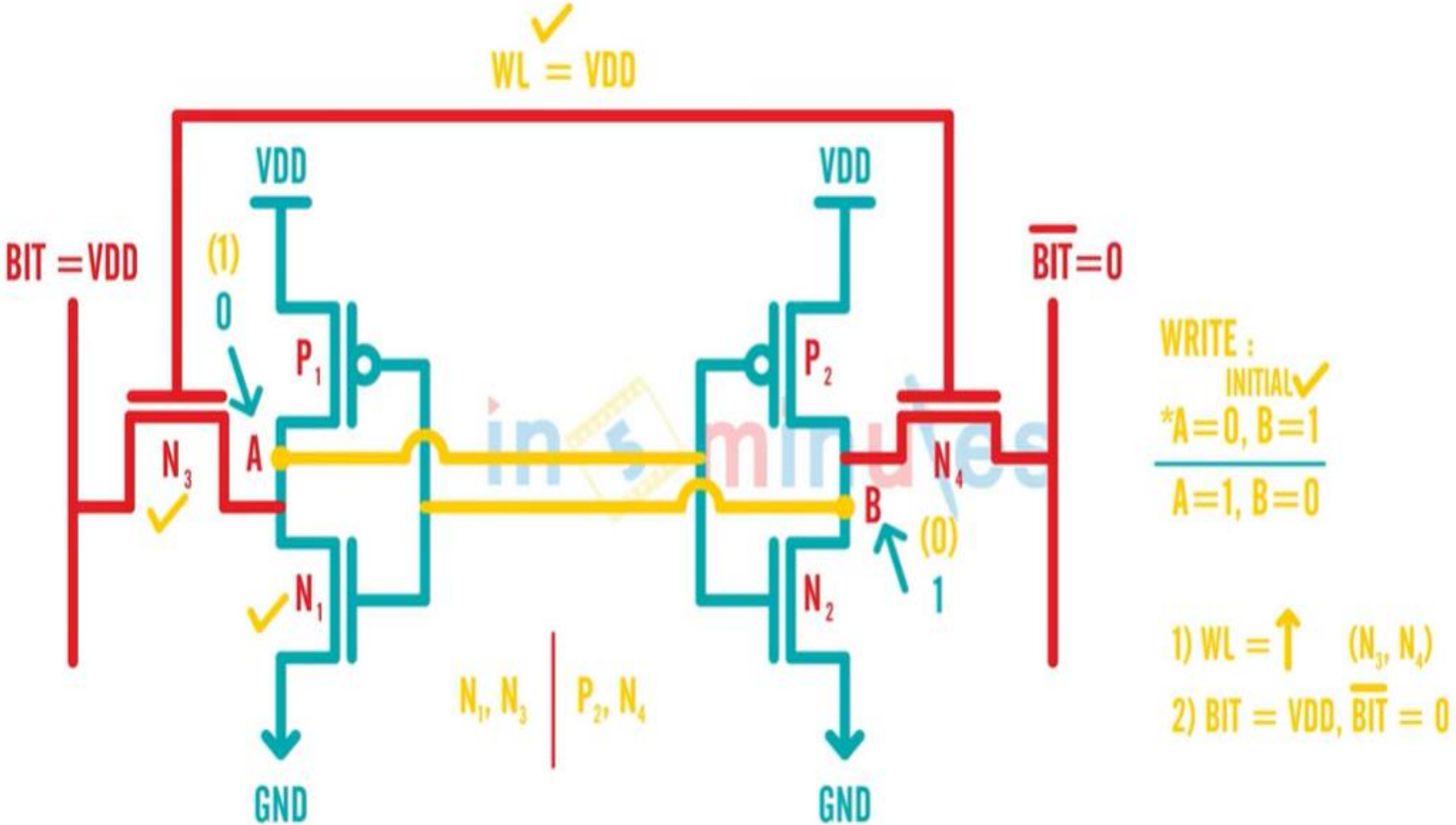
INITIAL

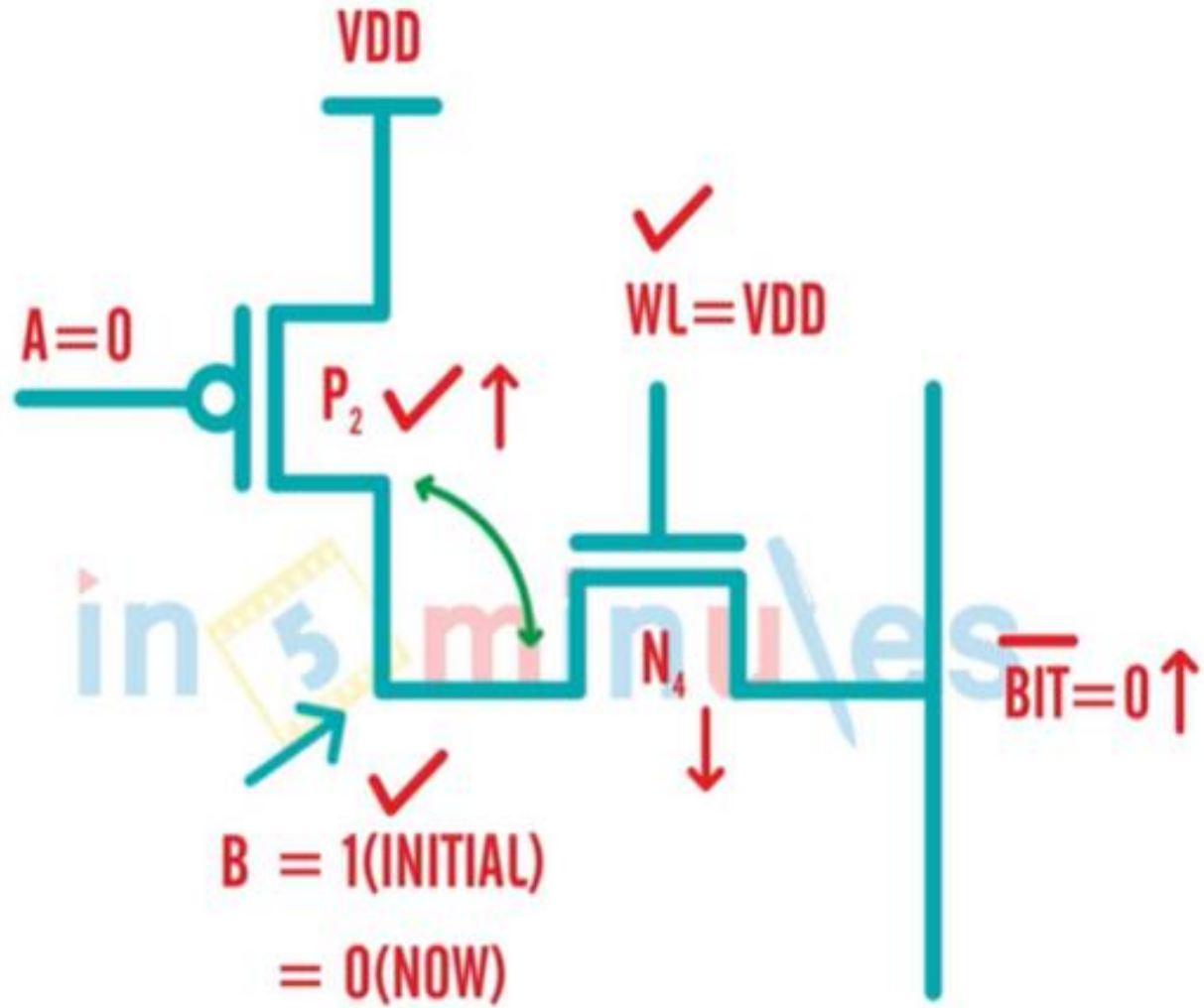
*A=0, B=1

A=1, B=0

1) WL = ↑ (N_3, N_4)

2) BIT = VDD, $\overline{BIT}$ = 0


WL = VDD
VDD
VDD
BIT = VDD
$\overline{BIT}$ = 0
(1)
0
P_1
P_2
N_3
A
N_4
B
(0)
1
N_1
N_2
N_1, N_3 | P_2, N_4
GND
GND
WRITE :
INITIAL
*A = 0, B = 1
A = 1, B = 0
1) WL = ↑ (N_3, N_4)
2) BIT = VDD, $\overline{BIT}$ = 0



$(W/L)N_4 > (W/L)P_2$

$RN_4 < RP_2$

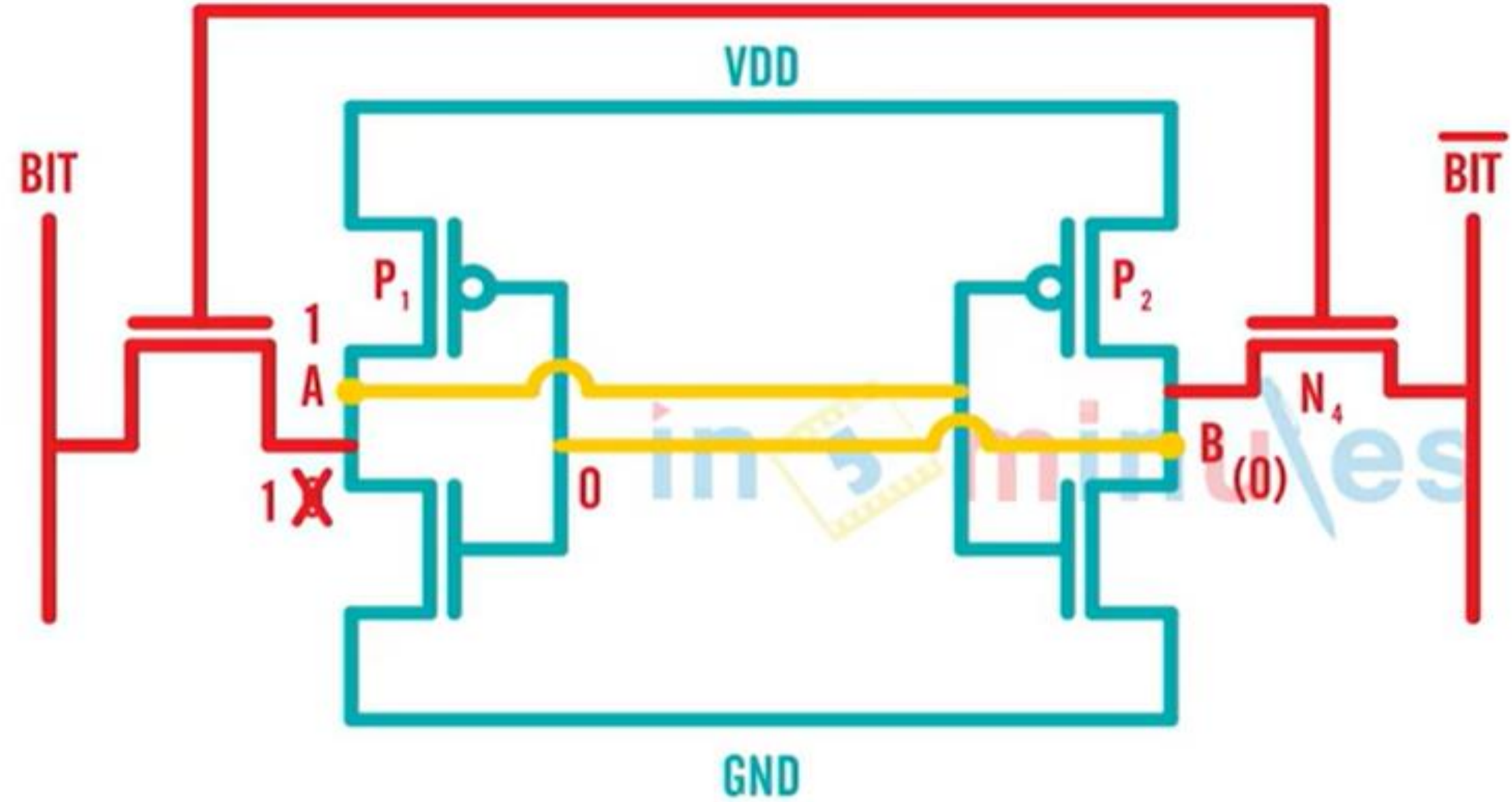
$N_4 \downarrow$

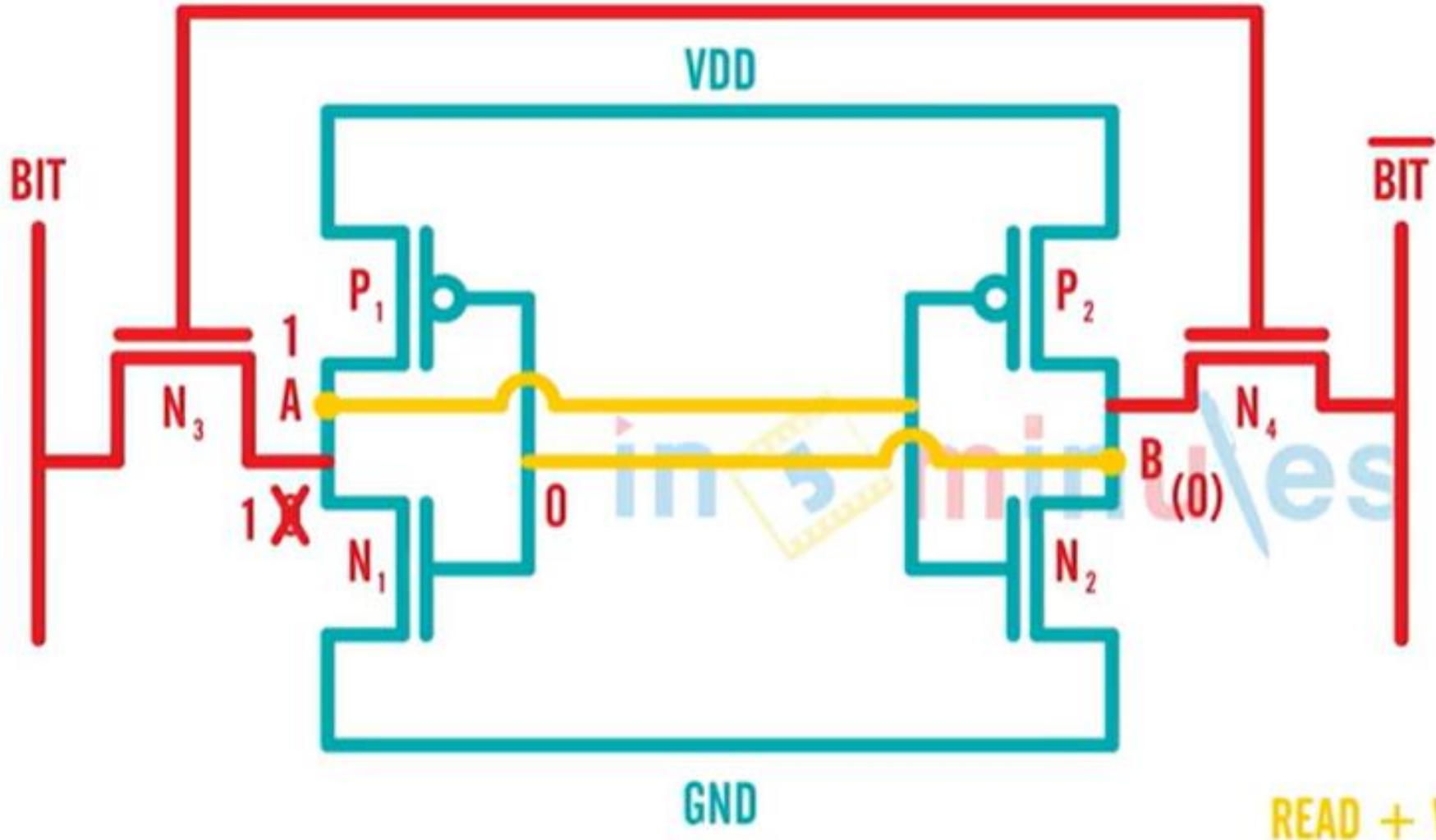
$P_2 \uparrow$

(NODE B)

N_4 WINS

0 @ NODE B


VDD
BIT
$\overline{BIT}$
P_1
P_2
1
A
1
0
B
(0)
N_4
GND



N3, N4 CALLED
PASS / ACCESS TRANSISTOR

READ + WRITE STABILITY

$(W/L)_{NMOS} > (W/L)_{PASS/ACCESS} > (W/L)_{PMOS}$

N1/N2 (N3/N4)