Name :

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test I – Jan 2023

Programme	:	B.Tech (ECM)	Semester	:	Winter 2022-2023
Course Title	:	Signal Processing	Code	:	BECM301L
			Class Nbr(s)	:	CH2022235002336
Faculty(s)	:	Dr.Suchetha M	Slot	:	F1+TF1
Time	:	90 Minutes	Max. Marks	:	50

Answer all the Questions

Q.No.	Question Description	Marks
1.	Determine the following signals are energy or power signals i) $x[n] = (1/8)^n u[n]$ ii) $x[n] = \sin(2\pi n/3)$	[5]
2	Give the graphical representation of the following signals i) $x[n] = 3\,u[n-6] + \frac{1}{2}\,u[-n]$ ii) Plot first 5 samples of the following $x[n] = (0.2)^n\,u[n-1]$	[5]
3.	Determine whether the system $y[n]=x[4n+1]+3$ is memory less, causal, linear, time invariant and stable.	[10]
4.	Determine the response of the LTI system whose input $x(n)$ and impulse response $h(n)$ are given by $x(n) = \{1, \underset{\uparrow}{3}, 5, -1, -2\}, h(n) = \{1, \underset{\uparrow}{4}, 1, -2, 1\}$ using graphical method.	[10]
5.	A causal system is represented by the following difference equation $y(n) + \frac{1}{4}y(n-1) = x(n) + \frac{1}{2}x(n-1)$ (a) Find H(z) and give the corresponding ROC. (b) Is the system stable? (c) Find unit impulse response.	[10]
6.	Using the properties of z-transform, Determine X(z) (a) $x(n)=na^n u(n)$ (b) $x(n)= 2^n\,u(n-2)$	[10]

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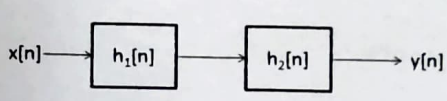
Continuous Assessment Test II – March 2023

Programme	:	B.Tech (ECM)	Semester	:	WS 2022-23
Course	:	Signal Processing	Code	:	BECM301L
			Class Nbr	:	CH2022235002336
Faculty	:	Dr. Suchetha M	Slot	:	F1+TF1
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		Find the DTFT and plot the magnitude and phase spectrum of the following (i) $x(n)= (0.2)^n u(n-1)$ (ii) $x(n)= (0.3)^{n+1} u(n)$	[10]
2.		The system is depicted by cascade interconnection of LTI systems shown below.  The impulse responses are given as $h1[n] = \delta[n] - 2\delta[n-1] + 3\delta[n-2]$ and $h2[n] = r[n] - r[n-2] - 2u[n-2]$ Compute Linear convolution using circular convolution to find output, when input is $x[n] = u[n] - u[n-2]$.	[10]
3.		When the input sequence in the natural order and the output of the DFT sequence is in the bit reversed order, identify the method to find the DFT of the given sequence $x(n) = \{2, 0, 2, 1, 2, 2, 2, 3\}$.	[10]
4.		Use a **monotonic analog filter and bilinear transformation to design a digital filter** that passes a high frequency of 1000Hz and above from an audio signal of sampling frequency 20KHz with a stopband cut-off frequency of 500Hz at 20dB attenuation. The allowed passband ripple is 3dB.	[10]
5.		An analog filter, with ripples in passband and monotonic in stopband, has the following specifications: α_p=3dB, α_s=16dB, f_p=1kHz, f_s=2kHz. Find the filter order N and poles of transfer function, S_k	[10]

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Reg. No. : 21BLC1160

Final Assessment Test (FAT) - APRIL/MAY 2023

Programme	B.Tech	Semester	Winter Semester 2022-23
Course Title	SIGNAL PROCESSING	Course Code	BECM301L
Faculty Name	Prof. Suchetha M	Slot	F1+TF1
		Class Nbr	CH2022235002336
Time	3 Hours	Max. Marks	100

Section A (3 X 5 Marks)
Answer All questions

01. Check whether the described system follows linearity, Causality, time-invariance, memoryless, and stability [5]

$$y[n] = \begin{cases} x[n-1], & n > 0 \\ 0, & n = 0 \\ x[2n+1], & n < 0 \end{cases}$$

02. If X (K) is computed using DFT for 8 point, what would be the computational complexity in terms of additions and multiplications. Compare with 8 point FFT computations. [5]

03. Convert H(s) to H (z) using Bilinear transformation for T= 1 second. [5]

$$H(s) = \frac{4s}{(s+0.5)(s+4)}$$

Section B (4 X 10 Marks)
Answer All questions

04. Determine the fundamental period of the following discrete time signal if periodic. [10]

$$x[n] = 2\sin(3\pi n) + 3\cos(5\pi n) + 5\sin(2\pi n)$$

Compute the energy and power of the above signal.

05. Find X(k) using 8 –point Decimation in Time for [10]

x(n)={0, 1, 2, 3, 4, 5, 6, 7}

06. Design a Butterworth IIR lowpass filter that satisfies the following specifications. [10]

Passband ripple ≤ 4.436 dB

Stopband attenuation ≥ 20 dB

Passband edge frequency = 0.35 π rad/sample

Stopband edge frequency ≒ 0.7 π rad/sample.

07. Define Very Large Instruction Word (VLIW). Draw and explain the VLIW Architecture in detail. [10]

SECTION C (3 X 15 Marks)
Answer All questions

08. A causal LTI system is described by difference equation [15]

$$6y[n] = -11y[n-1] - 3y[n-2] + 6x[n-1]$$

i) Find Transfer function, H (z). Plot poles and zeros of H (z) and indicate ROC. Further comment on stability.

ii) Find unit impulse response of the system.

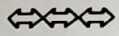
09. The desired frequency response of a low-pass filter is [15]

$$H_d(e^{j\omega}) = e^{-j3\omega}, \quad -\pi/4 \le \omega \le \pi/4 \quad \text{and}$$
$$H_d(e^{j\omega}) = 0, \quad \pi/4 < |\omega| \le \pi$$

Determine the filter coefficients using a Hanning window with window length, 7. Obtain the frequency response of the resultant filter.

10. Realize the system given by difference equation in Direct form –II and Parallel form. [15]

$$y(n) = -0.1\, y(n-1) + 0.72\, y(n-2) + 0.7\, x(n) - 0.252\, x(n-2)$$



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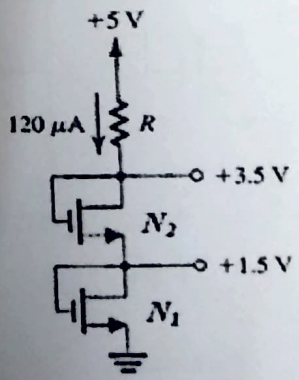
Continuous Assessment Test I – January 2023

Programme	: B. Tech (ECM)	Semester	:	WS 2022-23
Course	: VLSI System Design	Code	:	BECE303L
		Class Nbr	:	CH2022235001205 CH2022235001207 CH2022235001212 CH2022235001213
Faculty	: Dr Ananiah Durai S, Dr Lakshmi Priya G, Dr Ravi Sankar A, Dr Sakthivel. S M	Slot	:	B1+TB1
Time	: 90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		A VLSI design engineer develops a graphical processing unit for multimedia applications. For the above application, discuss the impact of different VLSI design styles on the cycle time and the achievable performance metrics. Also, briefly elaborate on the list of steps involved in the VLSI design flow for the above design.	10
2.		The circuit in Figure 1 shows NMOS transistors with a threshold voltage of 1 V, $\mu_n C_{ox}$ = 120μA/V², λ = 0, and lengths of 1 μm each. Find the device width and the respective value of R for both N_1 and N_2 to obtain the voltage and current values indicated.  **Figure 1**	10
3.		(i) Sketch the MOS capacitance (C_G) variation if the gate voltage (V_G) is ramped slowly, from accumulation condition to depletion and then to inversion. Also, discuss with relevant capacitances expression on the dependency of C_G variation with semiconductor capacitance (C_S) for accumulation, depletion, and inversion conditions. **(5 marks)**	10

(ii) How does the velocity saturation limit I_{DSat}? For a very short channel length, discuss the I_{Dsat} dependency parameters. **(5 marks)**

4. (i) With a neat circuit diagram, describe the voltage transfer characteristics (VTC) of a CMOS inverter. Mark the different regions in the VTC and comment on the operating mode (i.e., linear or saturation) of NMOS and PMOS transistors. **(3 marks)**

(ii) Write the drain current expressions of transistors in regions 2, 3, and 4 of the VTC in terms of V_{IN}, V_{DD} and V_{OUT}. **(3 marks)** **10**

(iii) Derive the expression for V_{IT}, i.e., input transition voltage, also called switching threshold. If the NMOS width is increased four times for the fixed PMOS width, what will happen to the Input Transition Voltage (V_{IT}) of the inverter? Assume the threshold voltage of both transistors is the same. **(4 Marks)**

5. Implement the following logic functions using static CMOS logic style;

i) $f = \overline{[B.(A+C)] + (D.E)}$

ii) $f = \overline{R + S + (T.U)}$ **10**

Size the transistors for the worst-case delay of RC of an inverter with a load capacitance of C. Assume $\mu_N = 3\ \mu_P$ for the first logic function and $\mu_N = 2.5\ \mu_P$ for the second logic function.

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Continuous Assessment Test II – March 2023

Programme	:	B. Tech. (ECM)	Semester	:	WS 2022-23
Course	:	VLSI System Design	Code	:	BECE303L
			Class Nbr	:	CH2022235001205 CH2022235001207 CH2022235001213 CH2022235001212
Faculty	:	Dr Ananiah Durai S, Dr Lakshmi Priya G, Dr Ravi Sankar A, Dr Sakthivel. S M	Slot	:	B1+TB1
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		For the circuit shown in **Fig. 1**, determine whether the transistors in the figure are "ON" or "OFF" for different states. (complete Table 1 by filling in the states). Evaluate the output voltage and hence identify the circuit.	5

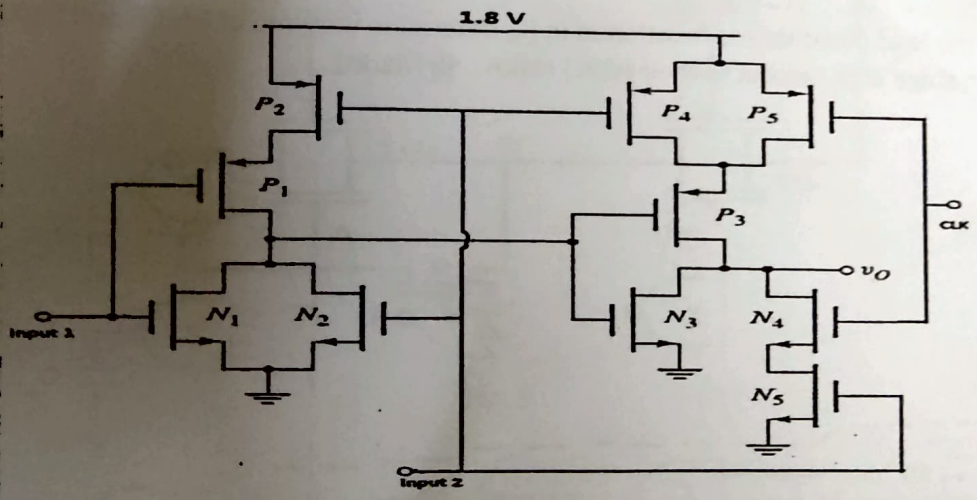

Fig. 1

Table 1

CLK	Input 1	Input 2	N_1	N_2	N_3	N_4	N_5	Vo
1	0	0						
1	0	1						
1	1	0						
1	1	1						

2. With neat cross-sectional sketches, explain the fabrication process flow of Fig. 2 shown below. Draw all the photomasks assuming, 7

Positive photoresist if your register number (consider the last four digits of, say, 21BEC1001) is odd and

Negative photoresist if your register number (consider the last four digits of, say, 21BEC1004) is even.

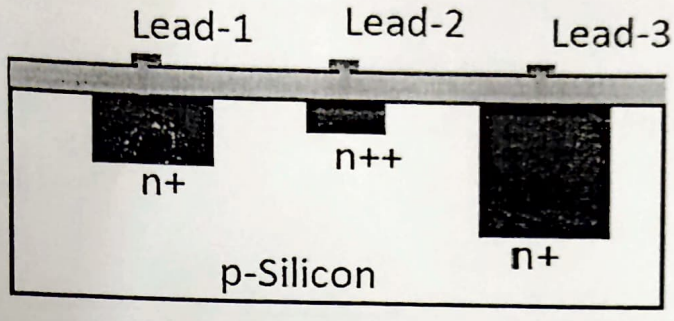

Fig. 2

3. Implement the following Boolean logic function using static CMOS logic style and draw its optimized stick diagram using Euler graph 8

$$F = \overline{(D+E)A+BC}$$

4. (i) Estimate the minimum delay of the path from A to B for the circuit shown in Fig. 3 and size the gates (X, Y, Z) to achieve this delay with two different load capacitors; (a) C_L = 70 (b) C_L = 100. **(10 Marks)** 15

(ii) For the load capacitances mentioned in (i), determine the ratio of NMOS and PMOS in each stage with respect to their (W/L) ratios. **(5 Marks)**

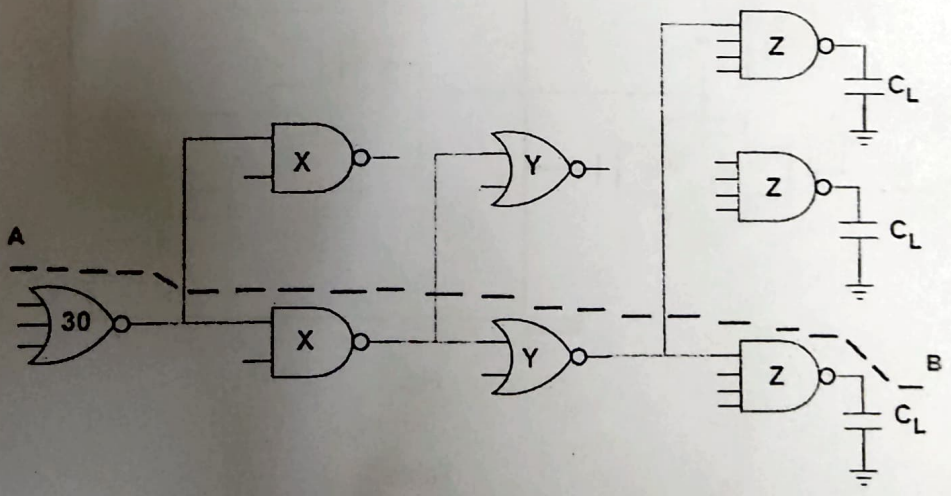

Fig. 3

5. a Evaluate the voltages at all the nodes of the pass-transistor circuit shown in **Fig. 4.** Assume that the threshold voltage of all the transistors is 0.65 V. Ignore the body effect. Please note that the gate terminals of a few transistors in the second and third rows are biased with different voltages. 4

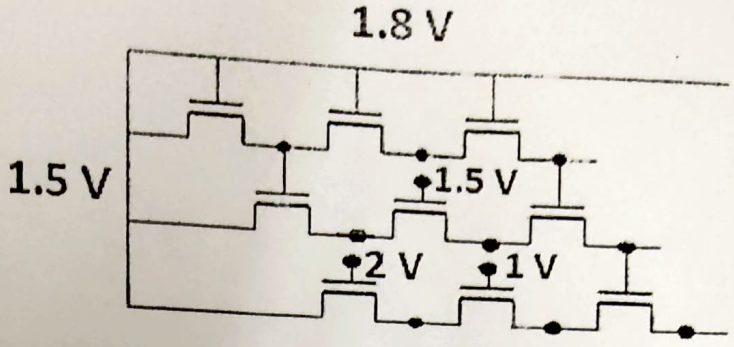

Fig. 4

The circuit shown in Fig. 5 is realized using transmission gates and pass transistors. Construct a truth table with the input variables A, B, and C and identify the function implemented by X. Assume that the complementary signals of variables A and C are readily available.

b

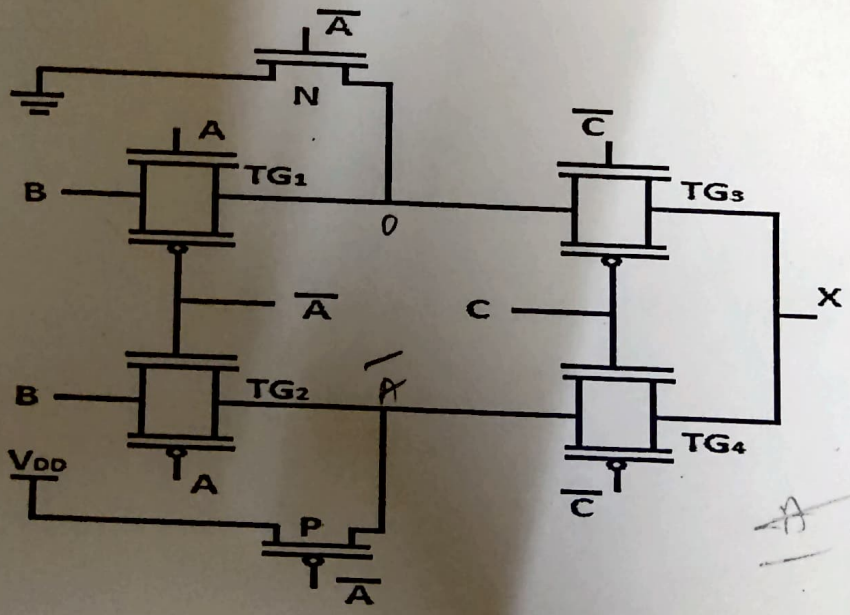

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Fig. 5

c One of the major problems of static CMOS logic is the number of transistors required to implement a logic function. It is known that pseudo-NMOS logic addresses this particular issue of static CMOS logic. Instead of **pseudo-NMOS,** can you implement the following logic function using the **pseudo-PMOS** logic style? 4

$$Out = A(B + C) + DE$$

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Reg. No. : 21BLC1160

Final Assessment Test (FAT) - APRIL/MAY 2023

Programme	B.Tech	Semester	Winter Semester 2022-23
Course Title	VLSI SYSTEM DESIGN	Course Code	BECE303L
Faculty Name	Prof. G Lakshmi Priya	Slot	B1+TB1
		Class Nbr	CH2022235001212
Time	3 Hours	Max. Marks	100

Section A (9 X 10 Marks)
Answer All questions

01. a) Derive an expression for the drain current of an N-channel enhancement type MOSFET from the first principles. Draw the transfer and output I-V characteristics of the transistor. **(7 Marks)** [10]
b) From the drain current expression at the saturation region, comment on how to increase the current for a fixed gate-to-source voltage. **(3 Marks)**

02. Consider the NMOS transistor in a 0.65 µm process with W/L = 1.95/0.65. In this process, the gate oxide thickness is 11 nm, and the mobility of electrons is 350 cm^2/V.s. The threshold voltage is 0.75 V. Plot I_{ds} vs. V_{ds} for V_{gs} = 0, 1, 2, 3, 4, and 5 V. Assume five different V_{ds} values to get smooth I_{ds}. [10]

03. A positive edge-triggered register on a Master-Slave configuration is shown in Figure 1. Implement the same using transmission gates. Briefly explain how the 'clock load per transistor' can be reduced using a modified diagram **(7+3 Marks)** [10]

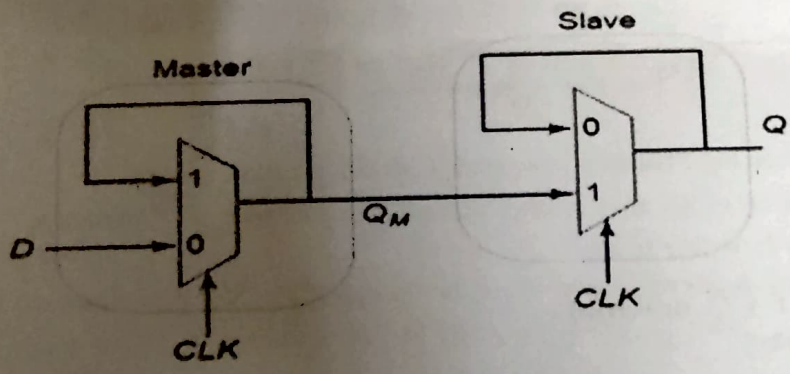

Figure 1

04. An NMOS inverter with a saturated load is shown in Figure 2. Draw the cross-sectional diagram of the same. With neat sketches, explain the fabrication process flow of the device using a self-aligned poly-gate process. We know that a typical fabrication of a CMOS inverter requires 6 photo masks. How many masks will be required to realize this inverter? Assume either positive or negative tone photo-resist. Does the inverter fabrication require a 'p-well,' ' n-well,' or 'twin-well' process? Comment on the same. **Note: You may ignore the bulk diffusion and consider only 3-terminals for FETs.** [10]

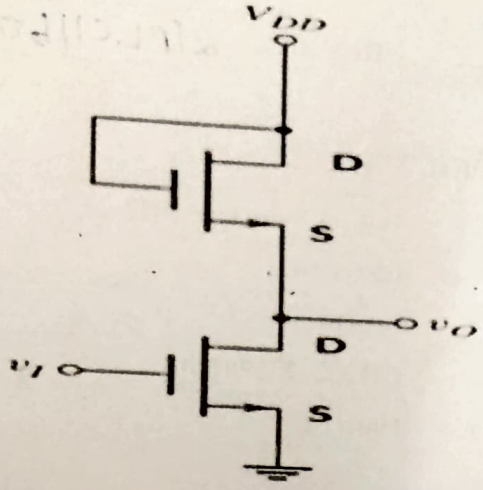

Figure 2

05. Estimate the minimum delay of the path from A to B in Figure.3 and the transistor sizes (X, Y) to achieve this delay. Also, determine the ratio of NMOS and PMOS in each stage with respect to their (W/L) ratios. [10]

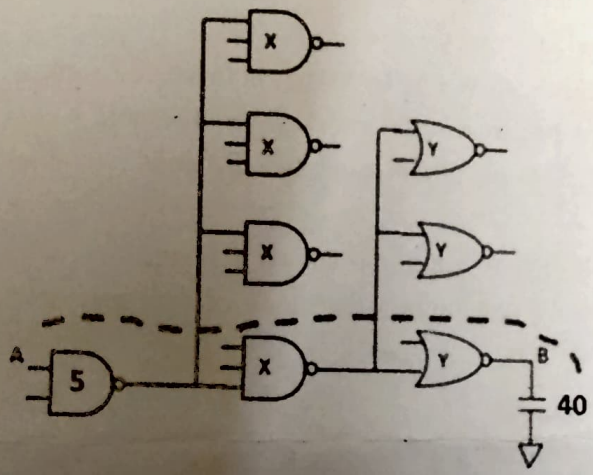

Figure 3

06. Implement the following Boolean logic function using static CMOS logic style, and size the transistors for the worst-case delay of RC of an inverter with a load capacitance of C. Assume $\mu_n = 3\mu_P$ for F_1 & $\mu_n = 4\mu_P$ for F_2 during the sizing. [10]

(i) $F_1 = \overline{A(B+C) + D(E+F)}$ **(6 Marks)**

(ii) $F_2 = \overline{XY+Z}$ **(4 Marks)**

07. Compare the implementation of the following functions with Pseudo NMOS and domino logic, and determine the performances of the two in terms of power and delay. Also, comment on the transistor numbers. [10]

(i) $F_1 = \overline{(A+C).D(B+E)}$ **(5 Marks)**

(ii) $F_2 = \overline{(ABCD)+E}$ **(5 Marks)**

08. a) For the given circuit in Figure 4, calculate the timing for all the paths and then identify the path which violates the timing requirement based on the required arrival time. **(5 Marks)** [10]

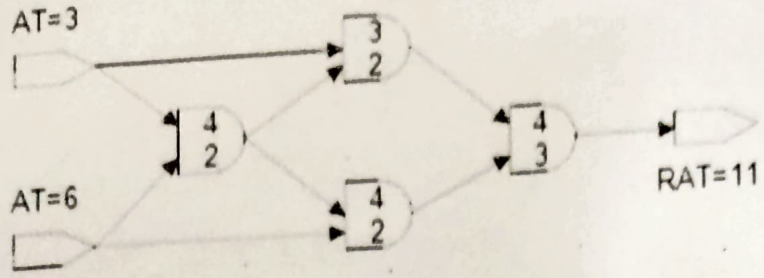

Figure 4

b) With a neat sketch of the waveform, elaborate the Setup Time & Hold time calculation for an RTL circuit with launch & Capture Flops. **(5 Marks)**

09. With neat sketches, explain how "read" and "write" operations are carried out in a CMOS 6T-SRAM cell. Write the conditions on sizing for proper "read" and "write" operations considering the 300 nm technology node. **[10]**

Section B (2 X 5 Marks)

Answer All questions

10. The circuit shown in Figure 5 is realized using Differential Cascode Voltage Switch Logic (DCVSL). Construct a truth table with the input variables A, B, C, and D and identify the function implemented by F and $\bar{F}$. **[5]**

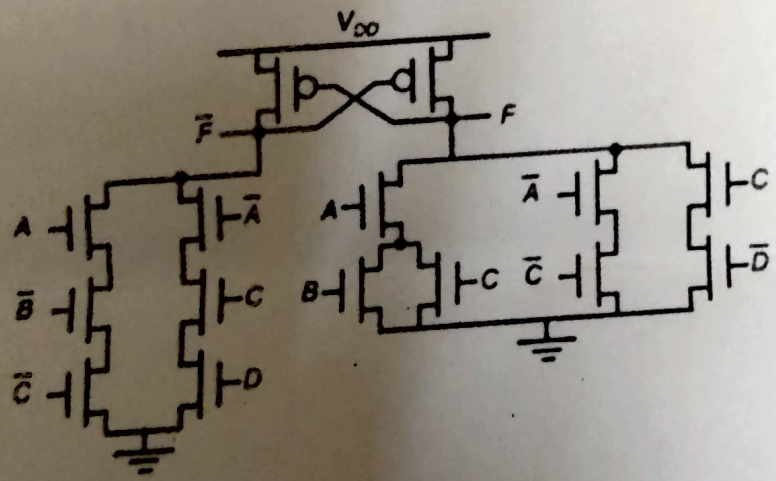

Figure 5

11. Enumerate the various stages that must be traversed throughout the physical design flow of an Integrated Circuit (IC) before the specifications can be taped out. **[5]**

OR

Discuss the various stages and challenges involved in the 'design to realization' of a MEMS microsensor system.

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