VLSI Design Overview and MOSFET Theory

Unit -1

by
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IC & its Levels of Integration

Integrated circuits contain millions of transistors, which can be mass-produced very cheaply. It is less expensive, more reliable, and more compact in size than the conventional circuit.

Other benefits of ICs:

- **Easy to produce in large scale**
- **Low power consumption**
- **Low noise**
- **High-temperature stability**
- **Debugging is simple**

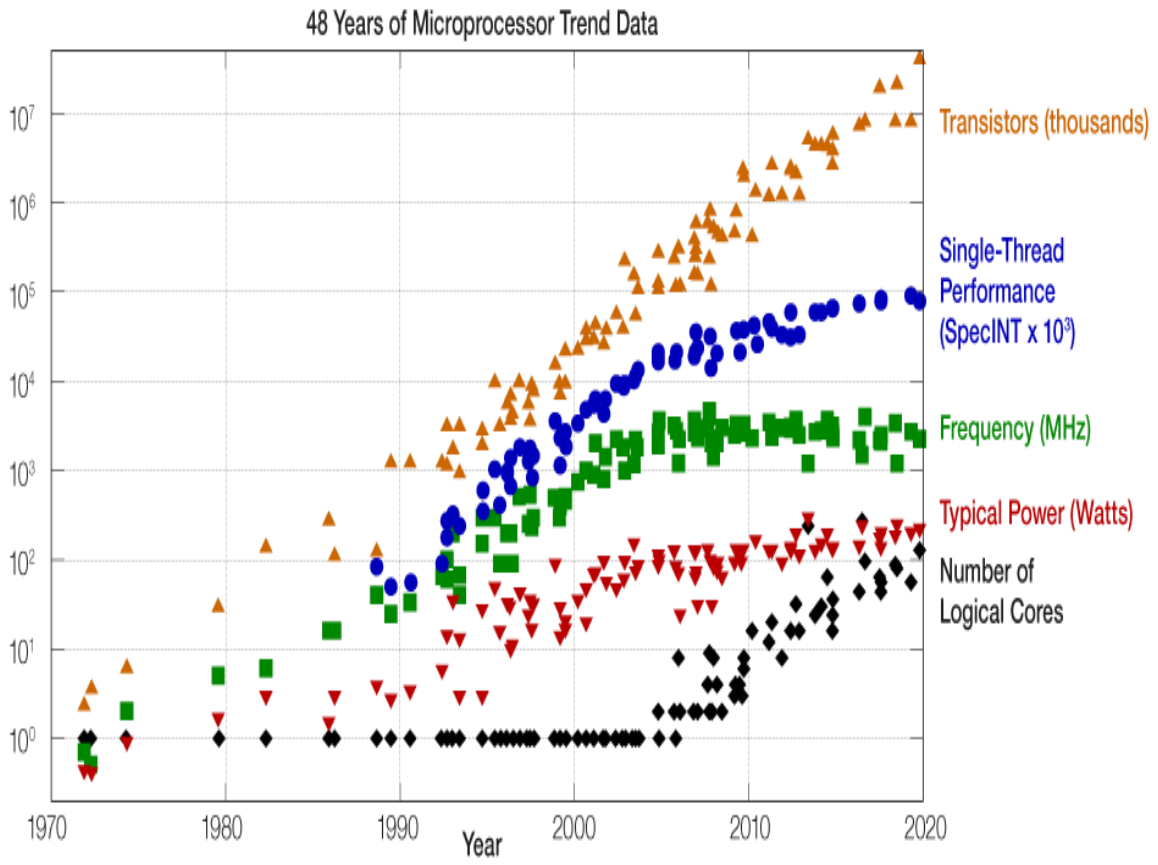
Applications of ICs:

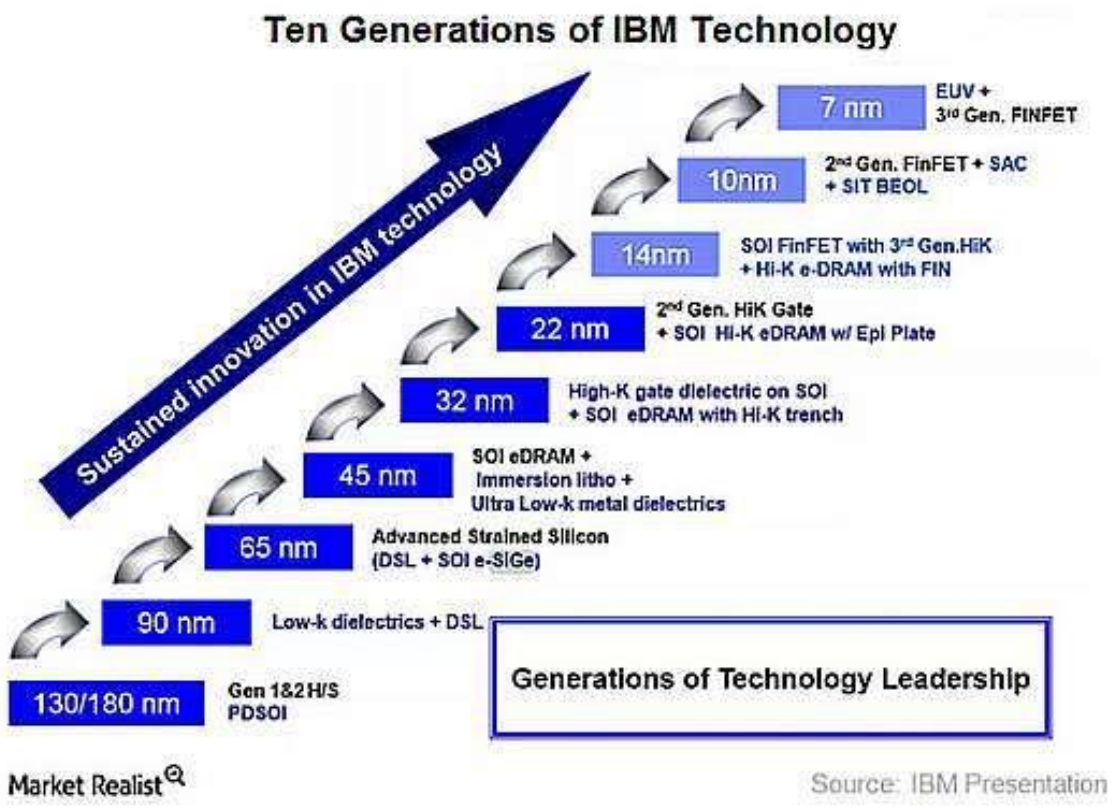
- Personal computer
- Cellular phone
- Internet
- Wireless communication
- Automobile electronics
- Medical applications

IC Density of Integration

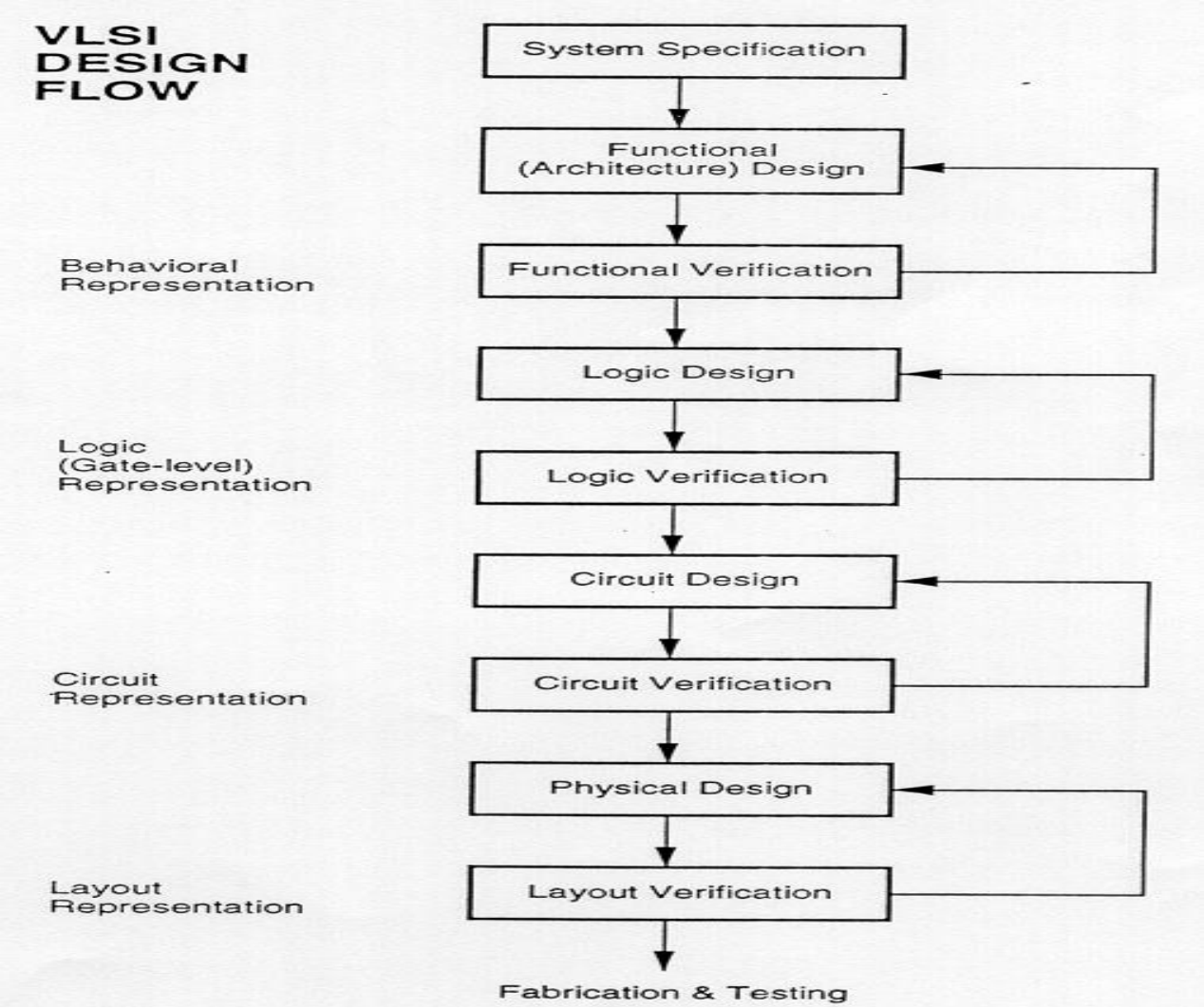
Density of Integration / Complexity	Gates per IC
SSI: Small-Scale Integration • Logic Gates (AND, OR, NAND, NOR)	<10
MSI: Medium-Scale Integration • Flip Flops • Adders / Counters • Multiplexers & De-multiplexers	10 – 100
LSI: Large-Scale Integration •Small Memory Chips •Programmable Logic Device	100 – 10,000
VLSI: Very Large-Scale Integration •Large Memory Chips •Complex Programmable Logic Device	10,000 – 100,000
ULSI: Ultra Large-Scale Integration •8 & 16 Bit Microprocessors	100,000 – 1,000,000
GSI: Giga-Scale Integration •Pentium IV Processor	>1,000,000

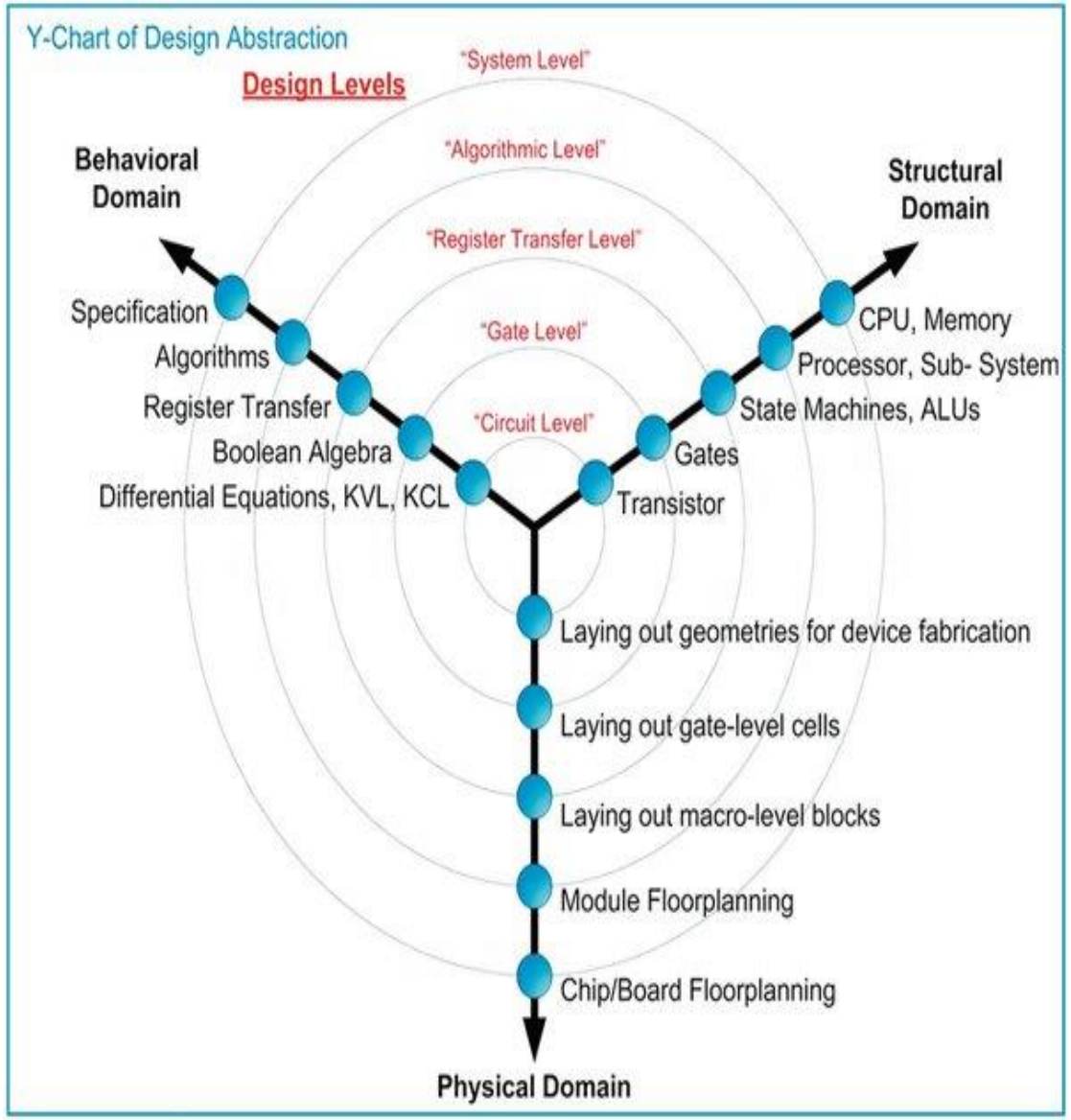
Moore's Law


48 Years of Microprocessor Trend Data
Transistors (thousands)
Single-Thread Performance (SpecINT x 10³)
Frequency (MHz)
Typical Power (Watts)
Number of Logical Cores
Year
1970
1980
1990
2000
2010
2020
Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2019 by K. Rupp


Ten Generations of IBM Technology
Sustained innovation in IBM technology
7 nm
EUV + 3rd Gen. FINFET
10nm
2nd Gen. FinFET + SAC + SIT BEOL
14nm
SOI FinFET with 3rd Gen.HiK + Hi-K e-DRAM with FIN
22 nm
2nd Gen. HiK Gate + SOI Hi-K eDRAM w/ Epi Plate
32 nm
High-K gate dielectric on SOI + SOI eDRAM with Hi-K trench
45 nm
SOI eDRAM + Immersion litho + Ultra Low-k metal dielectrics
65 nm
Advanced Strained Silicon (DSL + SOI e-SiGe)
90 nm
Low-k dielectrics + DSL
130/180 nm
Gen 1&2 H/S PDSOI
Generations of Technology Leadership
Market Realist
Source: IBM Presentation

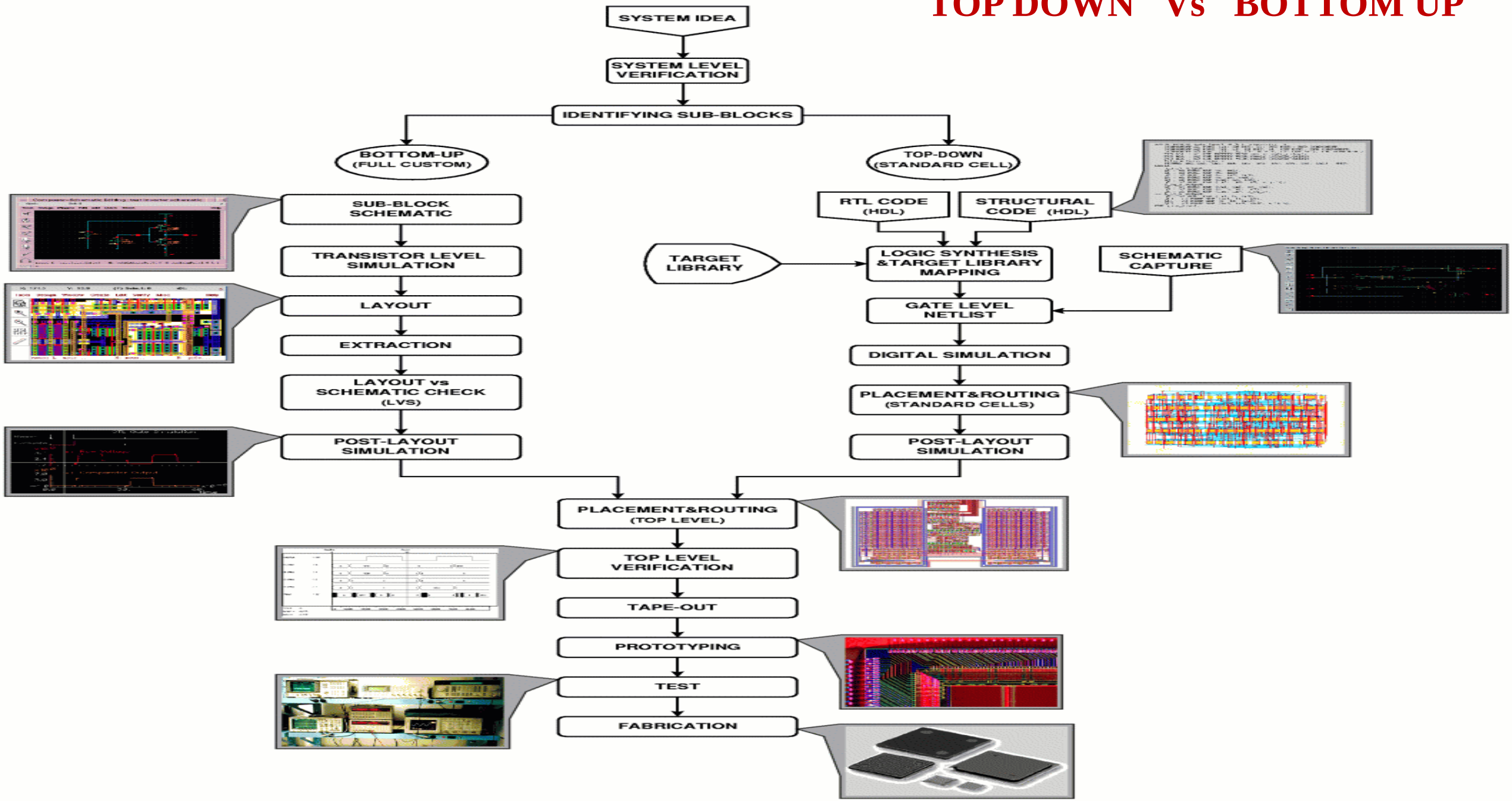
VLSI DESIGN FLOW



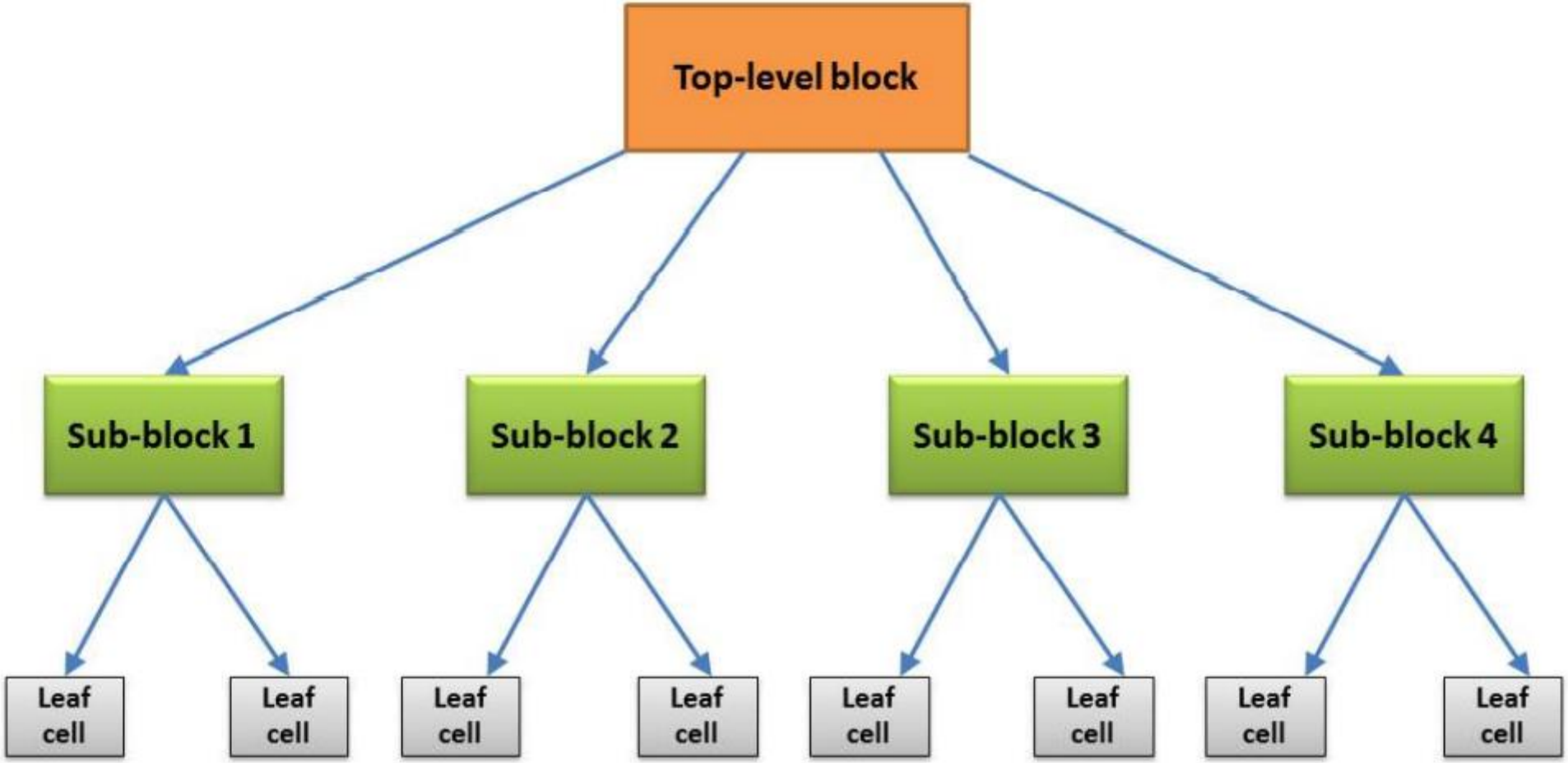


VLSI DESIGN FLOW

TOP DOWN Vs BOTTOM UP



Top-down Design Methodology



Structured Design Approach

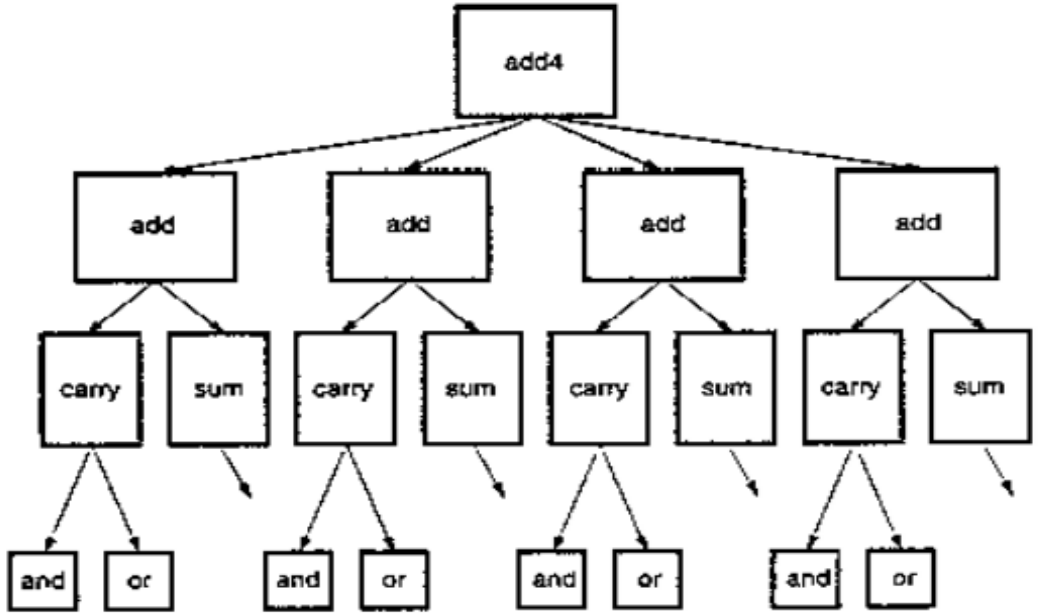
Classical techniques for reducing the complexity of IC design are:

1. Hierarchy
2. Regularity
3. Modularity
4. Locality

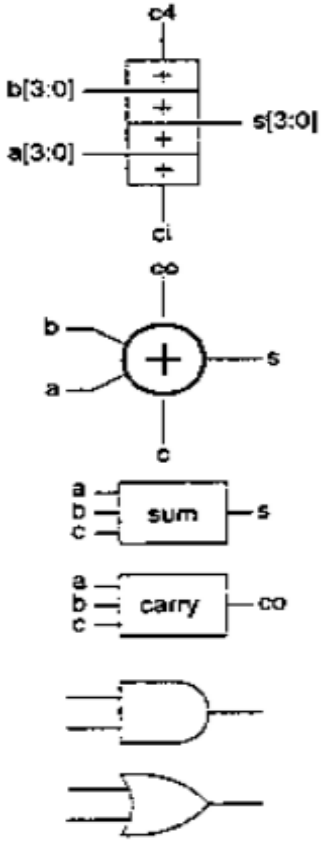
Design Hierarchy

Structural decomposition of a 4-bit adder into its components

Design Hierarchy



(a)



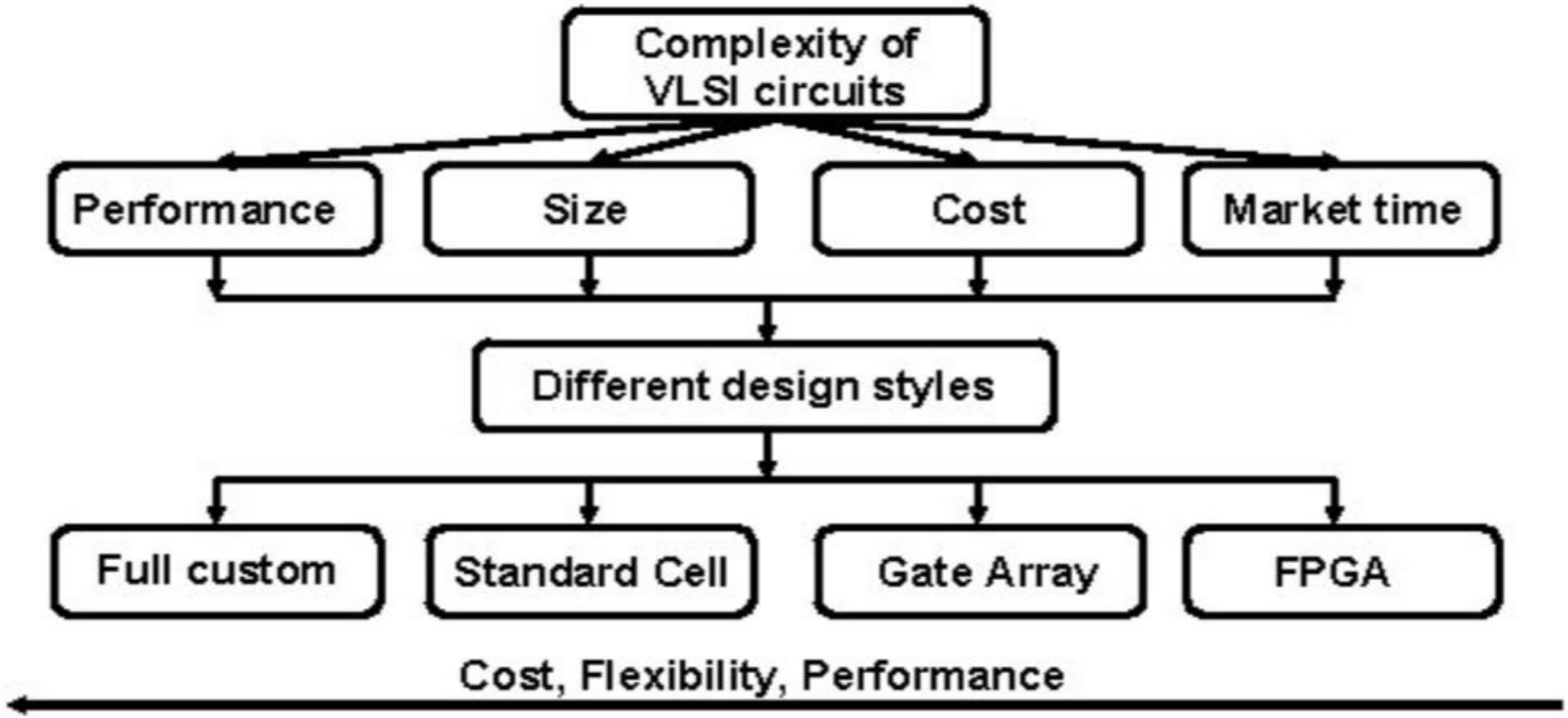
Hierarchy: **“Divide and conquer “ technique involves dividing a module into submodules and then repeating this operation on the sub-modules until the complexity of the smaller parts becomes manageable.**

Regularity: **The hierarchical decomposition of a large system should result in not only simple, but also similar blocks, as much as possible. Regularity usually reduces the number of different modules that need to be designed and verified, al all levels of abstraction**

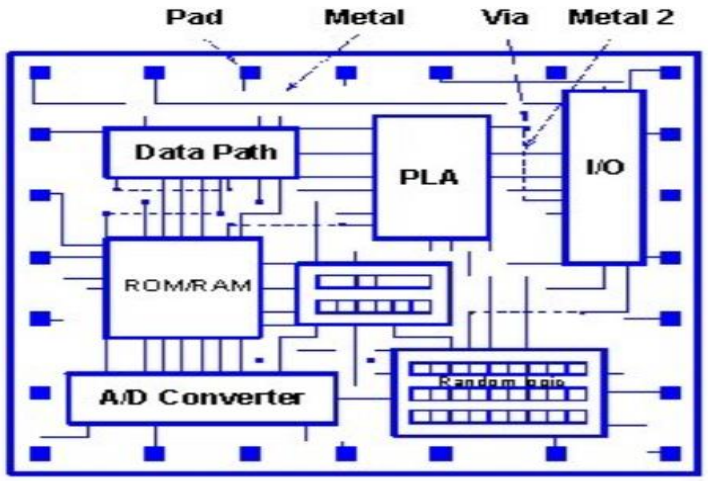
Modularity: **The various functional blocks which make up the larger system must have well-defined functions and interfaces**

Locality: **Internal details remain at the local level. The concept of locally also ensures that connections are between neighboring modules, avoiding long-distance connections as much as possible**

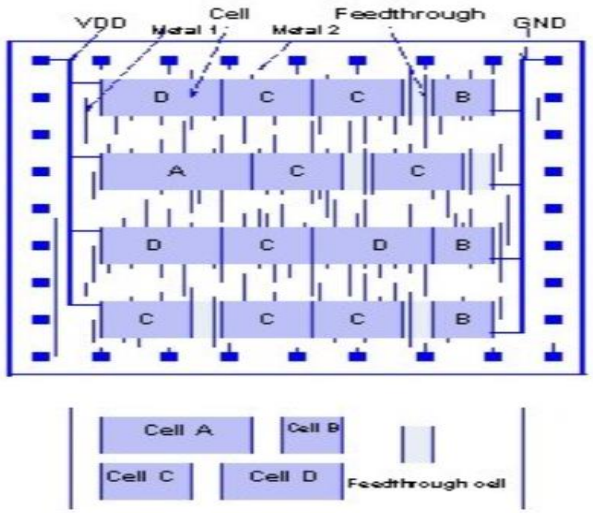
Design Styles



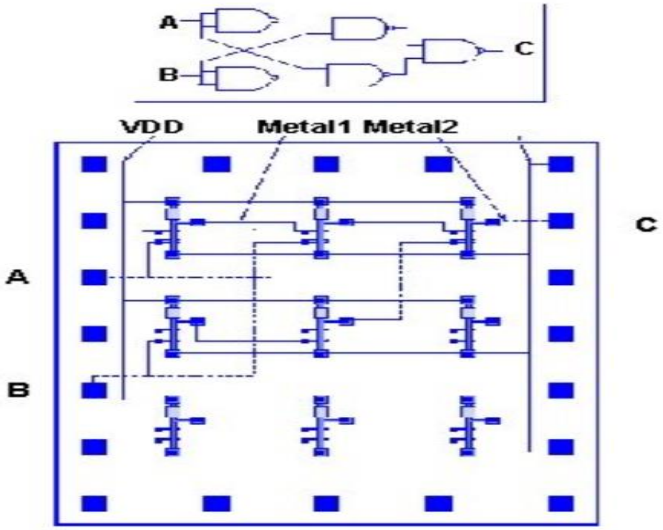
Full Custom Design Style



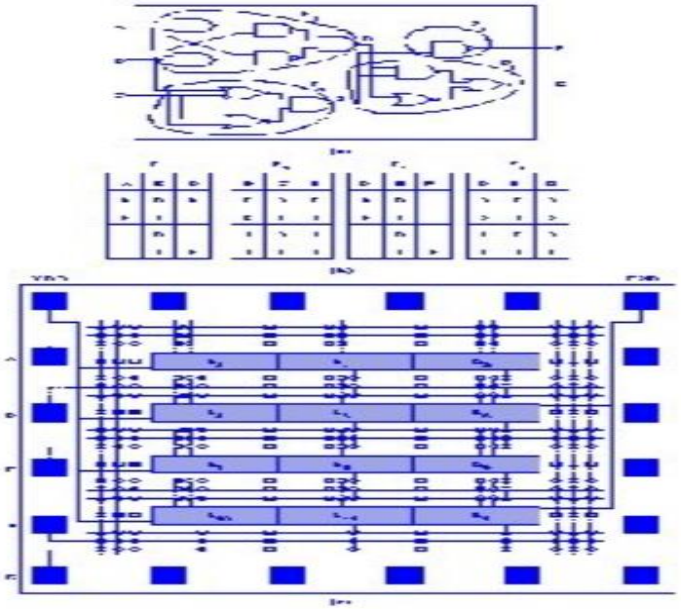
Standard Cell Design Style



Gate Array Design Style



FPGA Design Style



Comparisons of Design Styles

	style			
	full-custom	standard cell	gate array	FPGA
cell size	variable	fixed height *	fixed	fixed
cell type	variable	variable	fixed	programmable
cell placement	variable	in row	fixed	fixed
interconnections	variable	variable	variable	programmable

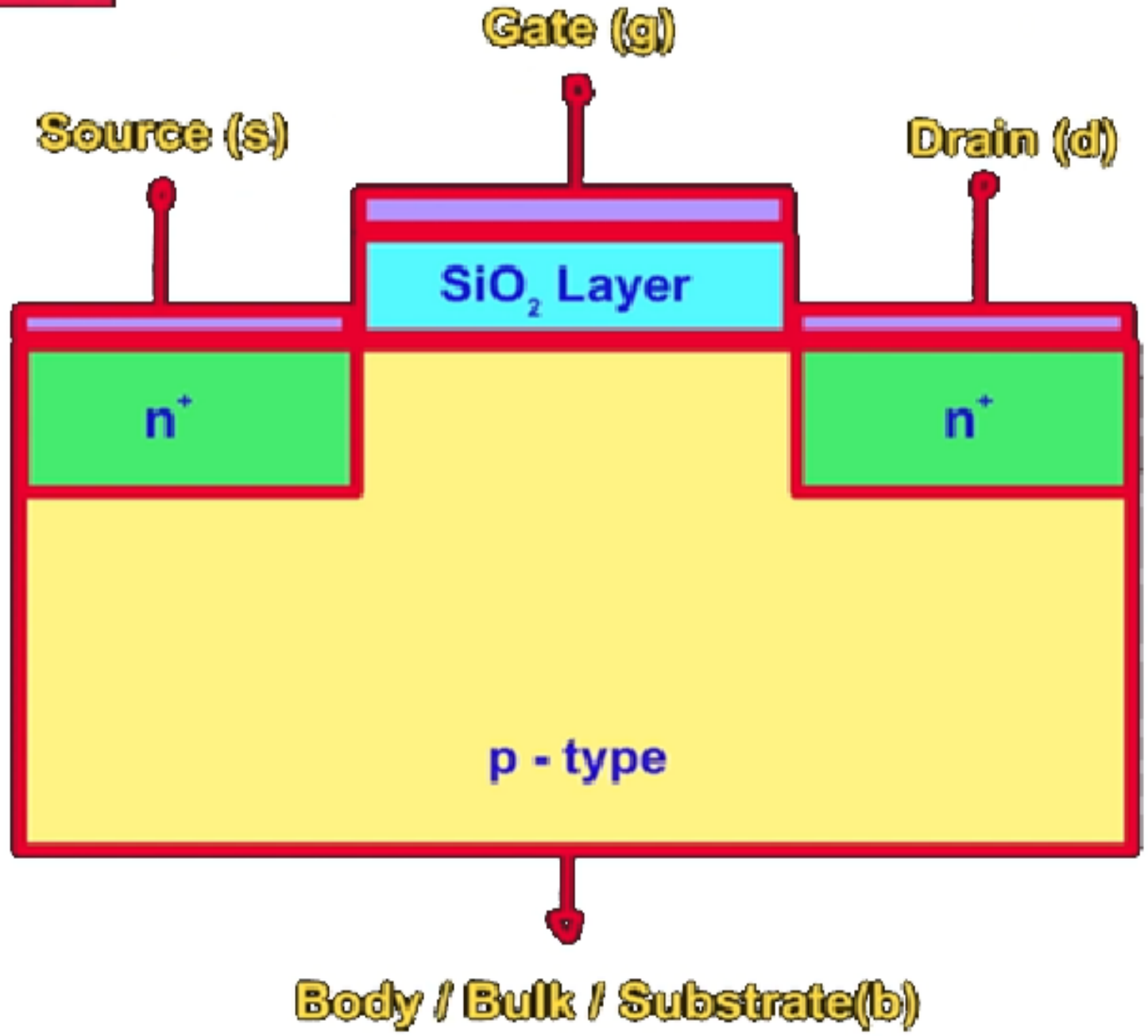
	style			
	full-custom	standard cell	gate array	FPGA
Area	compact	compact to moderate	moderate	large
Performance	high	high to moderate	moderate	low
Fabrication layers	ALL	ALL	routing layers	none

Design Quality :

Measured to improve chip design

- **Testability (ensure correct functionality- achieved by good test vectors, design of testable chip, reliable test fixtures)**
- **Yield & manufacturability(chip yield is computed by the ratio of good tested chips by total number of tested chips)**
  - **Yield is affected by – mishandling wafer, process variation, functional failure, manufacturing failure, short circuits & open connections during fabrication**
- **Reliability (depends on design & process conditions) affected by Electrostatic discharge, Electrical stress, Latch up in CMOS I/O, Oxide breakdown, On chip Noise and Cross talk, Power & Ground Bouncing.**
- **Technology Updation.(Adhere to new design rules & undergo technology update without change in functionality, allows us to reuse with least cost)**

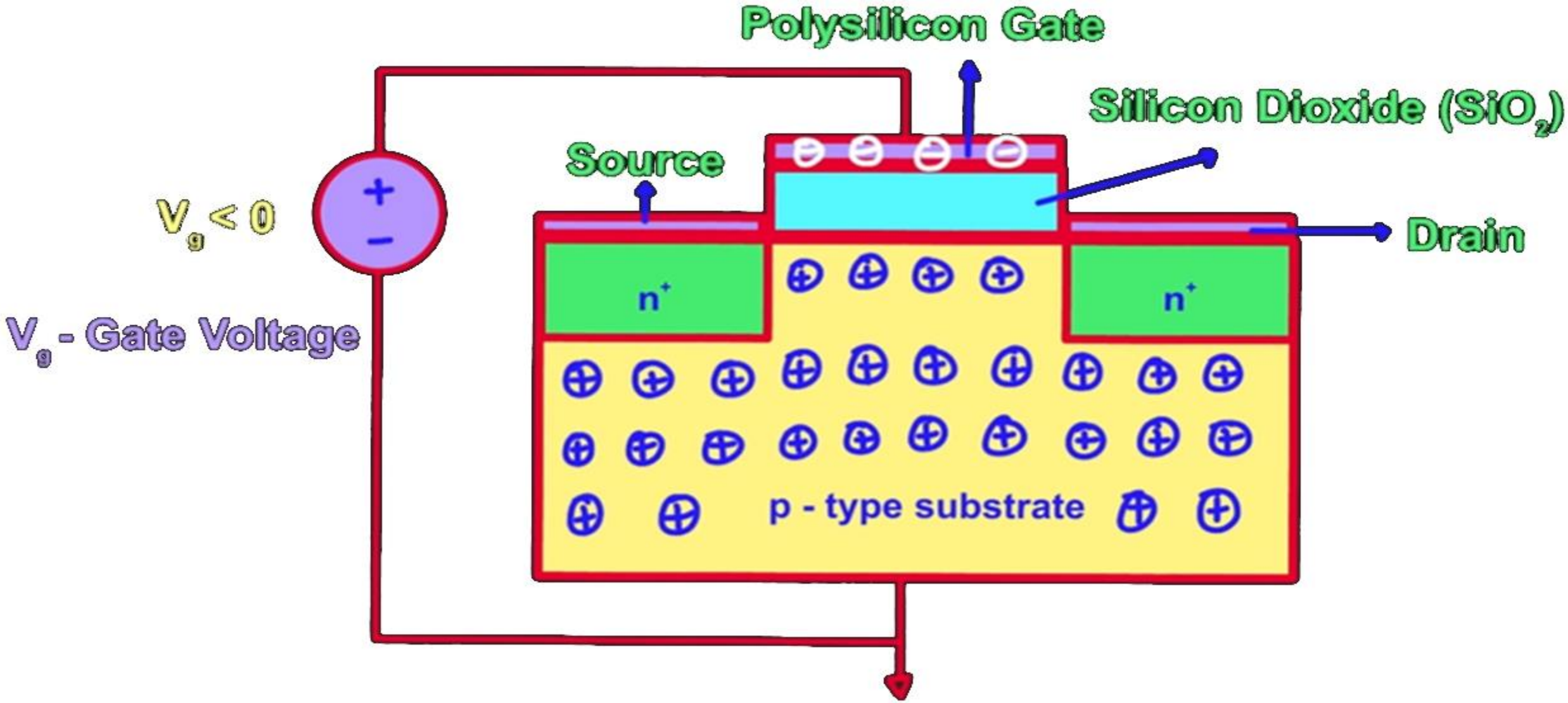
NMOS TRANSISTOR



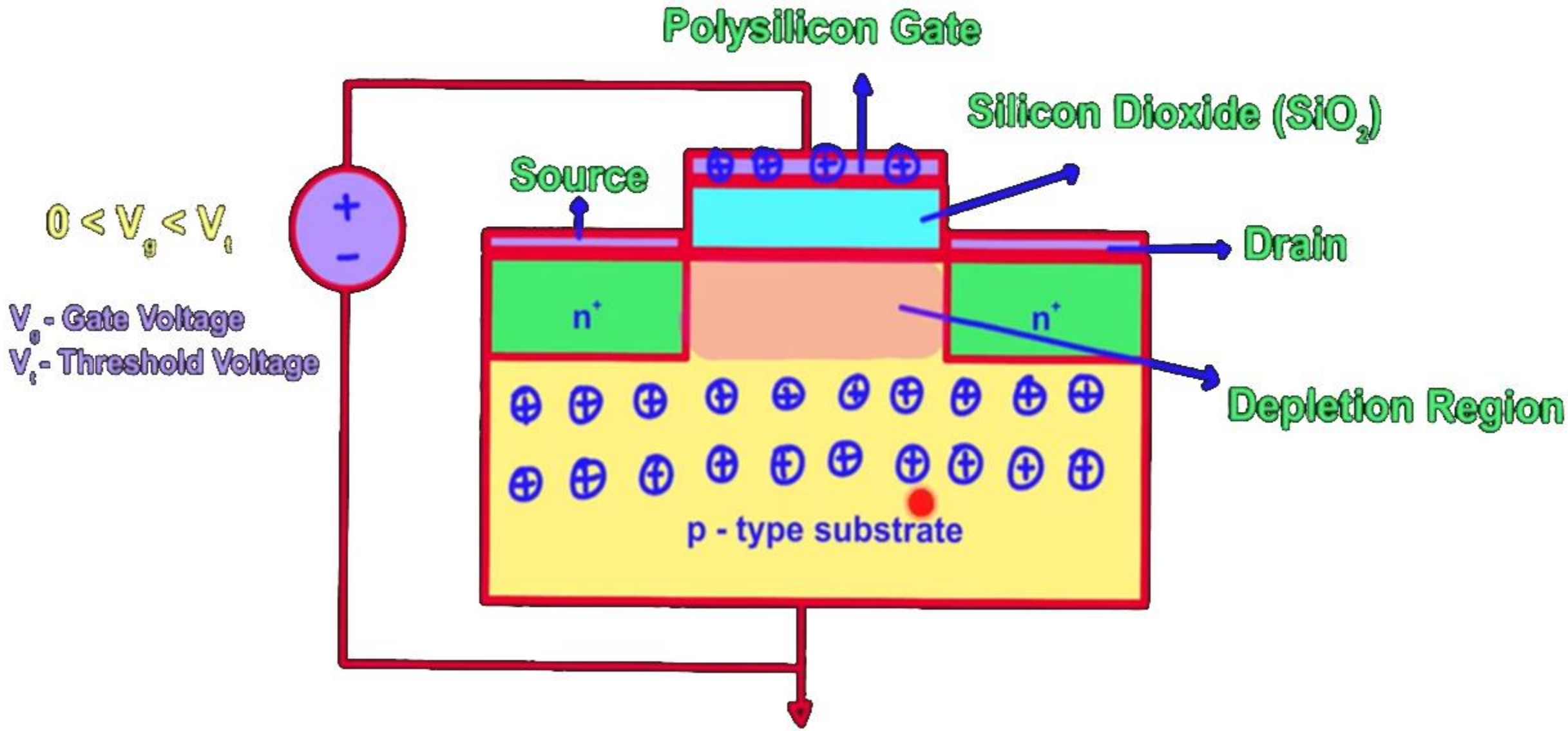
THRESHOLD VOLTAGE (V_t)

- Threshold voltage is defined as the gate voltage at which a MOS transistor starts to conduct.
- It is also defined as the gate voltage at which strong inversion occurs.
- Positive for NMOS Transistor
- Negative for PMOS Transistor

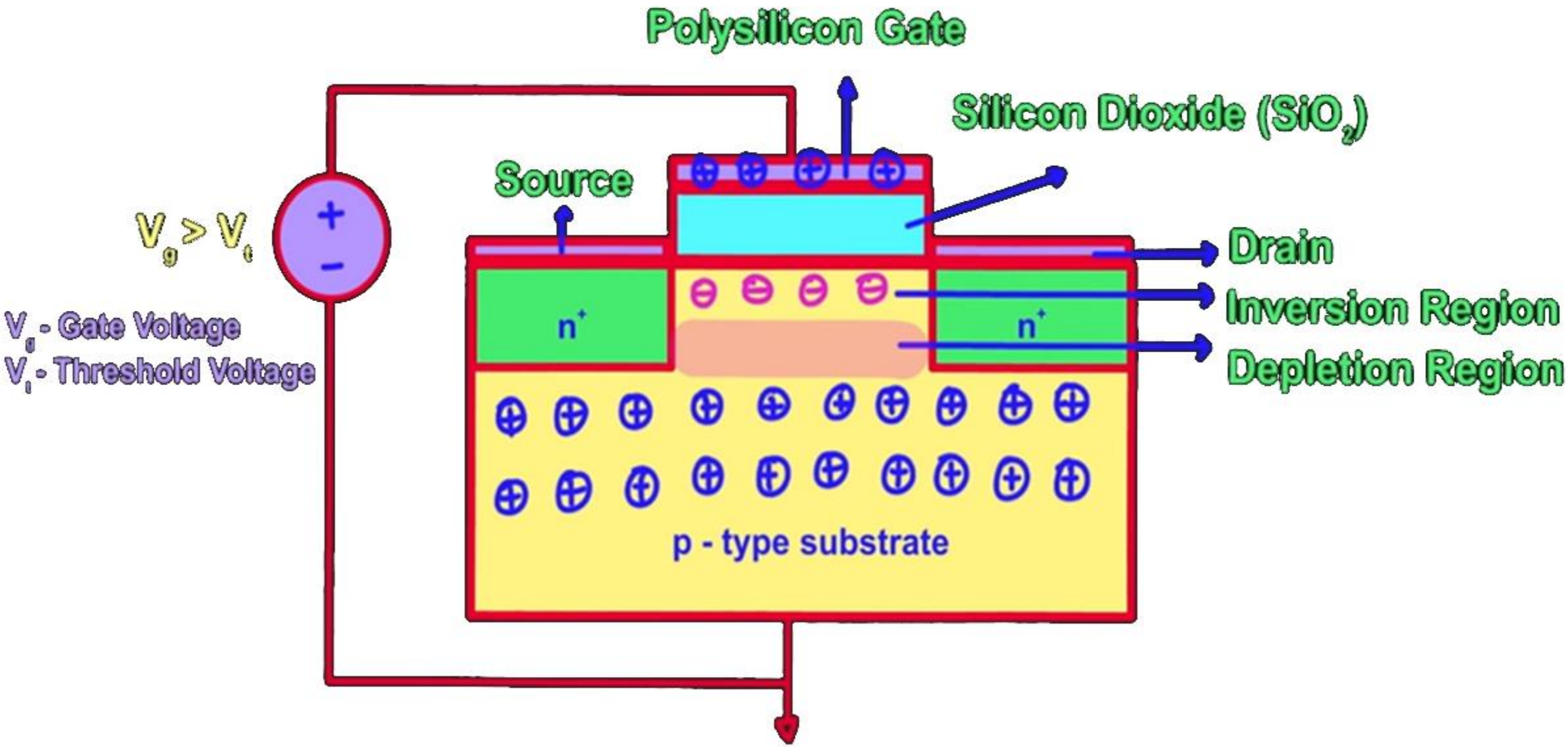
ACCUMULATION MODE ($V_g < 0$)



DEPLETION MODE ($0 < V_g < V_t$)

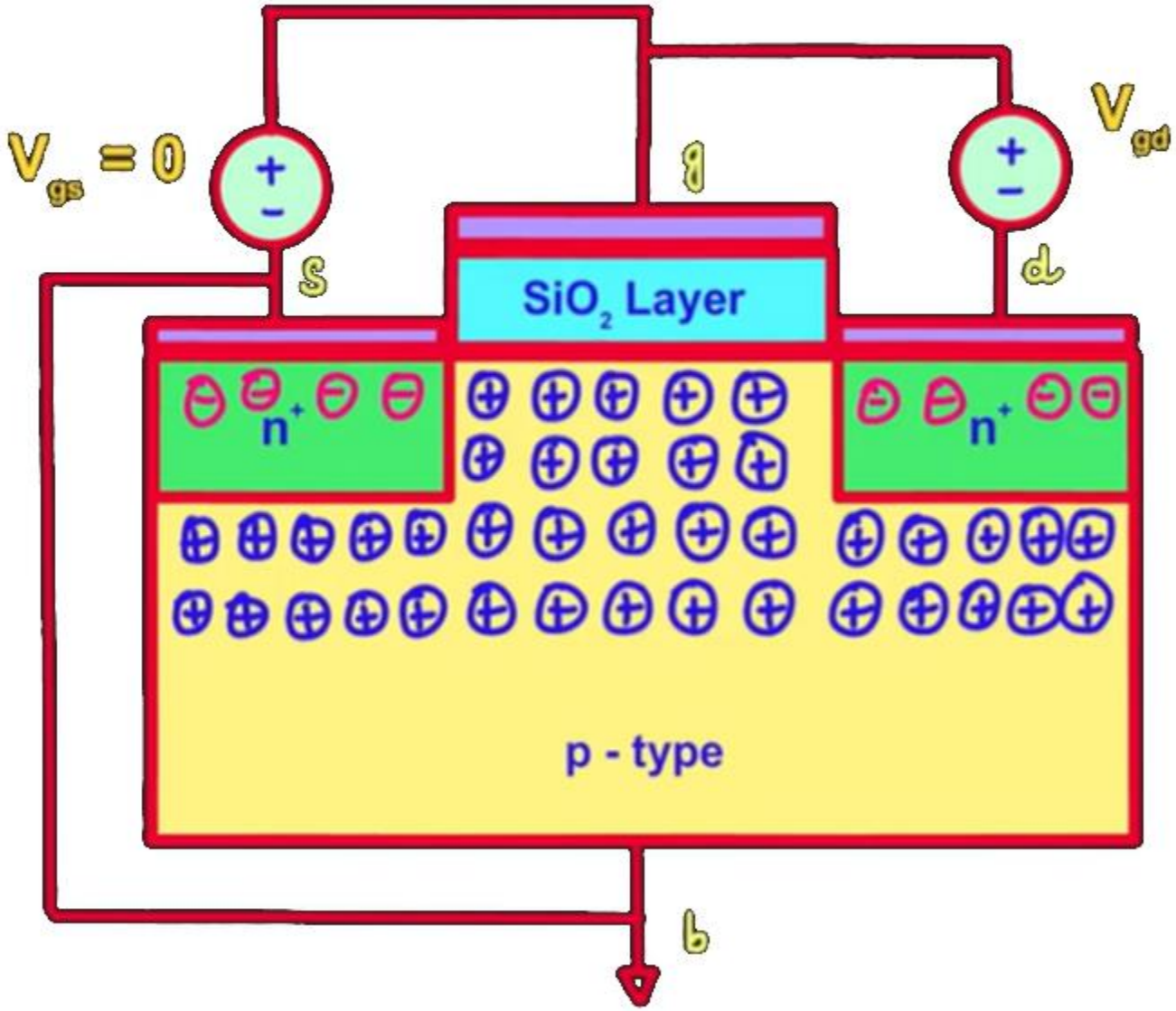


INVERSION MODE ($V_g > V_t$)



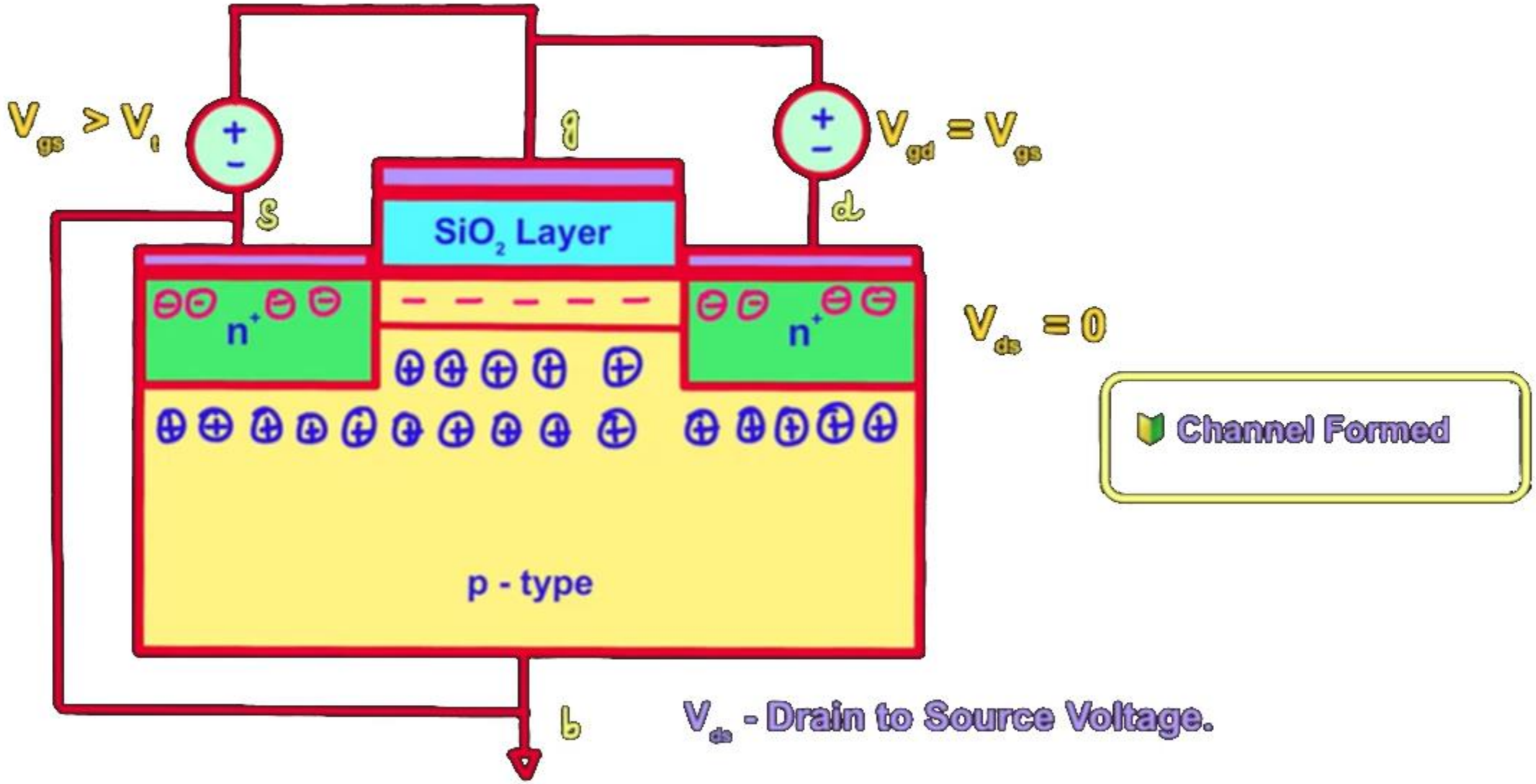
CUT - OFF REGION: $V_{gs} < V_t$

V_{gs} - Gate to Source Voltage
V_t - Threshold Voltage
V_{gd} - Gate to Drain Voltage
I_{ds} - Drain to Source current

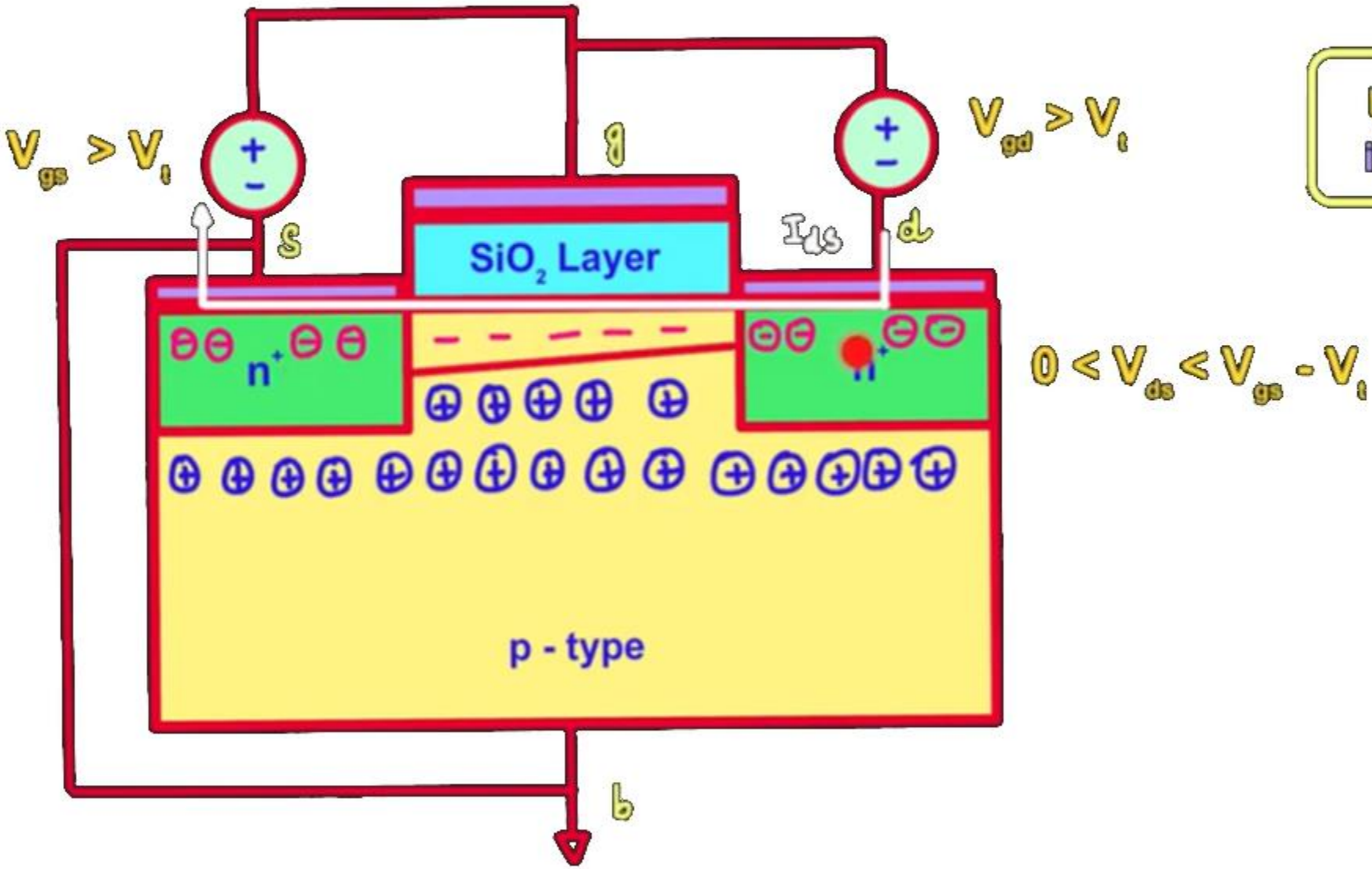


- No formation of channel
- $I_{ds} = 0$

LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$



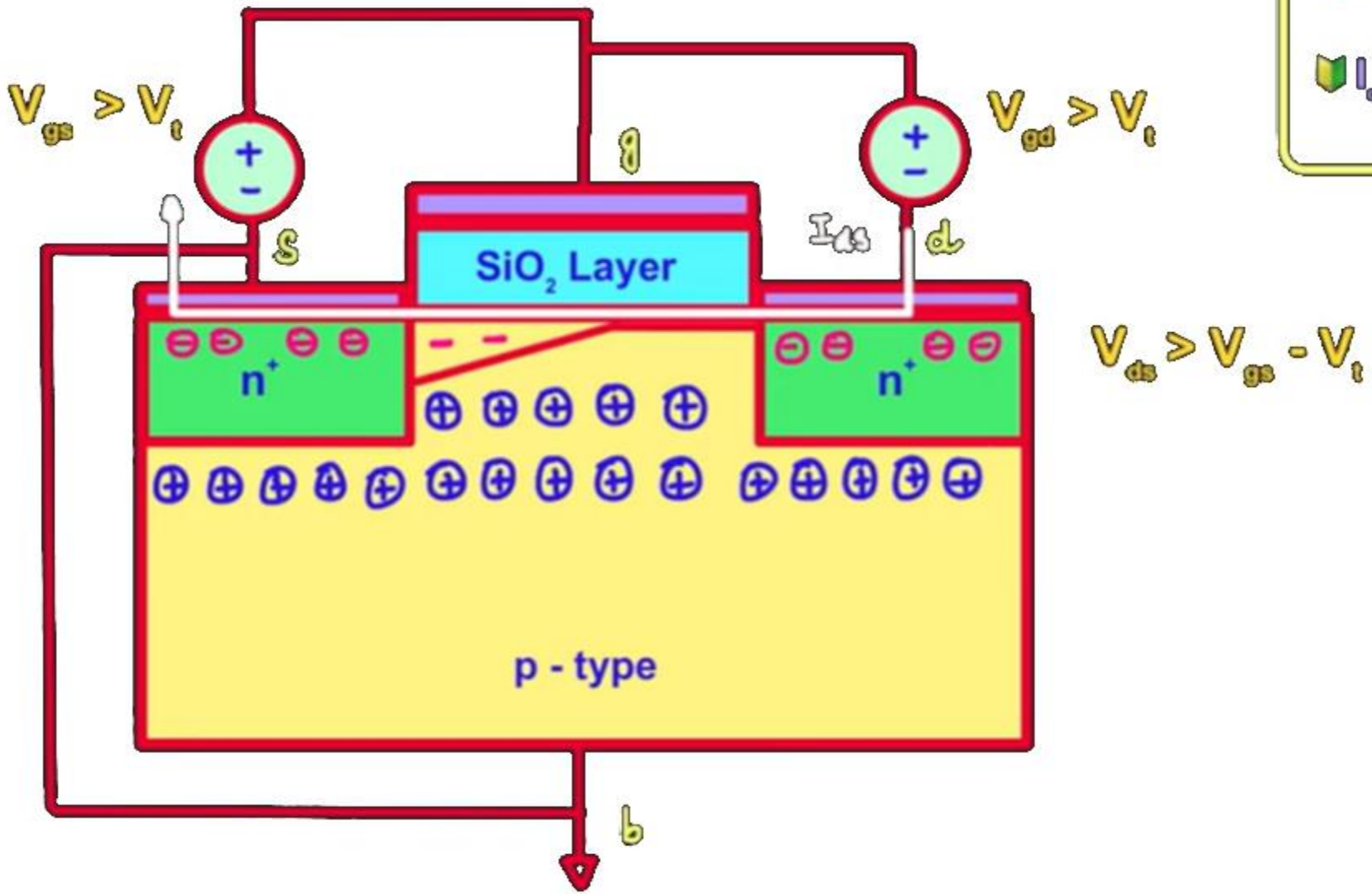
LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$



I_{ds} increases with increase in V_{ds}

SATURATION REGION: $V_{gs} > V_t$; $V_{ds} > (V_{gs} - V_t)$

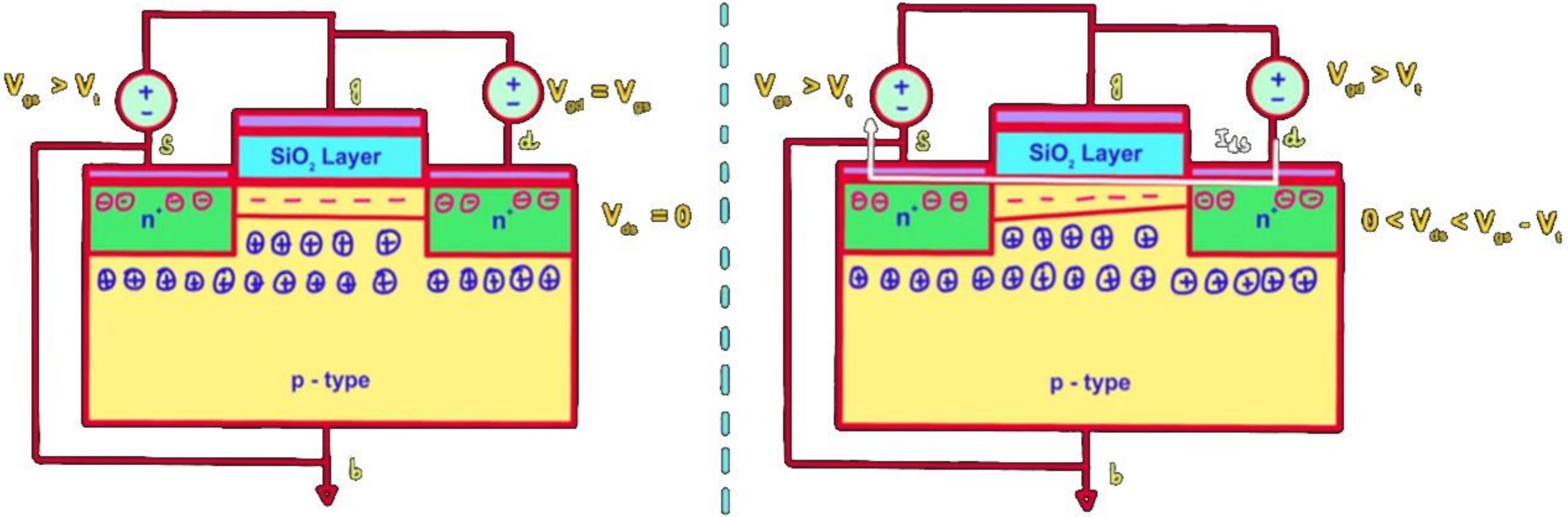
- Channel - Pinched Off
- I_{ds} is independent of V_{ds}



SUMMARY

Voltage conditions	Region	Transistor Behaviour
$V_{gs} < V_t$	Cut - Off	Transistor is in OFF state
$V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$	Linear / Resistive / Ohmic / Triode / Non - Sat.	♦ Transistor is in ON state ♦ Acts as a Resistor ♦ I_{ds} increases with V_{ds}
$V_{gs} > V_t$; $V_{ds} > (V_{gs} - V_t)$	Saturation	♦ Transistor is in ON state ♦ Acts as a Current Source ♦ I_{ds} independent of V_{ds}

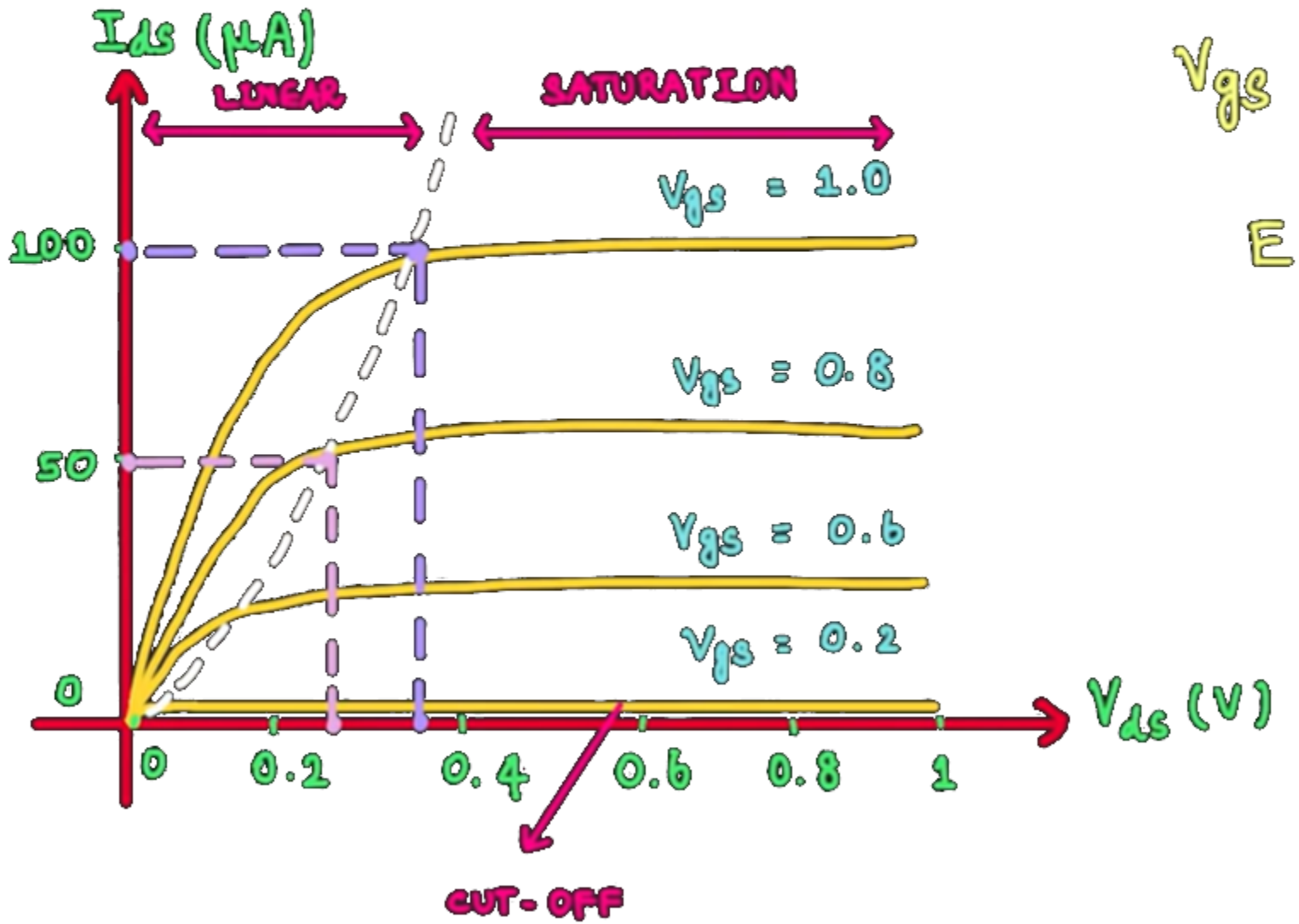
LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$



V_{gs} - Gate to Source Voltage; V_t - Threshold Voltage; V_{gd} - Gate to Drain Voltage; I_{ds} - Drain to Source current
V_{ds} - Drain to Source Voltage

I - V Characteristics of nMOS Transistor

How I_{ds} increases linearly with increase in V_{ds}?



$V_{gs} > V_t$ and $0 < V_{ds} < V_{gs} - V_t$

$E \uparrow$; $v_d = \mu E$ → Electric Field

v_d: drift velocity; μ: mobility

$\uparrow \mu = \frac{v_d}{E} \uparrow$; $\uparrow J_n = nqE\mu \uparrow$

J_n: current density

* $\boxed{\text{Current Density } (J_n) = n\, q\, E\, \mu_n \ (A/m^2)}$

where ; n = particle (electrons) density (particles/m^3)

q = electronic charge (C)

E = Electric Field (V/m)

μ_n = mobility of electrons (m^2/V-s) = $\frac{v_d}{E}$

v_d = Drift Velocity (m/s)

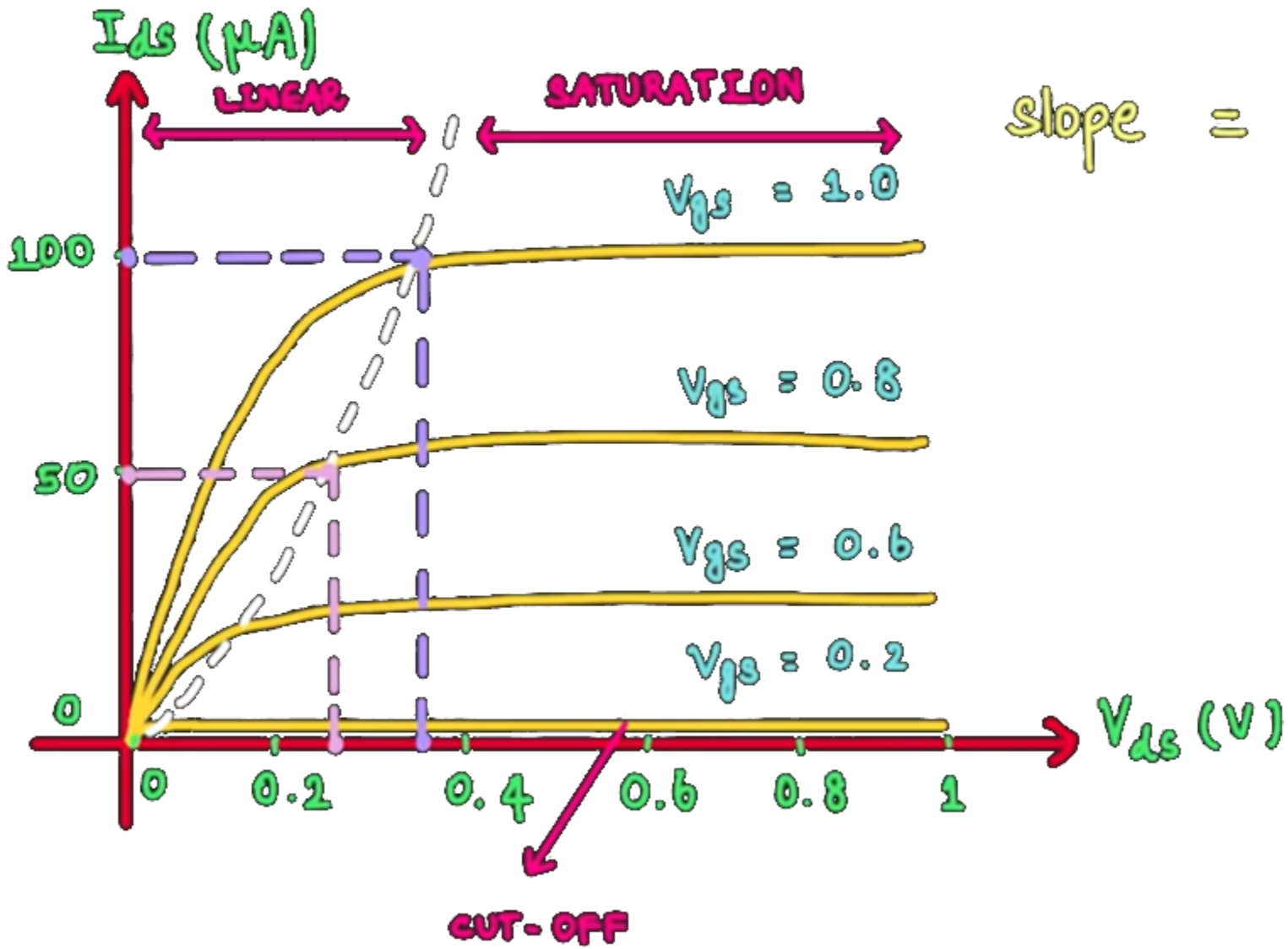
$V_{ds} \uparrow \quad E \uparrow$

$v_d \uparrow \quad \mu_n \uparrow \quad J_n \uparrow \quad I \uparrow$

* $\boxed{\text{Current } (I) = J_n A \quad (A)}$

where; A = Area (m^2)

I - V Characteristics of nMOS Transistor



$$\text{slope} = \frac{\Delta I_{ds}}{\Delta V_{ds}} \quad \text{and} \quad R = \frac{V_{ds}}{I_{ds}}$$

$$\boxed{R = \frac{1}{\text{slope}}}$$

$$V_{ds} \propto I_{ds}$$

$$V = IR$$

LINEAR / RESISTIVE / OHMIC REGION $V_{gs} > V_t ; 0 < V_{ds} < (V_{gs} - V_t)$

$$\text{slope} = \frac{\Delta I_{ds}}{\Delta V_{ds}} \quad \text{and} \quad R = \frac{V_{ds}}{I_{ds}}$$

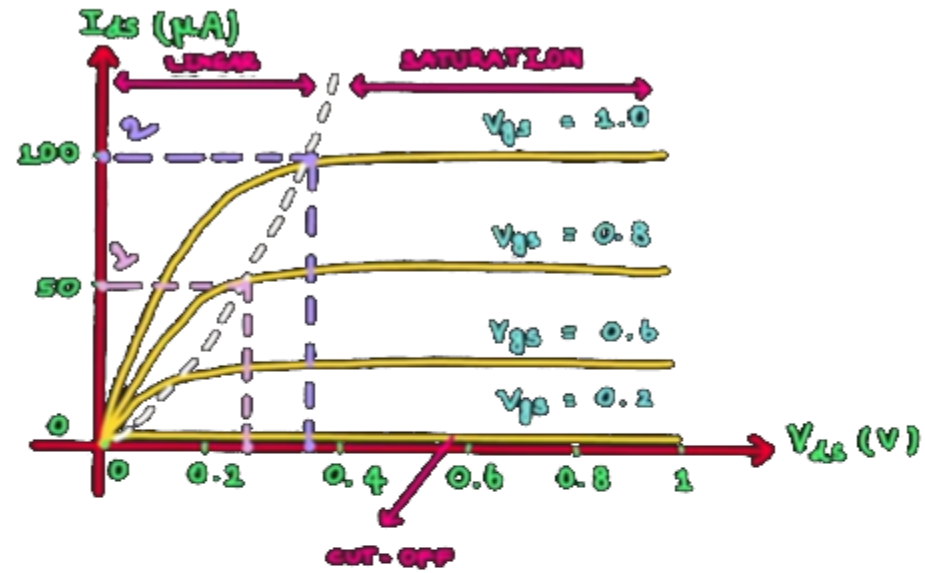
$$\boxed{R = \frac{1}{\text{slope}}}$$

$$\text{slope}_1 = \frac{50-0}{0.25-0} = \frac{50}{0.25} = 200\ \mu A/V$$

@ $V_{gs} = 0.8V$

$$\text{slope}_2 = \frac{100-0}{0.35-0} = \frac{100}{0.35} = 285.7\ \mu A/V$$

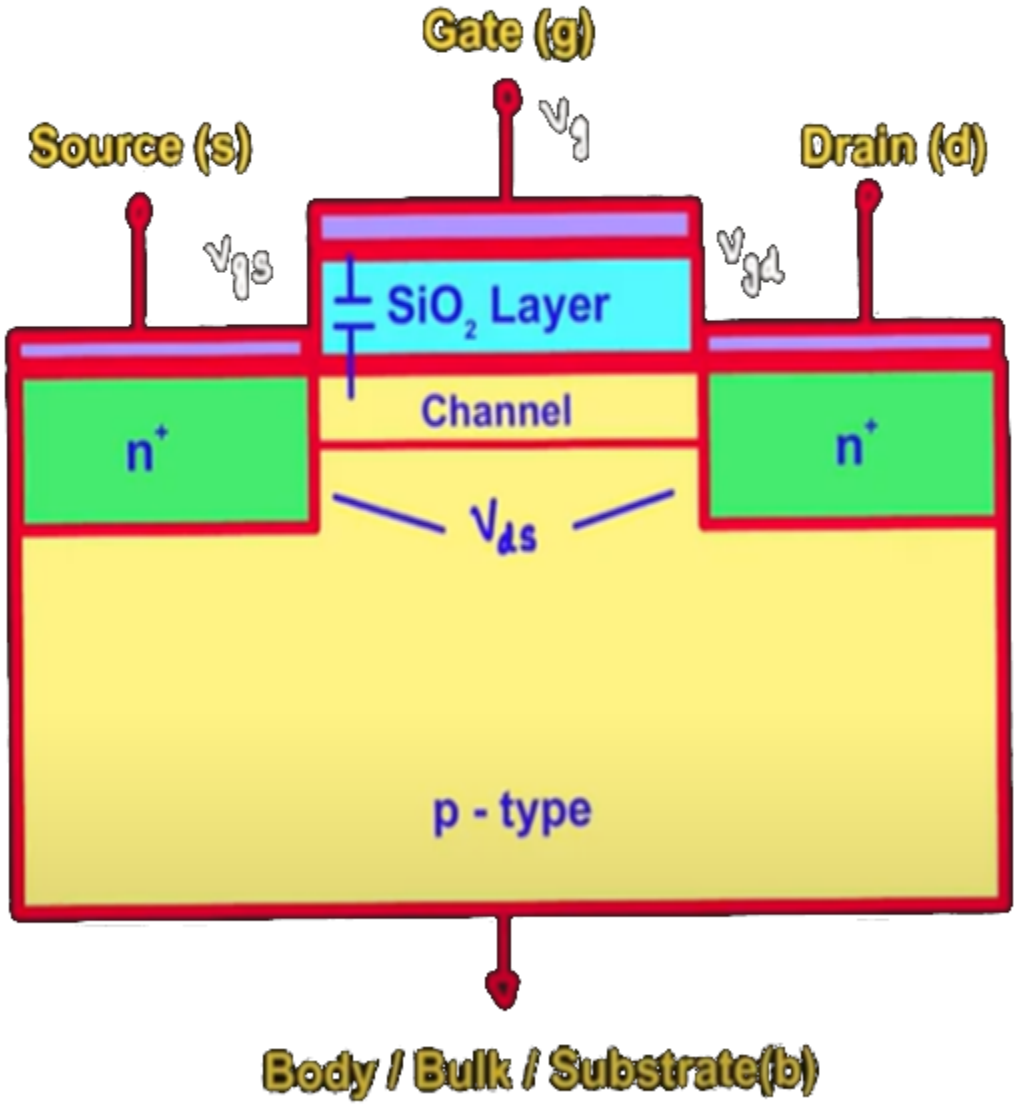
@ $V_{gs} = 1V$



V_{gs} - Gate to Source Voltage; V_t - Threshold Voltage; V_{gd} - Gate to Drain Voltage; I_{ds} - Drain to Source current
V_{ds} - Drain to Source Voltage.

For different values of V_{gs}, channel resistance (R) changes, hence by varying V_{gs} values, we can use FET as a **variable resistor** in linear region.

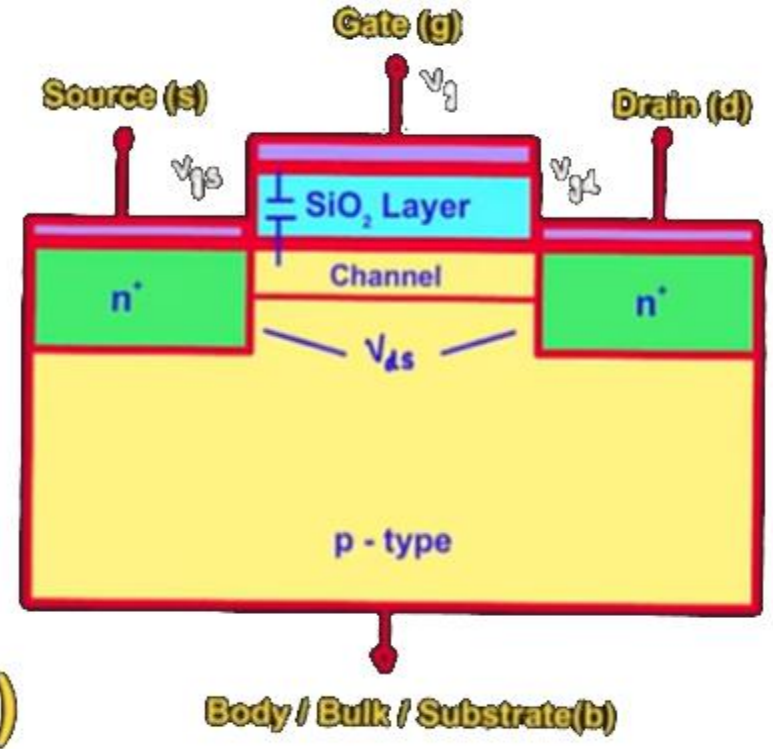
NMOS TRANSISTOR



Voltage conditions	Region
$V_{gs} < V_t$	Cut - Off
$V_{gs} > V_t; 0 < V_{ds} < (V_{gs} - V_t)$	Linear / Resistive / Ohmic / Triode / Non - Sat.
$V_{gs} > V_t; V_{ds} > (V_{gs} - V_t)$	Saturation

CUT - OFF REGION: $V_{gs} < V_t$

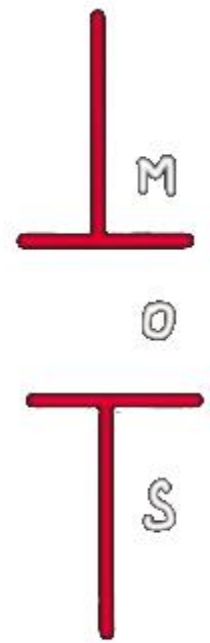
- Transistor is in OFF state.
- Hence, current through an OFF transistor is "0".



LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$

charge on each plate of a capacitor;

$$Q = CV$$



◆ LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$

charge in the channel ; $Q_{channel} = C_g (V_{gc} - V_t)$

where ; C_g - capacitance of gate to channel.

$V_{gc} - V_t$ - amount of voltage required to attract charge to the channel.

Let V_s - source voltage ; V_d - Drain voltage

$$\therefore \text{Average voltage} = V_c = \frac{V_s + V_d}{2} = V_s + \frac{V_{ds}}{2}$$

LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$

$$\therefore \text{Average voltage} = V_c = \frac{V_s + V_d}{2} = V_s + \frac{V_{ds}}{2}$$

$$V_{ds} = V_d - V_s$$

$$\frac{V_{ds}}{2} = \frac{V_d - V_s}{2}$$

$$V_s + \frac{V_{ds}}{2} = V_s + \frac{V_d - V_s}{2}$$

$$V_c = V_s + \frac{V_{ds}}{2} = \frac{2V_s + V_d - V_s}{2}$$

$$V_c = \frac{V_s + V_d}{2}$$

♦ LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$

$$Q_{channel} = C_g (V_{gc} - V_t) \; ; \; V_c = V_s + \frac{V_{ds}}{2}$$

$$V_{gc} = V_g - V_c = V_g - \left[V_s + \frac{V_{ds}}{2} \right]$$

$$(\because V_{gs} = V_g - V_s)$$

$$= V_g - V_s - \frac{V_{ds}}{2}$$

$$\therefore V_{gc} = V_{gs} - \frac{V_{ds}}{2}$$

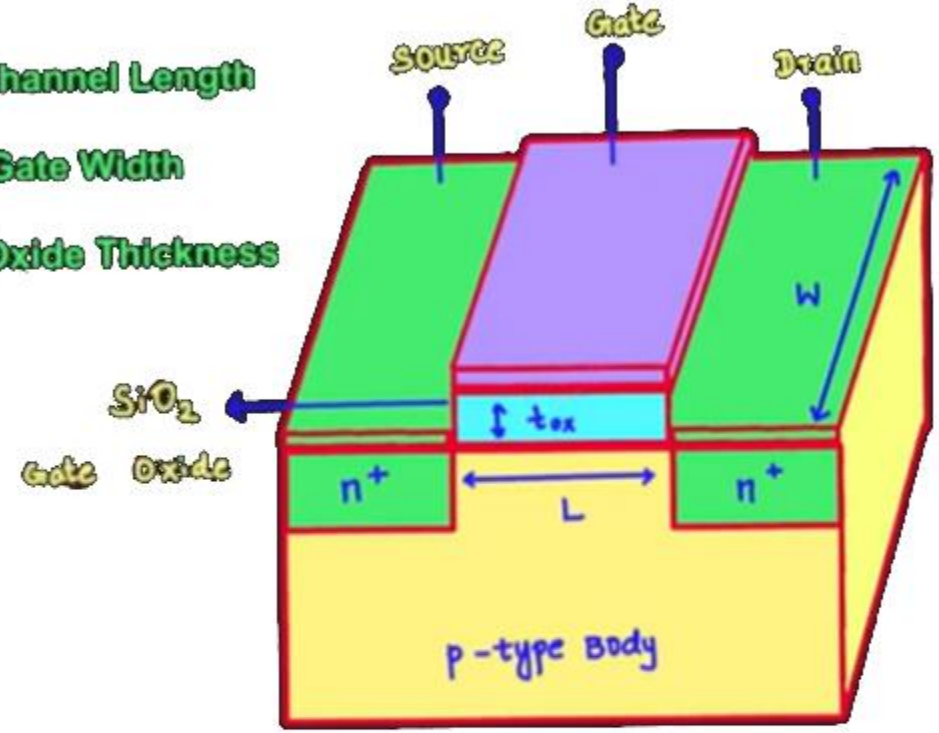
Estimation of Gate Capacitance

$$C_g = C_{ox} WL = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

L = Channel Length

W = Gate Width

t_{ox} = Oxide Thickness



where, $\varepsilon_{ox} = 3.9\varepsilon_0$ = permittivity of silicon dioxide (SiO_2)

ε_0 = permittivity of free space (8.85×10^{-14} F/cm)

t_{ox} = Oxide thickness

C_{ox} = Gate oxide capacitance $= \frac{\varepsilon_{ox}}{t_{ox}}$

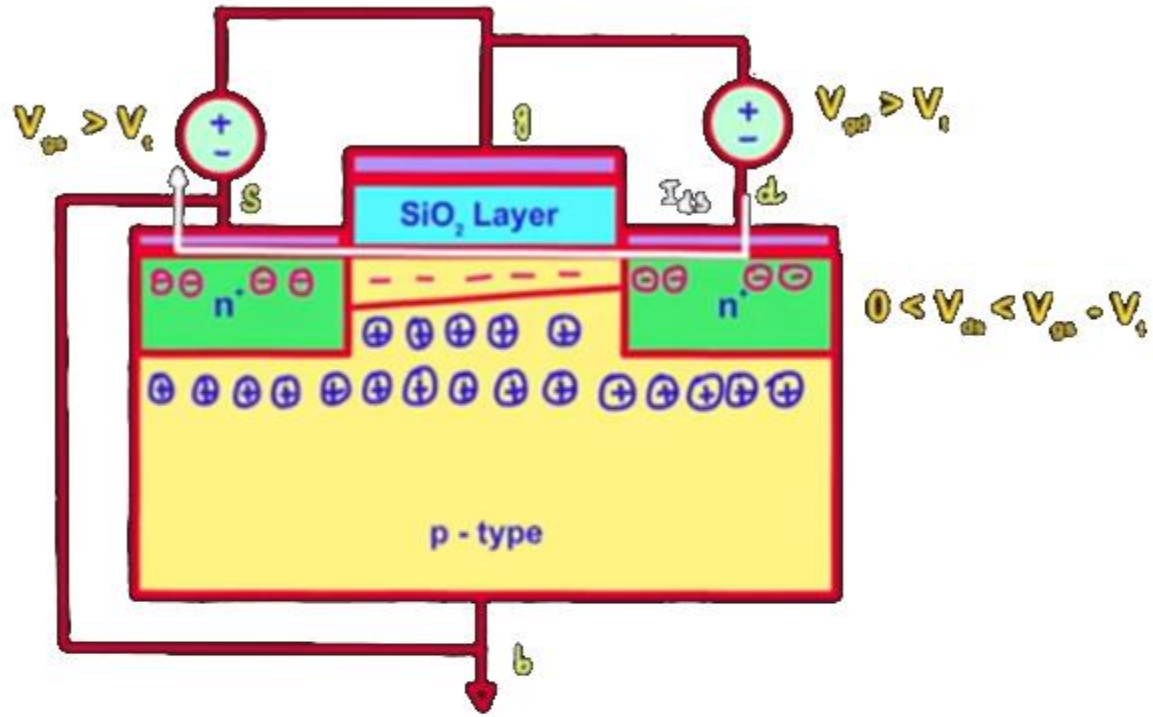
LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$

$$v = \mu_n E$$

where, v = velocity (m/s)

μ_n = mobility constant ($m^2/V.s$)

E = Electric Field (V/m)



$$E = \frac{V_{ds}}{L} \quad ; \qquad t_{ch} = \frac{L}{v}$$

LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$

Current between Source and Drain $(I_{ds}) = \dfrac{\text{Total charge in channel}}{\text{Time required to cross the channel}}$

$$I_{ds} = \frac{Q_{channel}}{t_{ch}}$$

where;

$$t_{ch} = \frac{L}{v} \; ; \quad v = \mu E \; ; \quad E = \frac{V_{ds}}{L}$$

$$v = \frac{\mu V_{ds}}{L} \quad \Rightarrow \quad \frac{L}{v} = \frac{L^2}{\mu \cdot V_{ds}}$$

LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$

$$Q_{channel} = C_g (V_{gc} - V_t)$$

where; $C_g = C_{ox} WL$ and $V_{gc} = V_{gs} - \frac{V_{ds}}{2}$

$$Q_{channel} = C_{ox} WL \left[\left(V_{gs} - \frac{V_{ds}}{2} \right) - V_t \right]$$

$$Q_{channel} = C_{ox} WL \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right]$$

LINEAR REGION: $V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$

$$Q_{channel} = C_{ox} WL \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right]; \quad t_{ch} = \frac{L^2}{\mu \cdot V_{ds}}$$

$$\therefore \quad I_{ds} = \frac{Q_{channel}}{t_{ch}} = \frac{C_{ox} W \cancel{L}}{L^{\cancel{2}}} \times \mu V_{ds} \left[(V_{gs} - V_t) - \frac{V_{ds}}{2} \right]$$

$$I_{ds} = \mu C_{ox} \frac{W}{L} \left[(V_{gs} - V_t) V_{ds} - \frac{V_{ds}^2}{2} \right]$$

$$\downarrow$$

$$\beta = \mu C_{ox} \frac{W}{L} = \text{Device Transconductance parameter}$$

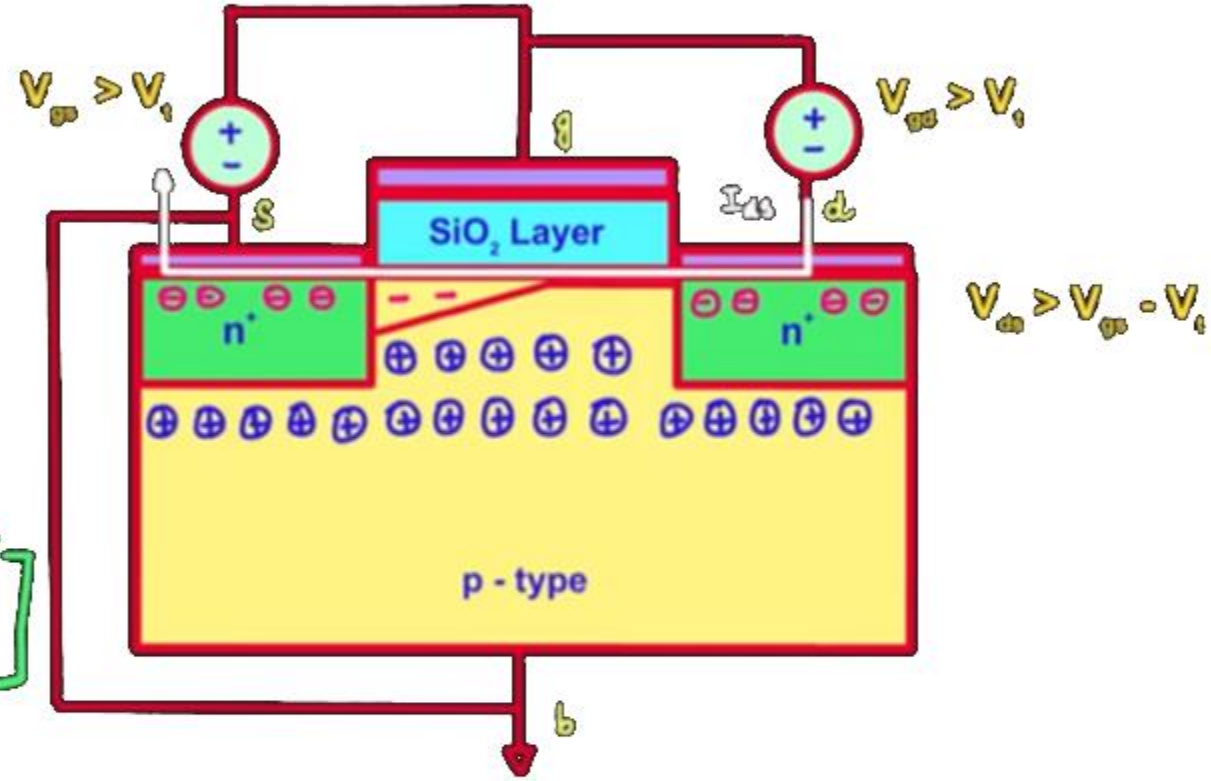
SATURATION REGION: $V_{gs} > V_t$; $V_{ds} > (V_{gs} - V_t)$

$$V_{ds} = V_{gs} - V_t$$

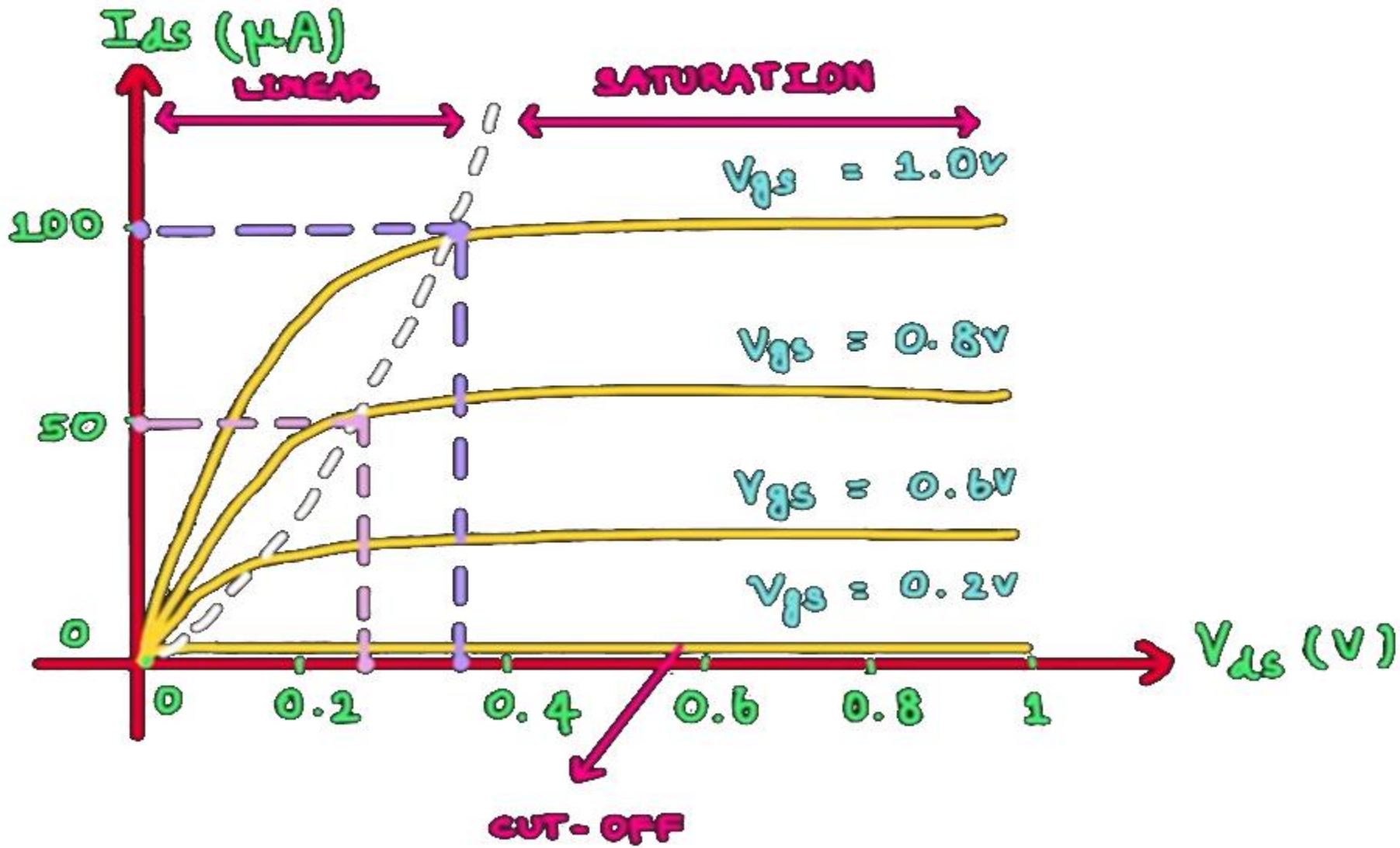
$$I_{ds} = \beta\left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

$$= \beta\left[(V_{gs} - V_t)^2 - \frac{(V_{gs} - V_t)^2}{2}\right]$$

$$\therefore \quad I_{ds} = \frac{\beta}{2}(V_{gs} - V_t)^2 \Rightarrow \text{Independent of } V_{ds}$$



I - V Characteristics of nMOS Transistor



SUMMARY

Voltage conditions	Region	I_{ds} equation
$V_{gs} < V_t$	Cut - Off	0
$V_{gs} > V_t$; $0 < V_{ds} < (V_{gs} - V_t)$	Linear / Resistive / Ohmic / Triode / Non - Sat.	$\beta\,[(V_{gs} - V_t) * V_{ds} - V_{ds}^2 / 2]$
$V_{gs} > V_t$; $V_{ds} \geq (V_{gs} - V_t)$	Saturation	$\beta / 2 * (V_{gs} - V_t)^2$

CAPACITANCES IN A MOS TRANSISTOR

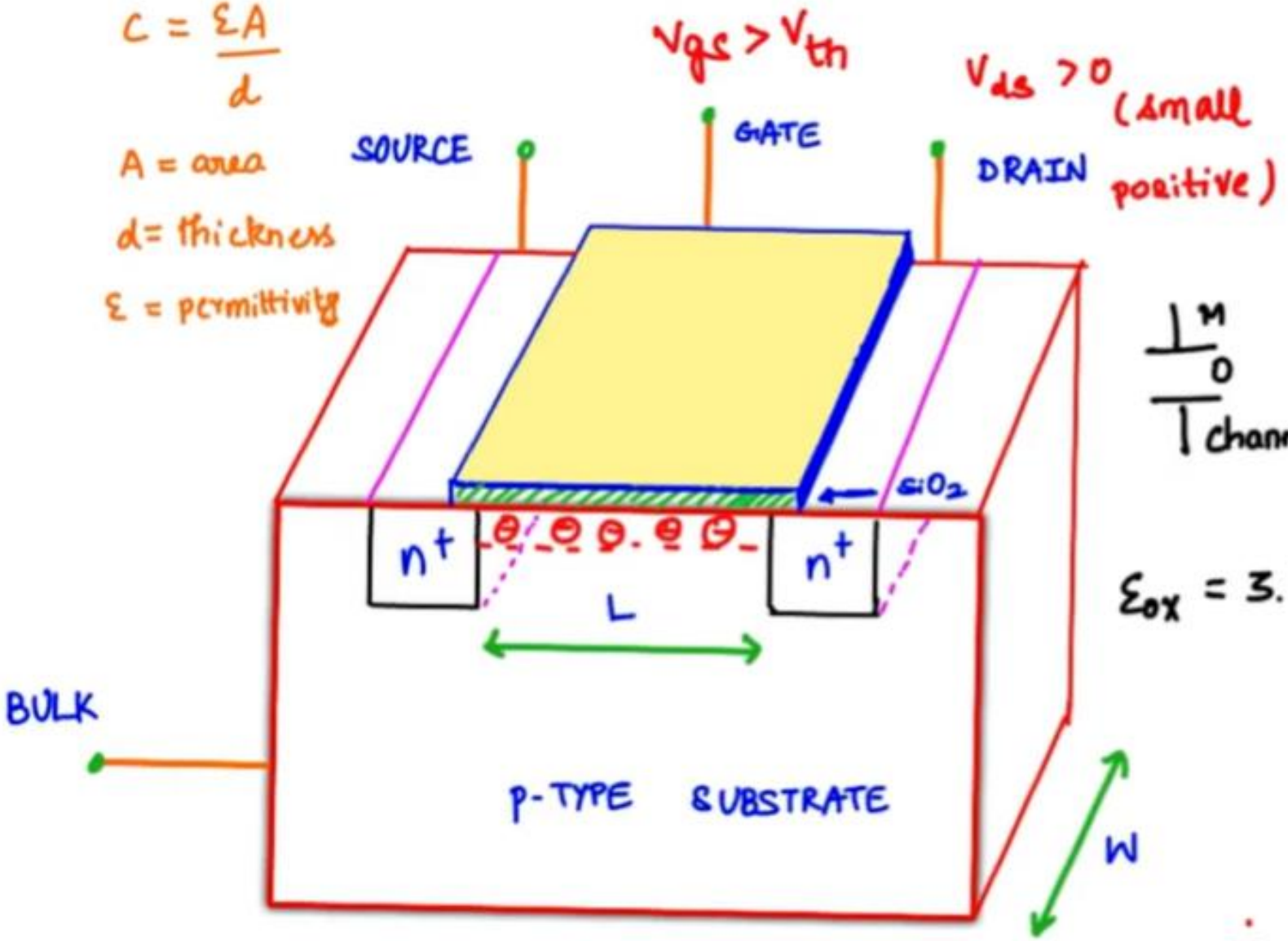
$V_{ds} < V_{dsat}$; $V_{dsat} = V_{gs} - V_t$

$C = \frac{\varepsilon A}{d}$

A = area

d = thickness

ε = permittivity



Gate capacitance:

$C_G = C_{ox} \cdot L \cdot W.$

where $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

Gate to Body, $C_{GB} = C_{ox} W L$

Gate to channel, C_{GC}

C_{GS} C_{GD}

$\varepsilon_{ox} = 3.9\varepsilon_0$

$C_{GC} = C_{GS} + C_{GD}$

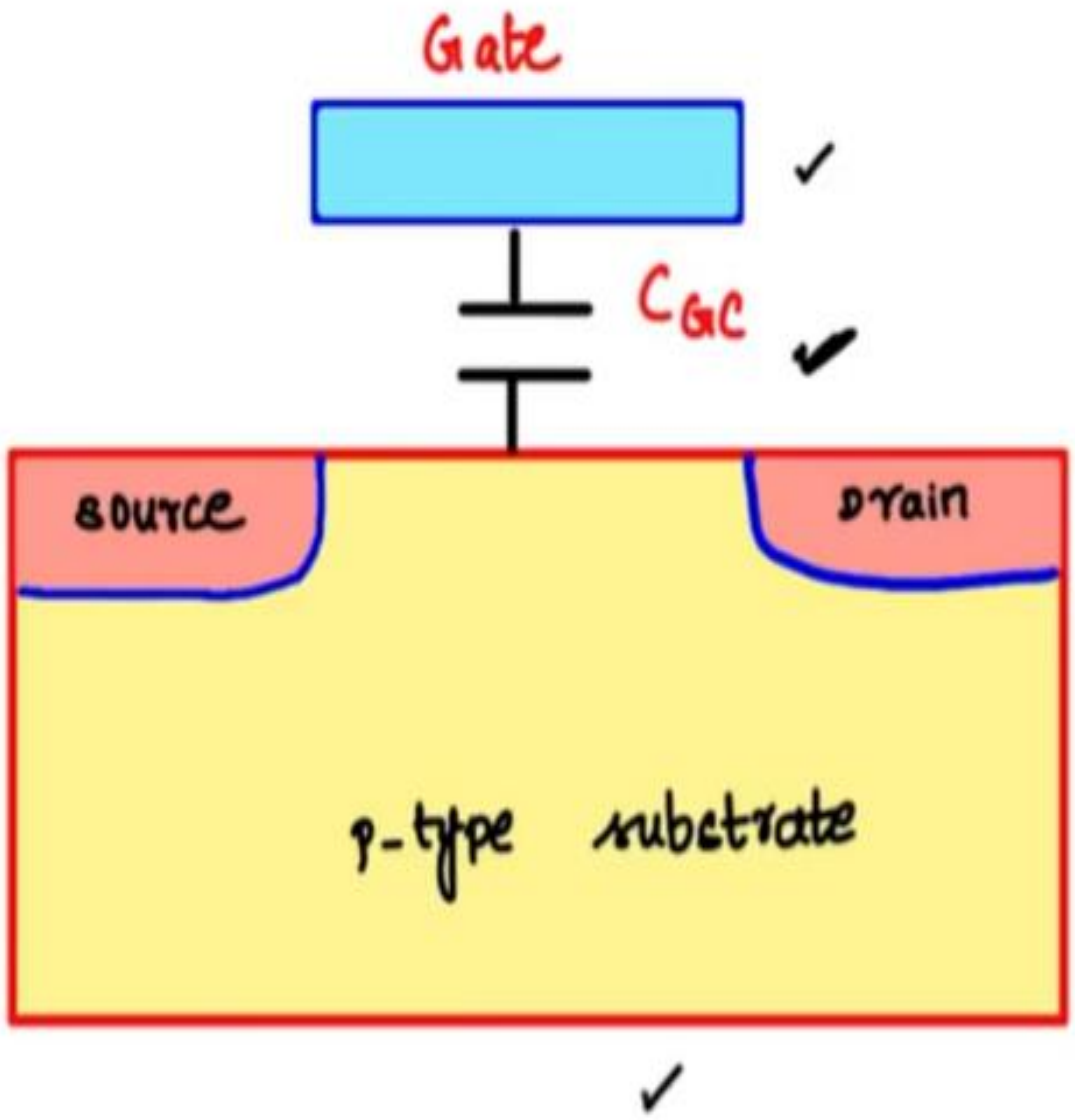
$C_{GC} = C_{ox} W.L$ (Linear)

$\therefore$ $C_{GS} = C_{GD} = \frac{1}{2} C_{ox} W L.$

Capacitance in CUT - OFF REGION:

$V_{gs} < V_{th} \Rightarrow$ CUT-OFF

✓ no channel - formation



$$C_{GB} = C_G = C_{ox} \cdot W \cdot L$$

$$C_{GC} = C_{GS} + C_{GD} = 0$$

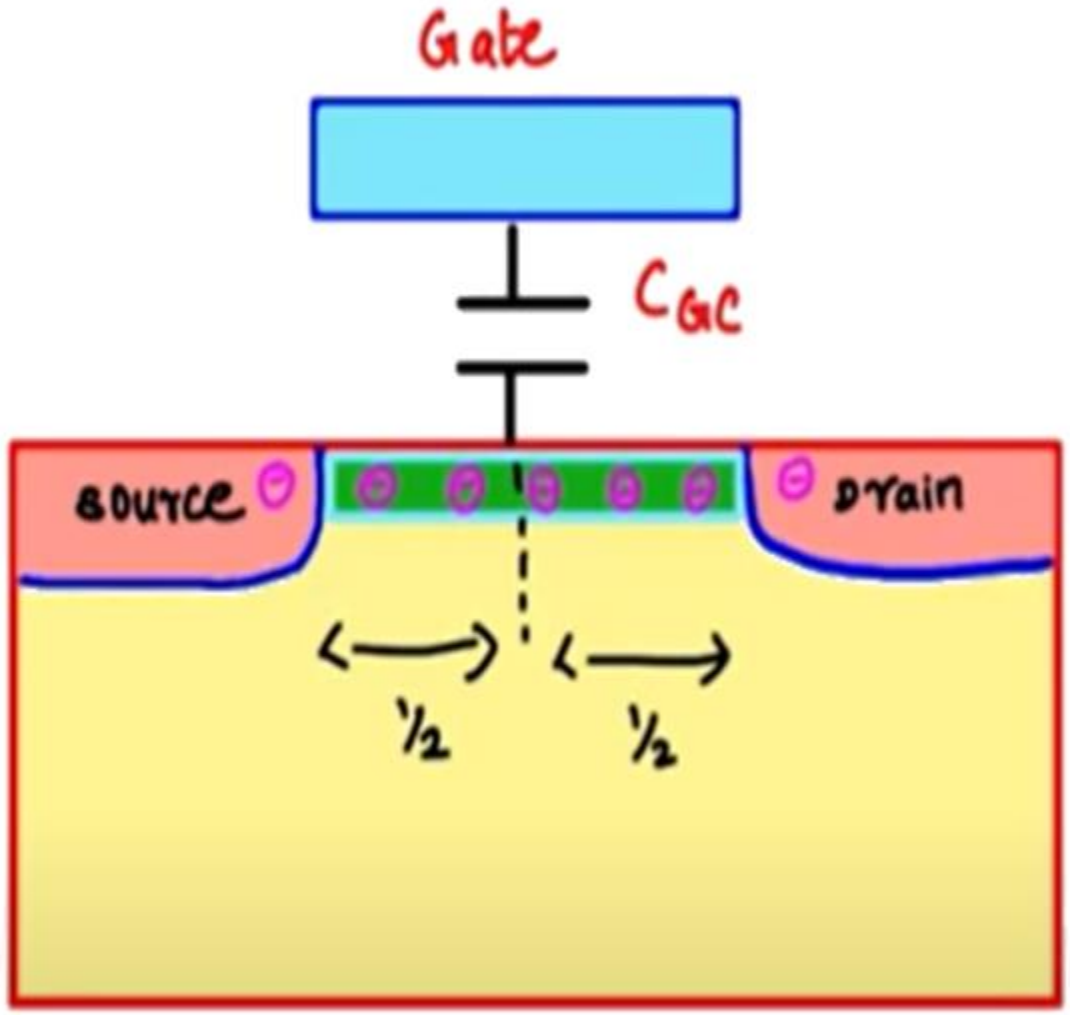
$$C_{GS} = 0$$

$$C_{GD} = 0$$

Capacitance in LINEAR REGION:

$V_{gs} > V_{th}$; $V_{ds} > 0$ and $V_{ds} < V_{dsat}$

Inversion Layer ⇒ channel



$$C_{GB} = 0$$

$$C_{GC} = C_{GS} + C_{GD} = C_G = C_{ox} \cdot W \cdot L$$

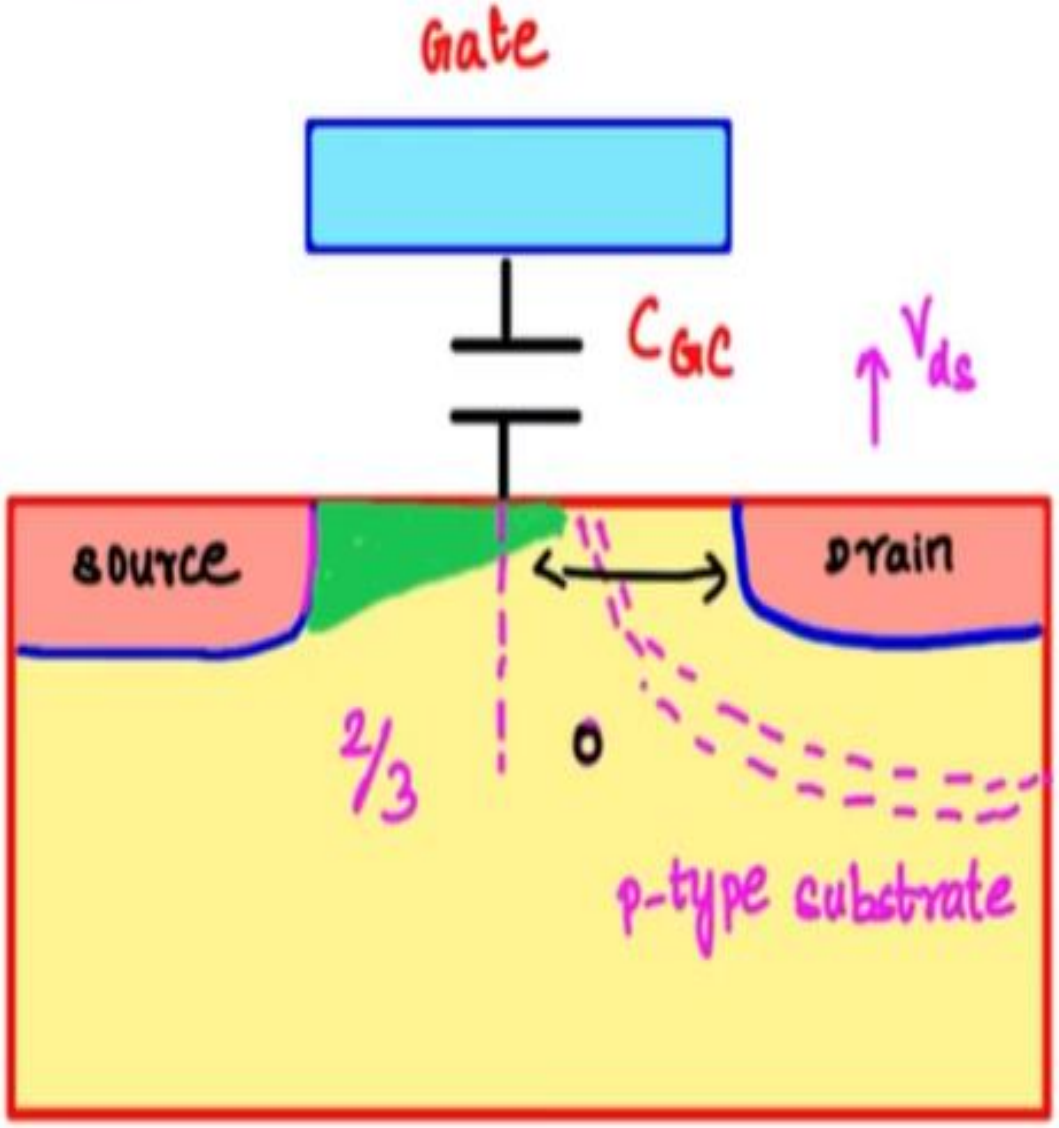
$$C_{GS} = \frac{1}{2} C_{ox} \cdot W \cdot L$$

$$C_{GD} = \frac{1}{2} C_{ox} \cdot W \cdot L$$

Capacitance in SATURATION REGION:

$V_{gs} > V_{th}$; $V_{ds} \geq V_{dsat}$

channel – pinched off



$$C_{GB} = 0$$

$$C_{GC} = C_{GS} + C_{GD} = \frac{2}{3} C_{ox} . W . L$$

$$C_{GS} = \frac{2}{3} C_{ox} . W . L$$

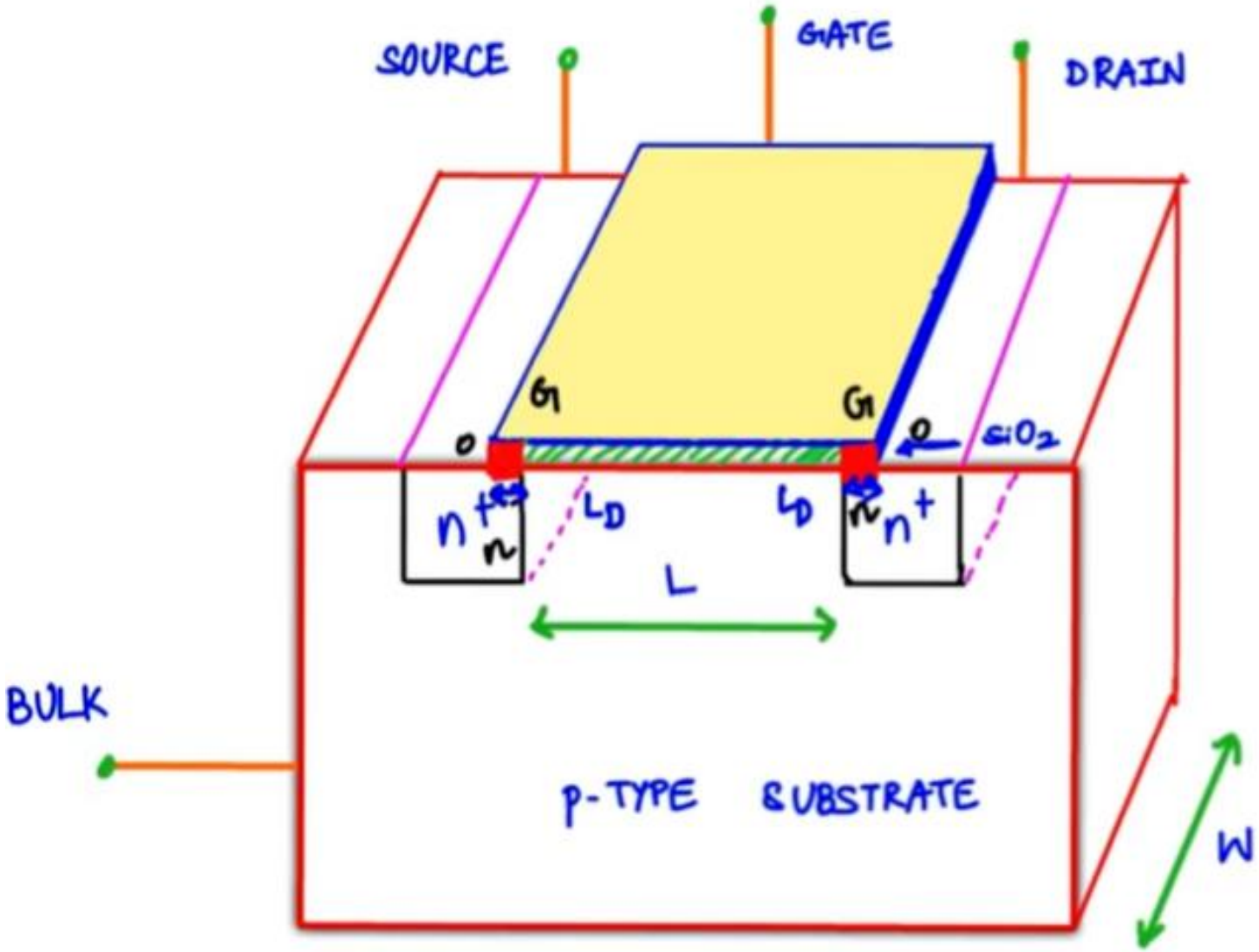
$$C_{GD} = 0$$

Capacitance in three regions of operation of MOS Transistor

CAPACITANCE	CUT-OFF	LINEAR	SATURATION
C_{GB}	$C_{ox}WL$	0	0
$C_{GC} = C_{GS} + C_{GD}$	0	$C_{ox}WL$	$2/3[C_{ox}WL]$
C_{GS}	0	$1/2[C_{ox}WL]$	$2/3[C_{ox}WL]$
C_{GD}	0	$1/2[C_{ox}WL]$	0

OVERLAP CAPACITANCES:

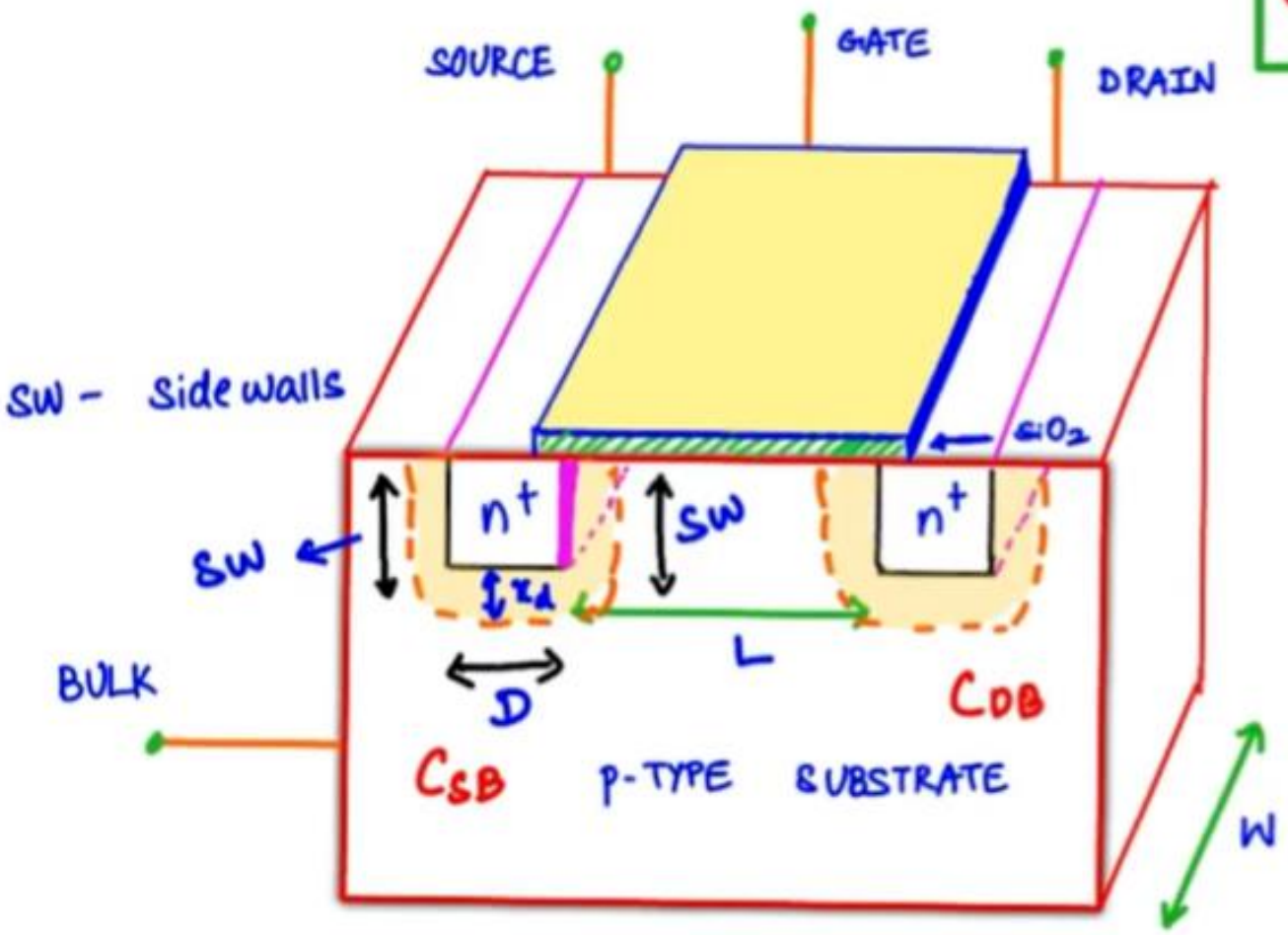
L_D = Lateral Diffusion length



C_{gs} (overlap) = $C_{ox} \cdot W \cdot L_D$

C_{gd} (overlap) = $C_{ox} \cdot W \cdot L_D$

DIFFUSION CAPACITANCE MODEL



$$C_{sb} = AS \times C_{jbs} + PS \times C_{jbssw}$$

where $AS = D \times W$

$PS = 2(D + W) = 2D + 2W$

Having, one sidewall facing the channel & in contact with gate

$PS = D + D + W = 2D + W.$

C_{jbs} = junction capacitance between bulk and bottom of source (F/cm^2)

C_{jbssw} = junction capacitance between bulk and sidewalls of source (F/cm)

$$C_{jbs} = C_J \left[1 + \frac{V_{sb}}{\psi_0} \right]^{-M_J}$$

where ; C_J = Junction capacitance @ zero bias

M_J = Junction grading coefficient (0.5 to 0.33)

ψ_0 = Built-in potential $= V_T \ln \left(\frac{N_A N_D}{n_i^2} \right)$

SIDEWALL CAPACITANCE:

$$C_{jbssw} = C_{JSW}\left[1 + \frac{V_{sb}}{\psi_{sw}}\right]^{-M_{JSW}}$$

SIDEWALL CAPACITANCE IN COMMON TO GATE & CHANNEL:

$$C_{jbsswg} = C_{JSWG}\left[1 + \frac{V_{sb}}{\psi_{swg}}\right]^{-M_{JSWG}}$$

AT ZERO BIAS:

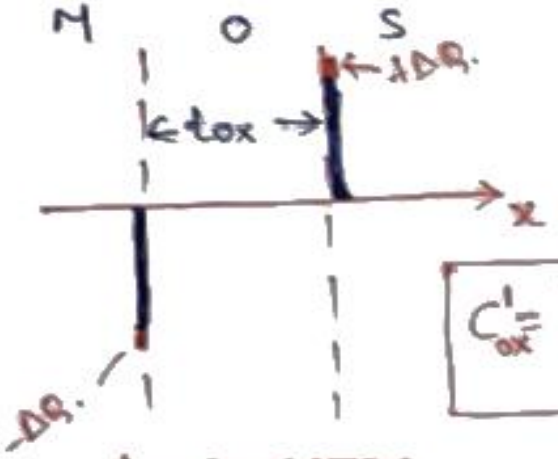
$\Rightarrow$ $C_{jbs} = C_J$; $C_{jbssw} = C_{JSW}$; $C_{jbsswg} = C_{JSWG}$

ALSO $\boxed{C_{DB} \approx C_{SB}}$ (Because of symmetrical structure)

C-V Characteristics

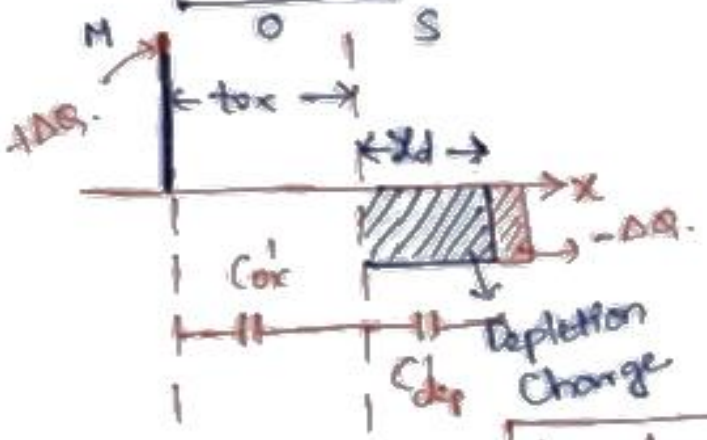
$V + \Delta V$ $\quad$ $Q + \Delta Q$

$$C = \frac{\Delta Q}{\Delta V}$$



$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

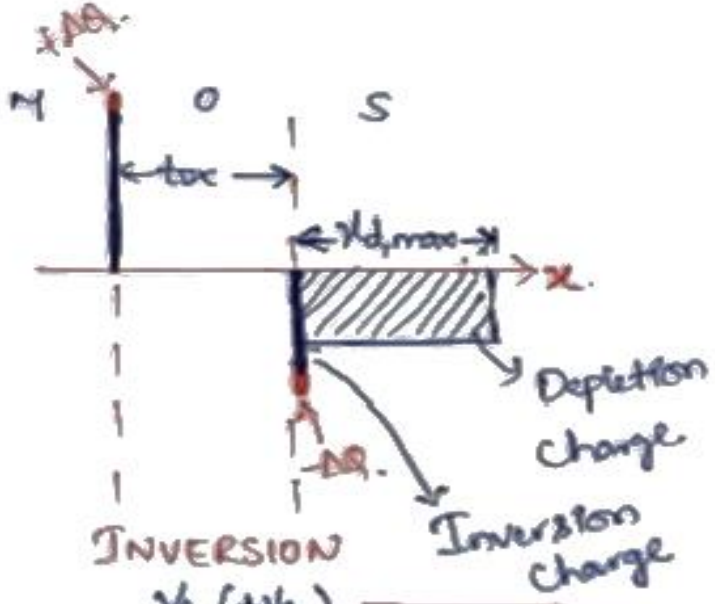
ACCUMULATION
V_G (−ve)



DEPLETION
V_G (+ve Small)

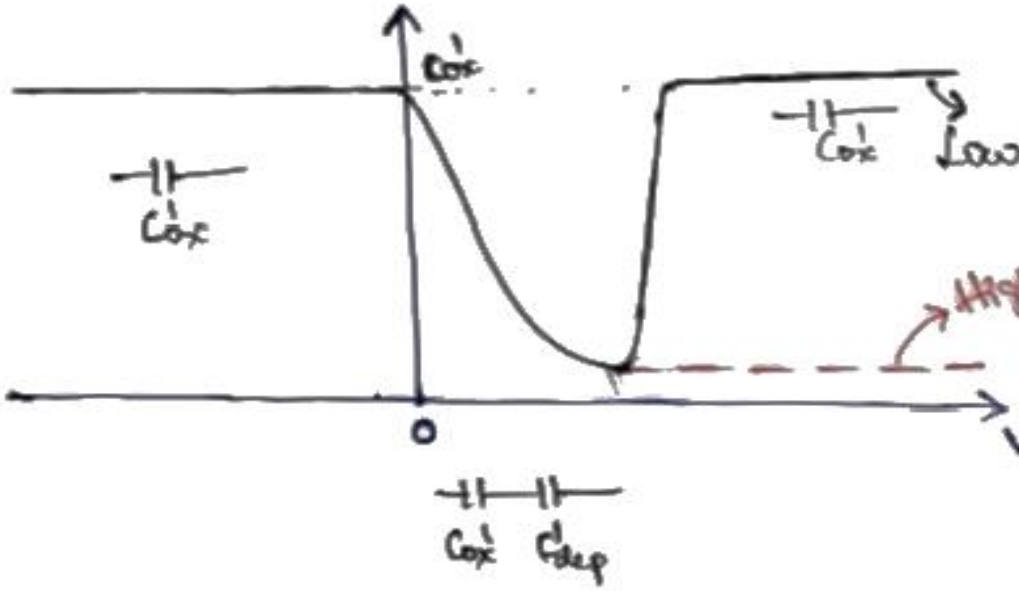
$$\frac{1}{C'} = \frac{1}{C'_{ox}} + \frac{1}{C'_{dep}}$$

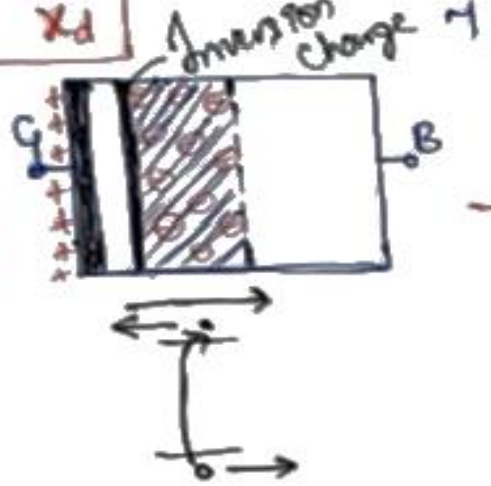
$$C'_{dep} = \frac{\varepsilon_{si}}{X_d}$$

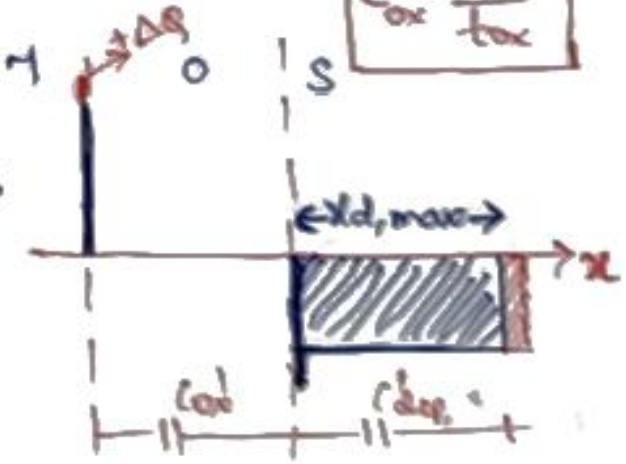


INVERSION
V_G (+ve)

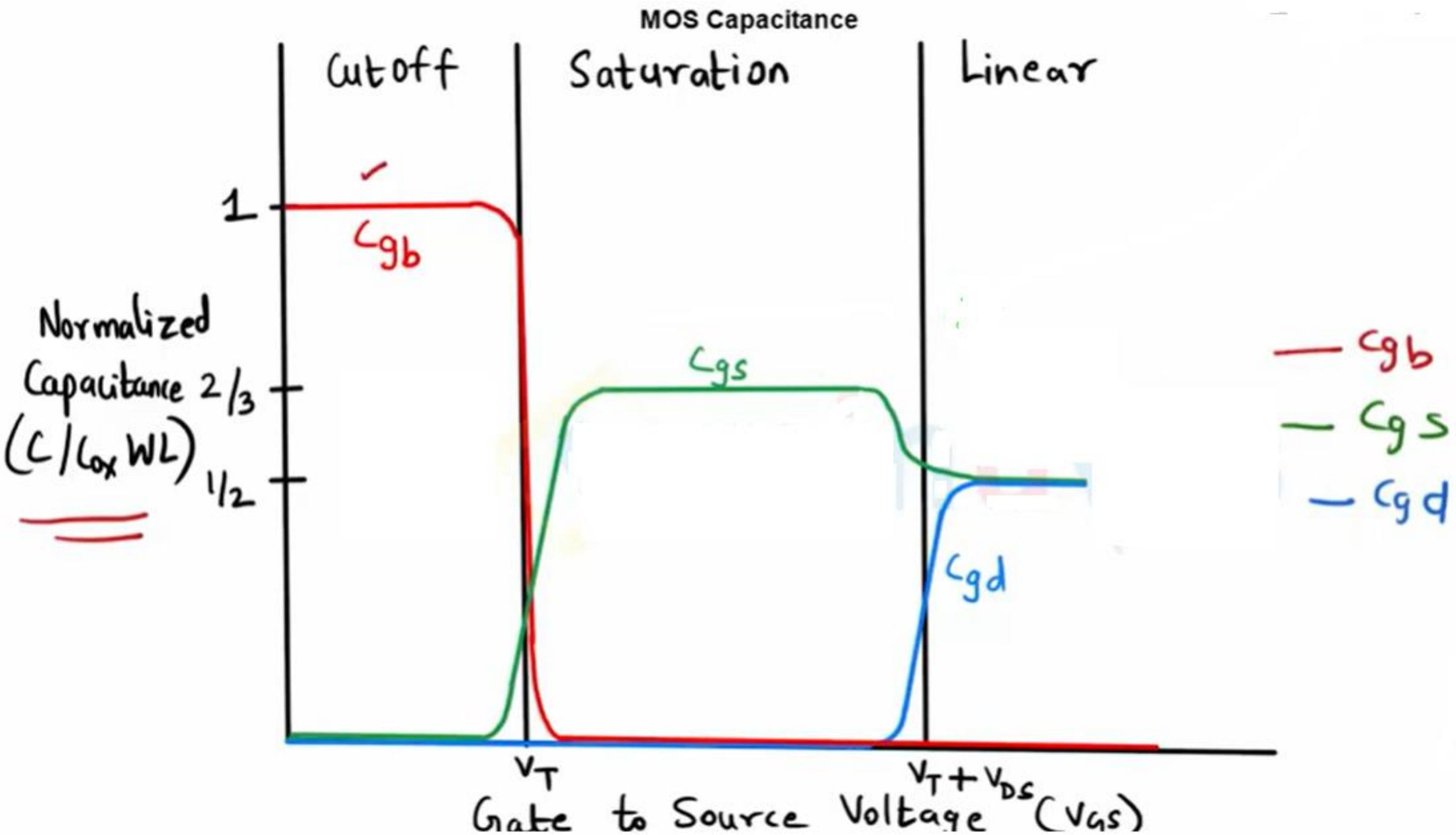
$$C'_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$



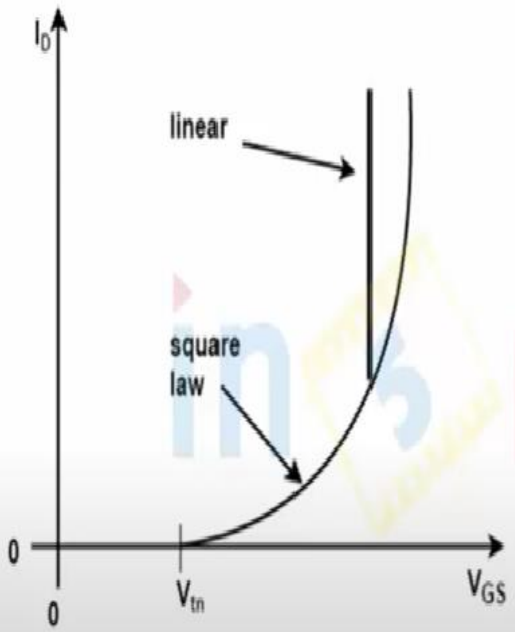




$$\frac{1}{C'} = \frac{1}{C'_{ox}} + \frac{1}{C'_{dep}(X_{d,max})}$$


MOS Capacitance
Cutoff
Saturation
Linear
1
2/3
1/2
Normalized Capacitance (C/Cox WL)
Cgb
Cgs
Cgd
VT
VT+VDS
Gate to Source Voltage (Vgs)
Cgb
Cgs
Cgd

Non Ideal Effects -Velocity Saturation



$$I_{D,sat} = \frac{\mu_n C_{ox} W}{2L} \frac{(V_{gs}-V_{tn})^2}{\left(1+\frac{V_{gs}-V_{tn}}{LE_c}\right)}$$

$$1 + \frac{(V_{gs}-V_{tn})}{LE_c}$$

$$v_d = \frac{\mu E_{lat}}{1+\left(\frac{E_{lat}}{LE_c}\right)}$$

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \frac{(V_{gs}-V_{tn})^2}{1+\frac{(v_{gs}-V_{tn})}{LE_c}}$$

$$I_{D,sat} = \frac{\mu_n C_{ox}}{2} \frac{W E_c (V_{gs}-V_{tn})^2 / L}{1+(V_{gs}-V_{tn})}$$

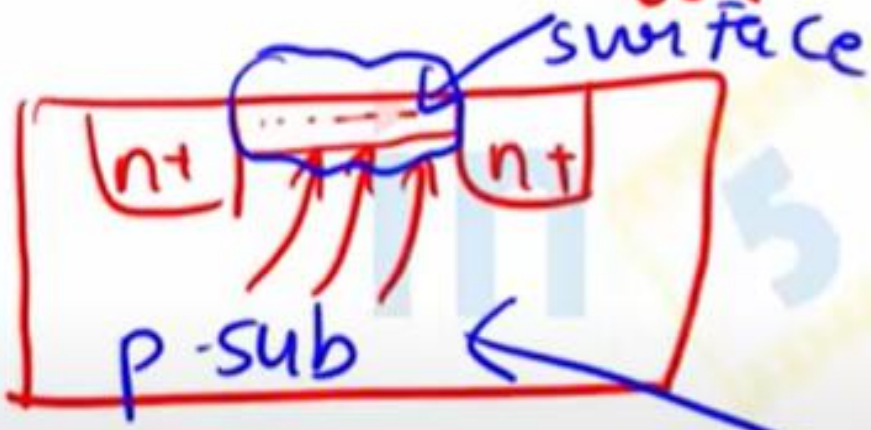
$$E_{lat} = V_{DS}/L \;;$$

$$E_{ver} = V_{gs}/t_{ox} \;;$$

Non Ideal Effects - Mobility Degradation

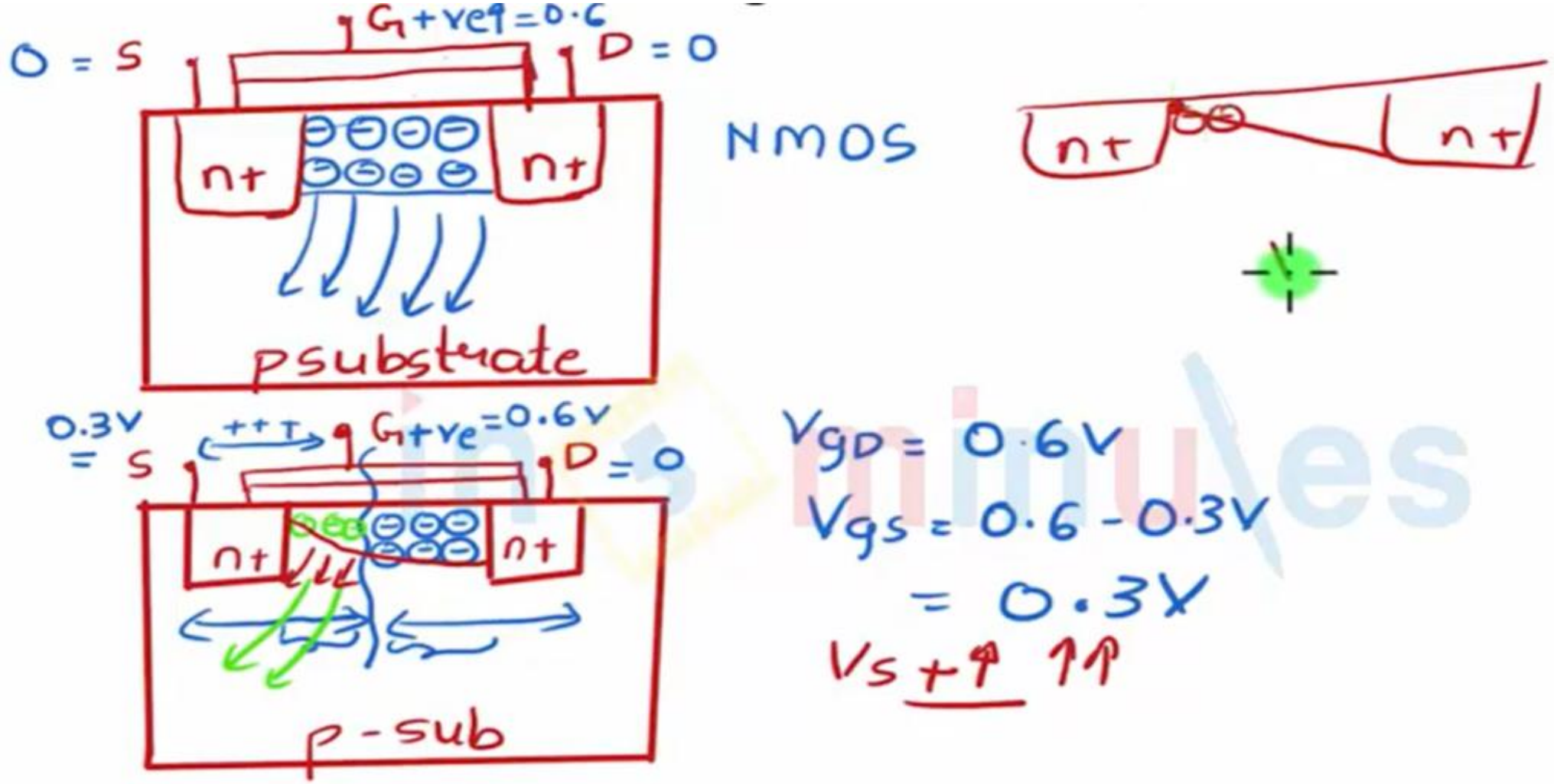
$E_{ver} = \frac{V_{gs}\uparrow}{t_{ox}}$;

$V_{gs} \ldots\ldots \uparrow +ve$



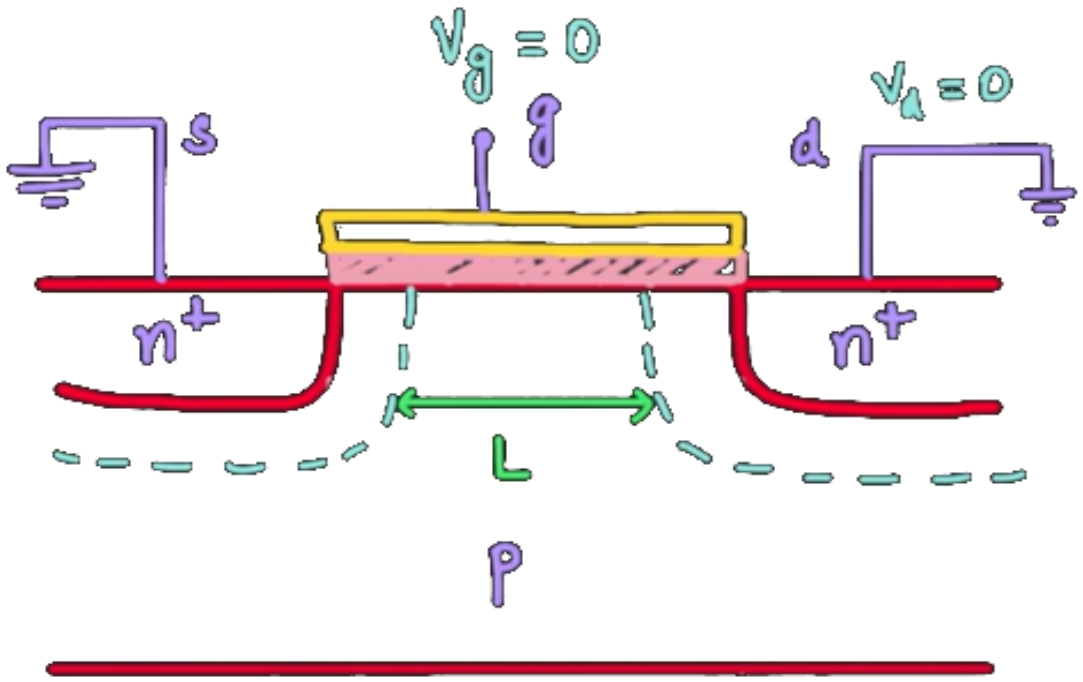
$$\mu_n = \frac{\mu_{no}}{1+\eta(V_{gs}-V_{tn})}$$

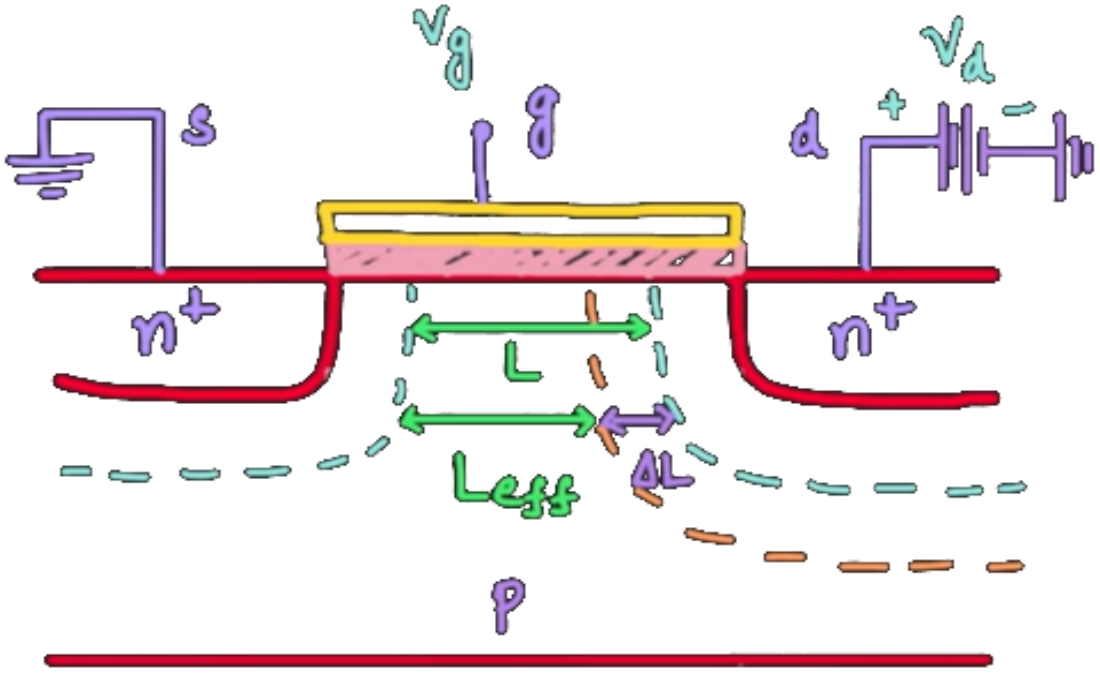
Non Ideal Effects - Channel Length Modulation



Channel Length Modulation

CHANNEL LENGTH MODULATION (CLM)





$$L_{eff} = L - \Delta L$$

$\Delta L \uparrow$ when $V_{ds} \uparrow$

$\therefore \Delta L \propto V_{ds}$ $\therefore \Delta L \approx \lambda' V_{ds}$

Channel Length Modulation

As V_{ds} is very large; N - channel transistor is in Saturation Region

$$I_{ds,n} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{gs} - V_{th,n})^2$$

$$L_{eff} = L - \Delta L;$$

$$\therefore L_{eff} = L - \Delta L = L\left(1 - \frac{\Delta L}{L}\right)$$

$$I_{ds,n} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L\left(1 - \frac{\Delta L}{L}\right)}(V_{gs} - V_{th,n})^2$$

$$\therefore I_{ds,n} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th,n})^2 \times \left(1 - \frac{\Delta L}{L}\right)^{-1}$$

Channel Length Modulation

$$\therefore I_{ds,n} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th,n})^2 \times \left(1 - \frac{\Delta L}{L}\right)^{-1}$$

ΔL is always smaller than 'L'

$$\therefore \left(1 - \frac{\Delta L}{L}\right)^{-1} \approx (1 - x)^{-1}$$

$$(1 - x)^{-1} = 1 + x + x^2 + \dots$$

'x' less than 1 $\rightarrow$ we always neglect the higher order terms

Channel Length Modulation

$$\left(1 - \frac{\Delta L}{L}\right)^{-1} \approx 1 + \frac{\Delta L}{L}$$

$$\therefore I_{ds,n} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th,n})^2\left(1 + \frac{\Delta L}{L}\right)$$

$$\Delta L \approx \lambda' V_{ds} \quad \therefore \frac{\Delta L}{L} \approx \frac{\lambda'}{L} V_{ds} \quad \therefore \frac{\Delta L}{L} \approx \lambda V_{ds}$$

$$I_{ds,n} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th,n})^2(1 + \lambda V_{ds})$$

Channel Length Modulation

Drain Resistance : $\downarrow \quad R = \frac{\rho L}{A} \downarrow$

$$\because \quad I_{ds}' = \underbrace{\frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th,n})^2}_{I_{ds}} (1 + \lambda V_{ds})$$

$$I_{ds}' = I_{ds} (1 + \lambda V_{ds})$$

with CLM

without CLM

Channel Length Modulation

Drain Resistance :

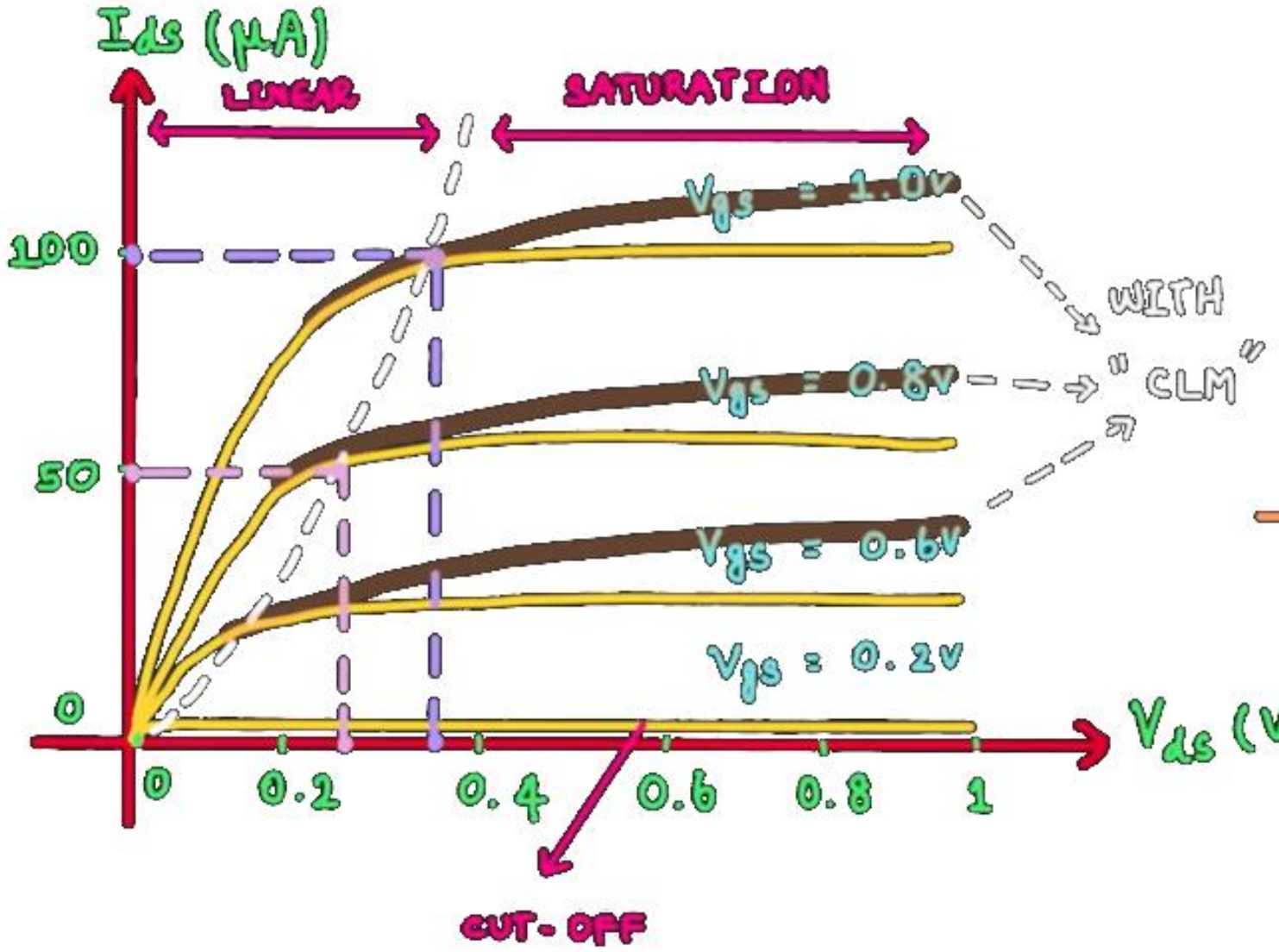
$$I_{ds}' = I_{ds}\,(1 + \lambda V_{ds})$$

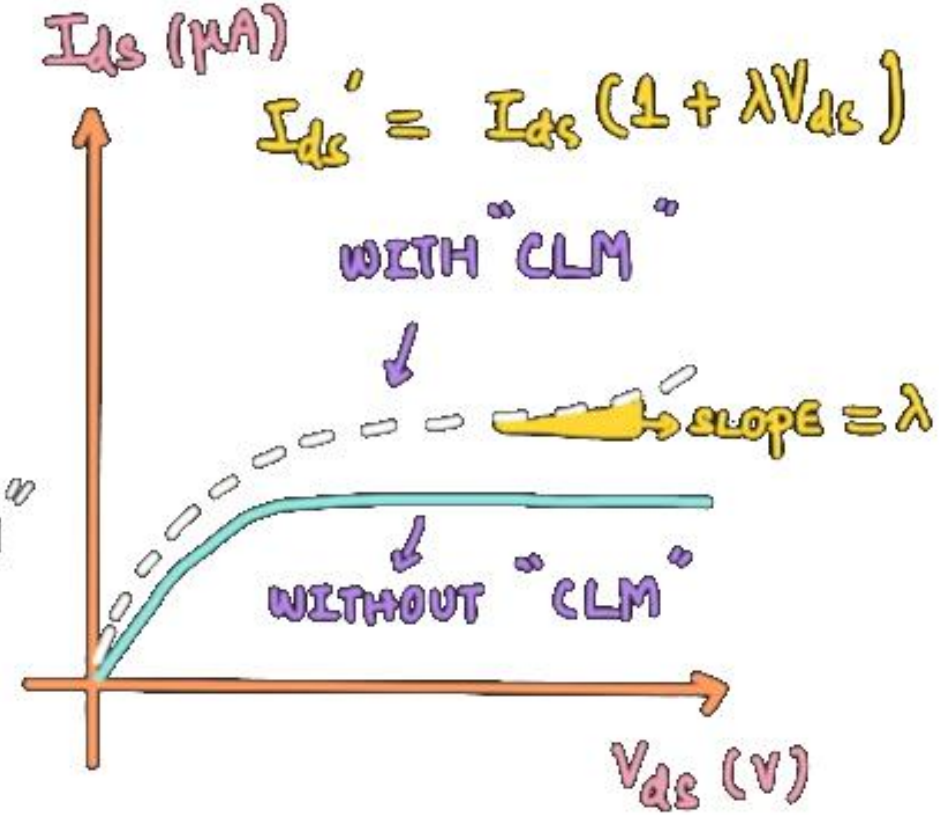
$$\therefore\ r_d = \frac{\partial V_{ds}}{\partial I_{ds}'} \qquad \text{now;} \quad \frac{1}{r_d} = \frac{\partial I_{ds}'}{\partial V_{ds}}$$

$$\therefore\ \frac{1}{r_d} = \frac{\partial}{\partial V_{ds}}\left[I_{ds}\,(1 + \lambda V_{ds})\right] = \lambda I_{ds}$$

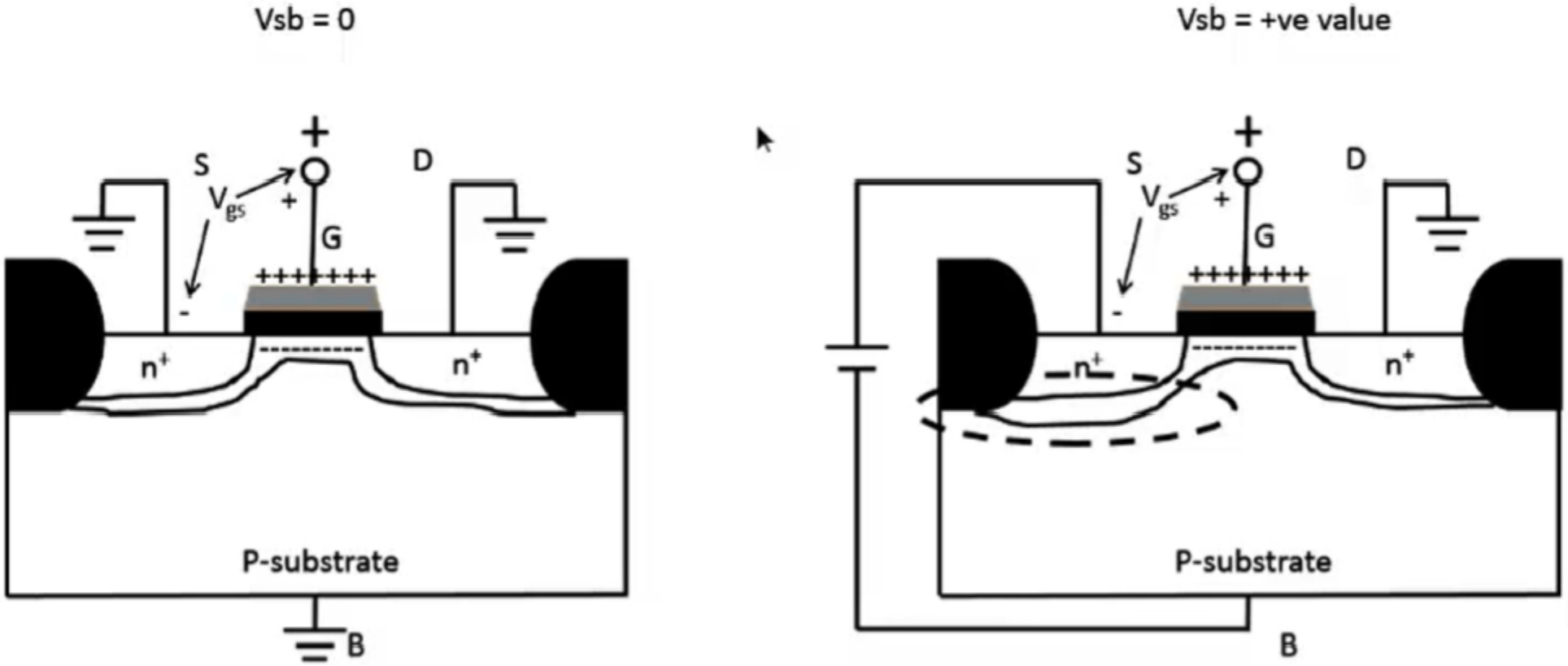
$$\therefore\ r_d = \frac{1}{\lambda I_{ds}} = \frac{1}{\lambda/2\ \mu_n C_{ox}\ \frac{W}{L}\ (V_{gs} - V_{th,n})^2}$$

I - V Characteristics of nMOS Transistor





Non Ideal Effects - BODY Effect



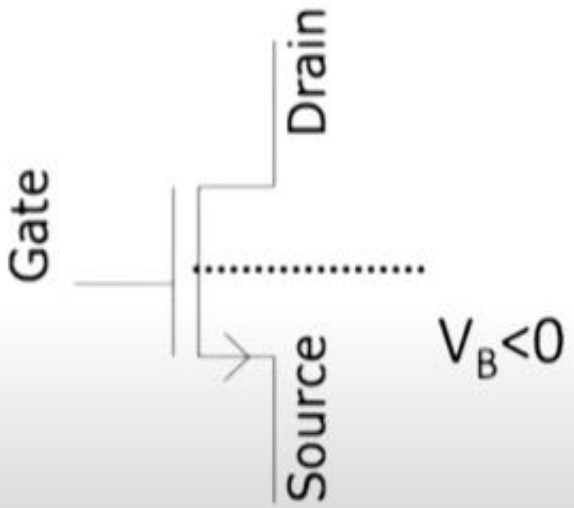
Additional Reverse bias between source 'S' and substrate (or Bulk) 'B'
Therefore, depletion layer width is slightly high near 'S'

BODY Effect

- What happen if the body bias is applied?

➢ To keep the source and drain junctions remain reverse biased, we applied body voltage $V_B<0$.

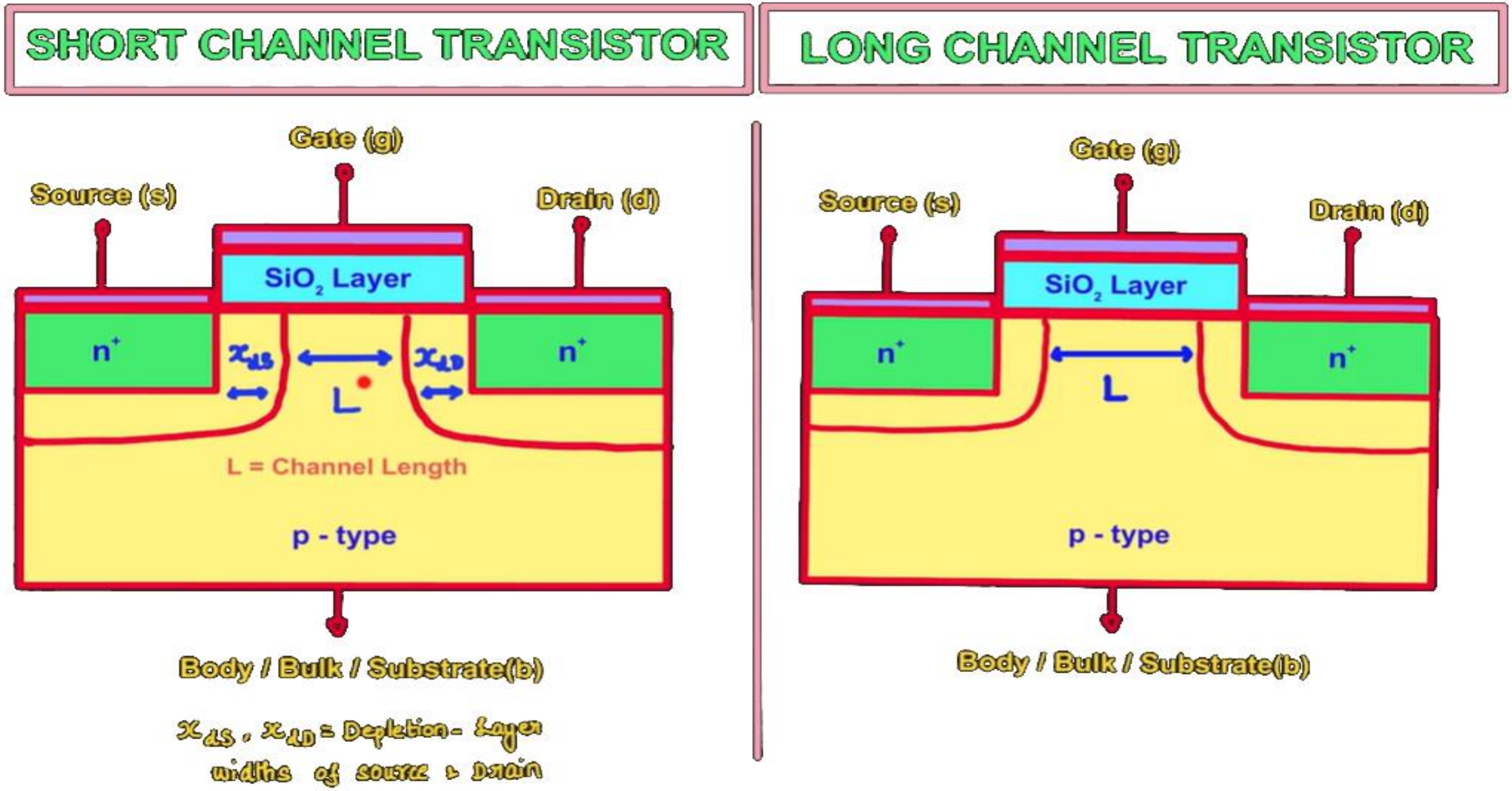
○ This decreases the impact of gate-bias and hence increases the threshold voltage.



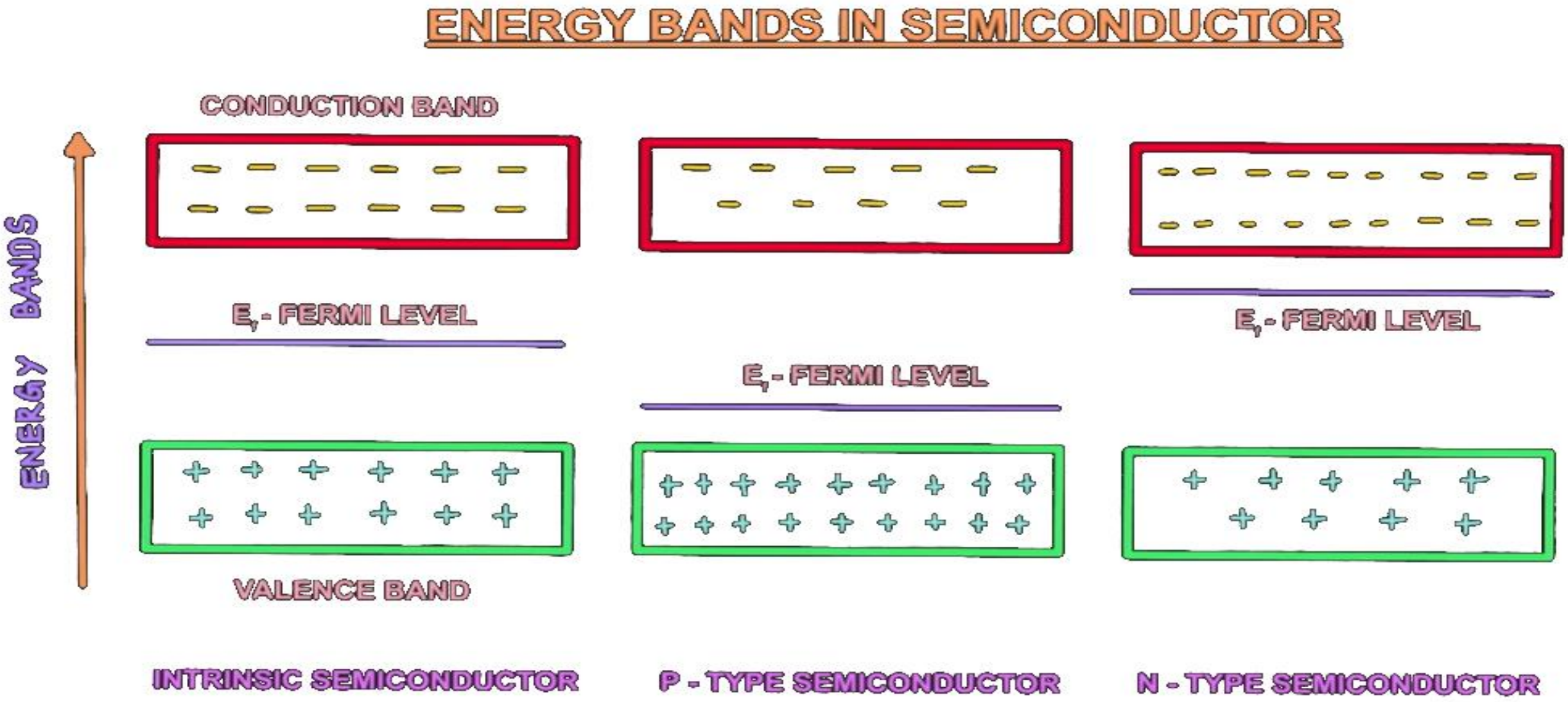
$$V_T = V_{TH} + \gamma\left(\sqrt{\left|2\Phi_F + V_{SB}\right|} - \sqrt{\left|2\Phi_F\right|}\right)$$

where $\gamma = \frac{\sqrt{2\varepsilon q N_{sub}}}{C_{ox}}$ is body coefficient and V_{SB} is source-body potential.

Drain Induced Barrier Lowering(DIBL)

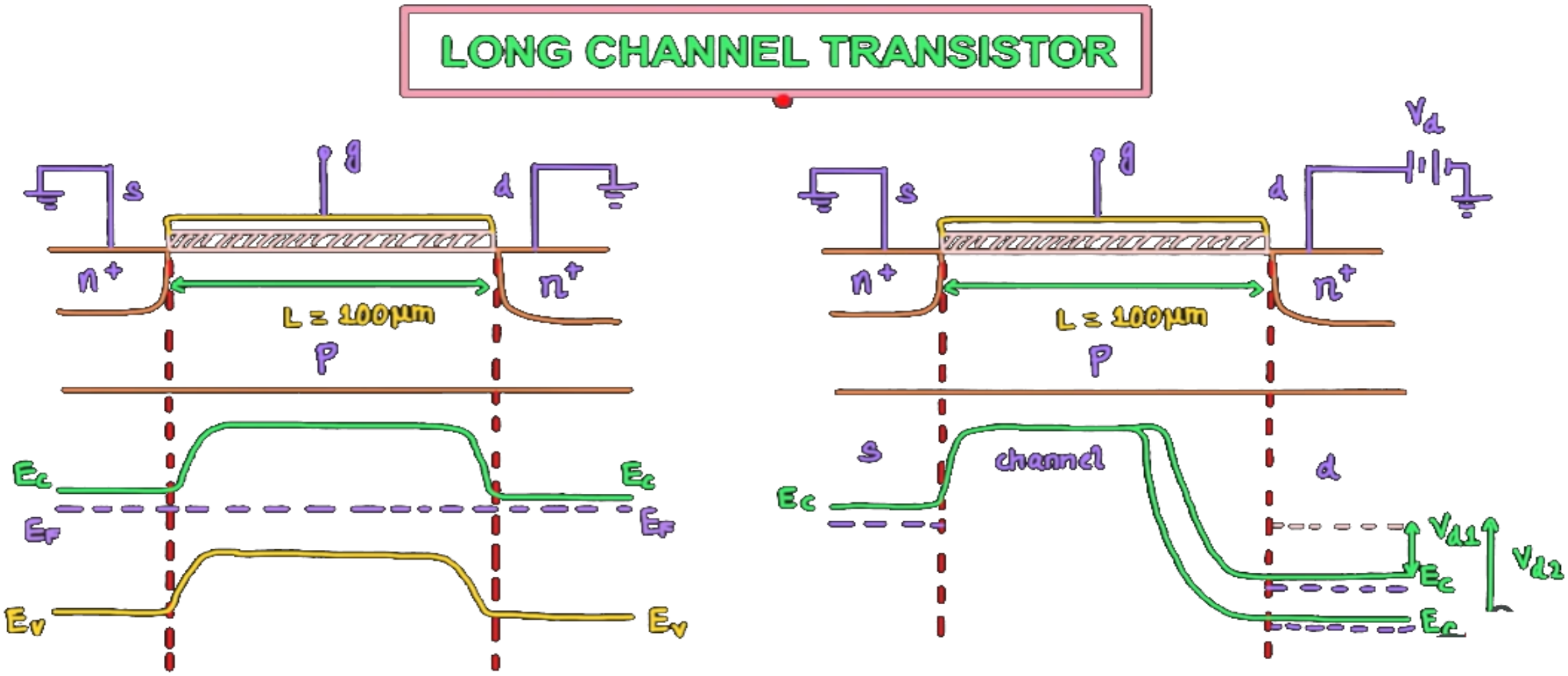


Drain Induced Barrier Lowering(DIBL)

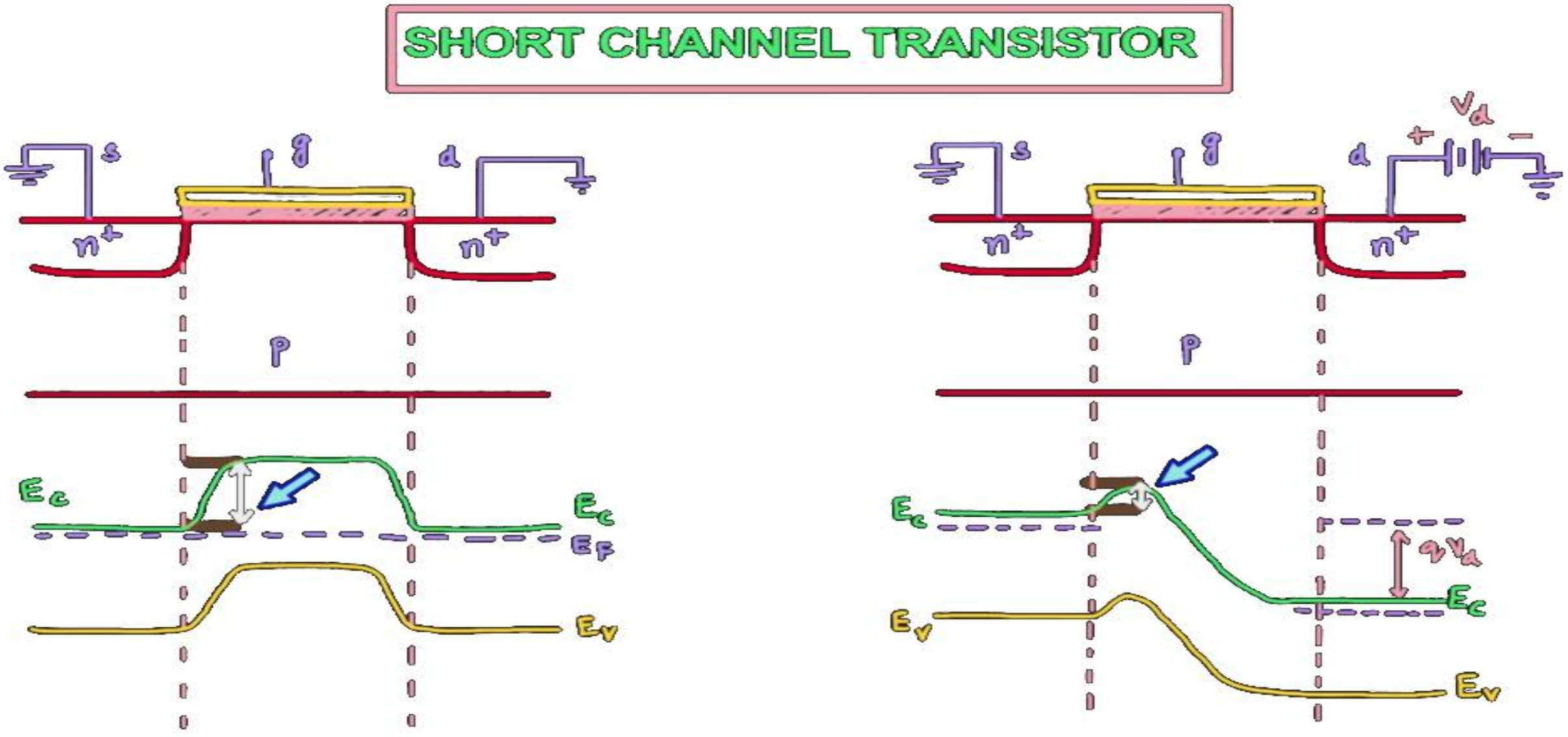


E

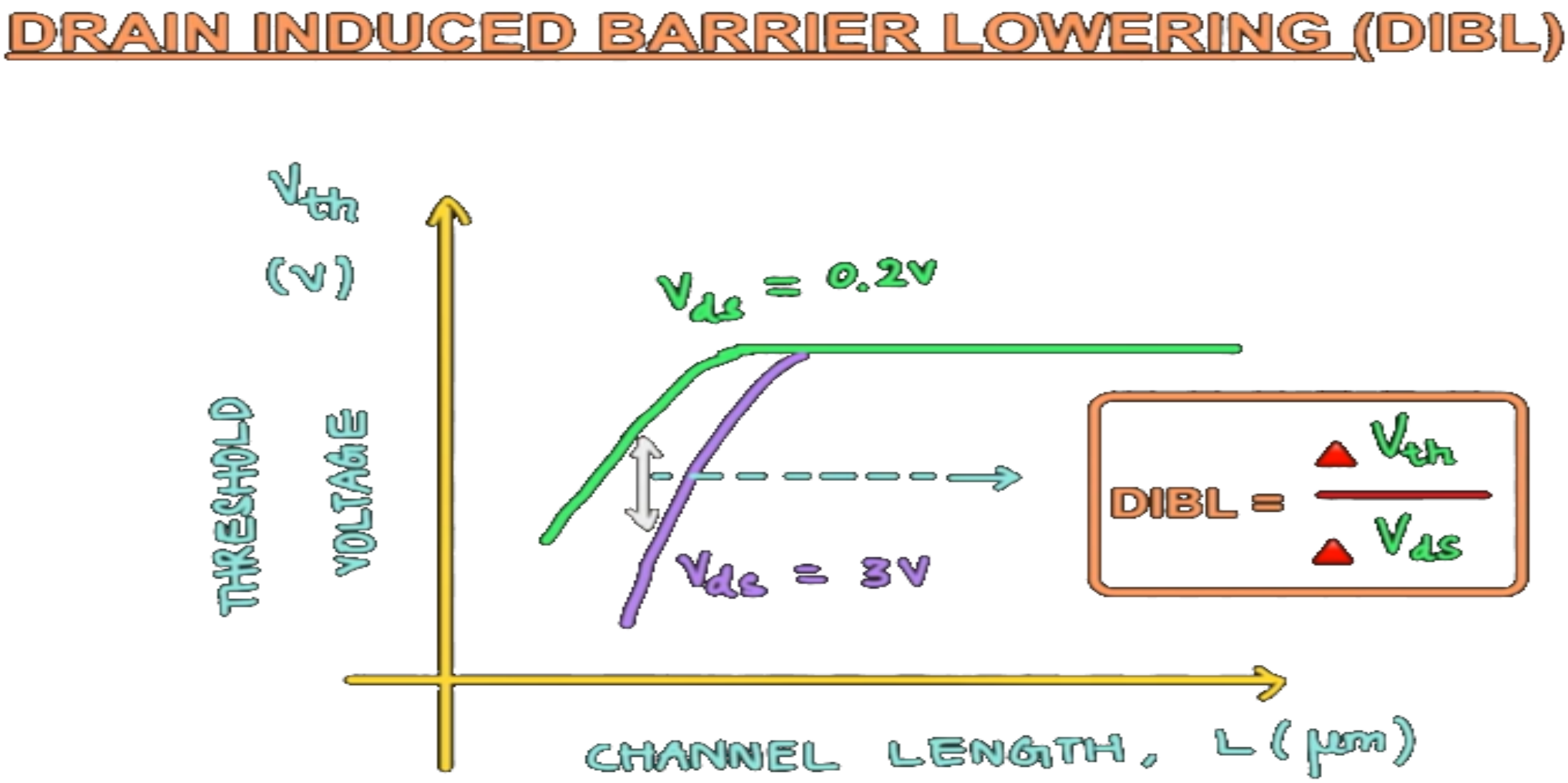
Drain Induced Barrier Lowering(DIBL)



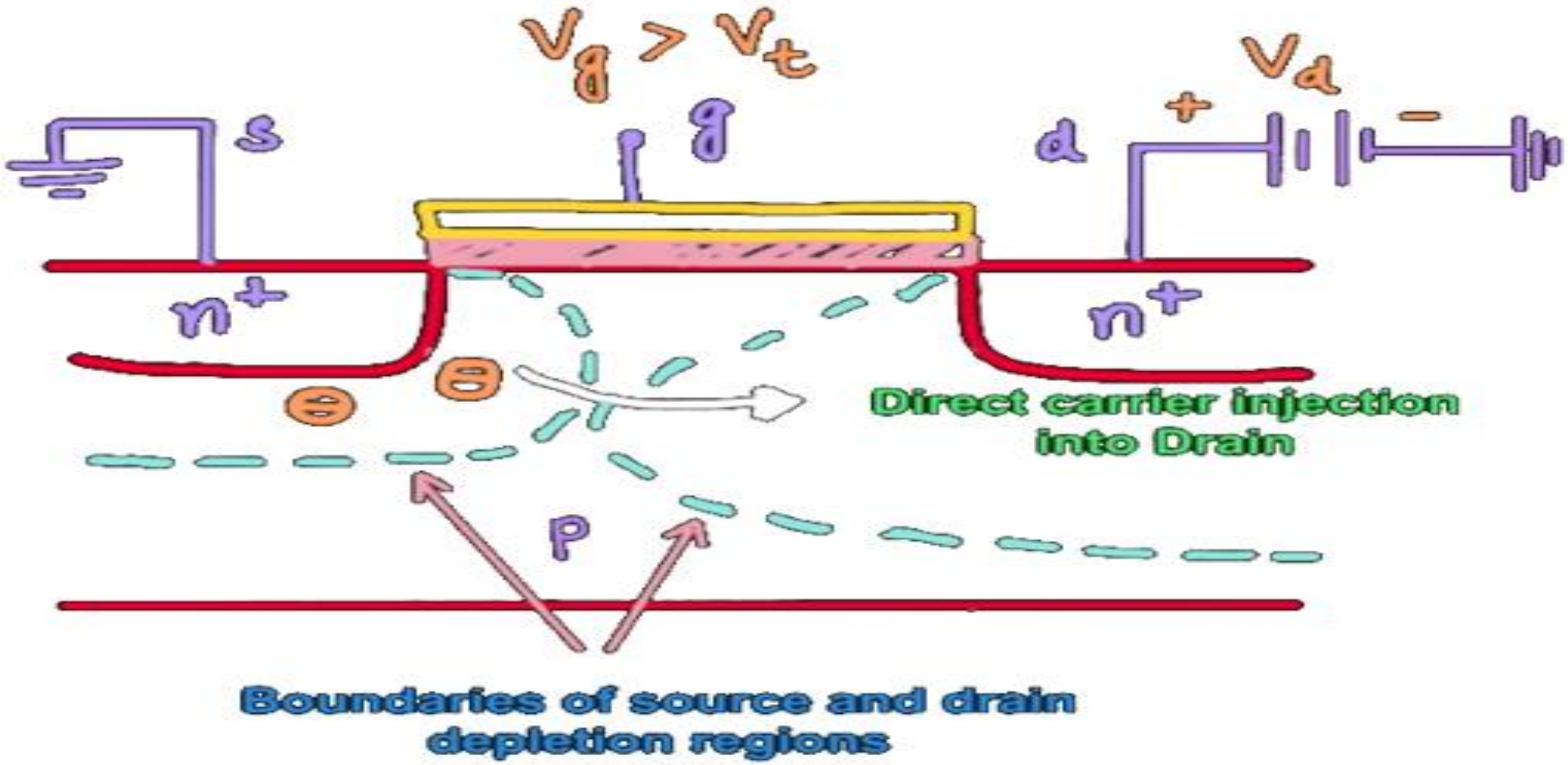
Drain Induced Barrier Lowering(DIBL)



Drain Induced Barrier Lowering(DIBL)



PUNCH THROUGH EFFECT



SCALING: REDUCING PHYSICAL DIMESIONS KEEPING GEOMENTRICAL RATIOS SAME

- **ADVANTAGES**

❖ **PACKAGING DENSITY (↑)**

❖ **SIZE CHIP(↓)**

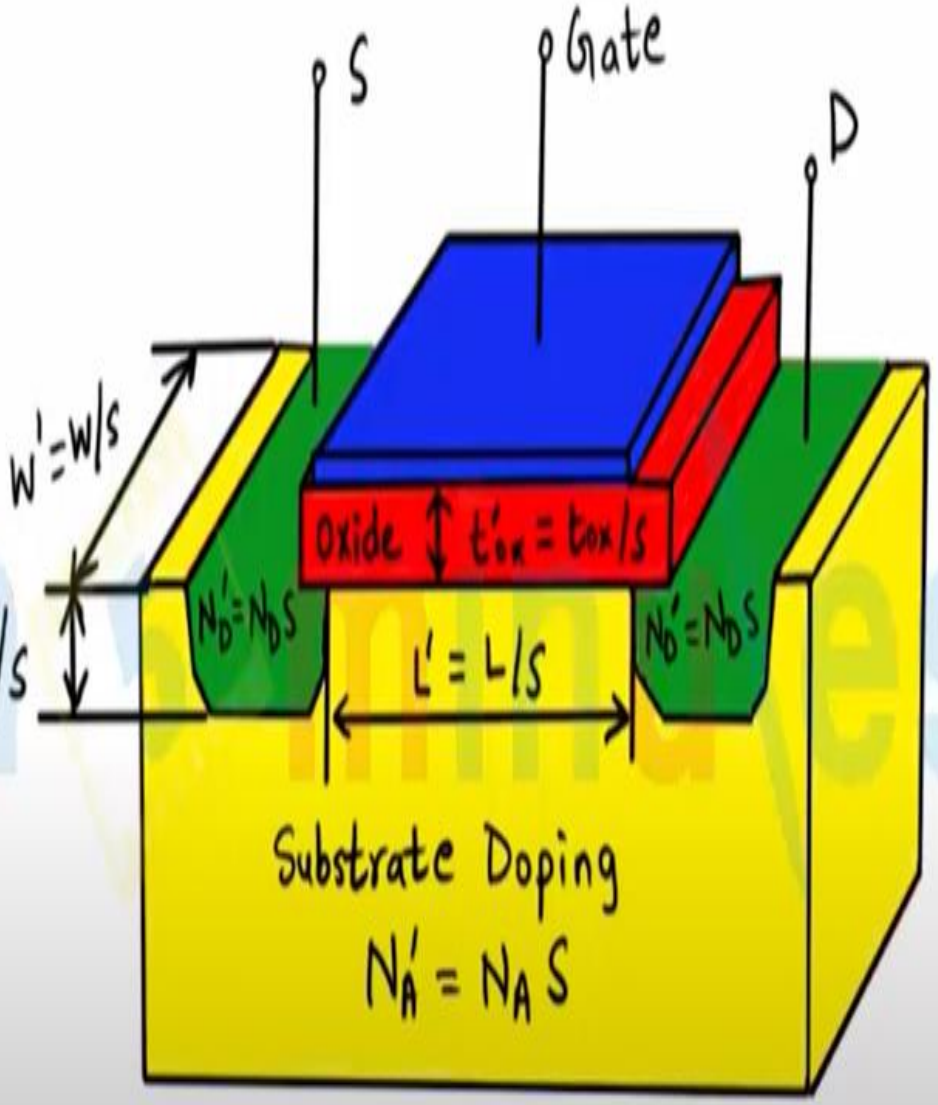
❖ **MULTIFUCNTION CHIP**

TYPES OF SCALING

➢ **CONSTANT FILED SCALING (FS)**

➢ **CONSTANT VOLTAGE SCALING(PS)**

Constant Field Scaling



a) Oxide capacitance (C_{ox}):

$$C_{ox} = \epsilon_{ox}/t_{ox}$$

$$C'_{ox} = \epsilon_{ox}/t'_{ox} \qquad \because t'_{ox} = \frac{t_{ox}}{s}$$

$$C'_{ox} = s\,\epsilon_{ox}/t_{ox}$$

$$\boxed{C'_{ox} = s\,C_{ox}}$$

b) Gate capacitance (C_g):

$$C_g = C_{ox}.\,W.\,L$$

$$C'_g = C'_{ox}.\,W'.\,L' \qquad \left(\because C'_{ox} = sC_{ox},\ W', L' = \frac{W}{s}, \frac{L}{s}\right)$$

$$= s.\,C_{ox}.\,\frac{W.L}{s^2}$$

$$\boxed{C'_g = C_g/s}$$

c) Current in linear region: ($I_{D,linear}$)

$$I_{D,(linear)} = \frac{\mu_n.C_{ox}}{2}\frac{W}{L}\left[2(V_{gs}-V_{tn})V_{DS} - V_{DS}^2\right]$$

$$C'_{ox} = sC_{ox};\ W', L' = \frac{W}{s}, \frac{L}{s},\ V' = V/s$$

$$I'_{D}(linear) = \frac{\mu_n}{2}.\,s.\,C_{ox}.\,\frac{W}{L}\left[2\left(\frac{V_{gs}}{s}-\frac{V_{tn}}{s}\right)\frac{V_{DS}}{s}-\frac{V_{DS}^2}{s^2}\right]$$

$$= \frac{s.\,I_D(linear)}{s^2} = \frac{I_{D,linear}}{s}$$

d) Current in saturation region ($I_{D,sat}$)

$$I_{D,(sat)} = \frac{\mu_n . C_{ox}}{2} \frac{W}{L} \left(V_{gs} - V_{tn} \right)^2$$

$$= \frac{s . C_{ox} \mu_n}{2} \frac{W}{L} \left(\frac{V_{gs}}{s} - \frac{V_{tn}}{s} \right)^2$$

$$I_D'(sat) = \frac{I_{D,(sat)} . \cancel{s}}{s^{\cancel{2}}}$$

$$= \frac{I_{D,sat}}{s}$$

f) Static P.D. or Instantaneous Power Dissipation:

$$\Downarrow \qquad\qquad \Downarrow$$

$$V_{DD} . I_D \qquad\qquad V_{DS} . I_D$$

$$= \frac{V_{DD}}{s} . \frac{I_D}{s} \qquad\qquad = \frac{V_{DS}}{s} . \frac{I_D}{s}$$

$$SPD' = \frac{SPD}{s^2} \quad ; \quad IPD' = \frac{IPD}{s^2}$$

e) Current Density (J):

$$J = \frac{I_D(L) \text{ or } I_D(s)}{A}$$

$$A = W . L$$

$$A' = W' . L'$$

$$= W/s \cdot \frac{L}{s}$$

$$\because W' = W/s, \quad L' = L/s$$

$$A' = A/s^2$$

$$= \frac{I_D}{\cancel{s}} . \frac{s^{\cancel{2}}}{A}$$

$$= s . I_D/A$$

g) Power Density (ψ): $\frac{P.D.}{A}$

$$A' = A/s^2 ;$$

$$P.D' = \frac{P.D}{s^2}$$

$$\psi' = \frac{P.D.}{\cancel{s^2}} \times \frac{\cancel{s^2}}{A}$$

$$\boxed{\psi' = \psi}$$

a) On Resistance : Ron

$$I_D(\text{linear}) = \frac{\mu_n C_{ox}}{\cancel{2}} \frac{W}{L} \left[\cancel{2}(V_{gs} - V_{tn})V_{DS} - \cancel{V_{DS}^2}\right]$$

$$\frac{1}{R_{on}} = \frac{I_D}{V_{DS}} = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{tn})$$

$$R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n \underset{\uparrow s}{C_{ox}} \frac{W\downarrow s}{L\downarrow s}(\underset{\downarrow s}{V_{gs}} - \underset{\downarrow s}{V_{tn}})}$$

$$R_{on} = \frac{V_{DS}\downarrow s}{I_D\downarrow s}$$

$$= \frac{V_{DS}}{\cancel{s}} \cdot \frac{\cancel{s}}{I_D} \qquad = \frac{1}{\mu_n \cdot \frac{\cancel{s}}{\cancel{s}} C_{ox}(V_{gs} - V_{tn})}$$

$\therefore$ R_{ON} = aftersca = before scaling

b) Delay $(\tau) = R_{ON} \cdot C_L$

$= R_{ON} \cdot C_g$

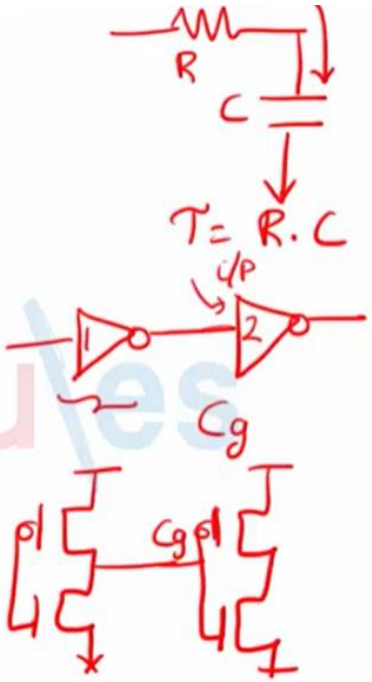
$C'_g = C_{ox} \cdot W \cdot L$

$= \frac{R_{ON} \cdot C_g}{s}$

$= s \cdot C_{ox} \cdot W \cdot L$

$C'_g = C_g / s^2$

$\boxed{\tau' = \tau / s}$



c) Frequency $\propto 1/D$

Delay got reduced by 's'

Freq ↑ increase by 's'

d) Dynamic Power Dissipation:

$\boxed{\propto} \cdot C_L \cdot f \cdot V_{DD}^2$

$C_L = C_g$

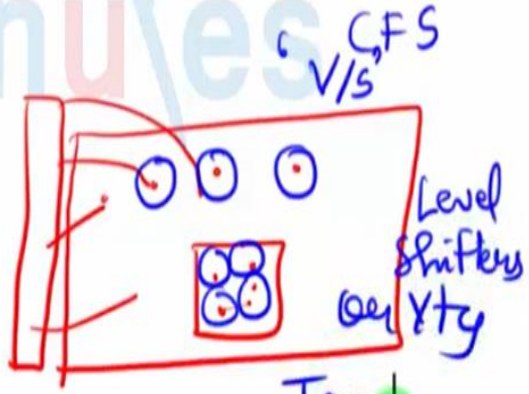
$C'_g = \frac{C_g}{s}$

$f' = s.f$

$V'_{DD} = \frac{V_{DD}}{s}$

$= \alpha \cdot \frac{C_g}{\cancel{s}} \cdot \cancel{s} f \cdot \frac{V_{DD}^2}{s^2}$

$DPD' = \frac{DPD}{s^2}$



Constant voltage Scaling

c) $I_{D(lin)} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)\left[2(V_{gs} - V_{tn})V_{DS} - V_{DS}^2\right]$

$I_D' = \frac{\mu_n C'_{ox}}{2}\left(\frac{W'}{L'}\right)\left[2(V_{gs} - V_{tn})V_{DS} - V_{DS}^2\right]$

$C'_{ox} = s\,C_{ox}$,

$W', L' = \frac{W}{s}, \frac{L}{s}$

$I_{D(L)}' = \frac{1}{s} I_{D(L)}$

d) $I_{D(sat)} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{gs} - V_{tn})^2$

$I_D'(sat) = \frac{\mu_n C'_{ox}}{2}\frac{W'}{L'}(V_{gs} - V_{tn})^2$

$I_D'(sat) = \frac{1}{s} I_D(sat)$

e) Current density $(J) = I_D / A$

$A = W \cdot L$

$A' = W' \cdot L'$

$= W/s \cdot L/s$

$A' = A/s^2$

$J' = s\,I_D \cdot \frac{s^2}{A}$

$J' = s^3 \cdot J$

a) Static P.D. or Instantaneous P.D.

$SPD = V_{DD} \cdot I_D$ $\qquad$ $V_{DS} \cdot I_D$

$SPD' = V_{DD} \cdot I_D'$ $\qquad$ $V_{DS} \cdot I_D'$

$= s \cdot I_D \cdot V_{DD}$ $\qquad$ $= s\,I_D \cdot V_{DS}$

$SPD' = s\,SPD$; $IPD = \frac{1}{s} IPD$

b) Power density (ψ): SPD/A

$S.P.D' = s\, S.P.D$

$A' = A/s^2$ $\qquad \psi' = SPD'/A'$

$A' = W'.L'$

$= \frac{W}{s} \cdot \frac{L}{s}$

$A' = A/s^2$

$= \frac{s.SPD}{A} \cdot s^2$

$$\boxed{\psi' = s^3 \psi}$$

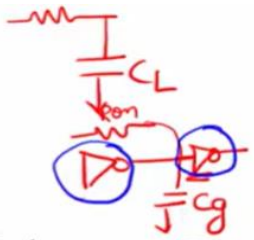
d) Delay $(\tau) = R_{on} C_L$

$= R_{on} \cdot C_g$

$\tau' = R'_{on} \cdot C_g'$

$\tau' = \frac{R_{on} \cdot C_g}{s^2}$

$\tau' = \frac{1}{s^2} \tau$



$R'_{on} = R_{on}/s$

$C'_g = C_g/s$

$F \propto 1/\tau$

e) so Frequency' $= s^2$ Frequency

c) On resistance:

$R_{on} = \frac{V_{DS}}{I_D}$; $\frac{1}{R_{on}} = \frac{I_D}{V_{DS}} = \mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{tn})$

$R'_{on} = \frac{V_{DS}}{I_D'}$ $\qquad \therefore R_{on} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{tn})}$

$I_D' = s I_D$ $\qquad = \uparrow s$

$R'_{on} = \frac{1}{s} R_{on}$

f) Dynamic Power dissipation: (DPD)

$DPD = C_L \cdot V_{DD}^2 \cdot B \cdot F$ $\qquad \because C_L = C_g$

$DPD = C_g \cdot V_{DD}^2 \cdot B \cdot F$ $\qquad B =$ constant

$C'_g = C_g/s$ $\qquad DPD' = \frac{C_g}{s} \cdot V_{DD}^2 \cdot B \cdot s^2 F$

V_{DD} unchanged

$F' = s^2 F$ $\qquad DPD' = s\, DPD$