CMOS Circuits
CMOS Logic Families

Unit -5

by
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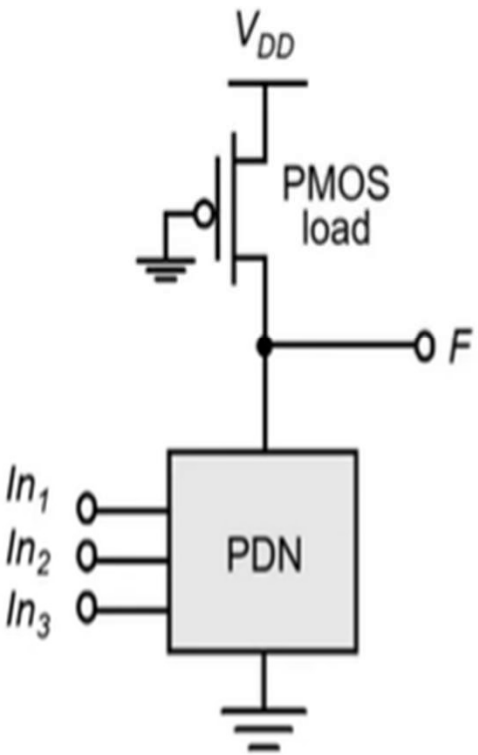
Ratioed Logic

Static CMOS – 2 N Transistors (N + N)

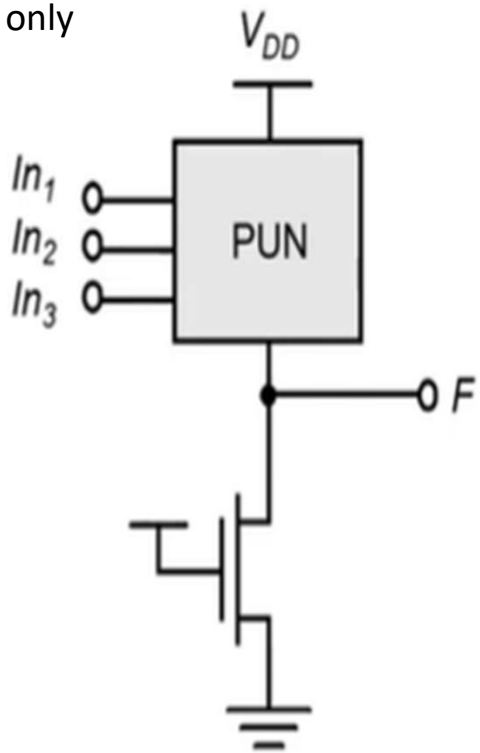
Pseudo NMOS/PMOS – N+1 transistors only

Pseudo NMOS- Weak Zero
Pseudo PMOS – Weak One

For Pseudo PMOS – Area is more



Pseudo NMOS Logic

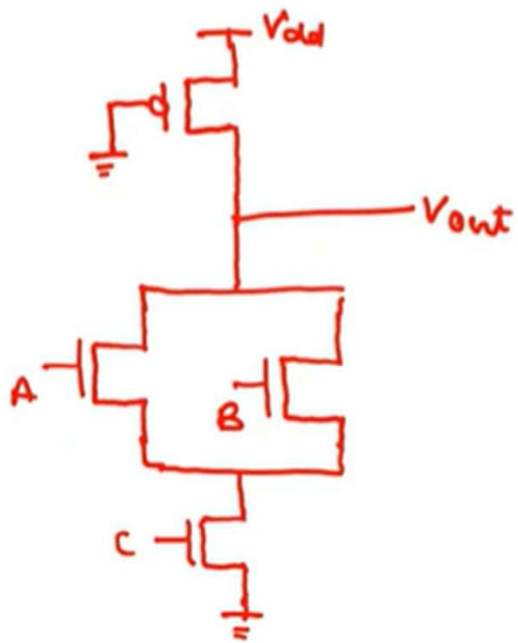


Pseudo PMOS Logic

Implement $F = \overline{(A+B)C}$ using Pseudo NMOS and Pseudo PMOS Logic

using Pseudo NMOS logic

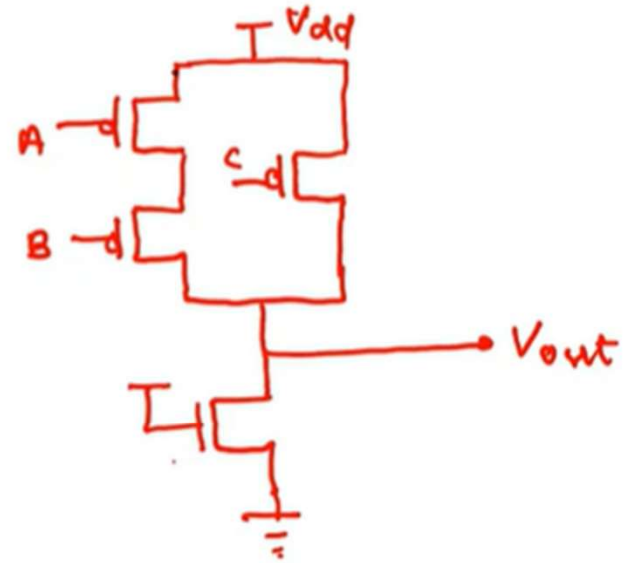
$\bar{F} = (A+B)C$



using Pseudo PMOS logic

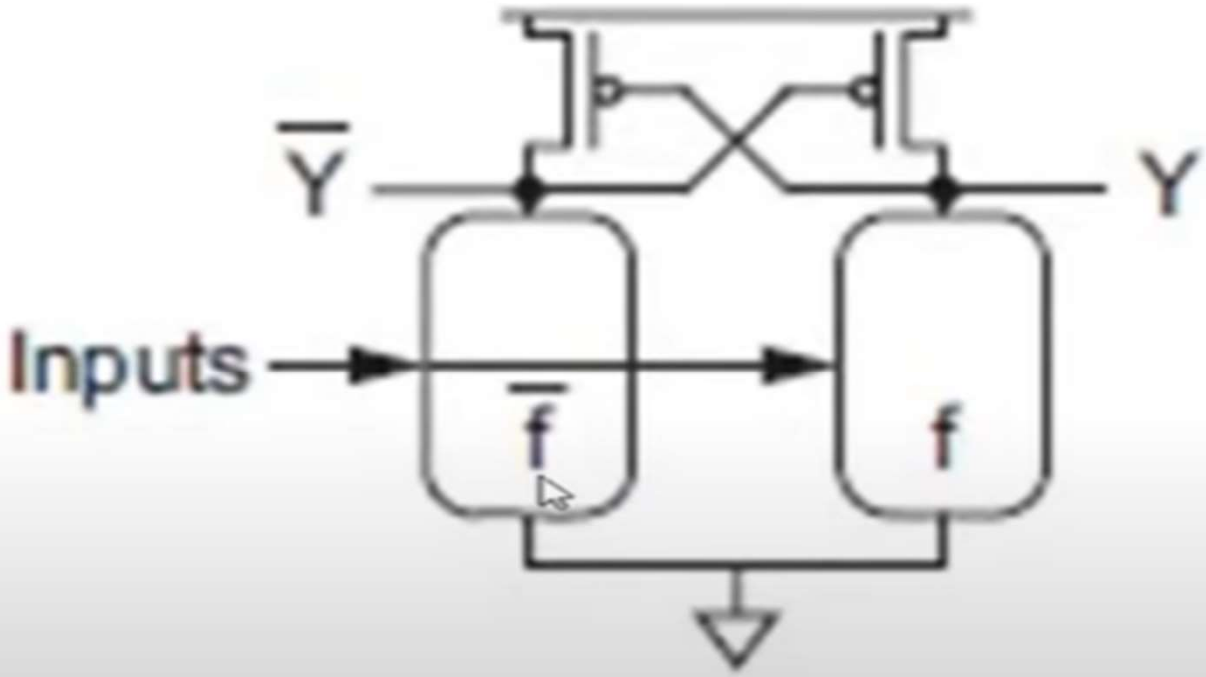
$F = \overline{(A+B)C} = \overline{(A+B)} + \bar{C}$

$= \bar{A}.\bar{B} + \bar{C}$



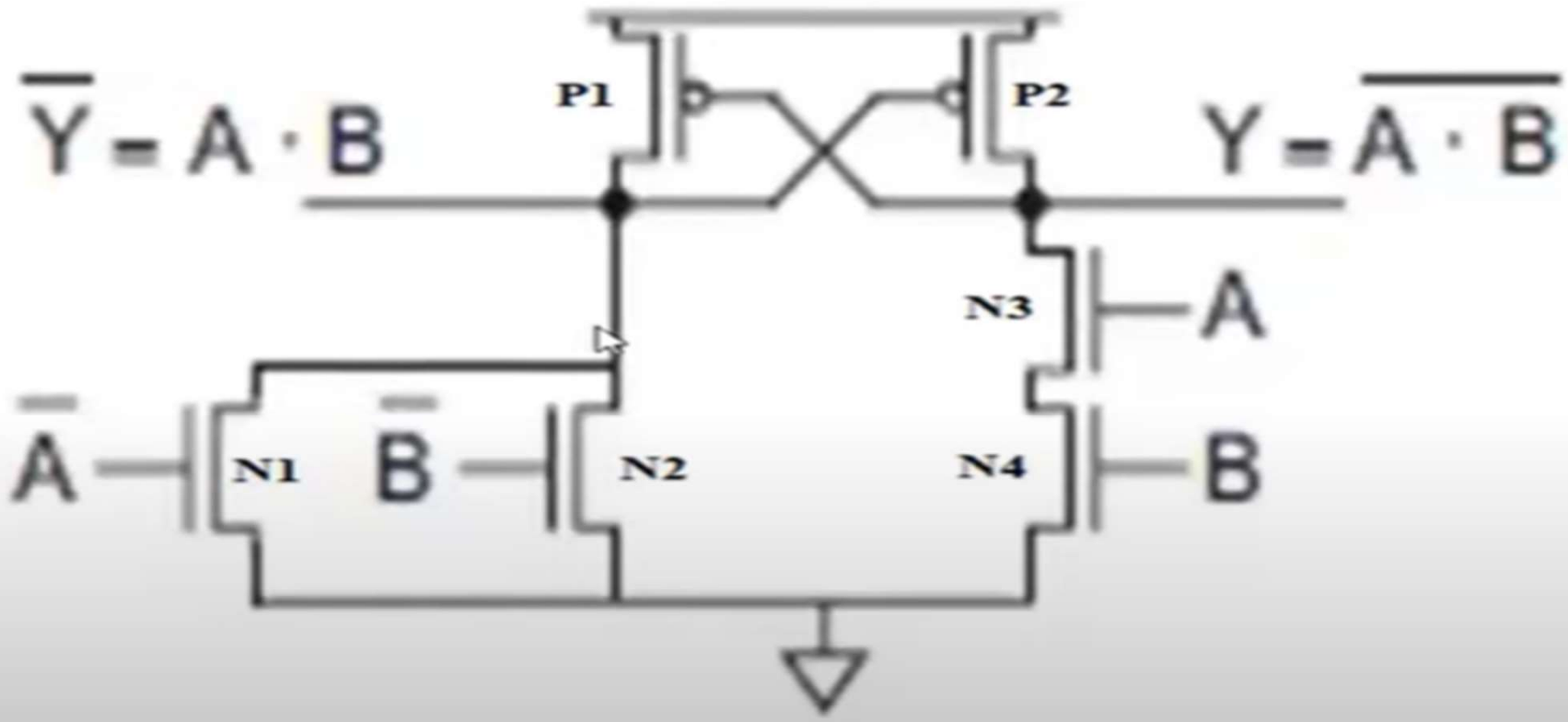
CVSL Logic

Cascode Voltage Switch Logic



CVSL Logic - (NAND & AND)

Cascode Voltage Switch Logic



Cascode Voltage Switch Logic

Inputs		Output
A	B	Y = A.B
0	0	0
0	1	0
1	0	0
1	1	1

Input		Output
A	B	$Y = \overline{A.B}$
0	0	1
0	1	1
1	0	1
1	1	0

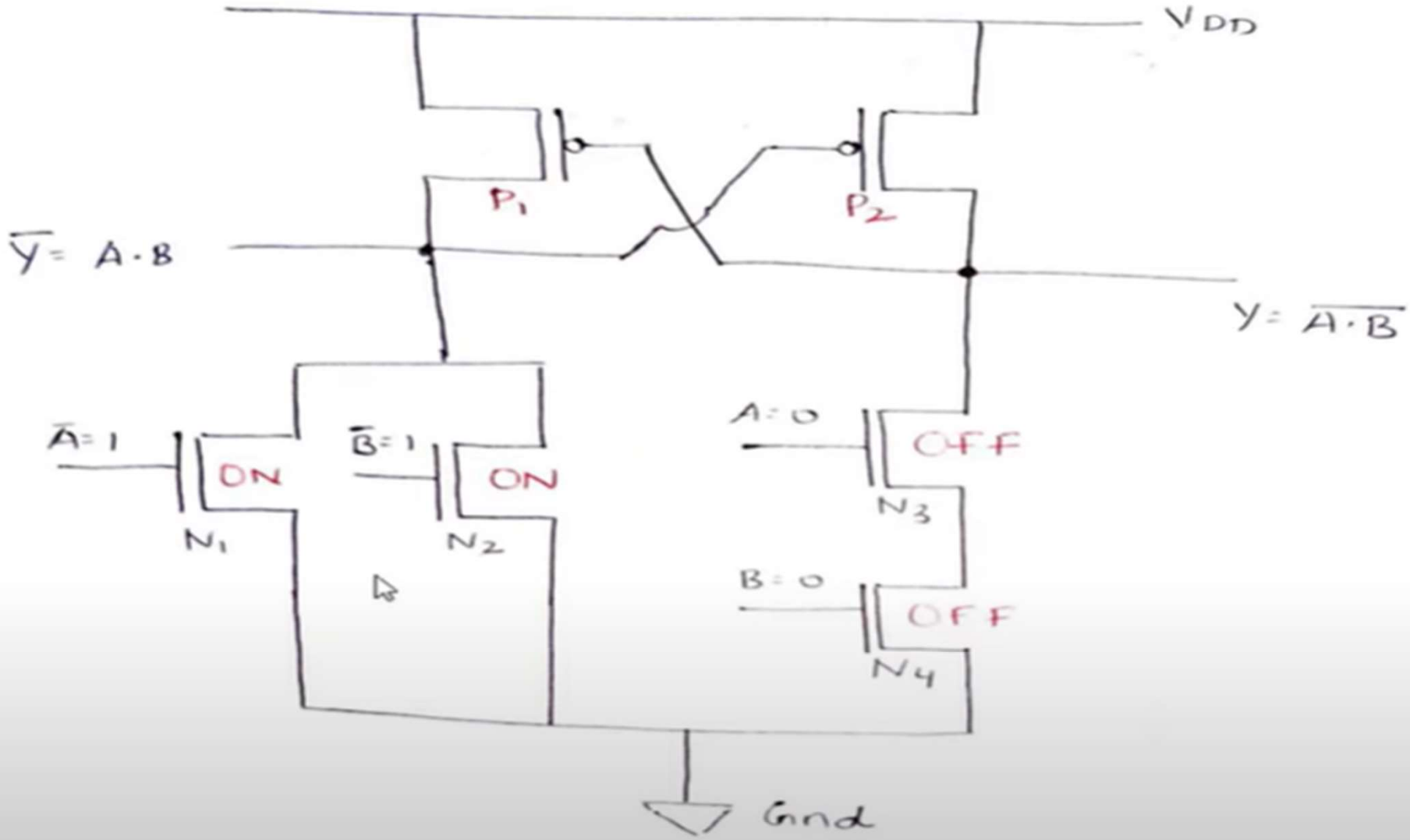
Cascode Voltage Switch Logic

Case :- 1, when $A = 0$; $B = 0$

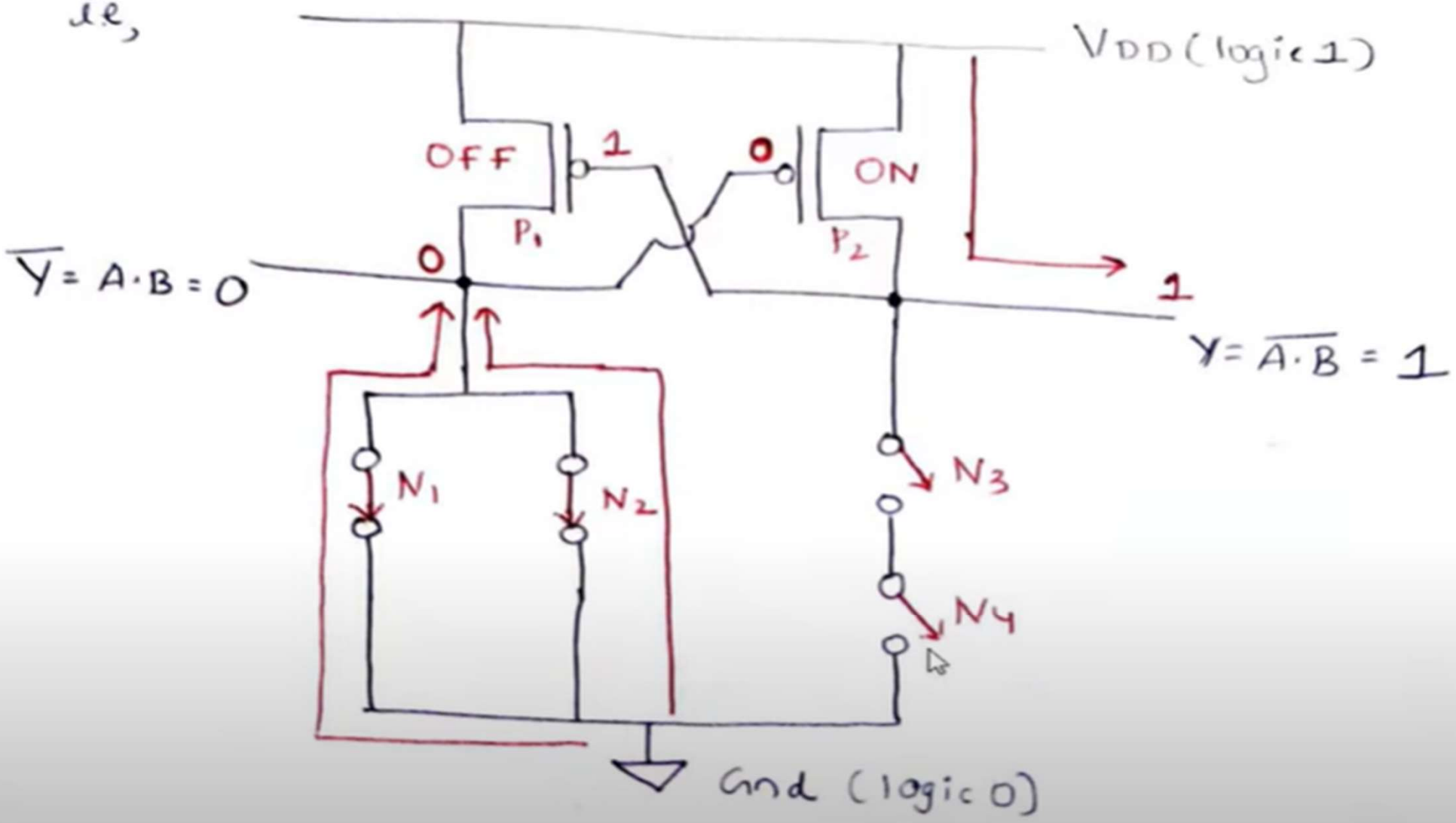
$\overline{A} = 1$; $\overline{B} = 1$

N_1 is ON ; N_2 is ON

N_3 is OFF ; N_4 is OFF


VDD
P1
P2
$\overline{Y} = A \cdot B$
$Y = \overline{A \cdot B}$
$\overline{A} = 1$
ON
N1
$\overline{B} = 1$
ON
N2
A = 0
OFF
N3
B = 0
OFF
N4
Gnd

ie,

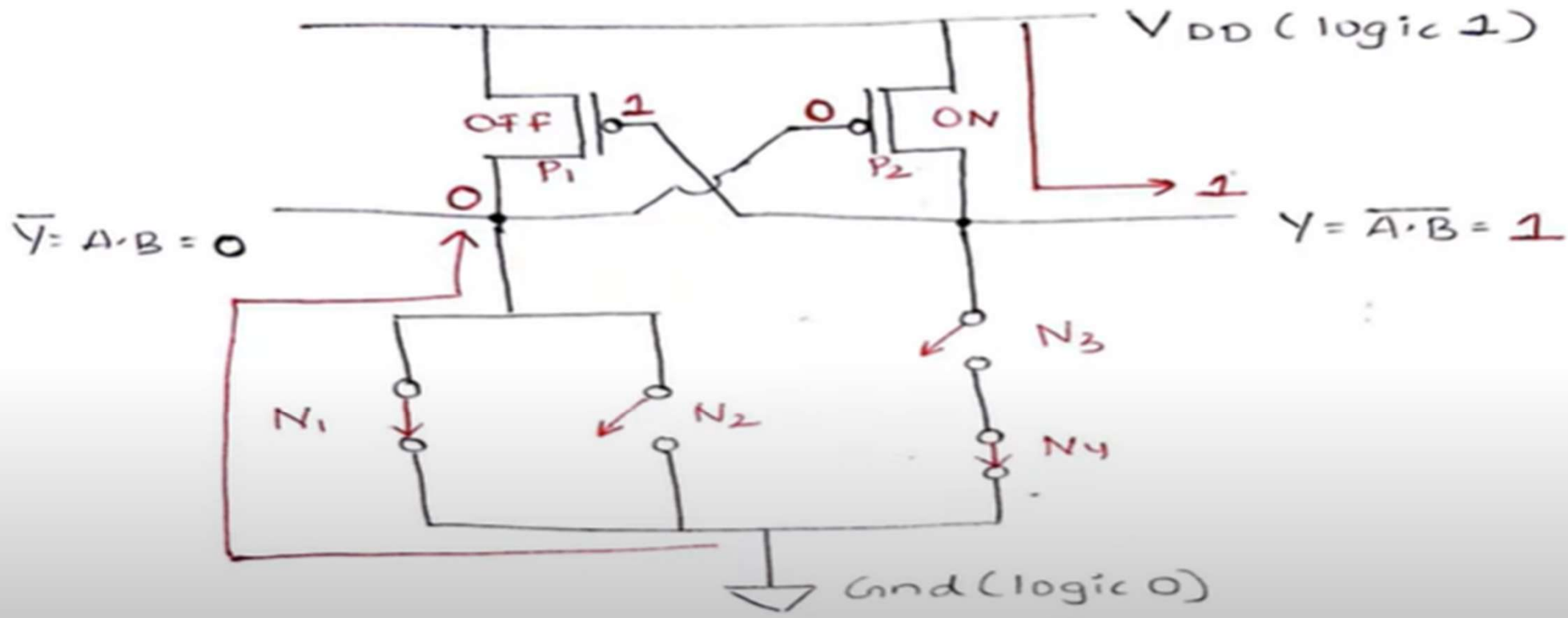

VDD (logic 1)
OFF
1
0
ON
P1
P2
0
1
$\overline{Y} = A \cdot B = 0$
$Y = \overline{A \cdot B} = 1$
N1
N2
N3
N4
Gnd (logic 0)

Case:-(ii) when $A = 0$; $B = 1$

$\bar{A} = 1$; $\bar{B} = 0$

hence N_1 is ON ; N_2 is OFF

N_3 is OFF ; N_4 is ON

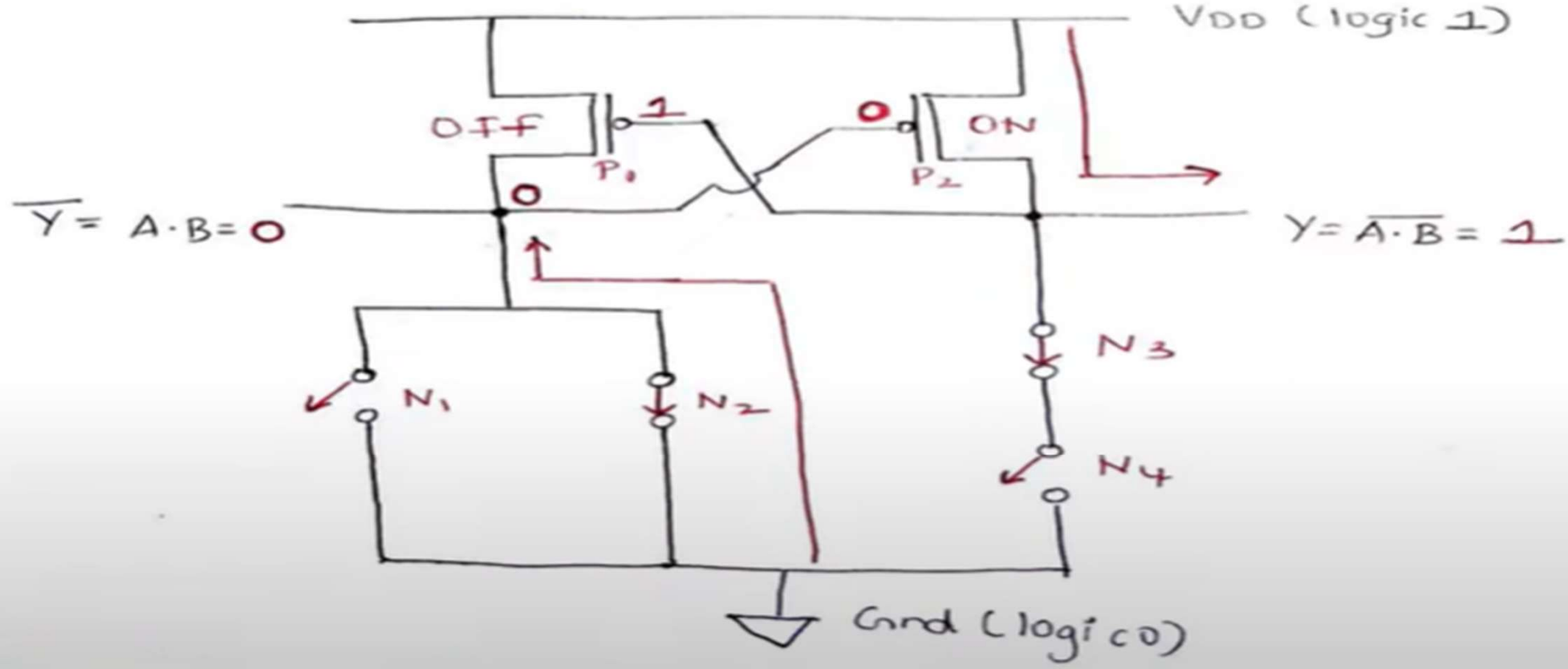


Case :- (iii) when $A = 1$; $B = 0$

$\overline{A} = 0$; $\overline{B} = 1$

hence N_1 is off ; N_2 is ON

N_3 is ON ; N_4 is OFF

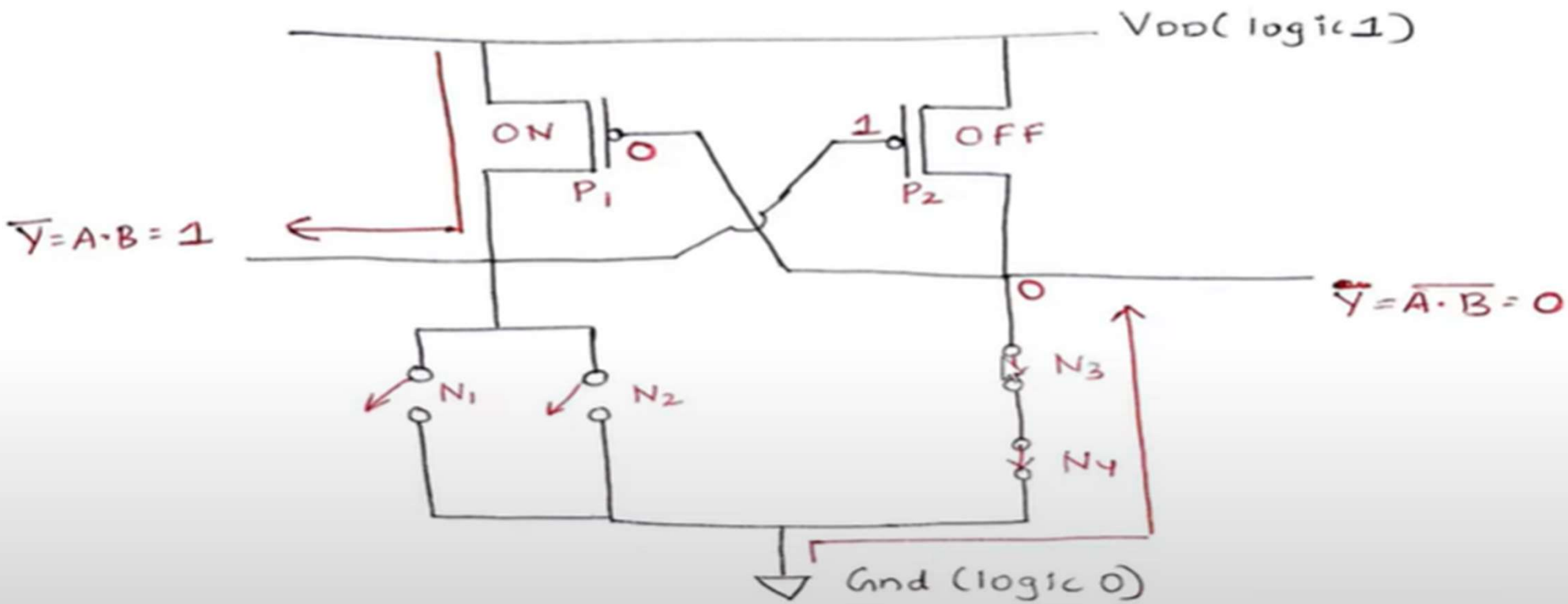


Case :- (iv) when $A = 1$; $B = 1$

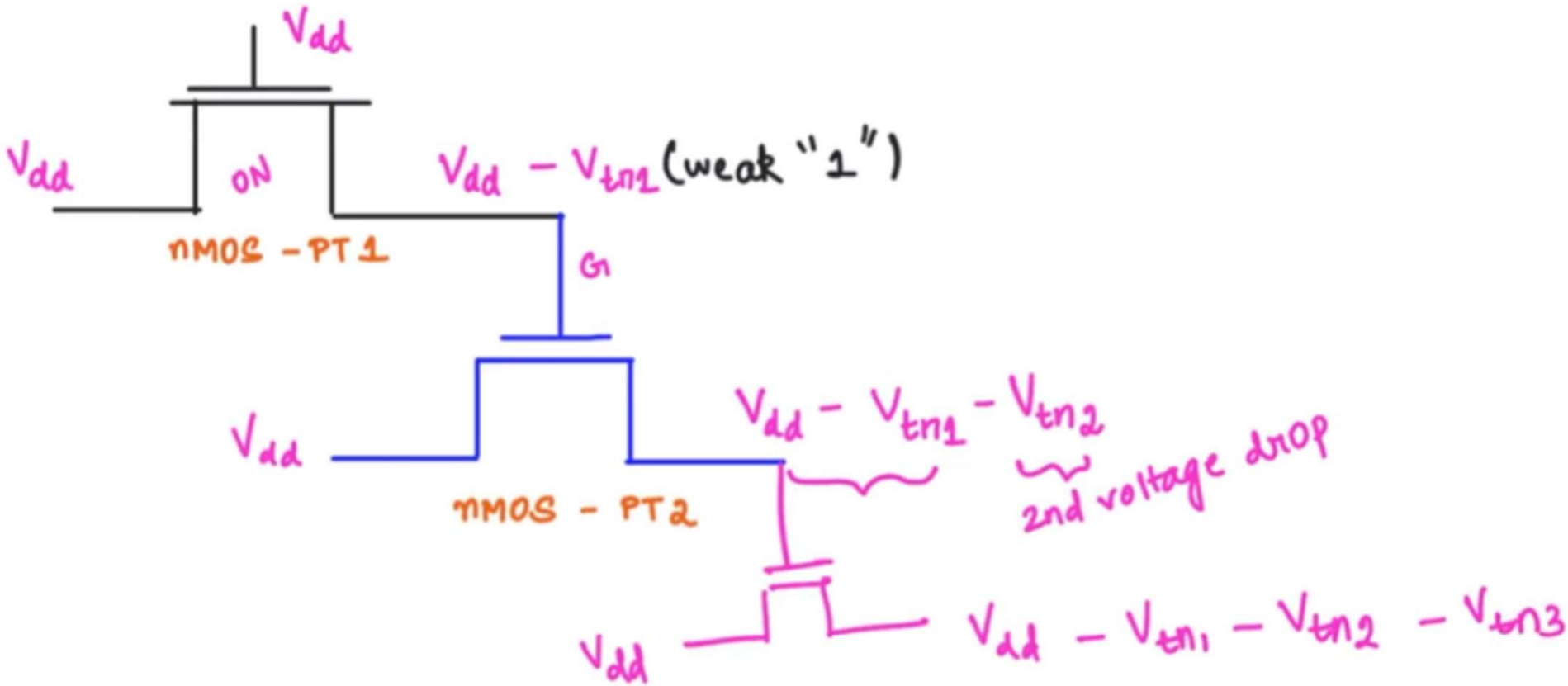
$\overline{A} = 0$; $\overline{B} = 0$

N_1 is OFF ; N_2 is OFF

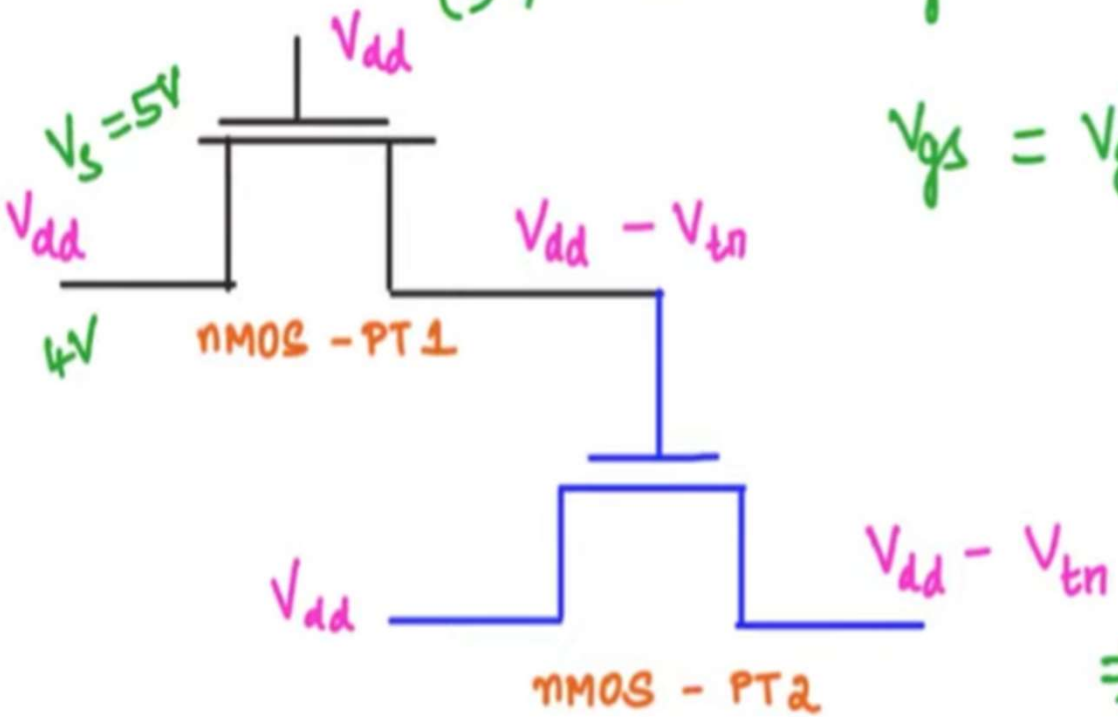
N_3 is ON ; N_4 is ON



✅ Cascading the Pass Transistors



Example Values:



ON $\Leftarrow V_{gs} > V_t$; let $V_t = 1V$

$V_{gs} = V_g - V_s = 5 - 5 = 0V$

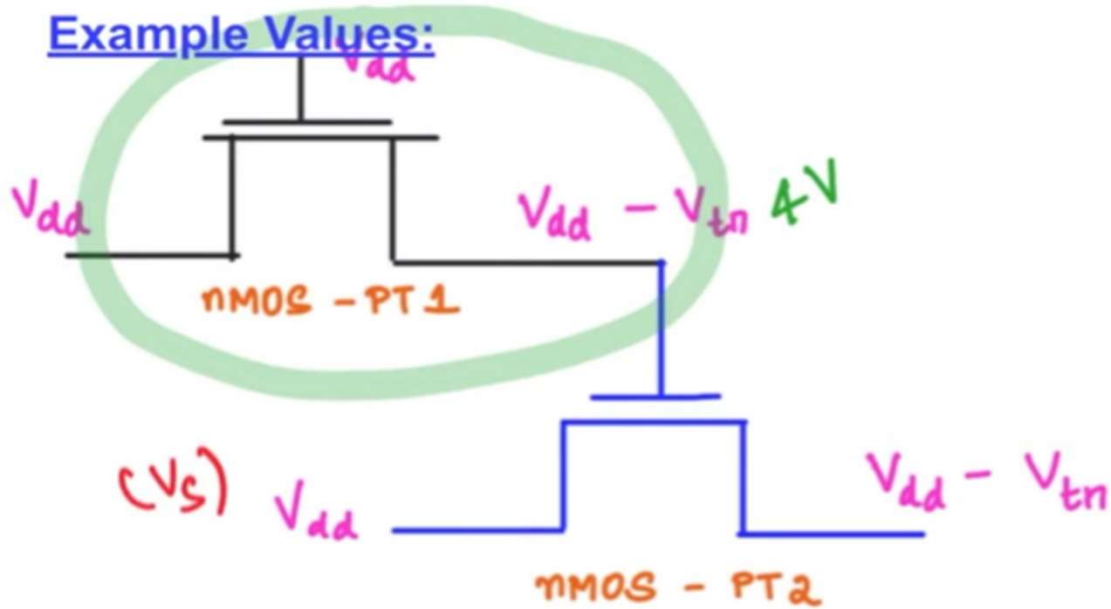
$\therefore \quad 0 < 1V$; $V_{gs} < V_t$

nMOS - PT1 → OFF

$\Rightarrow$ retains previous voltage "4V"

$V_{dd} - V_{tn} = 5 - 1 = 4V$

Example Values:



$V_g = 4V$; $V_s = 4V$ ✓

$V_{gs} = V_g - V_s = 0V$; $V_t = 1V$

$V_{gs} < V_t$

$\therefore$ nMOS − PT2 = OFF ✓

$V_g = 4V$; $V_s = 3V$

$V_{gs} = V_g - V_s = 4 - 3 = 1V$

$V_{gs} = V_t$ (nMOS − PT2 = ON)

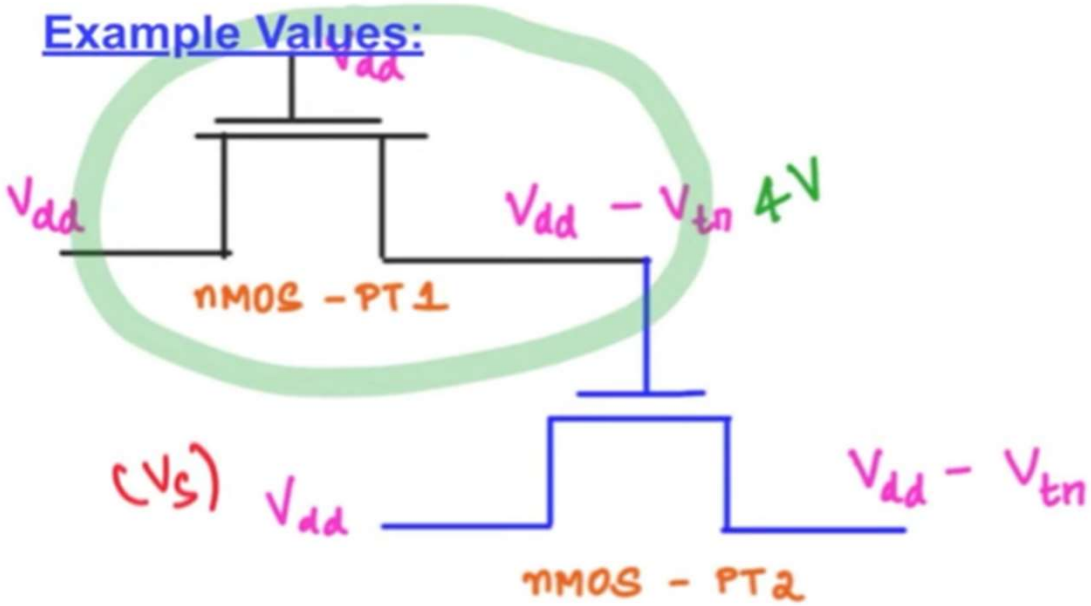
o/p drain voltage (PT2) = $V_s = 3V$

; $\underbrace{V_s = 4V;\ 5V}_{\text{PT2 = OFF state}}$

retain previous value.

$= 3V$

Example Values:



$V_g = 4V$; $V_s = 4V$ ✓

$V_{gs} = V_g - V_s = 0V$; $V_t = 1V$

$V_{gs} < V_t$

$\therefore$ nMOS − PT2 = OFF ✓

$V_g = 4V$; $V_s = 3V$

$V_{gs} = V_g - V_s = 4 - 3 = 1V$

$V_{gs} = V_t$ (nMOS − PT2 = ON)

o/p drain voltage (PT2) = $V_s = 3V$

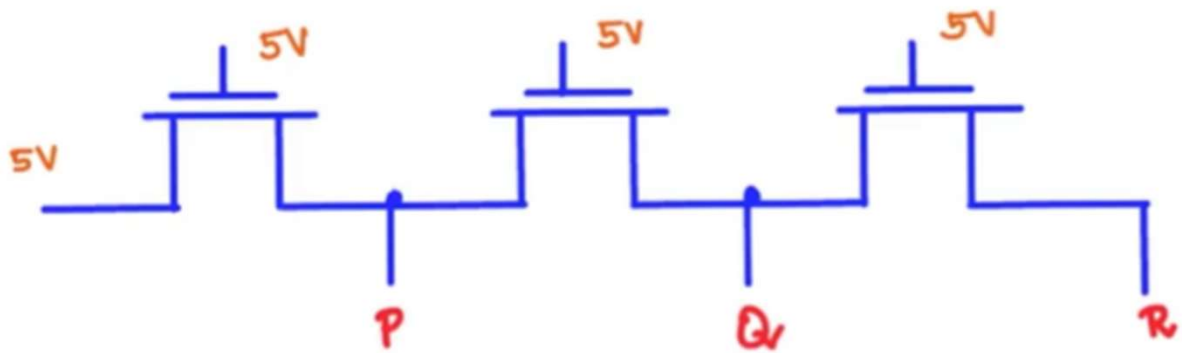
; $\underbrace{V_s = 4V;\ 5V}_{\text{PT2 = OFF state}}$

retain previous value.

$= 3V$

$V_{dd} - V_{tn} - V_{tn} = 5 - 1 - 1$
$= 3V$

In the following circuit employing pass transistor logic, all NMOS transistors are identical with a threshold voltage of 1V. The output voltages of P, Q, and R are;



1
2
3
4

SOLUTION:

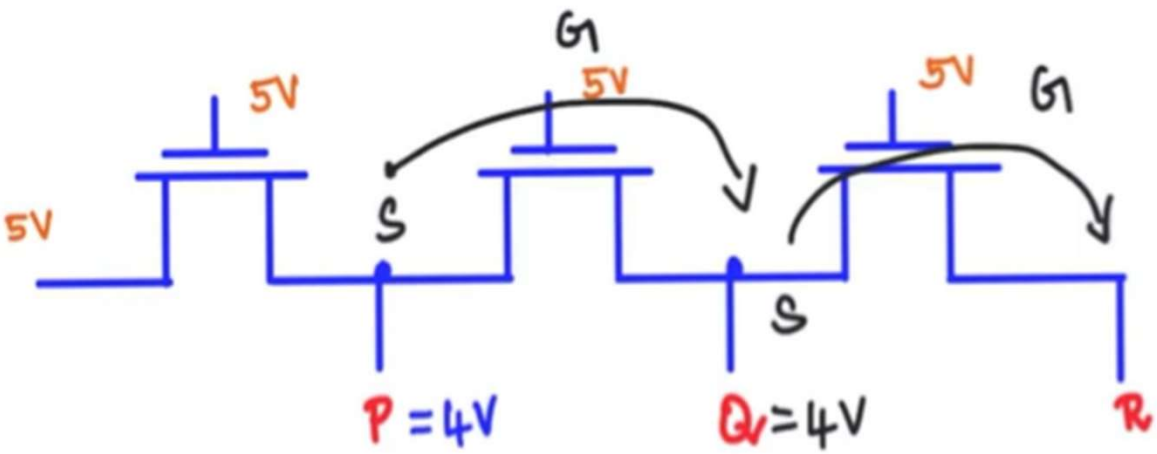
nMOS transistors; $V_t = 1V$; $V_g = 5V$; $V_s = 5V$ $\quad V_{dd} - V_t$

TO FIND: $V_P, V_Q, V_R = ?$ (o/p drain voltages) $\quad \boxed{V_P = 4V}$

V_P ? nMOS = ON; only when $V_{gs} \geq V_t$.

$V_{gs} = V_g - V_s = 5 - 5 = 0V$; $0 < 1V$; transistor = OFF.

$V_{gs} = 5 - 4 = 1V$; $V_{gs} = V_t$ $\therefore$ $V_P = 4V$ (source)



$V_R = ?$

$V_{gs} = V_g - V_s$

$= 5 - 4$

$= 1V$

$V_{gs} = V_t$

nMOS ⇒ ON

$V_Q = ?$

$V_{gs} = V_g - V_s = 5 - 4 = 1V$

$\boxed{V_{gs} = V_t}$ ⇒ nMOS = ON

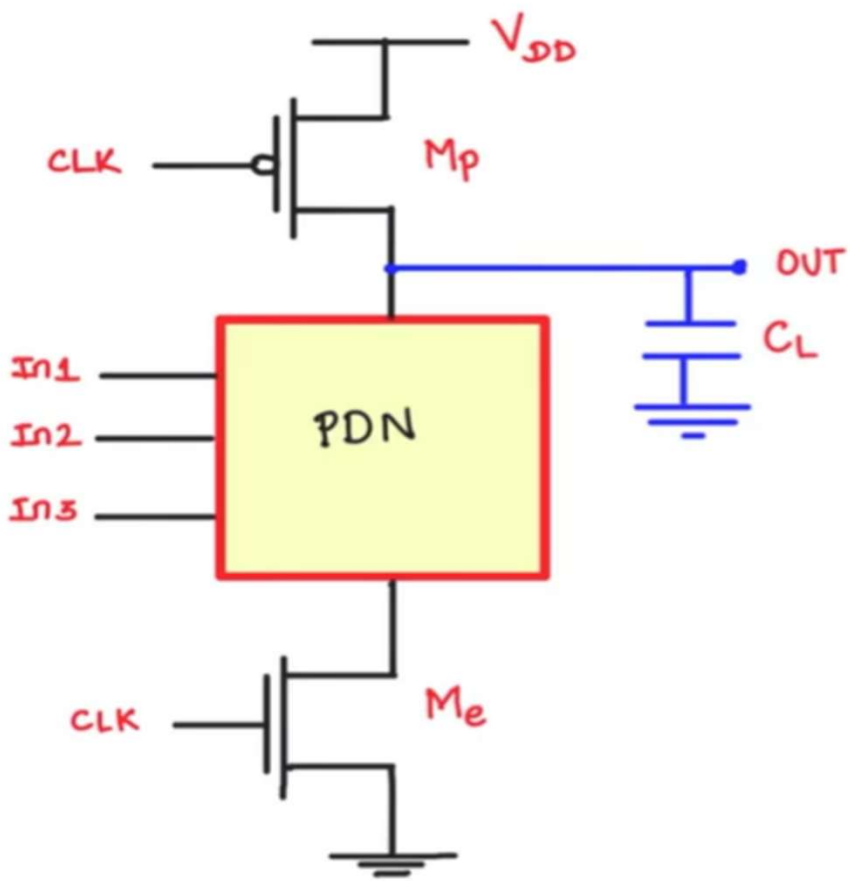
(drain) $\boxed{V_Q = 4V}$

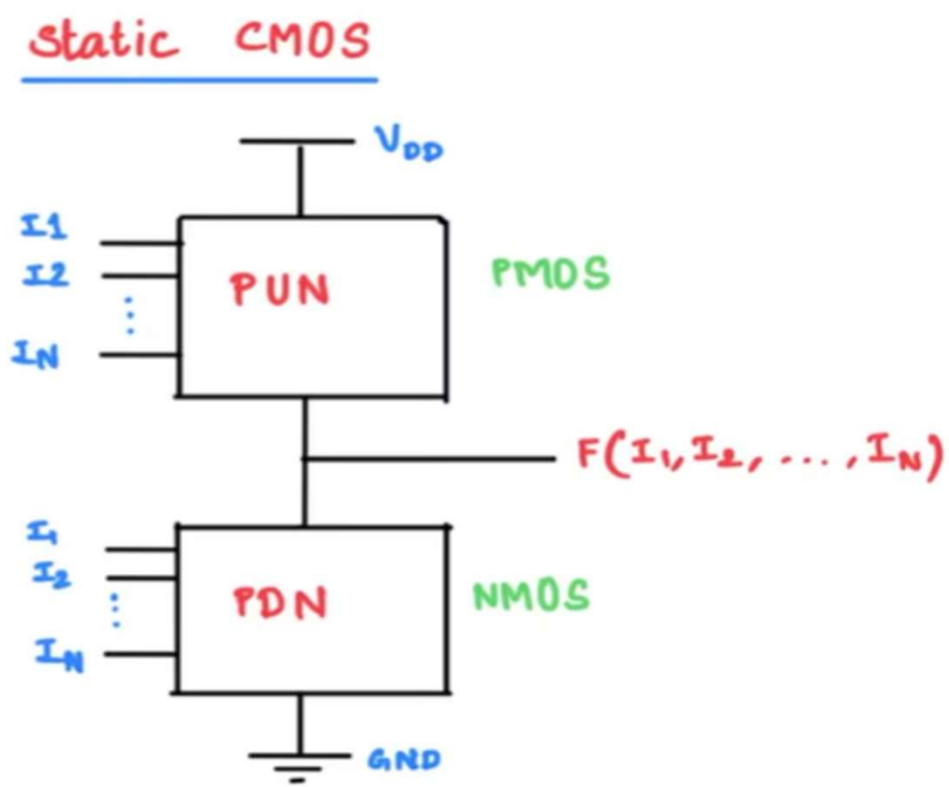
$\therefore \boxed{V_R = 4V}$

$\boxed{V_P = V_Q = V_R = 4V}$

Dynamic CMOS

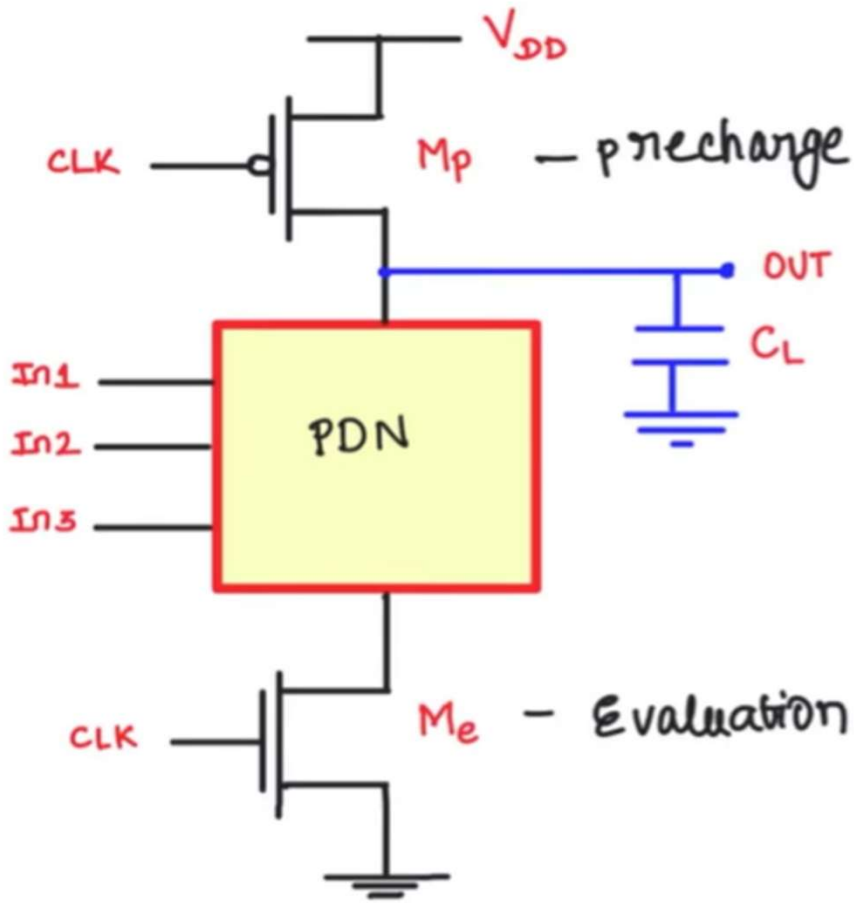
General structure of Dynamic CMOS Logic Design:





Dynamic CMOS

General structure of Dynamic CMOS Logic Design:



(i) CLK = 0 ; Mp – precharge
↓
ON

$V_{OUT} = V_{DD}$ (strong '1')

CLK = 0; Me – NMOS
↓
OFF

(ii) CLK = 1; Me – ON
Mp – OFF

Dynamic CMOS

$F = \overline{[A + (B.C)]}$

→ precharge – M_P ⇒ PMOS

→ Evaluation – M_e ⇒ NMOS

→ P & E ⇒ PDN ⇒ NMOS

→ output capacitor ⇒ C_L

→ CLOCK signal ⇒ CLK

Dynamic CMOS

$F = \overline{[A + (B.C)]}$

→ precharge – M_P ⇒ PMOS

→ Evaluation – M_e ⇒ NMOS

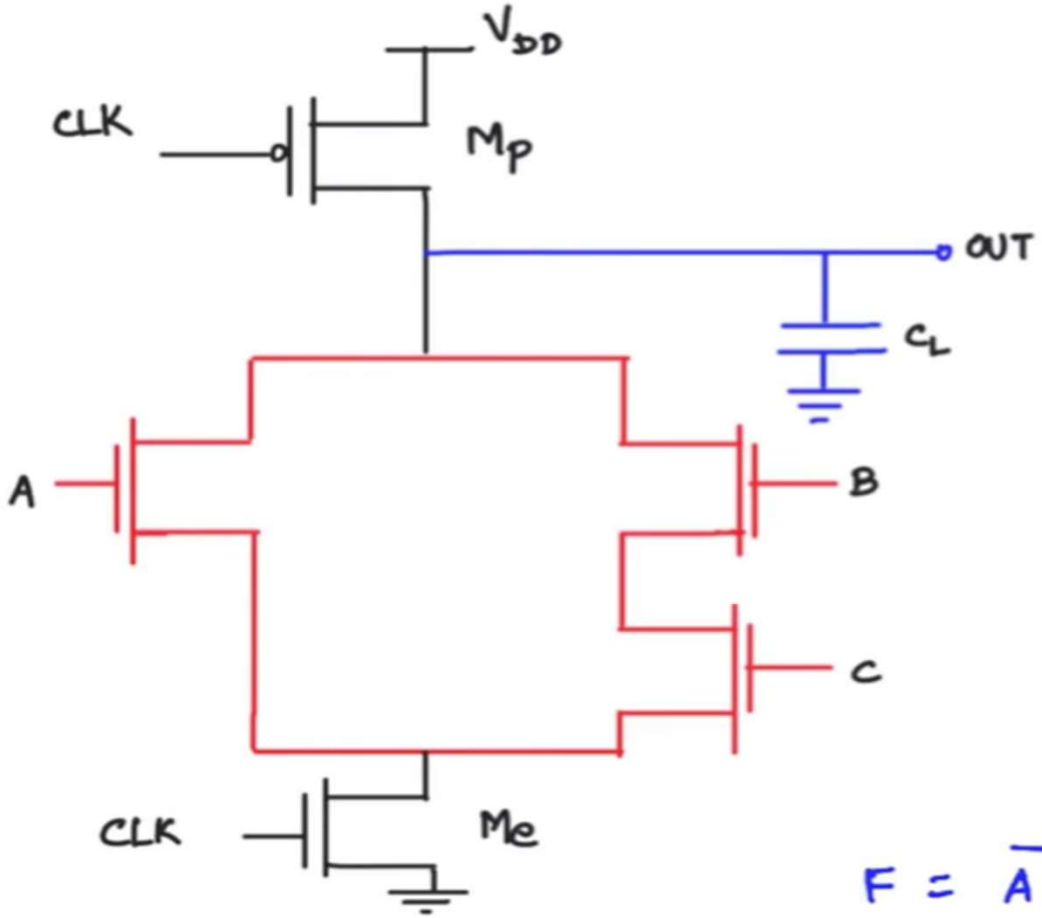
→ P & E ⇒ PDN ⇒ NMOS

→ output capacitor ⇒ C_L

→ CLOCK signal ⇒ CLK

Dynamic CMOS

Dynamic CMOS Design for F = [A + (B . C)]'



case (i): A = 0 ; B = 0 ; C = 0

CLK = 0 ; → PMOS → Mp = ON

↳ Me = OFF

$V_{CL} \rightarrow V_{DD}$.

(precharged to V_{DD})

CLK = 1 ; Me = ON ; Mp = OFF

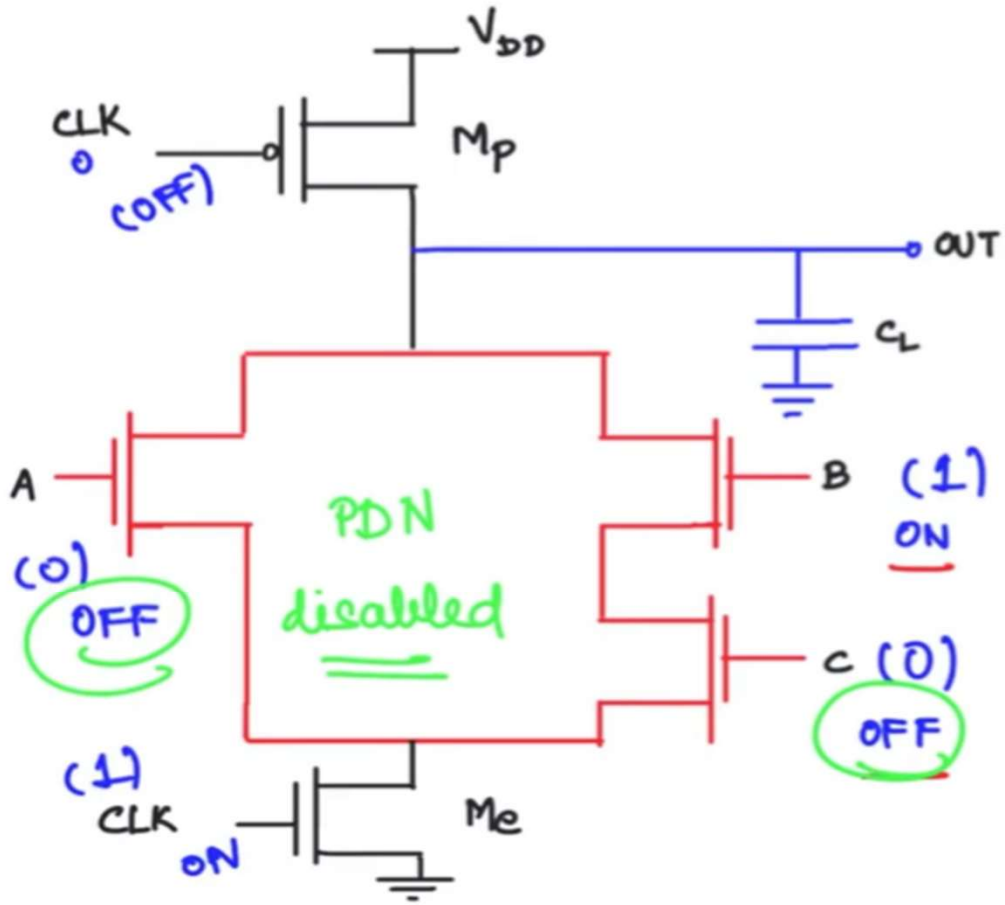
A = B = C = 0 ⇒ 3 – nMOS ↙ OFF

$$\boxed{V_{CL} = V_{DD}}$$

$$F = \overline{A + (B.C)} = 1 \approx V_{DD}$$

Dynamic CMOS

Dynamic CMOS Design for F = [A + (B . C)]'



case(ii): A = 0; B = 1; C = 0

CLK = 0; $V_{CL} = V_{DD}$ (precharged)

Me = OFF

CLK = 1; Evaluation.

$V_{CL} = V_{DD}$

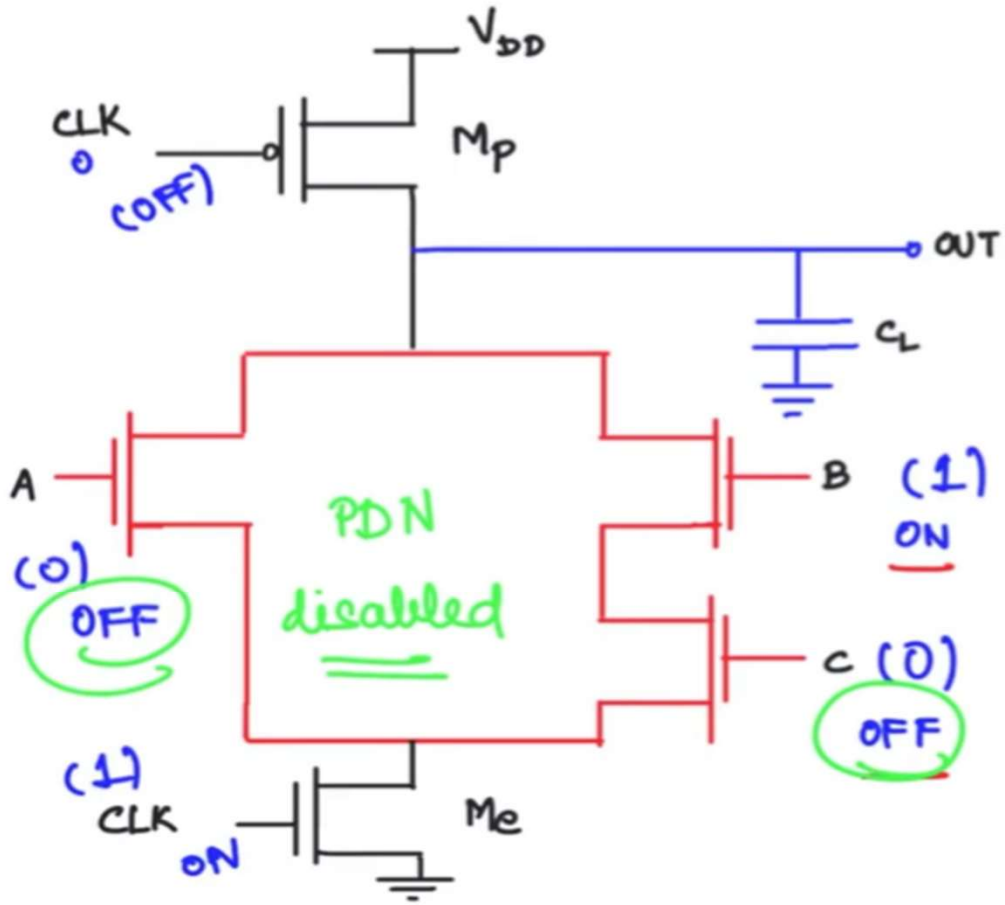
$F = \overline{A + (B.C)}$

$= \overline{0 + (1.0)}$

$F = 1 \approx V_{DD}$

Dynamic CMOS

Dynamic CMOS Design for F = [A + (B . C)]'



case(ii): A = 0; B = 1; C = 0

CLK = 0; $V_{CL} = V_{DD}$ (precharged)

Me = OFF

CLK = 1; Evaluation.

$V_{CL} = V_{DD}$

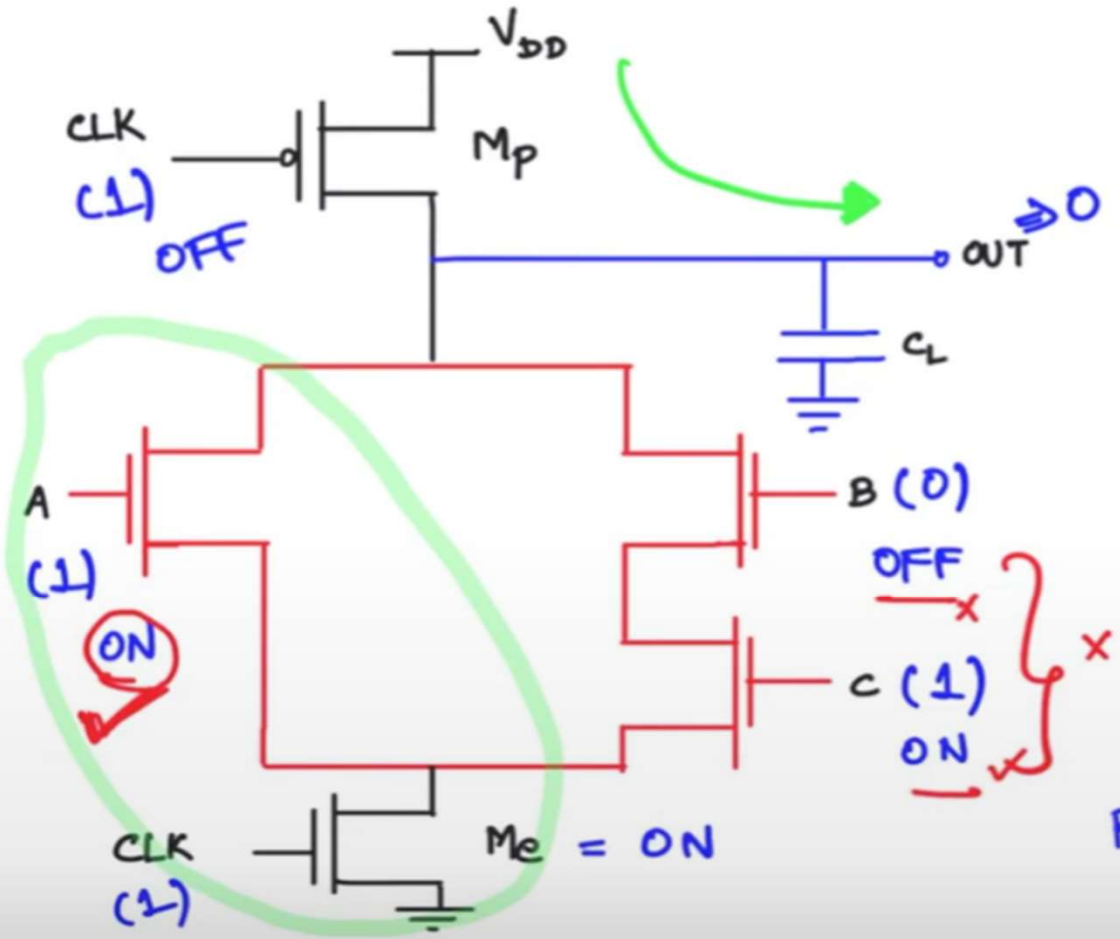
$F = \overline{A + (B.C)}$

$= \overline{0 + (1.0)}$

$F = 1 \approx V_{DD}$

Dynamic CMOS

Dynamic CMOS Design for F = [A + (B . C)]'



case (iii): A = 1; B = 0; C = 1

CLK = 0; Mp = ON; Me = OFF

$V_{CL} = V_{DD}$

CLK = 1; Me = ON

$V_{CL} = V_{DD}$

↓

V_{CL} = "0"

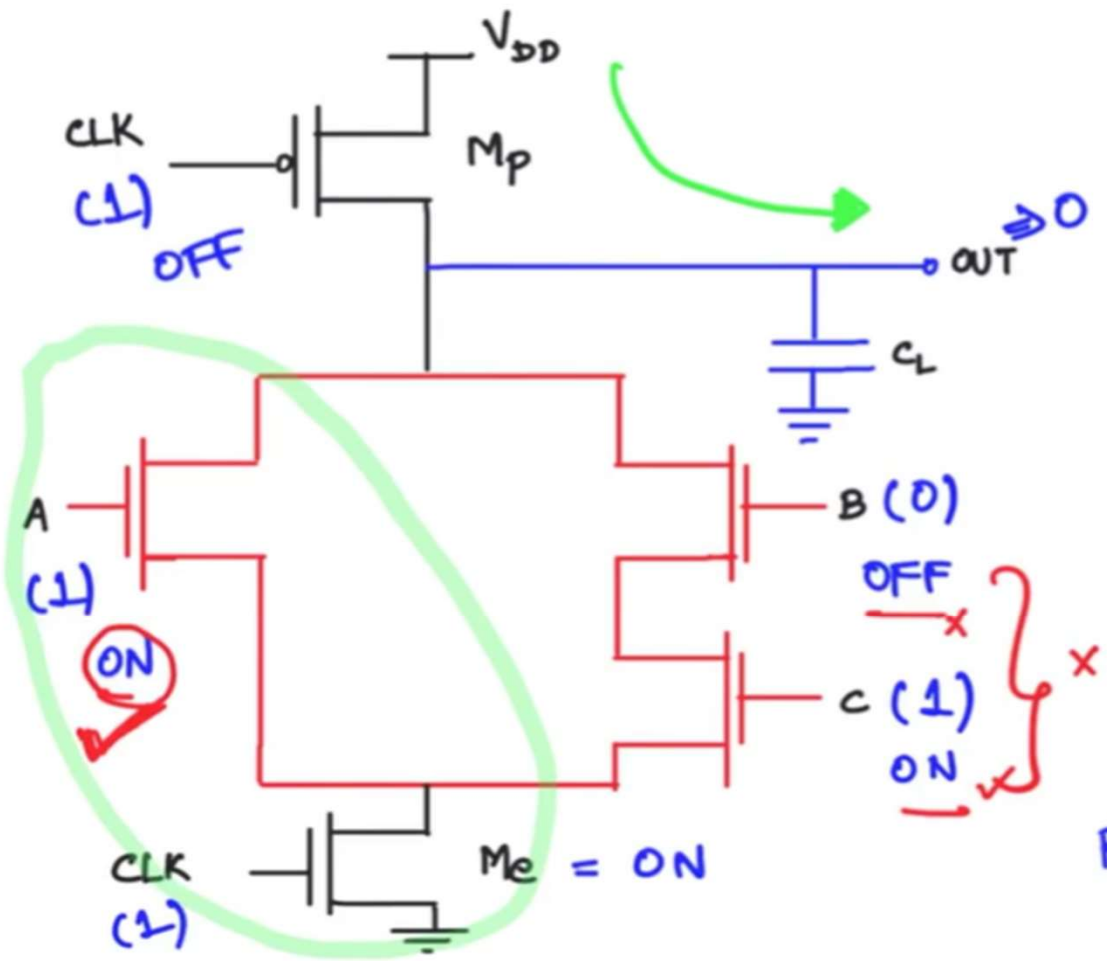
∴ $\boxed{F = 0}$

$F = \overline{A + (B.C)} = \overline{1+0} = \overline{1}$

$= 0$

Dynamic CMOS

Dynamic CMOS Design for F = [A + (B . C)]'



case (iii): A = 1; B = 0; C = 1

CLK = 0; M_p = ON; M_e = OFF

$V_{CL} = V_{DD}$

CLK = 1; M_e = ON

$V_{CL} = V_{DD}$

$\downarrow$

V_{CL} = "0"

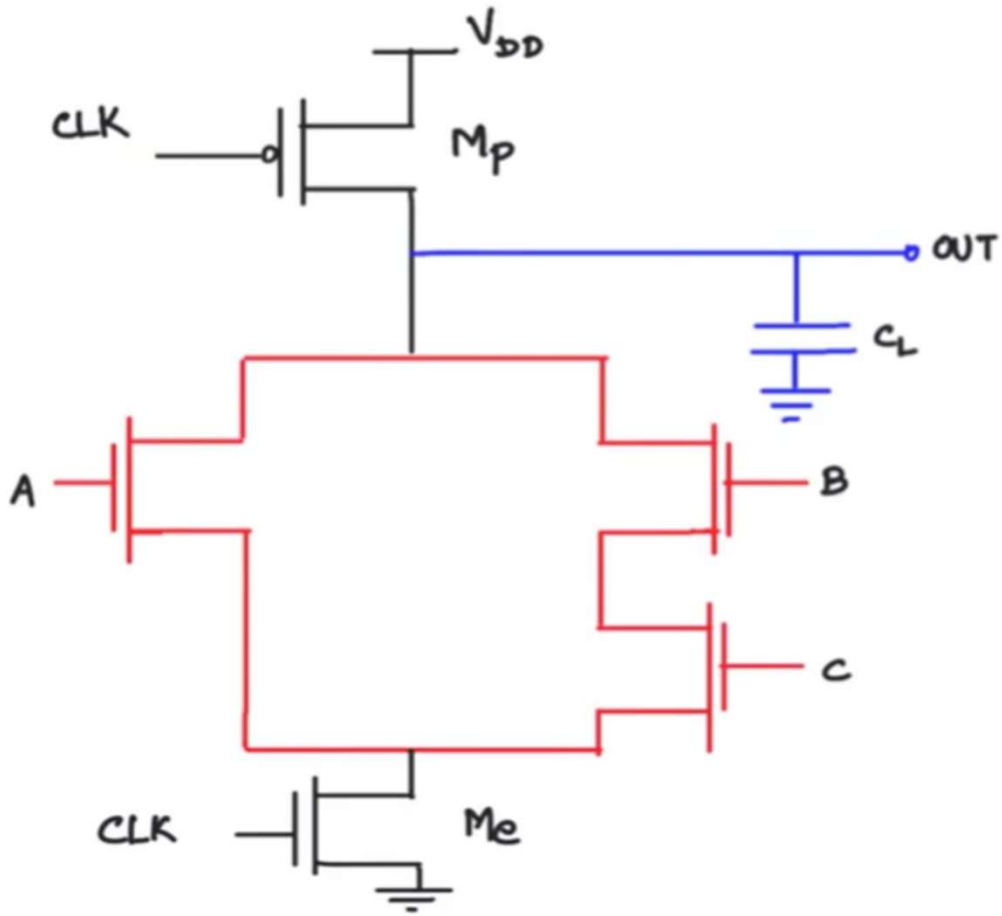
$\therefore$ $\boxed{F = 0}$

$F = \overline{A + (B.C)} = \overline{1 + 0} = \overline{1}$

$= 0$

Dynamic CMOS

Dynamic CMOS Design for F = [A + (B . C)]'



Total no. of transistors

$= 3 + 2 = 5$

Mp Me

In general, dynamic CMOS = N + 2

Static CMOS = 2N

= 6 ⇒ $F = \overline{A + (B.C)}$

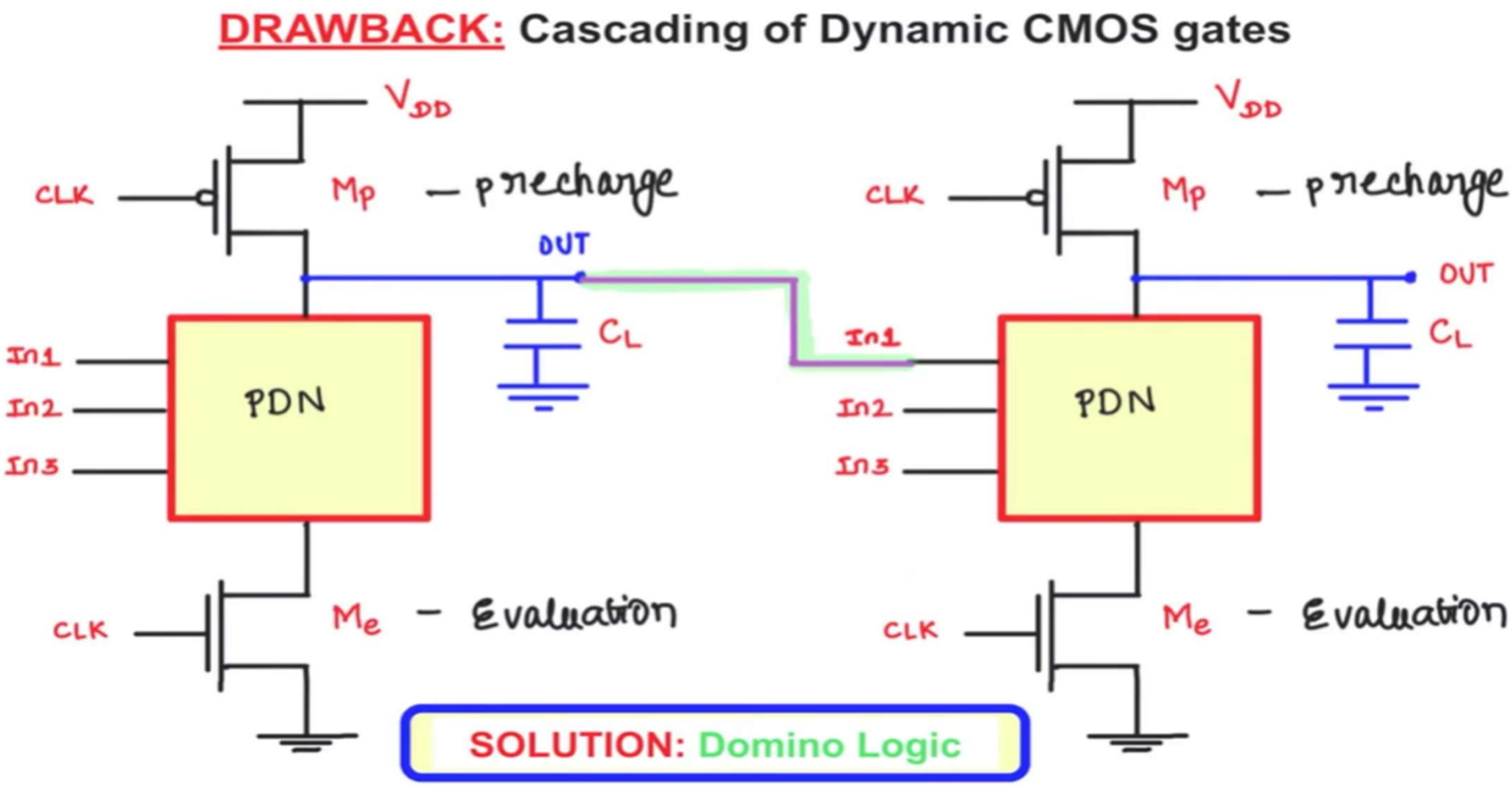
Dynamic CMOS

PROPERTIES OF DYNAMIC CMOS DESIGN

—V_{dd}

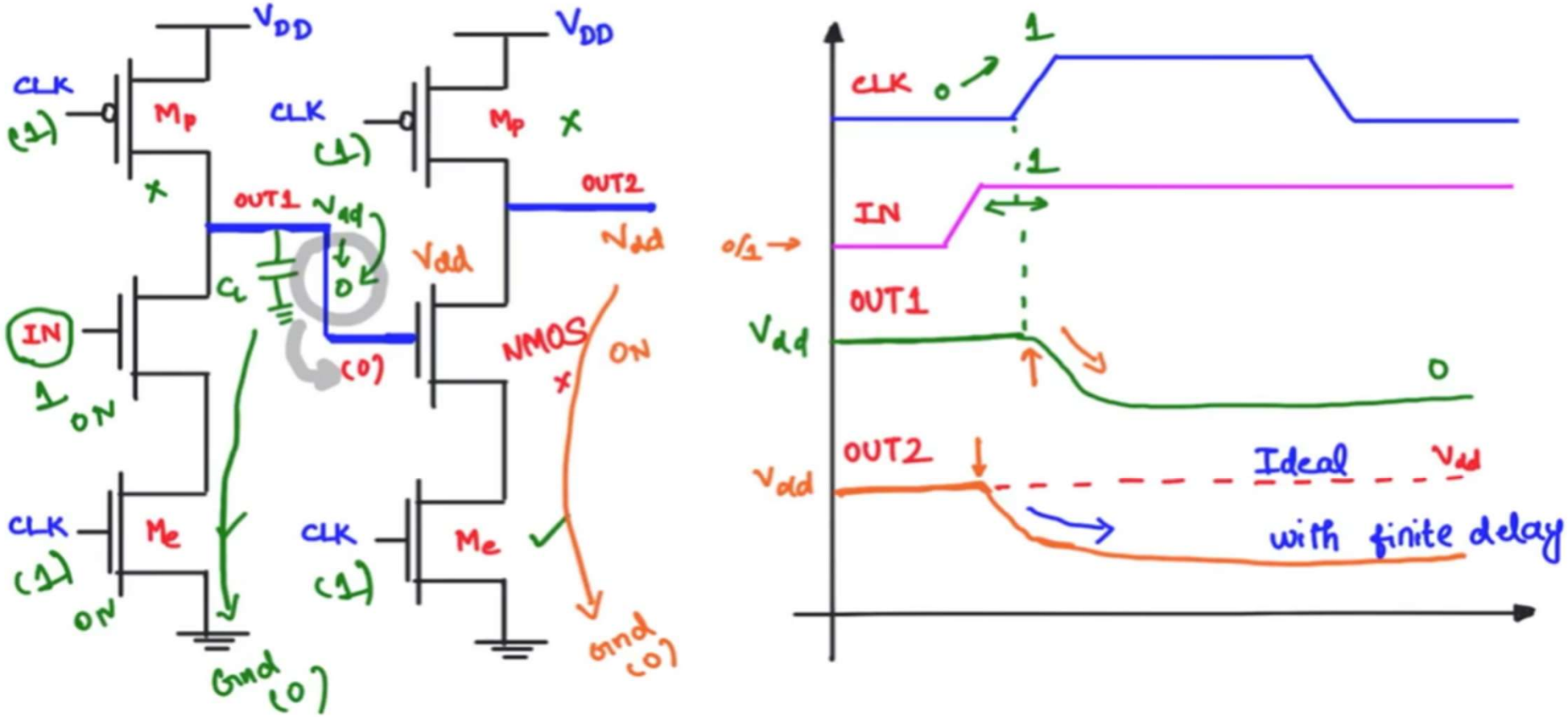
- The nMOS PDN network is similar to static CMOS.
- No. of transistors required is much lower than static CMOS.
  Dynamic (N + 2) versus Static (2N)
- No static current path between V_{DD} and GND. It consumes no static power.
- Less number of transistors, therefore faster switching speeds.

Dynamic CMOS



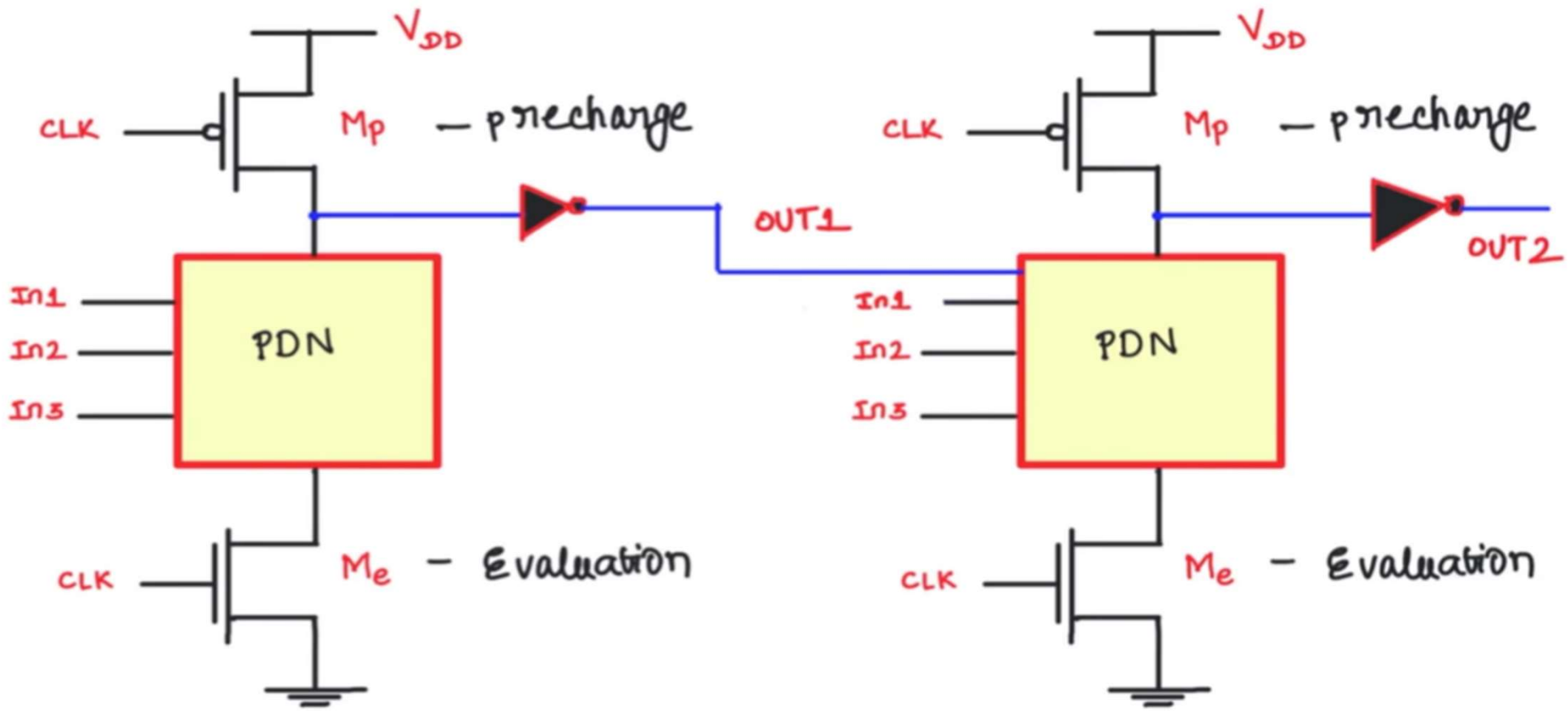
Domino CMOS

Cascading Problem of Dynamic Logic Gates



Domino CMOS

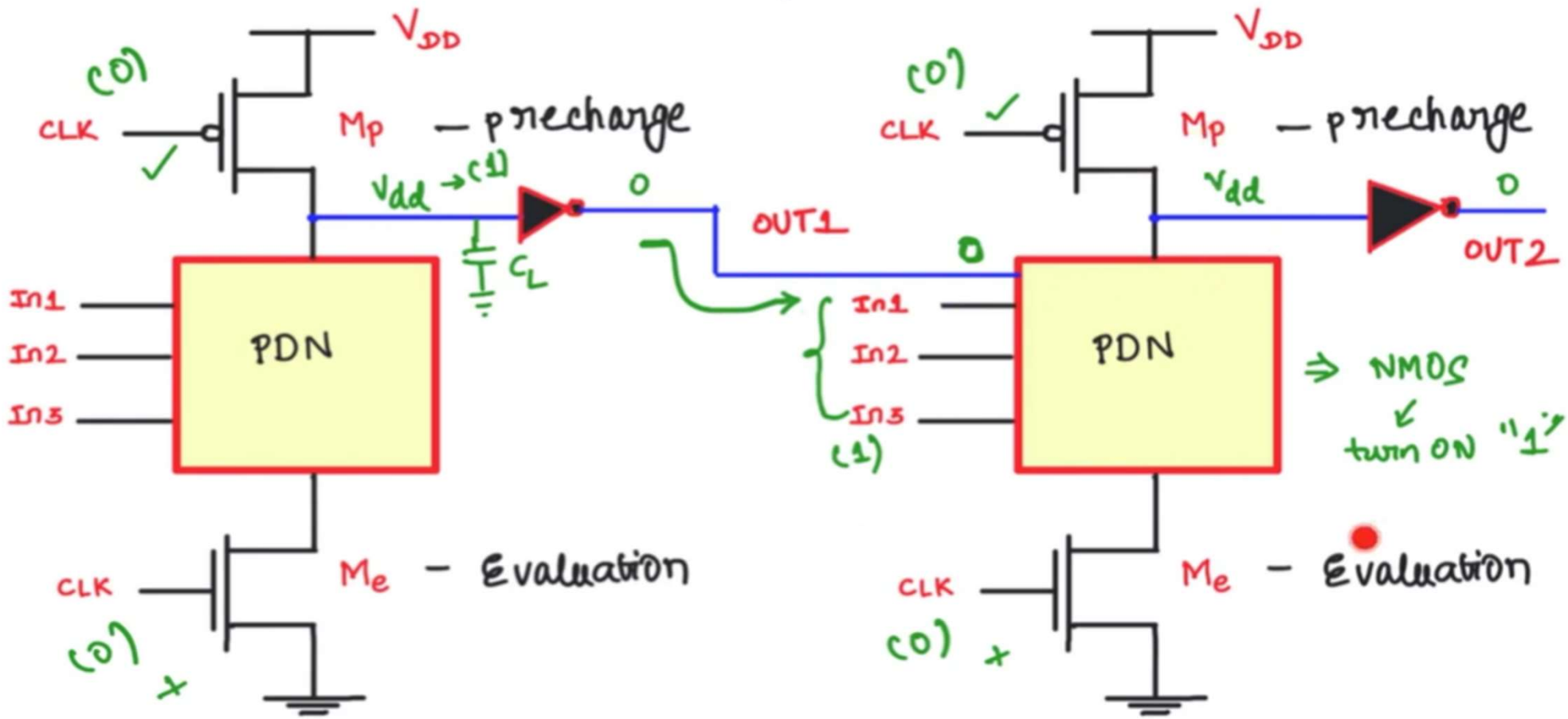
DOMINO LOGIC DESIGN



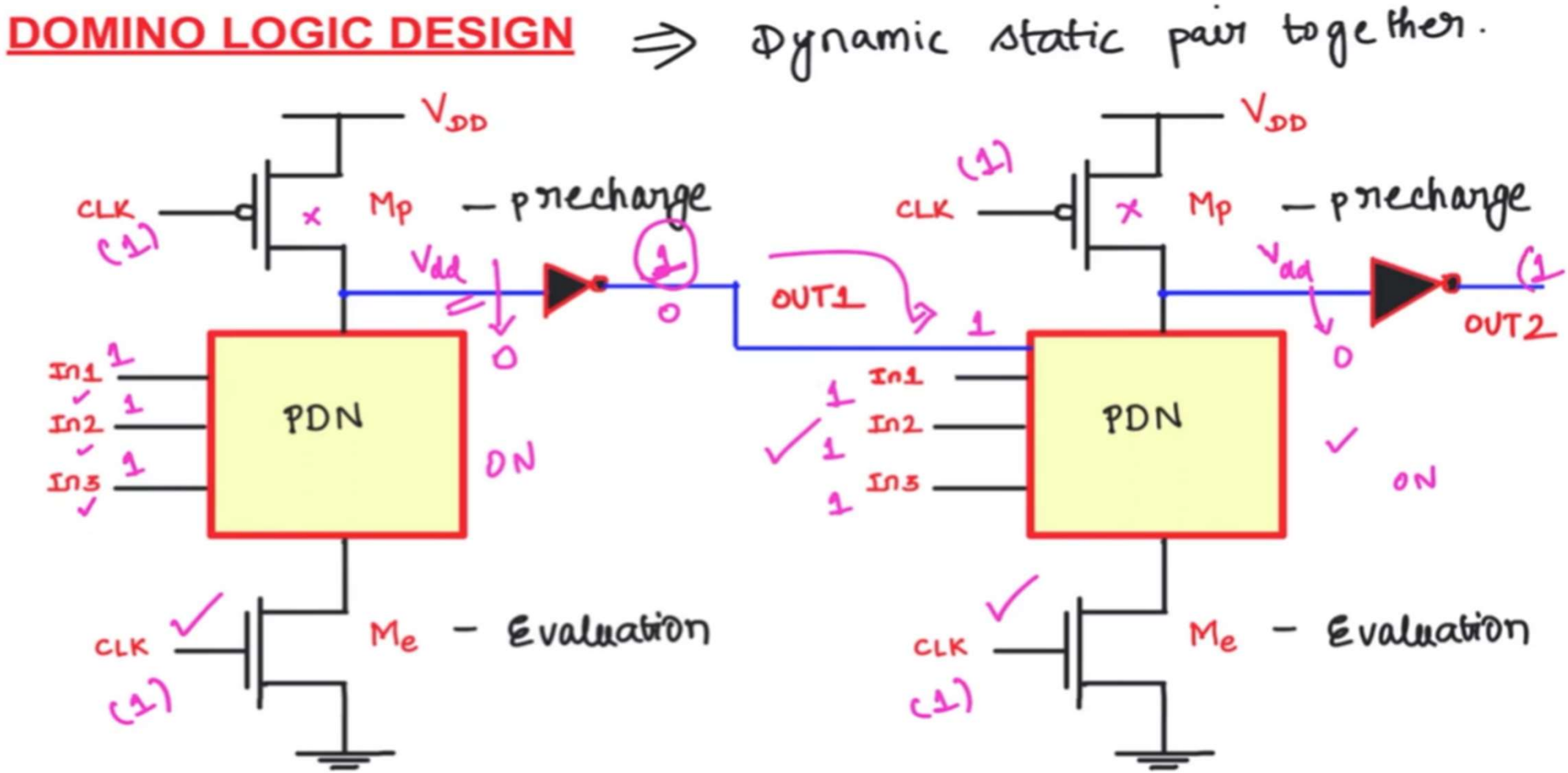
Domino CMOS

DOMINO LOGIC DESIGN

⇒ Dynamic static pair together.

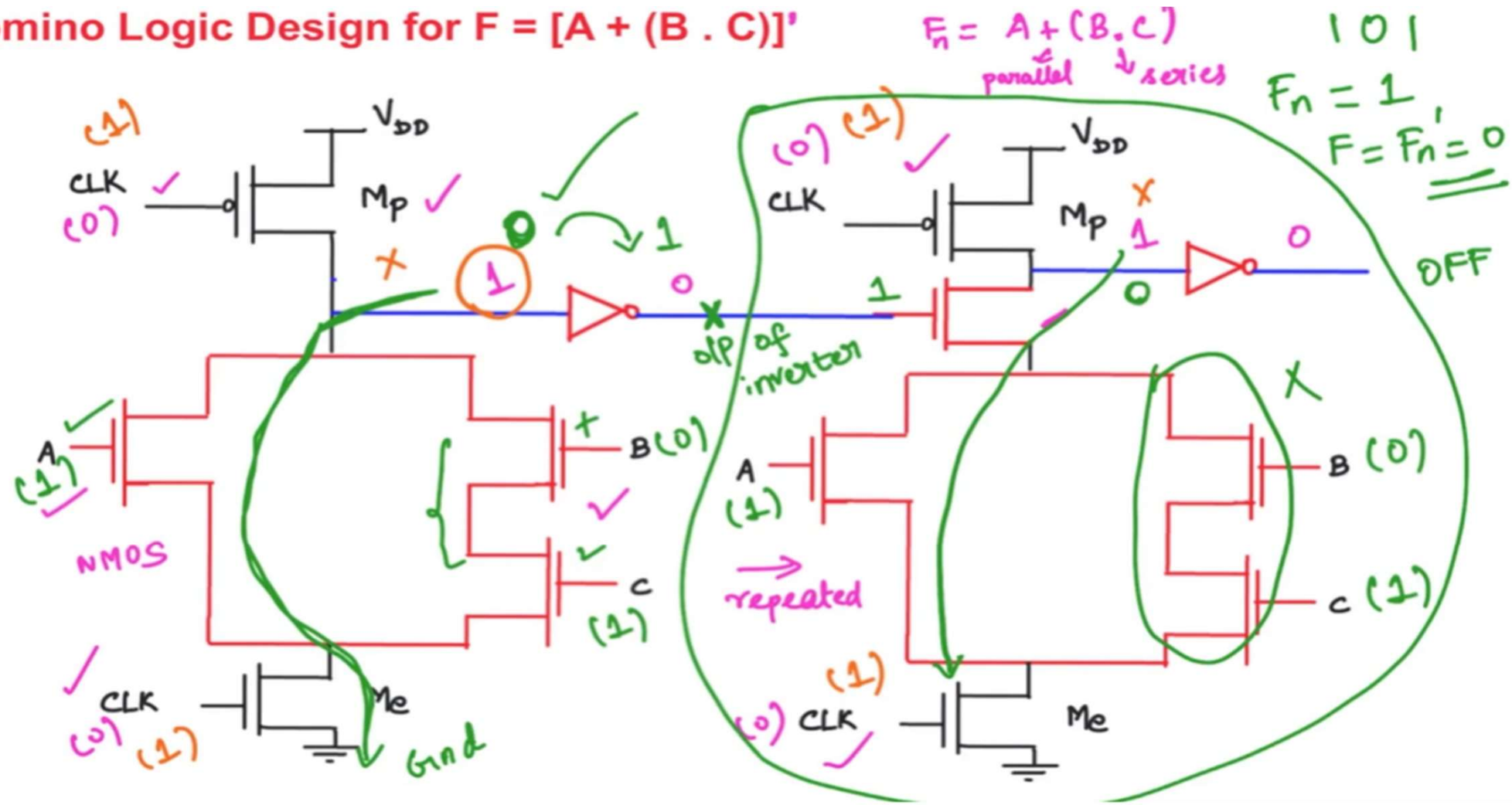


Domino CMOS


DOMINO LOGIC DESIGN
⇒ Dynamic static pair together.
VDD
CLK
Mp
– precharge
Vdd
OUT1
OUT2
In1
In2
In3
PDN
ON
Me
– Evaluation

Domino CMOS_CASCADING

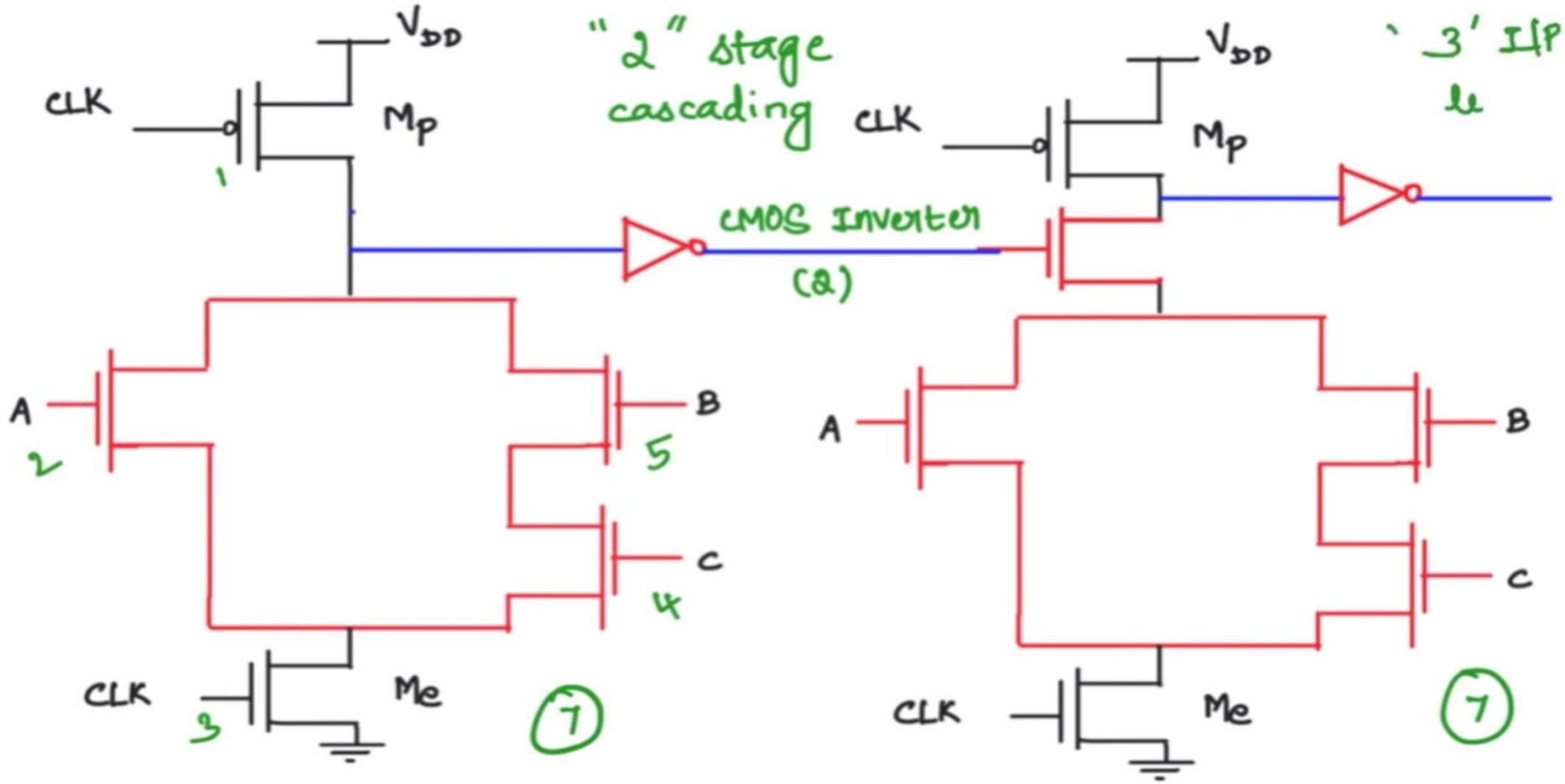
Domino Logic Design for F = [A + (B . C)]'



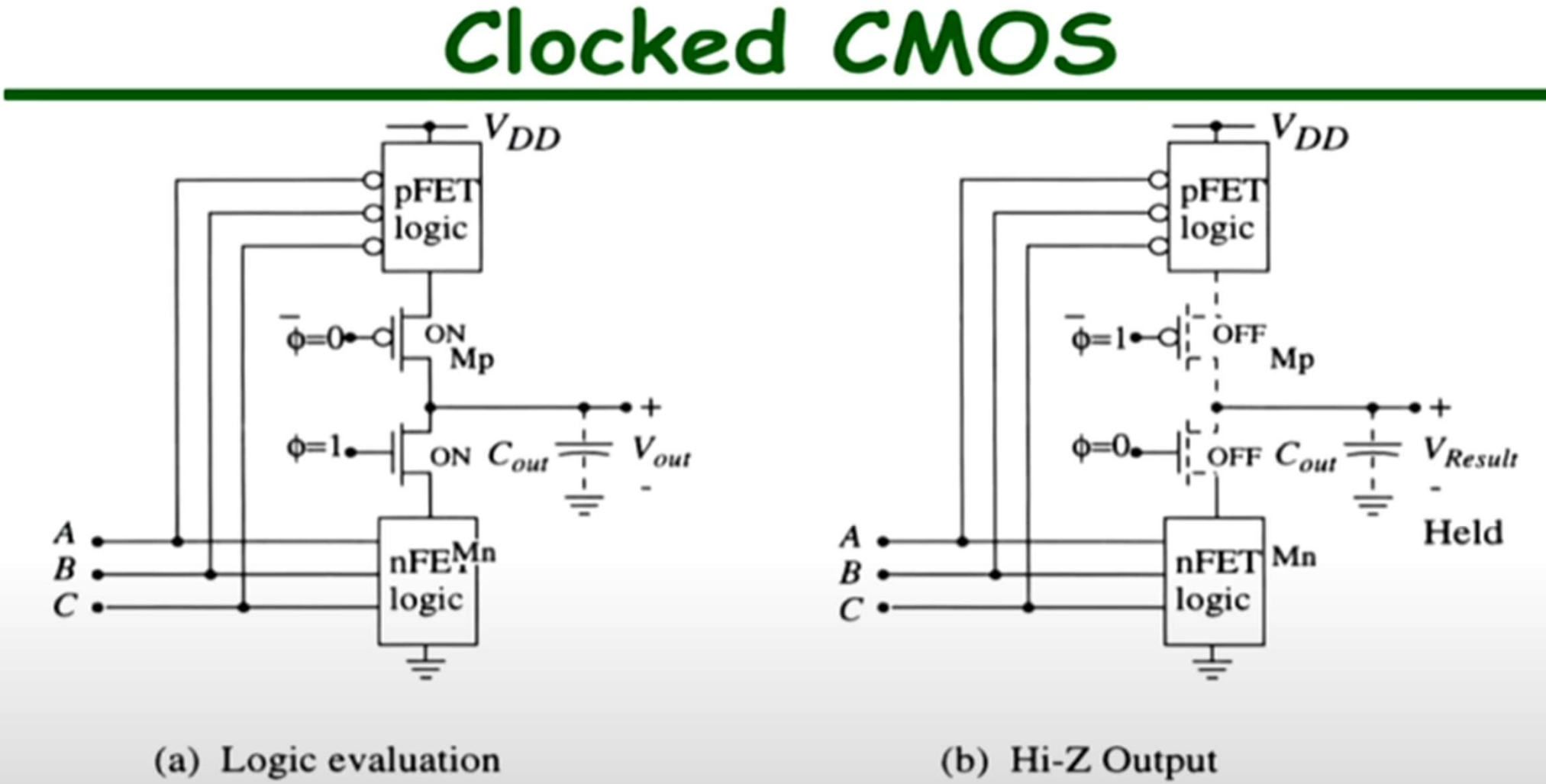
Domino CMOS_CASCADING

Domino Logic Design for F = [A + (B . C)]'

NO. OF TRANSISTORS = 14



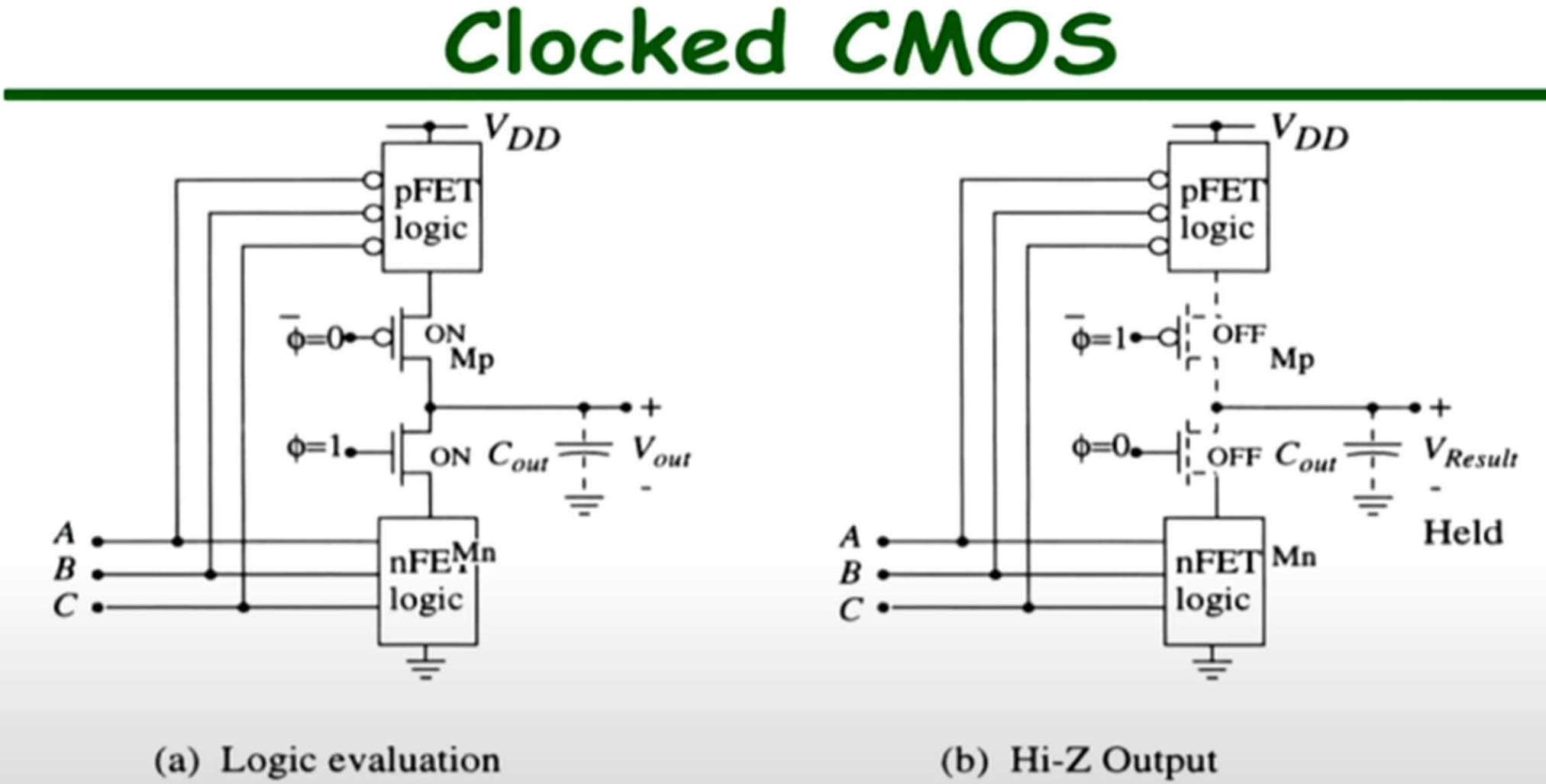
Clocked CMOS



(a) Logic evaluation

(b) Hi-Z Output

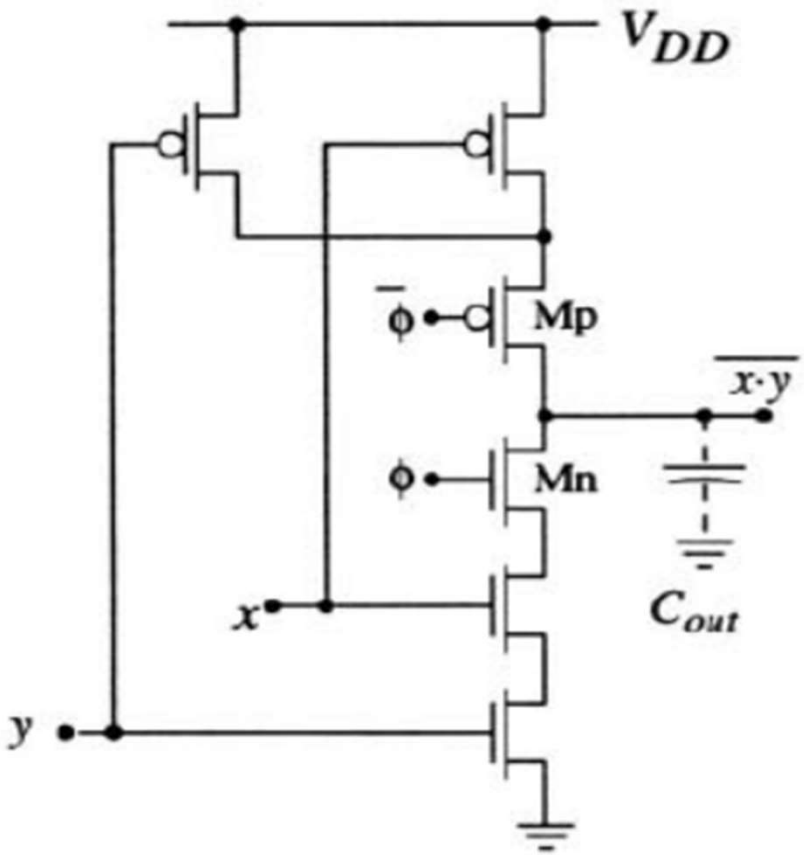
Clocked CMOS



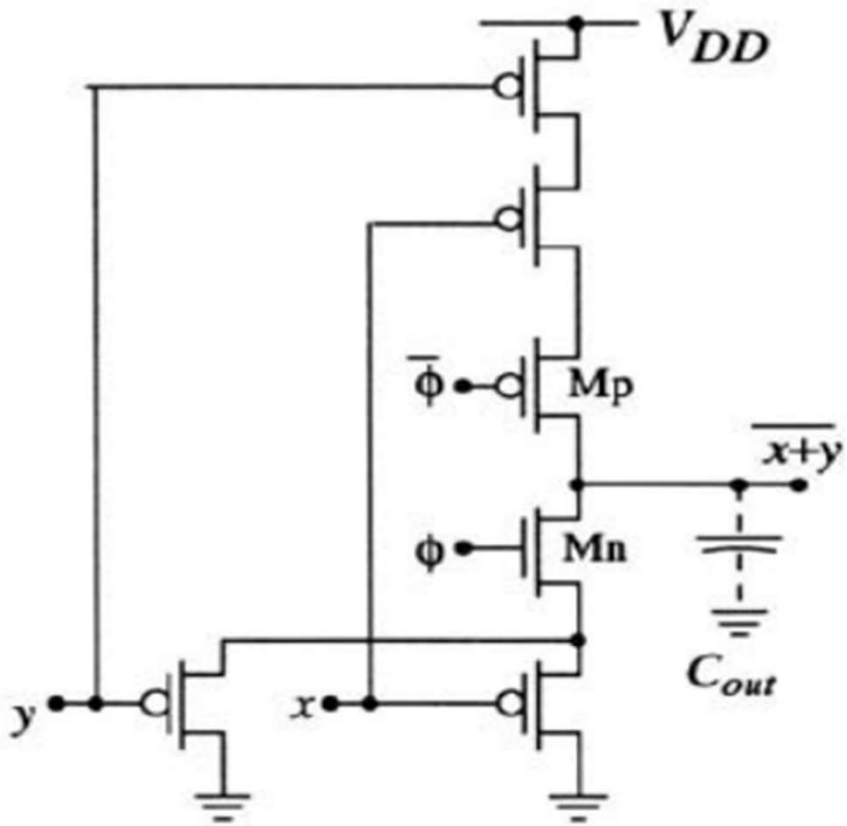
(a) Logic evaluation

(b) Hi-Z Output

Clocked CMOS

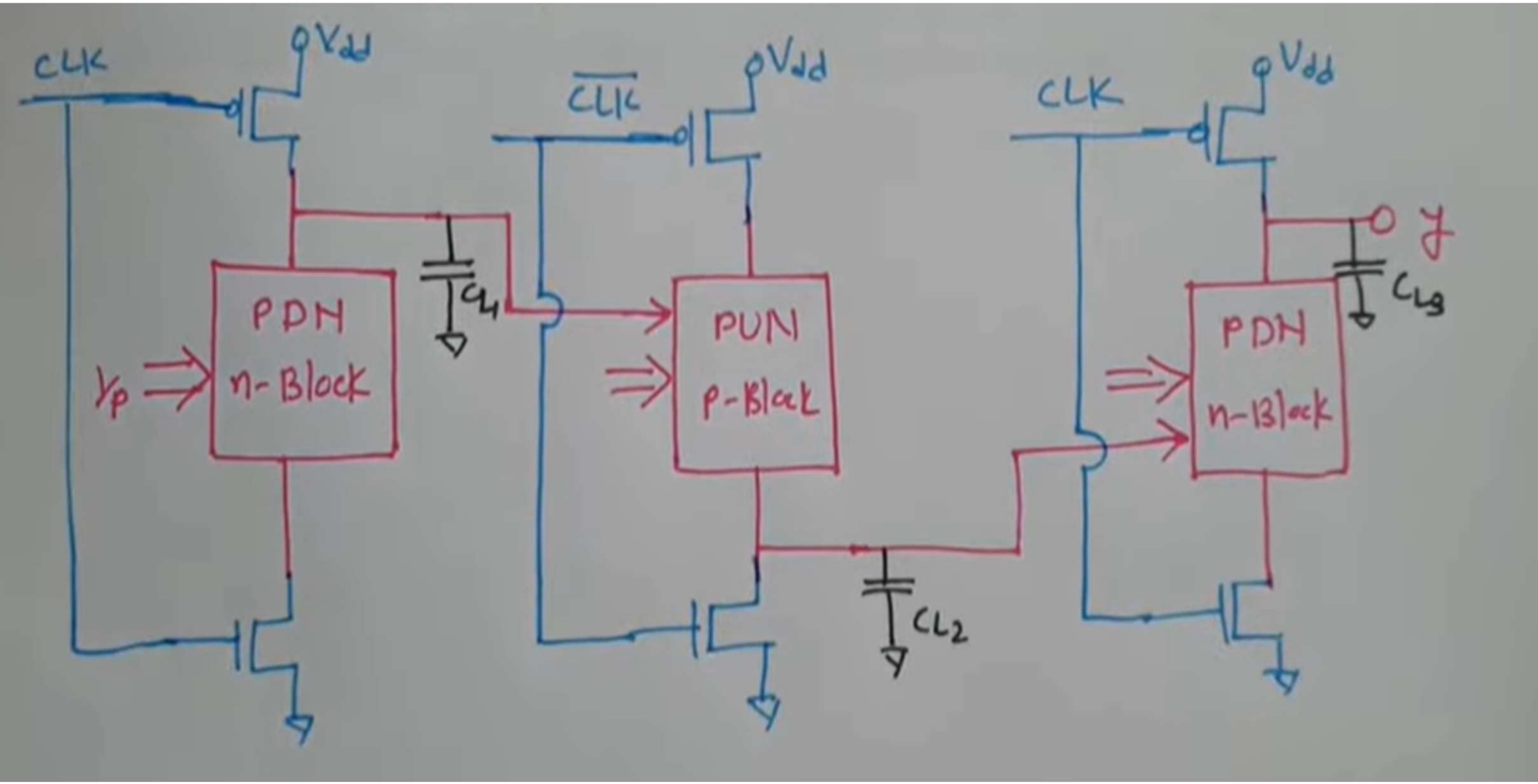


(a) NAND2 gate

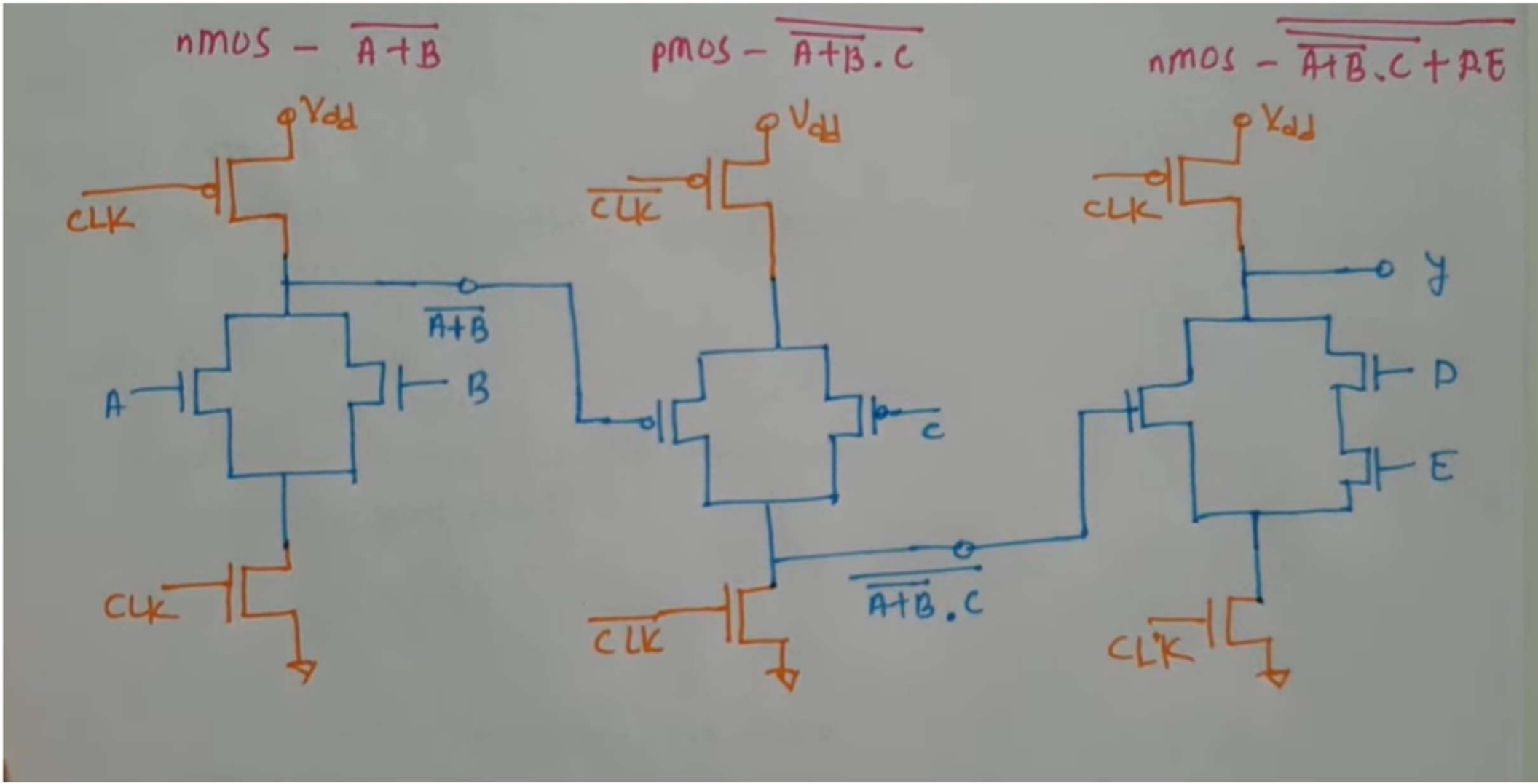


(b) NOR2 gate

NP CMOS


CLK
Vdd
PDN
n-Block
Vp
CL1
CLK
Vdd
PUN
p-Block
CL2
CLK
Vdd
PDN
n-Block
y
CL3

NP CMOS


nMOS – $\overline{A+B}$
pMOS – $\overline{\overline{A+B}.C}$
nMOS – $\overline{\overline{\overline{A+B}.C}+D.E}$
Vdd
CLK
A
B
$\overline{A+B}$
C
$\overline{A+B}.C$
Y
D
E