CMOS Logic Gates

Unit -2

by
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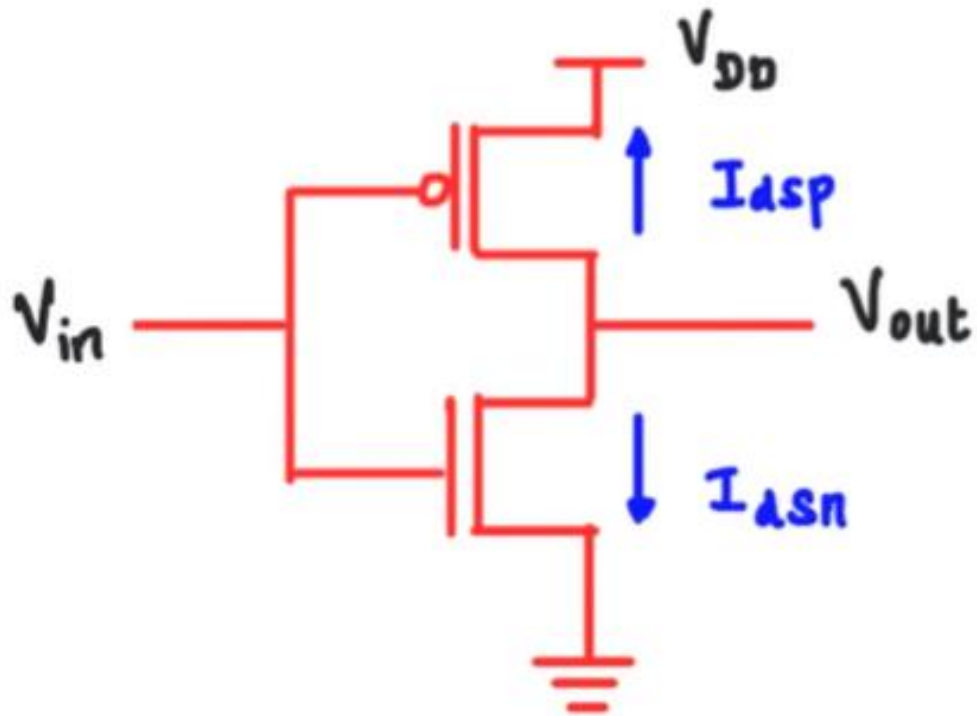
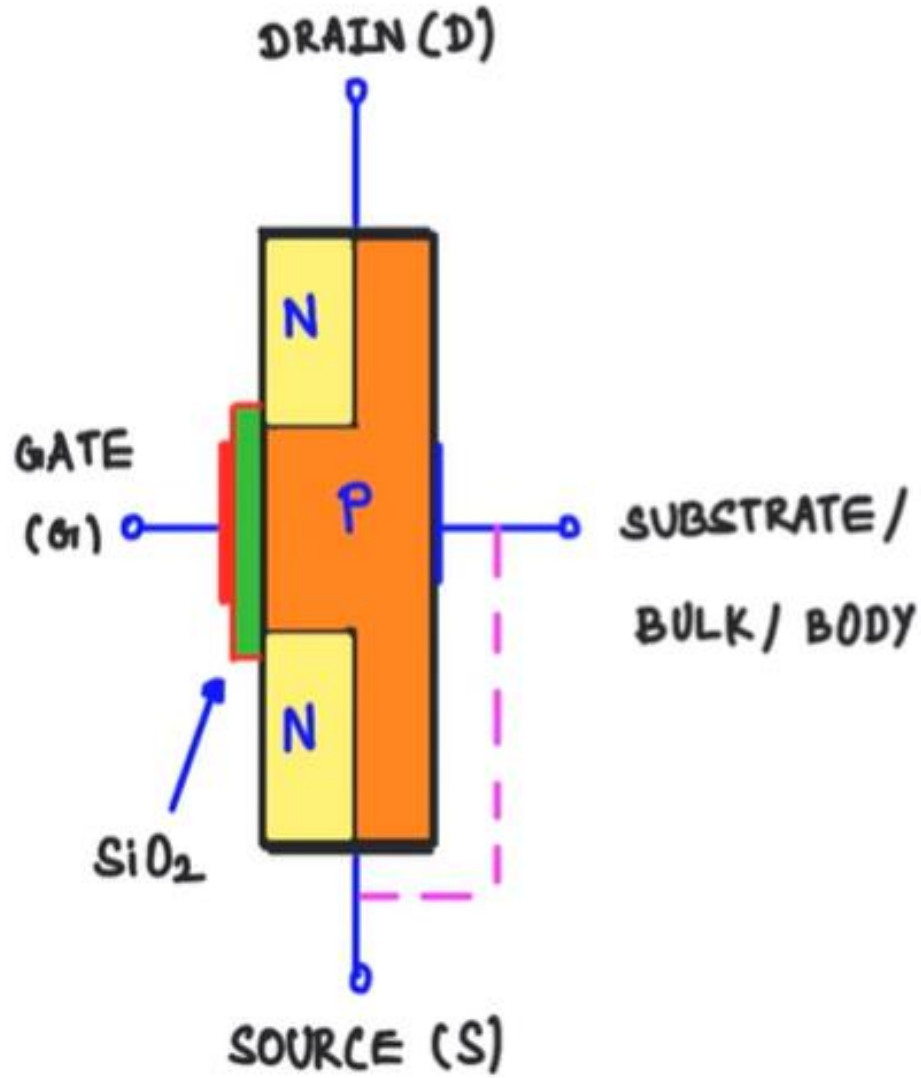
CMOS INVERTER

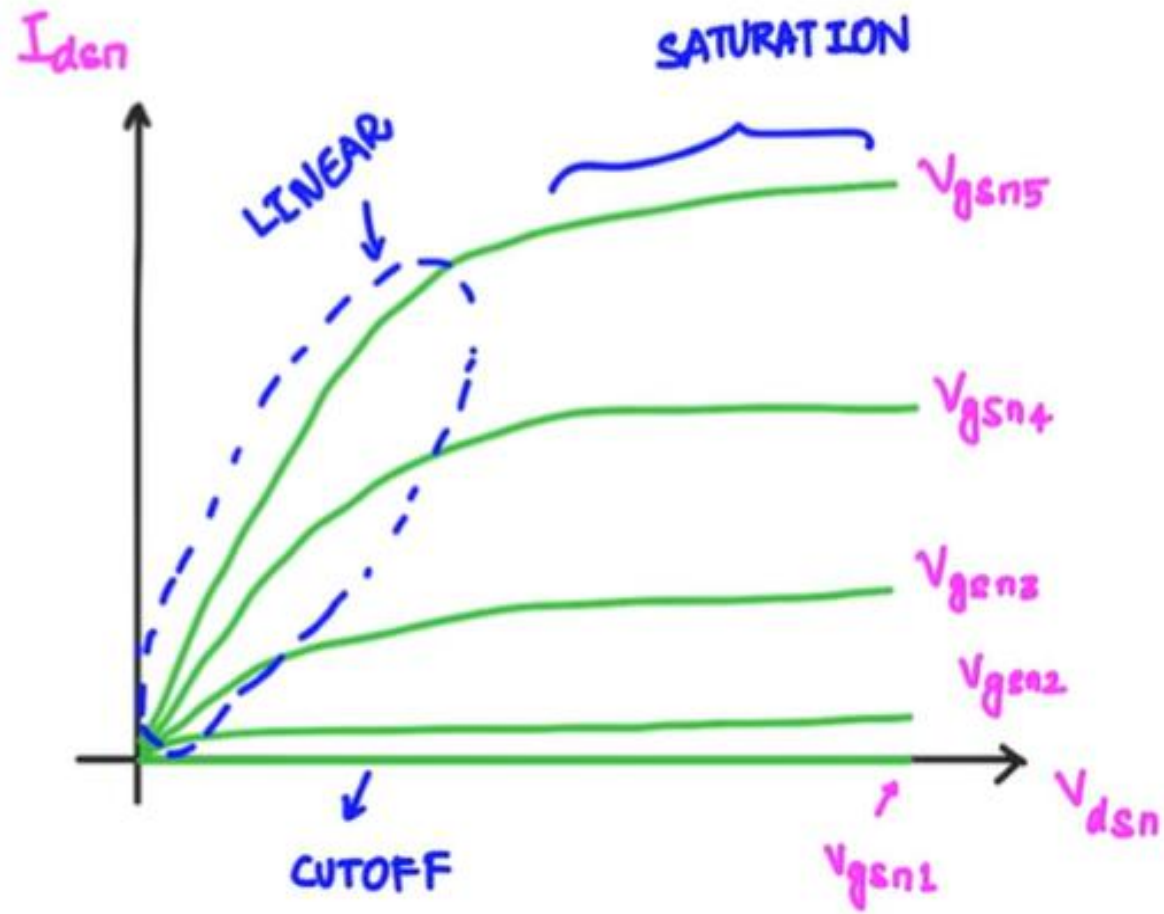
The DC input-output transfer characteristic is also called as **Voltage Transfer Characteristics (VTC).**

It is simply a plot of the output voltage (Vout) as a function of the input voltage (Vin) .



I - V CHARACTERISTICS OF NMOS

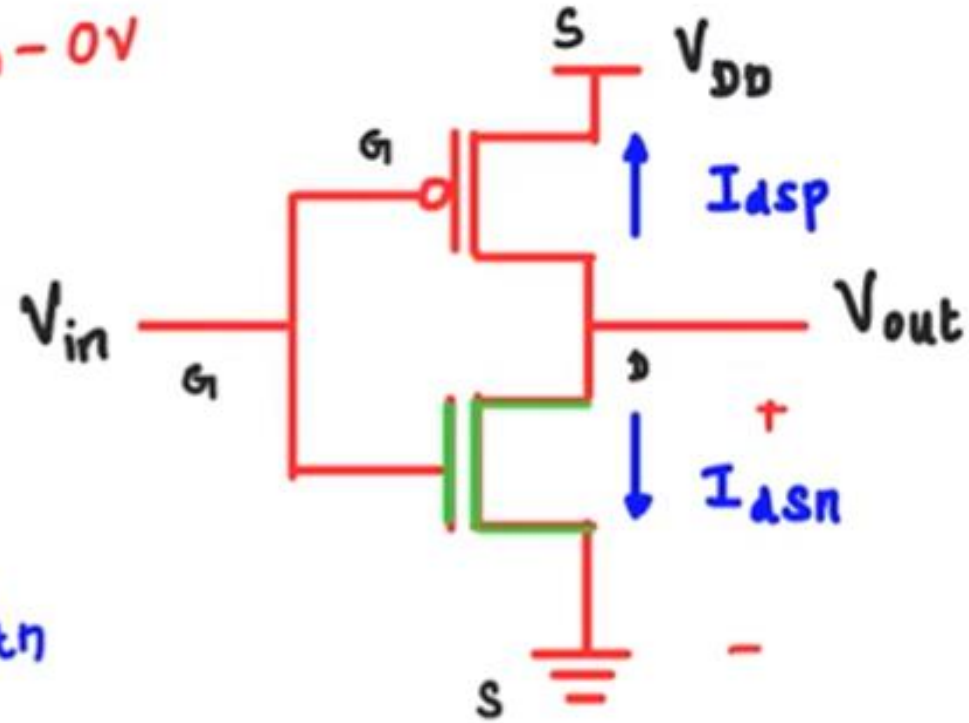




NMOS OPERATION

; $V_{gsn} = V_g - V_s = V_{in} - 0V$

$V_{gsn} = V_{in}$ ✓



CUT-OFF: $V_{gsn} < V_{tn}$

$V_{in} < V_{tn}$

LINEAR: $V_{gsn} > V_{tn}$; $V_{dsn} < V_{gsn} - V_{tn}$

$V_{in} > V_{tn}$; $V_{out} < V_{in} - V_{tn}$

$V_{dsn} = V_d - V_s$

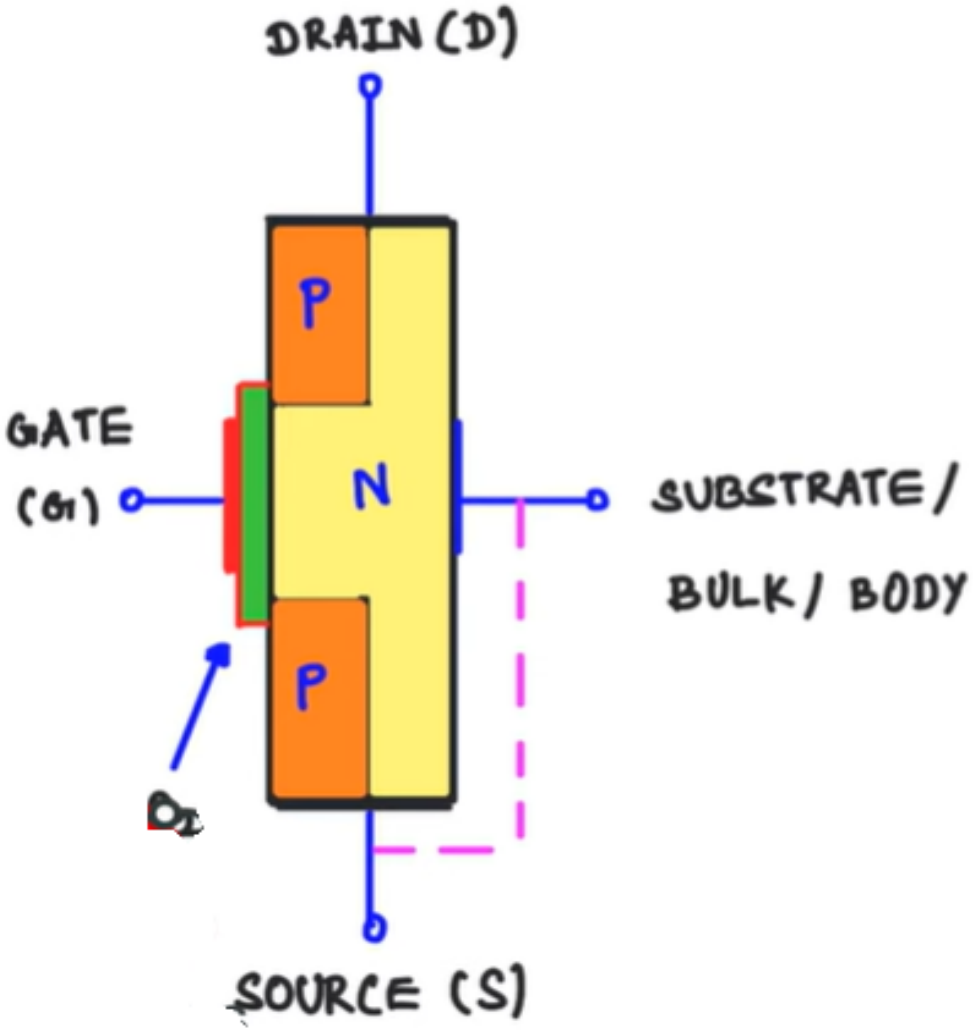
$= V_{out} - 0V$

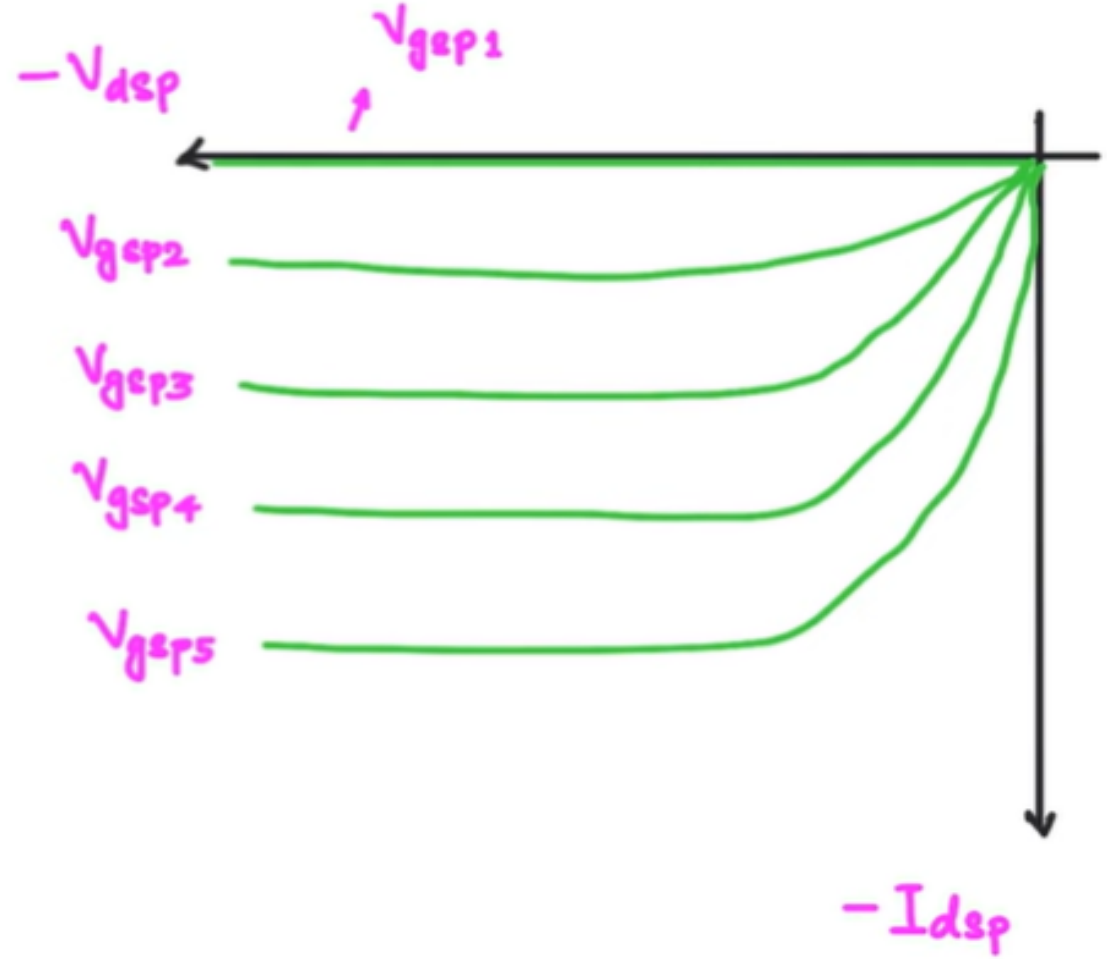
$\therefore V_{dsn} = V_{out}$

SATURATION: $V_{gsn} > V_{tn}$; $V_{dsn} > V_{gsn} - V_{tn}$

$V_{in} > V_{tn}$; $V_{out} > V_{in} - V_{tn}$

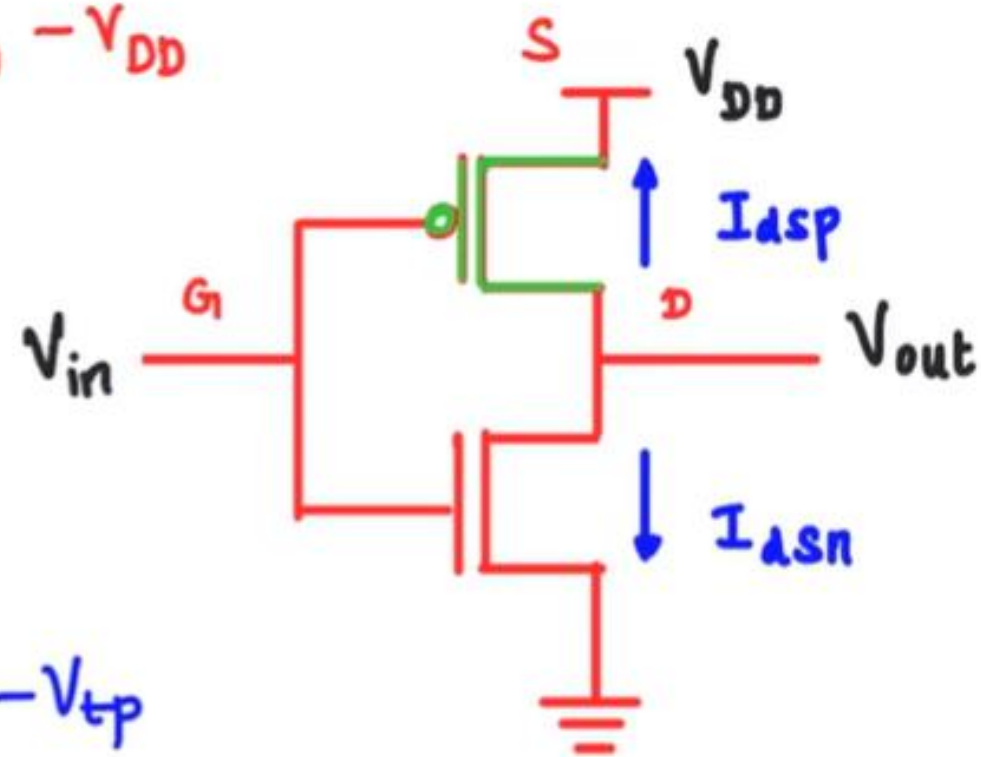
I - V CHARACTERISTICS OF PMOS





PMOS OPERATION

$V_{gsp} = V_g - V_s = V_{in} - V_{DD}$



CUT-OFF: $V_{gsp} > V_{tp}$

$V_{in} - V_{DD} > V_{tp}$

$V_{in} > V_{DD} + V_{tp}$

LINEAR: $V_{gsp} < V_{tp}$; $V_{dsp} > V_{gsp} - V_{tp}$

$V_{in} - V_{DD} < V_{tp}$ $\qquad$ $V_{out} > V_{in} - V_{tp}$

$\therefore V_{in} < V_{DD} + V_{tp}$

$V_{dsp} = V_d - V_s$

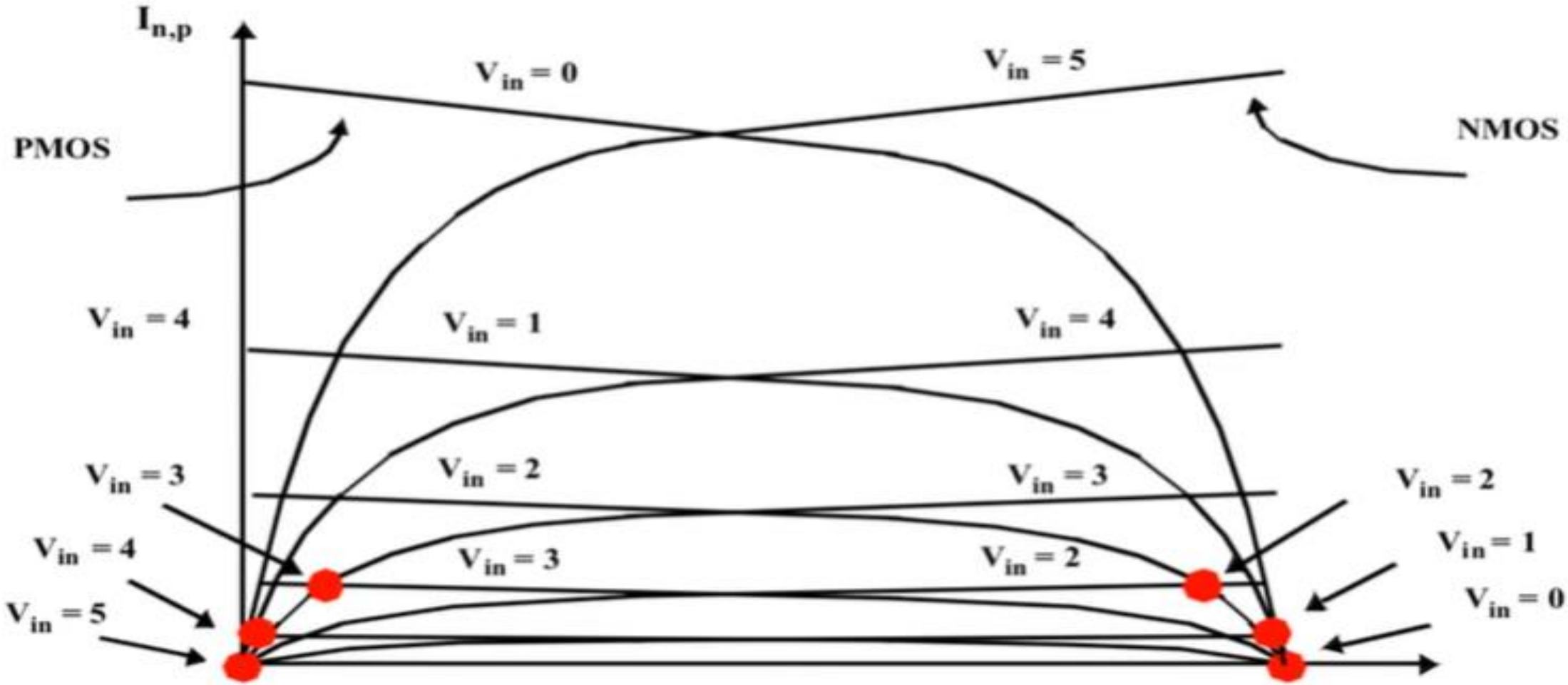
$V_{dsp} = V_{out} - V_{DD}$

SATURATION: $V_{gsp} < V_{tp}$; $V_{dsp} < V_{gsp} - V_{tp}$

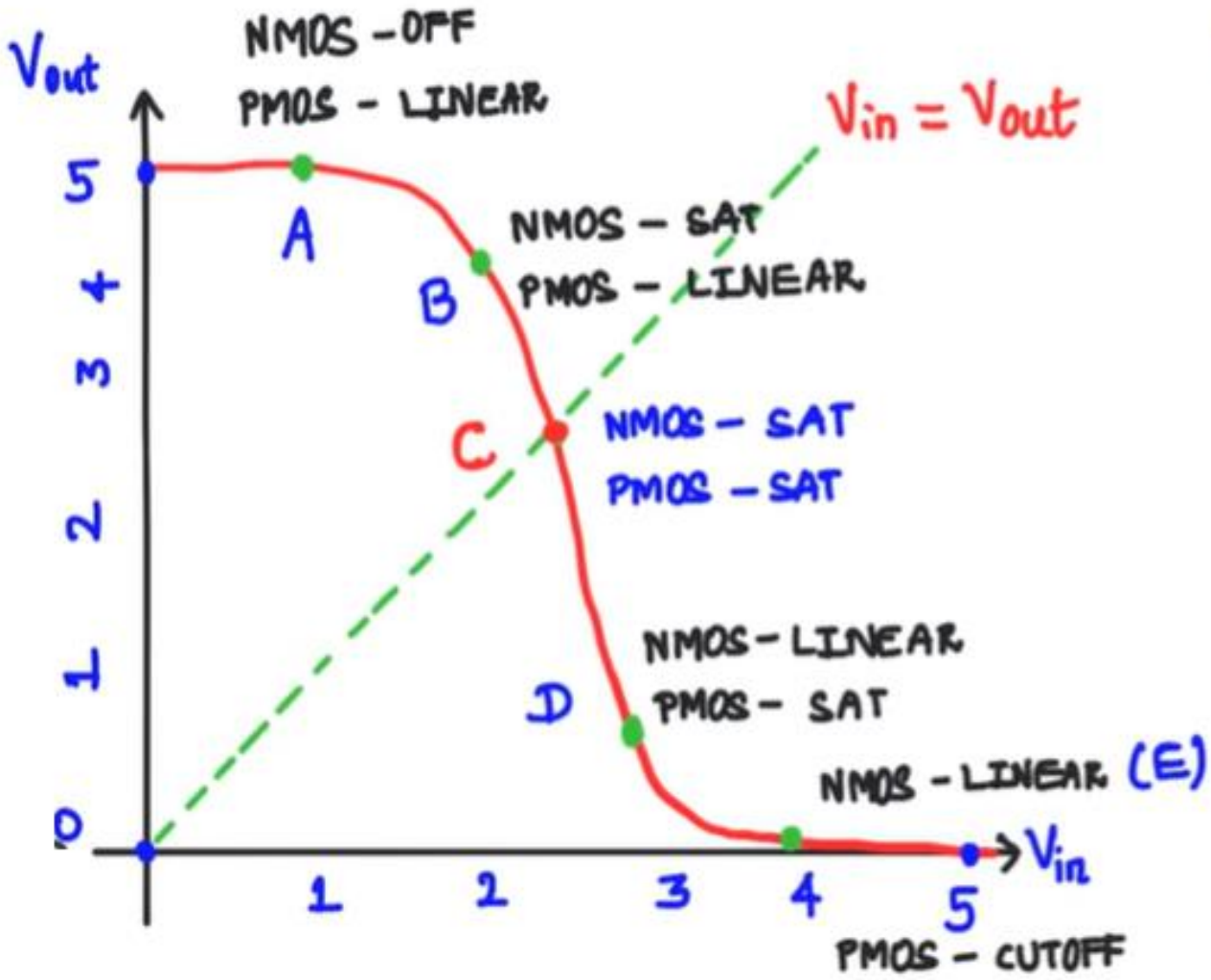
$V_{in} < V_{DD} + V_{tp}$; $V_{out} < V_{in} - V_{tp}$

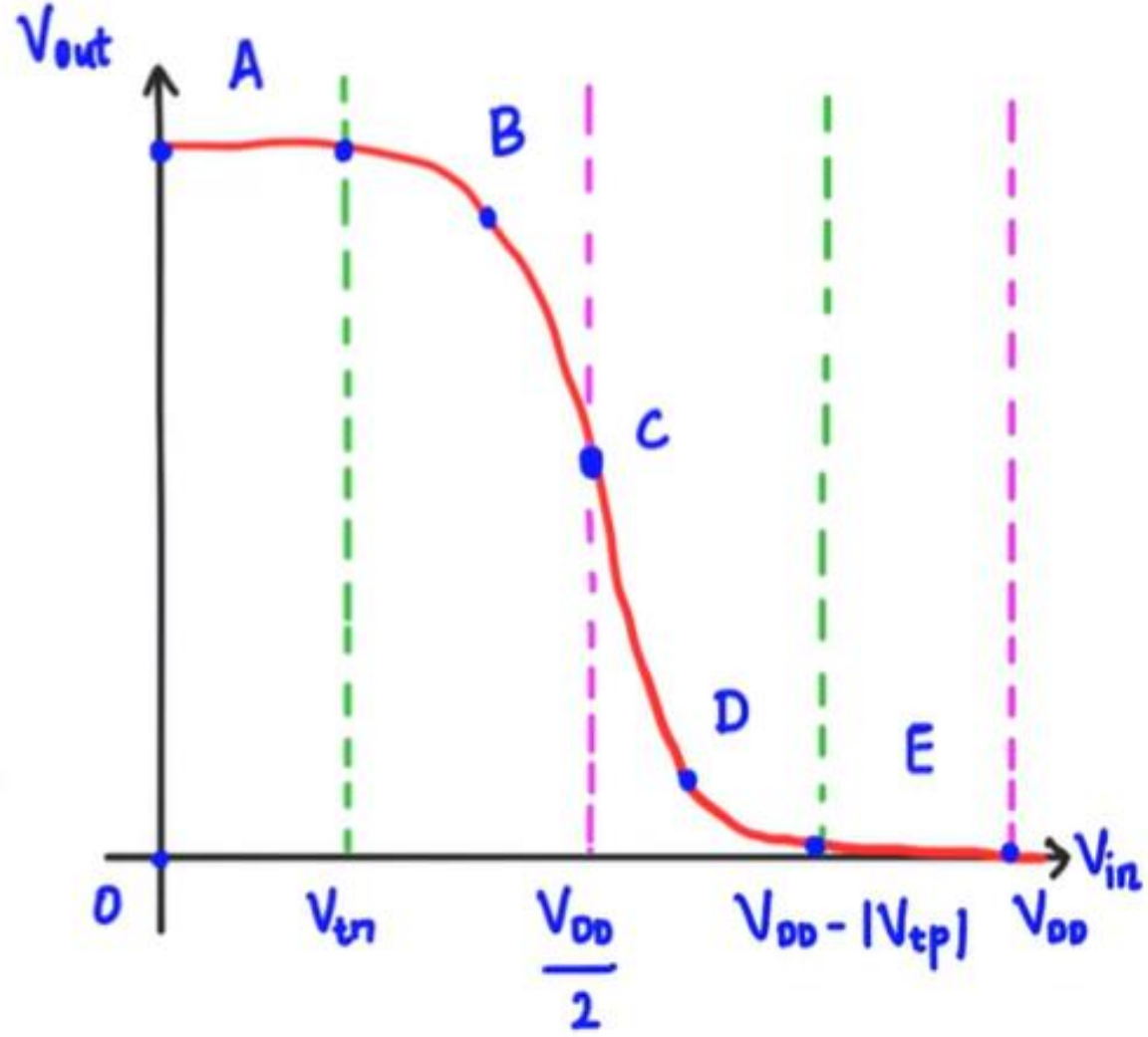
$V_{tp} < 0$

CMOS INVERTER - VTC GRAPH



CMOS INVERTER - VTC GRAPH





(SAT - SATURATION)

CASE 1: $V_{in} = 0\ V; V_{out} = 5\ V$ ⇒ REGION "A"

$V_{tn} = 1\ V;$
$V_{tp} = -1\ V$

NMOS: $V_{gsn} = V_g - V_s = V_{in} - V_s = 0 - 0 = 0V$

$\therefore \quad V_{gsn} < V_{tn} \Rightarrow$ CUT-OFF

PMOS: $V_{gsp} = V_{in} - V_{dd} = 0 - 5 = -5$

$V_{gsp} < V_{tp} \Rightarrow$ L/S

$V_{dsp} = V_{out} - V_{dd} = 0V$

$V_{gsp} - V_{tp} = -5 - (-1) = -5 + 1 = -4V \quad \therefore V_{dsp} > V_{gsp} - V_{tp}$

⇒ LINEAR

CASE 2: $V_{in} = 1\ V;\ V_{out} = 5\ V$ $\Rightarrow$ REGION "B"

$V_{tn} = 1\ V;$
$V_{tp} = -1\ V$

NMOS: $V_{gsn} = V_{in} = 1V \quad \therefore \quad V_{gsn} = V_{tn}$

NMOS – ON $\therefore$ L/S

$V_{dsn} = V_{out} = 5V$

$V_{gsn} - V_{tn} = 0V \quad \therefore \quad V_{dsn} > V_{gsn} - V_{tn} \quad \therefore$ NMOS - saturation

PMOS: $V_{gsp} = V_{in} - V_{dd} = 1 - 5 = -4V \quad \therefore \quad V_{gsp} < V_{tp} \therefore$ PMOS–ON

L/S

$V_{dsp} = V_{out} - V_{dd} = 0V \quad ; \quad V_{gsp} - V_{tp} = -4 + 1 = -3V$

$\therefore \quad V_{dsp} > V_{gsp} - V_{tp} \quad \therefore$ PMOS - linear.

CASE 3: $V_{in} = 2.5\ V;\ V_{out} = 2.5\ V \Rightarrow$ REGION "C"

$V_{tn} = 1\ V;$
$V_{tp} = -1\ V$

NMOS: $V_{gsn} = V_{in} = 2.5V > V_{tn}$ ∴ NMOS-ON (L/S)

$V_{dsn} = V_{out} = 2.5 > V_{gsn} - V_{tn}$ ∴ NMOS – saturation

$2.5 > 1.5V$.

PMOS: $V_{gsp} = V_{in} - V_{dd} = -2.5V < V_{tp}$ ∴ PMOS-ON (L/S)

$V_{dsp} = V_{out} - V_{dd} = 2.5 - 5 = -2.5$

and $V_{gsp} - V_{tp} = -2.5 + 1 = -1.5$

∴ $V_{dsp} < V_{gsp} - V_{tp}$ ∴ PMOS – saturation

CASE 4: $V_{in} = 4\ V;\ V_{out} = 1\ V$ ⇒ REGION "D"

$V_{tn} = 1\ V;$
$V_{tp} = -1\ V$

NMOS: $V_{gsn} = V_{in} = 4V > V_{tn}$ ∴ NMOS - ON (L/S)

$V_{dsn} = V_{out} = 1V$; $V_{gsn} - V_{tn} = 4 - 1 = 3V$

∴ $V_{dsn} < V_{gsn} - V_{tn}$ ∴ NMOS - linear

PMOS: $V_{gsp} = V_{in} - V_{dd} = 4 - 5 = -1V$; ∴ $V_{gsp} = V_{tp}$ ∴ PMOS - ON (L/S)

$V_{dsp} = V_{out} - V_{dd} = 5 - 5 = 0V$;

$V_{gsp} - V_{tp} = -1 + 1 = 0V$ ∴ $V_{dsp} = V_{gsp} - V_{tp}$

PMOS - saturation.

CASE 5: $V_{in} = 5\ V; V_{out} = 0\ V$ ⇒ REGION "E"

$V_{tn} = 1\ V;$
$V_{tp} = -1\ V$

NMOS: $V_{gsn} = V_{in} = 5V > V_{tn}$ ∴ NMOS -ON (L/S)

$V_{dsn} = V_{out} = 0V$; $V_{gsn} - V_{tn} = 4V$.

∴ $V_{dsn} < V_{gsn} - V_{tn}$ ∴ NMOS -Linear

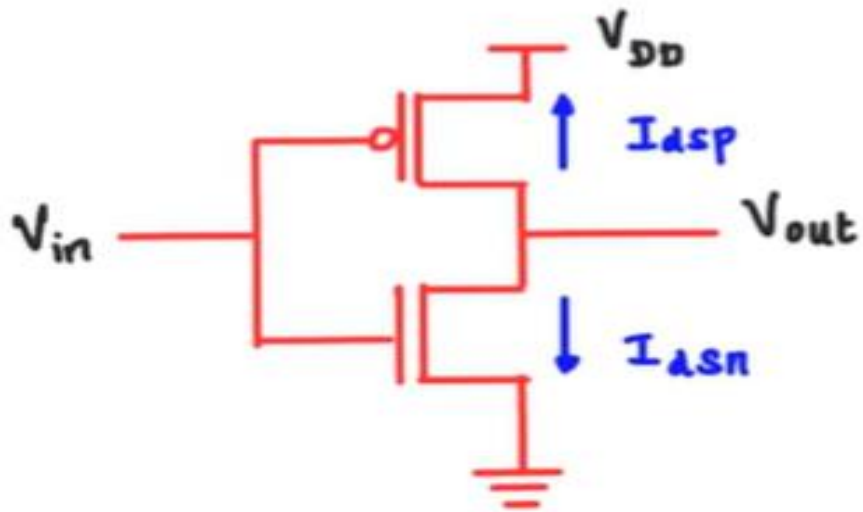
PMOS: $V_{gsp} = V_{in} - V_{dd} = 5 - 5 = 0V$

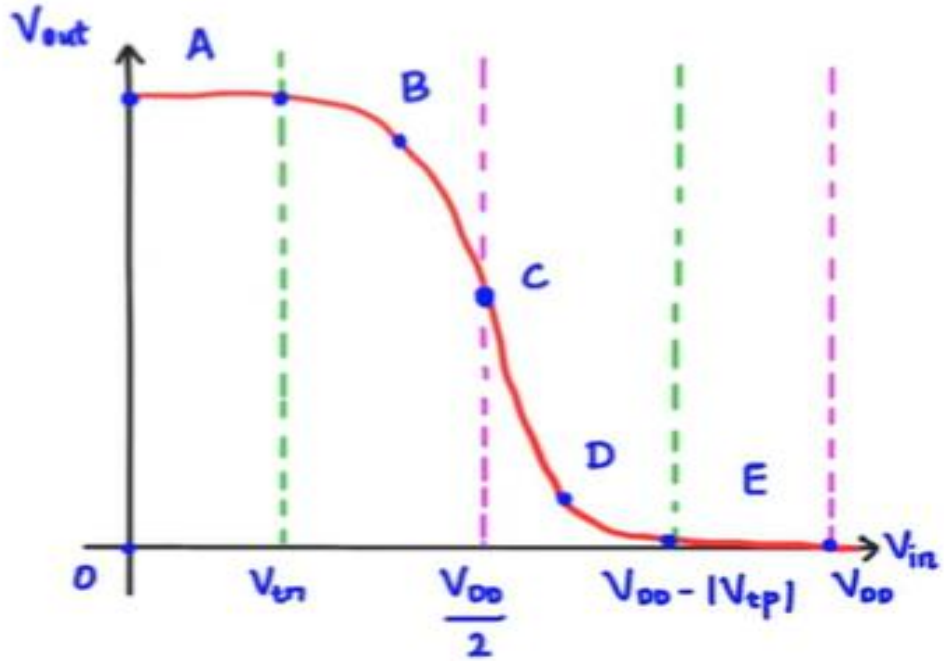
$V_{tp} = -1V$

∴ $V_{gsp} > V_{tp}$ ∴ PMOS -OFF (CUT-OFF)

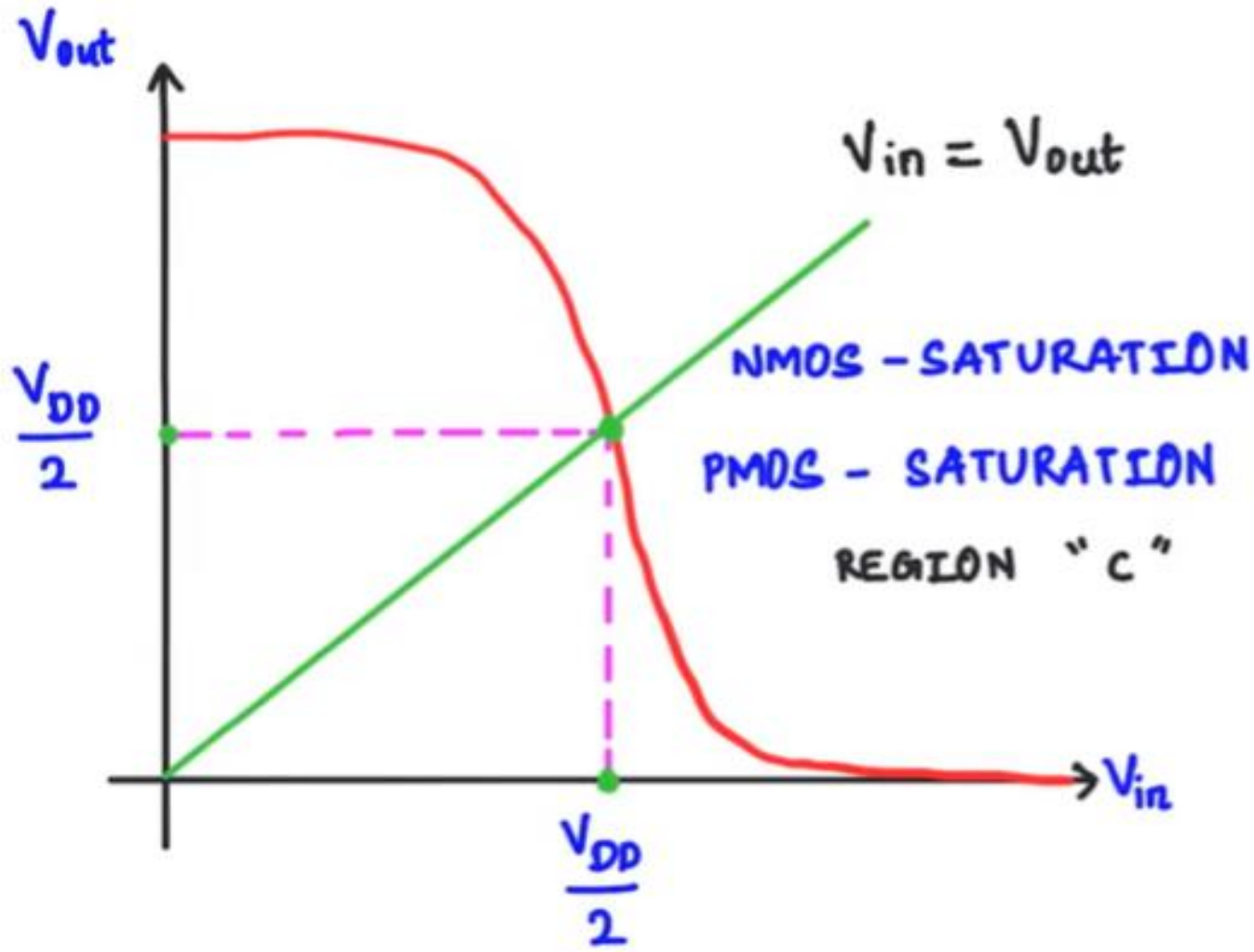
CMOS INVERTER - REGIONS OF OPERATION

REGION	CONDITION	PMOS	NMOS	OUTPUT
A	$0 \le V_{in} < V_{tn}$	Linear	Cut – Off	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	Linear	Saturation	$V_{out} > V_{DD} / 2$
C	$V_{in} = V_{DD}/2$	Saturation	Saturation	V_{out} sharps droply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	Saturation	Linear	$V_{out} < V_{DD} / 2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	Cut – Off	Linear	$V_{out} = 0$





CMOS INVERTER - SWITCHING THRESHOLD



$$I_{DSn} = -I_{DSp}$$

CMOS INVERTER - SWITCHING THRESHOLD

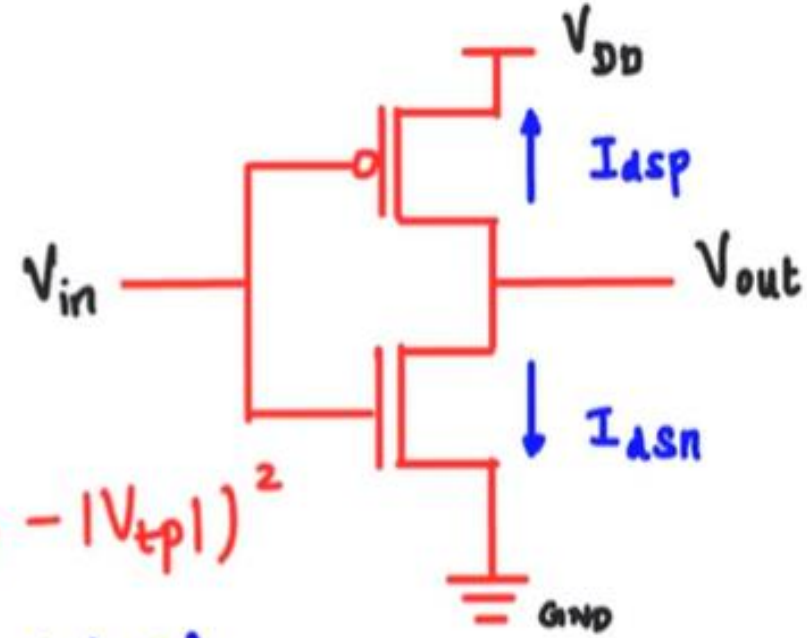
$V_{gs,n} = V_{in}$

$V_{ds,n} = V_{out}$

$V_{gs,p} = V_{in} - V_{DD}$

$V_{ds,p} = V_{out} - V_{DD}$

$$I_{DSn} = -I_{DSp}$$



$$\frac{\beta_n}{2}(V_{gs,n} - V_{tn})^2 = -\frac{\beta_p}{2} \times (V_{gs,p} - |V_{tp}|)^2$$

$$(V_{gs,n} - V_{tn}) = \sqrt{\beta_p/\beta_n}\,(V_{gs,p} - |V_{tp}|)$$

$$(V_{in} - V_{tn}) = \sqrt{\frac{\beta_p}{\beta_n}}\,(V_{in} - V_{DD} - |V_{tp}|)$$

CMOS INVERTER - SWITCHING THRESHOLD

$$(V_{in} - V_{tn}) = -\sqrt{\frac{\beta_p}{\beta_n}}\,(V_{in} - V_{DD} - |V_{tp}|)$$

$$V_{in} + \sqrt{\beta_p/\beta_n}\,V_{in} = V_{tn} + (V_{DD} + |V_{tp}|)\sqrt{\beta_p/\beta_n}$$

$$V_{in} = V_M = \frac{V_{tn} + (V_{DD} + |V_{tp}|)\sqrt{\beta_p/\beta_n}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}$$

CMOS INVERTER - SWITCHING THRESHOLD

$$V_{in} = V_M = \frac{V_{tn} + (V_{DD} + |V_{tp}|)\sqrt{\beta_p/\beta_n}}{1 + \sqrt{\frac{\beta_p}{\beta_n}}}$$

$\beta_n = \beta_p$ (Symmetrical CMOS Inverter)

$V_{tn} = -|V_{tp}|$

$$V_M = \frac{V_{DD}}{2}$$

CMOS INVERTER - Beta Ratio Effect

V_M = SWITCHING THRESHOLD = $\frac{V_{DD}}{2}$; $\beta = \frac{\beta_p}{\beta_n}$

$\beta = 1$ $\quad \beta_p = \beta_n$; $\mu_n \left(\frac{W}{L}\right)_n = \mu_p \left(\frac{W}{L}\right)_p$

$\mu_n \simeq 1500\ cm^2/V\text{-}s$

$\mu_p \simeq 500\ cm^2/V\text{-}s$

$\mu_n \simeq 3\mu_p \Rightarrow \left(\frac{W}{L}\right)_p = 3\left(\frac{W}{L}\right)_n$

$V_M = \frac{V_{DD}}{2}$

$\beta < 1$ $\quad \beta_n > \beta_p$

STRONG - nMOS $\Rightarrow$ LO SKEWED INVERTER

$\left(\frac{W}{L}\right)_n > \left(\frac{W}{L}\right)_p$; $\frac{V_{DD}}{2}$ ↓ curve shifts LEFT

$\beta > 1$ $\quad \beta_p > \beta_n$

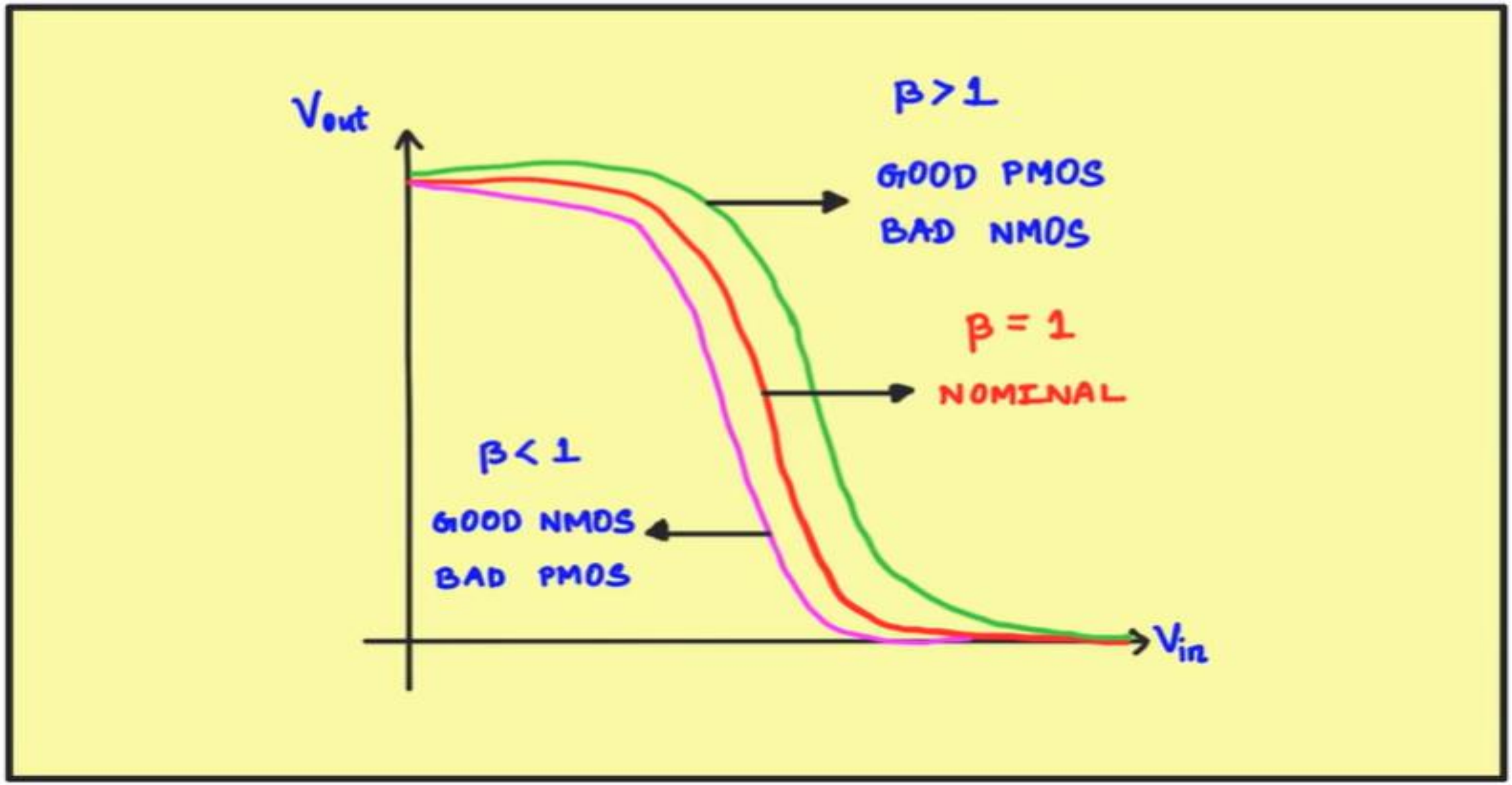
STRONG - PMOS

$\left(\frac{W}{L}\right)_p > \left(\frac{W}{L}\right)_n$

$\Rightarrow$ HI SKEWED INVERTER

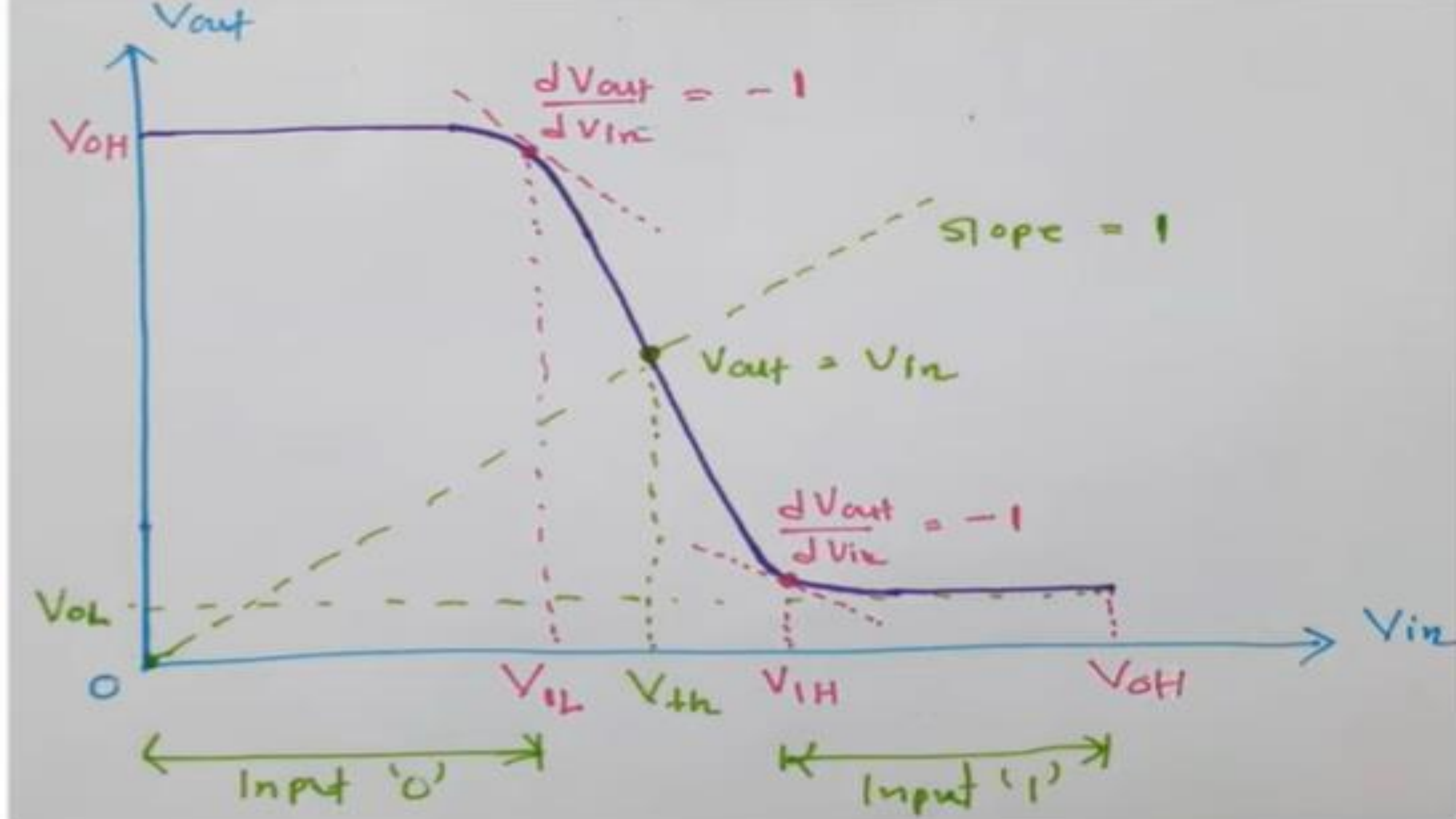
$\frac{V_{DD}}{2}$ ↑ curve shifts RIGHT.

CMOS INVERTER - Beta Ratio Effect

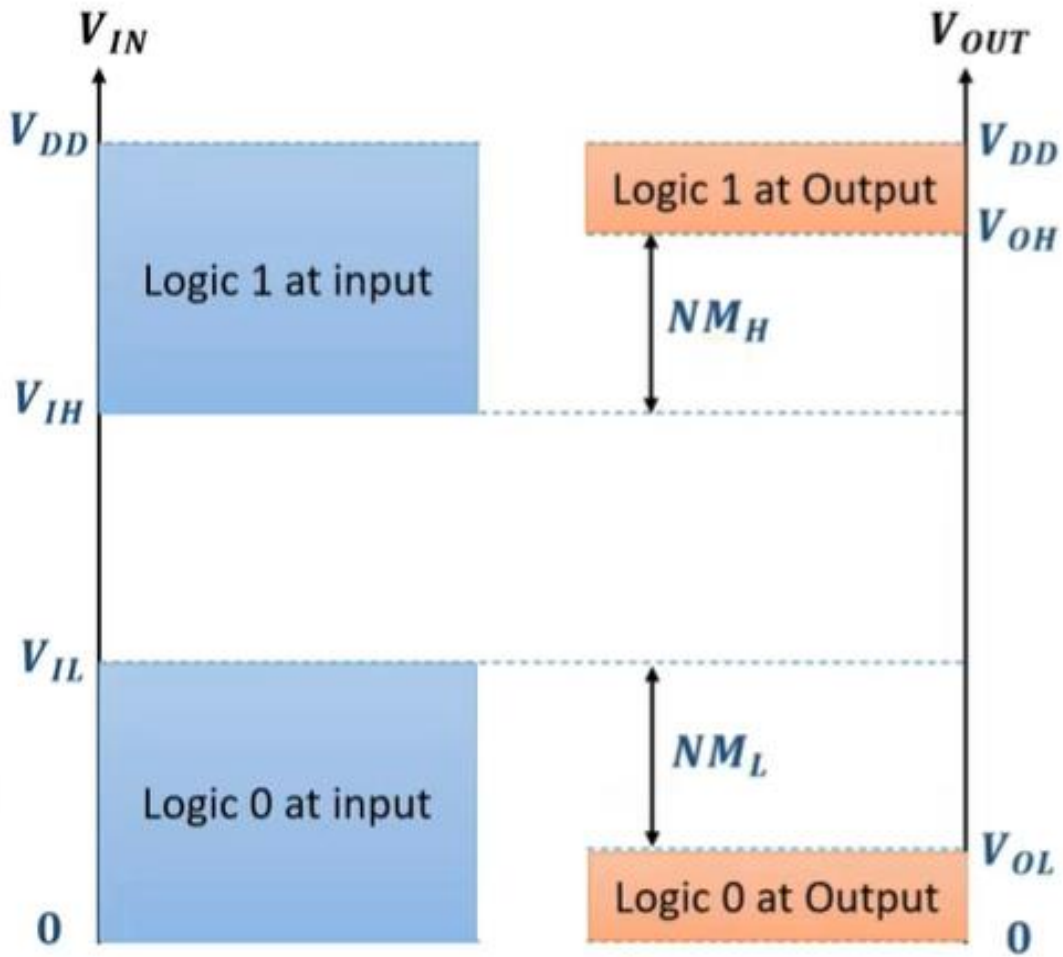


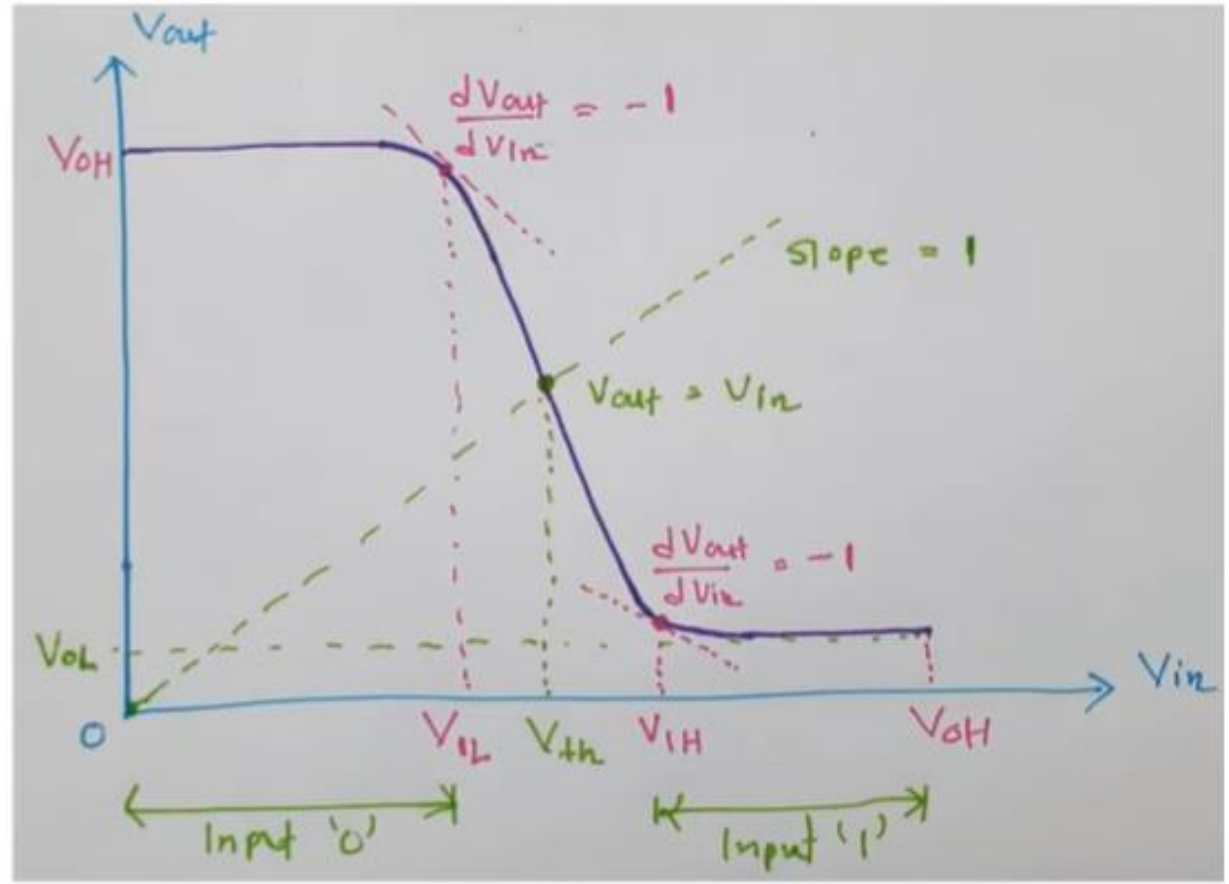
Basics of Noise Margin

- It explains, up to what extent, IC allows noise in transmission of logic '0' and logic '1'.
- In digital Integrated circuits, we don't receives only two voltages. (One for logic '0' and another for logic '1').
- Here we receives range of voltages and we identify logic '0' or '1' based on it.
- Received voltage range widens based on noise in the circuit. So for error less transmission, noise margin is required.


Vout
dVout/dVin = -1
VOH
Slope = 1
Vout = Vin
dVout/dVin = -1
VOL
Vin
0
VIL
Vth
VIH
VOH
Input '0'
Input '1'

Noise Margin based on VTC of inverter

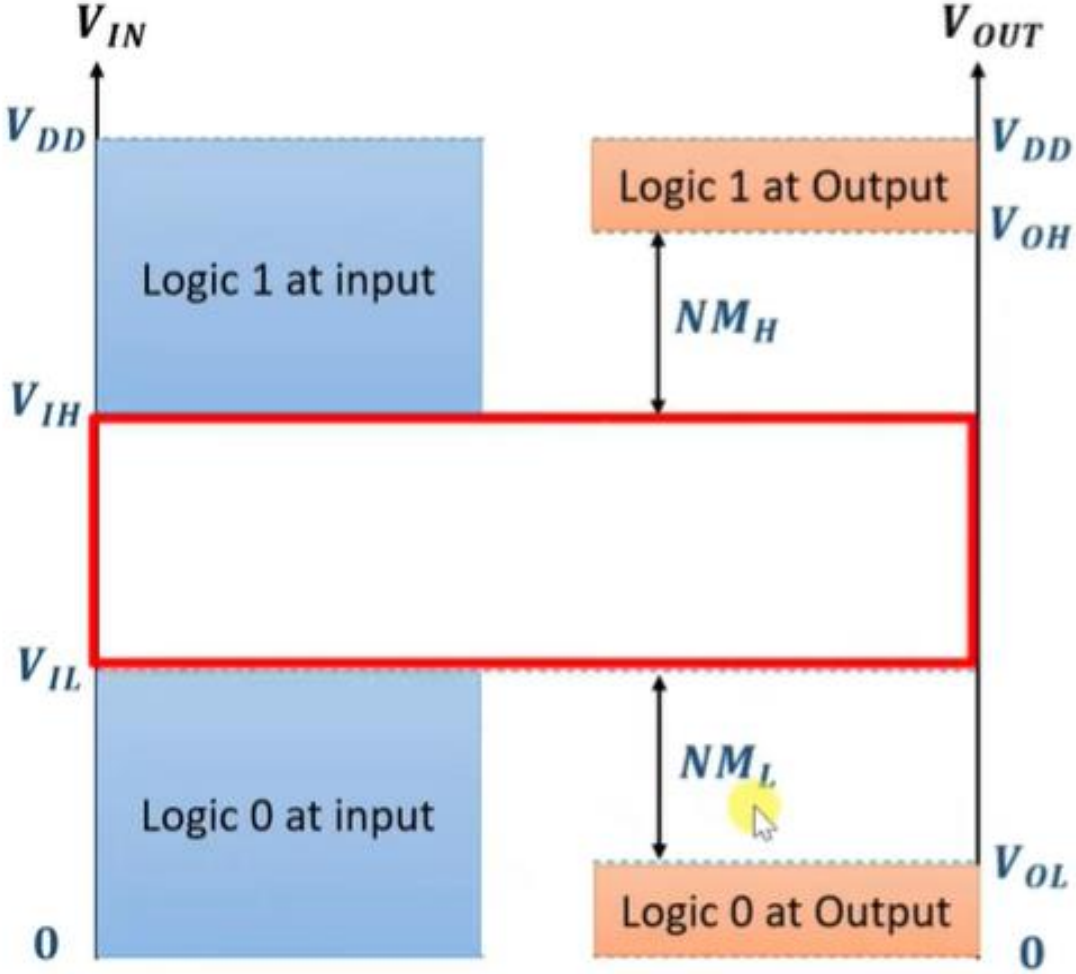


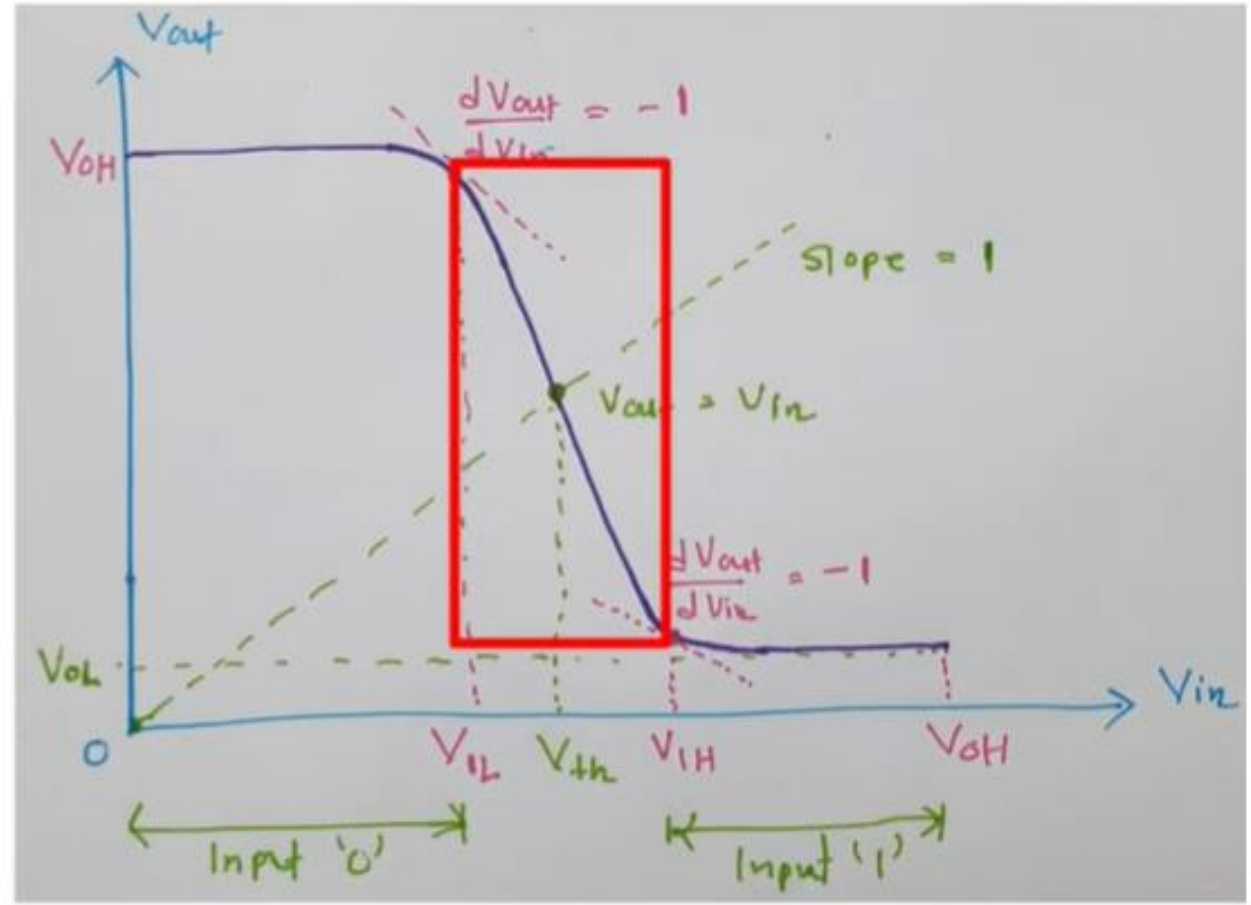


$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

Noise Margin based on VTC of inverter

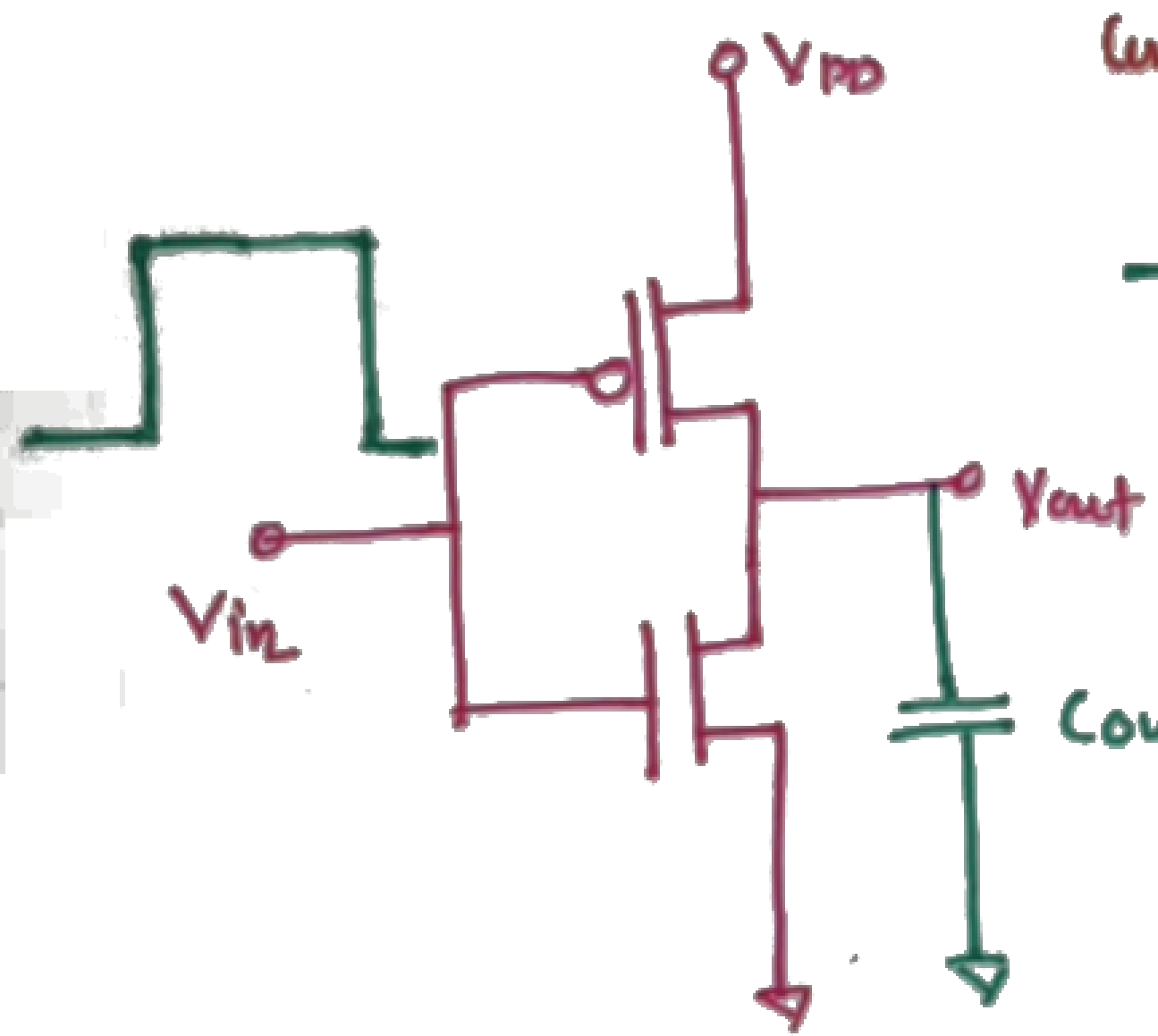


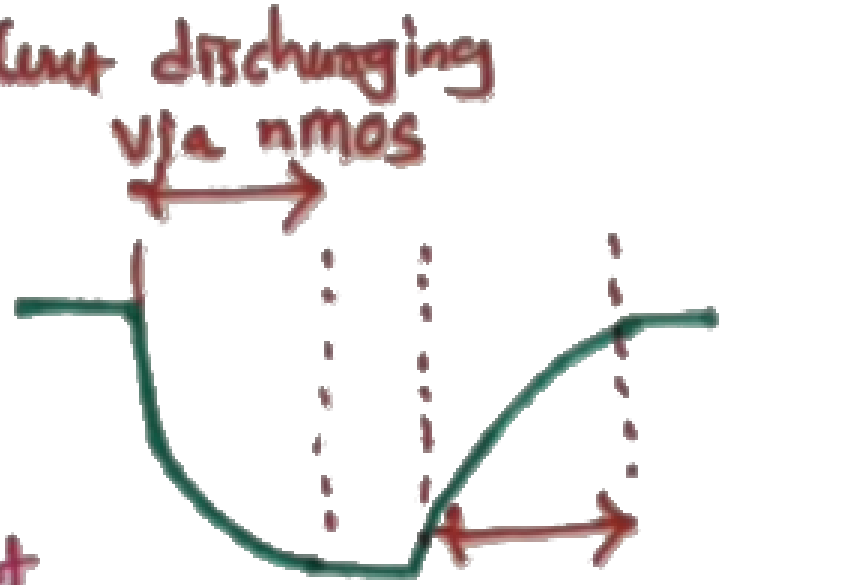


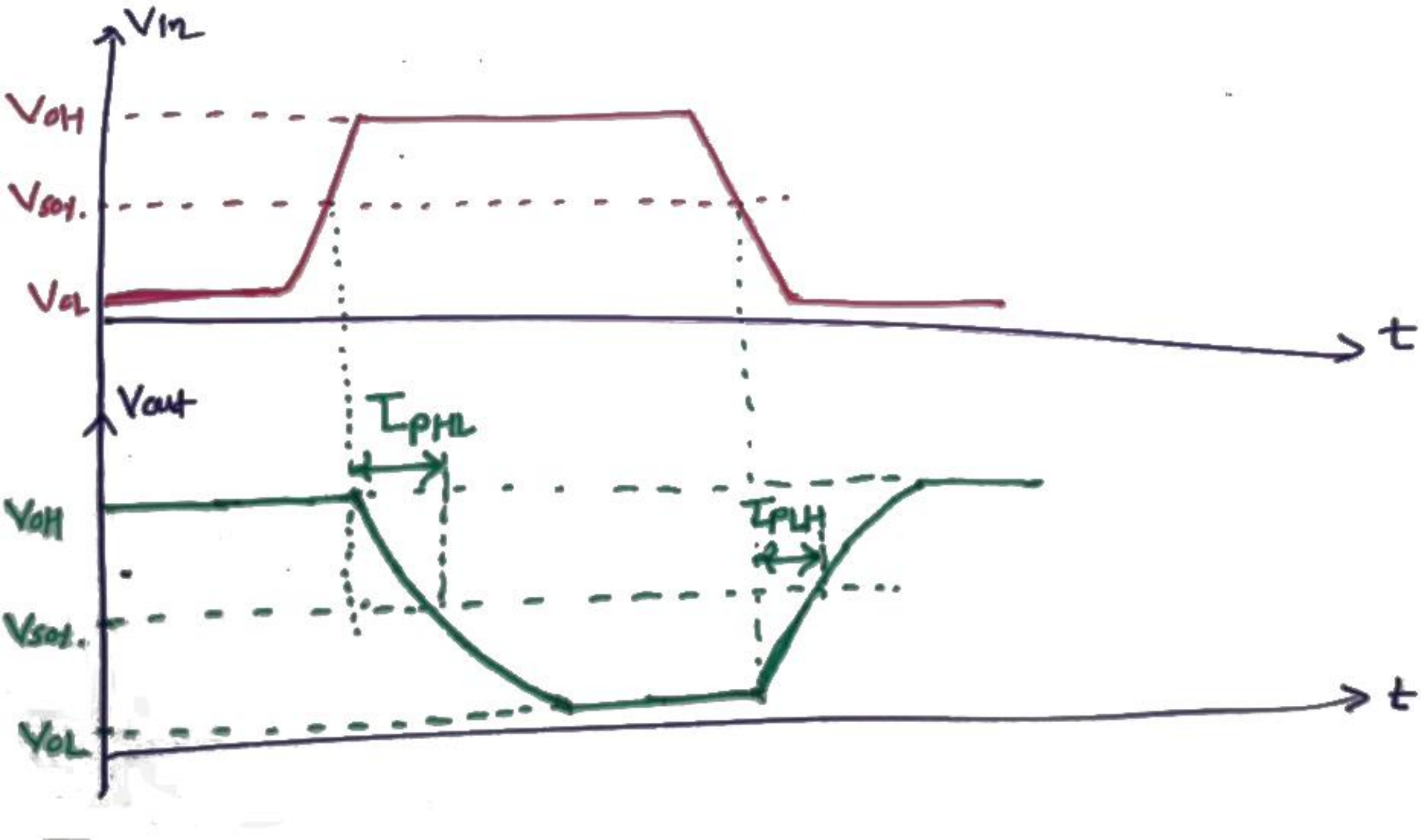
$$NM_H = V_{OH} - V_{IH}$$

$$NM_L = V_{IL} - V_{OL}$$

Propagation delay of CMOS Inverter

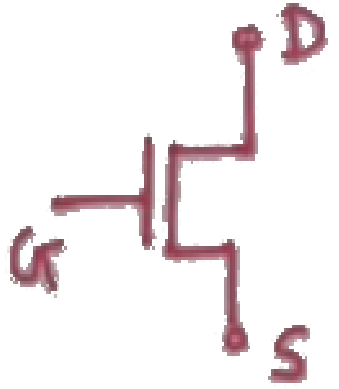





Vin
VOH
Vsol.
VOL
t
Vout
TpHL
TpLH
VOH
Vsol.
VOL
t

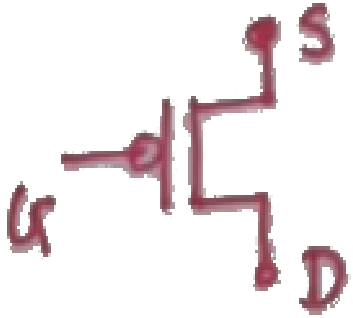
CMOS Logic Circuit rules

- CMOS
  - nMOS
  - pMOS

nMOS → 

→ If G = 0, OFF, (D to S as O.C.)

→ If G = 1, ON, (D to S as S.C.)

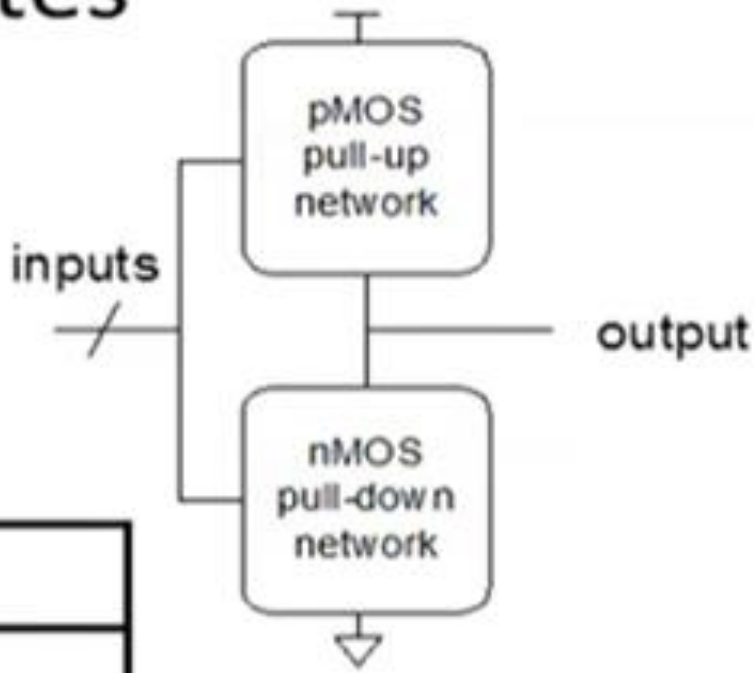
pMOS → 

→ If G = 0, ON, (S to D as S.C.)

→ If G = 1, OFF, (S to D as O.C.)

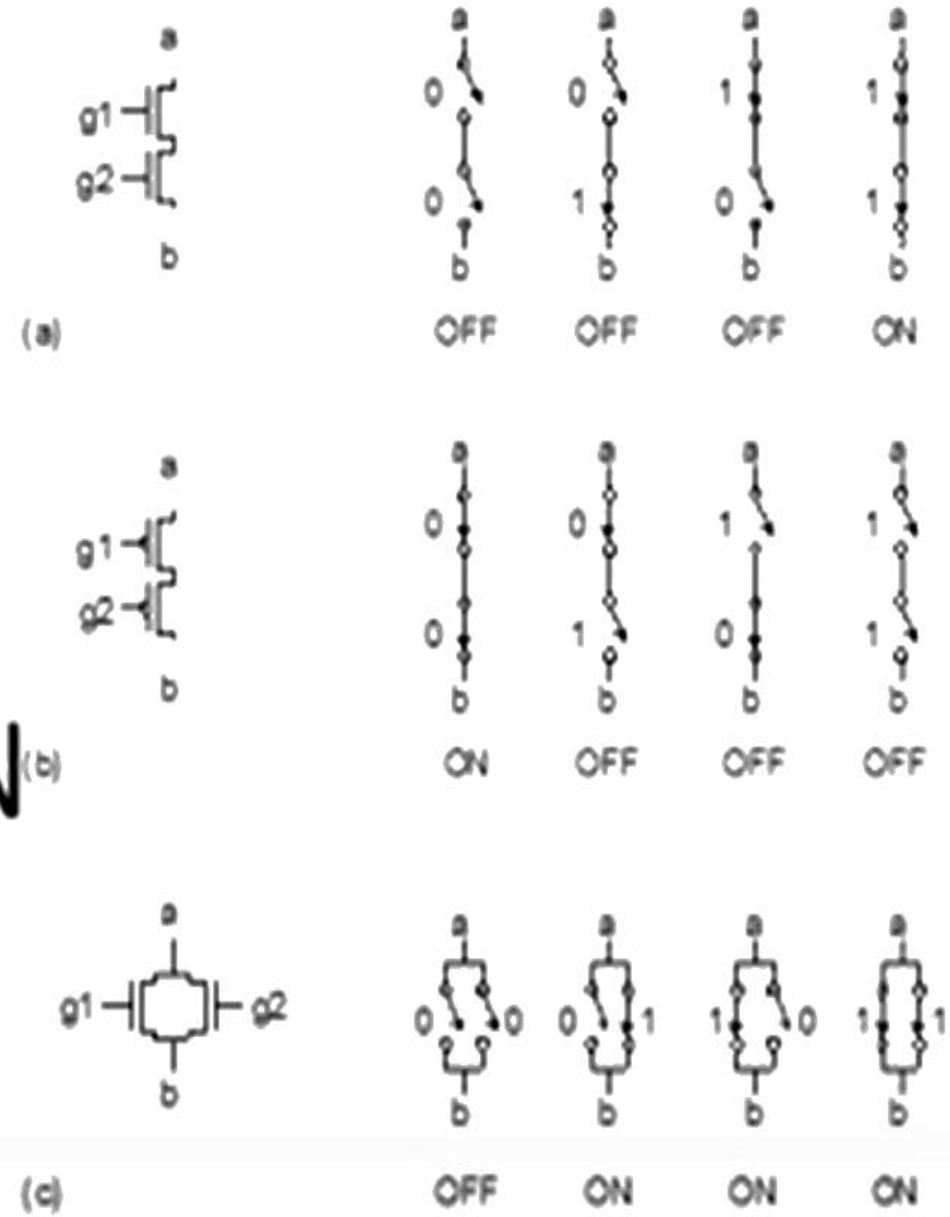
Complementary MOS (CMOS)

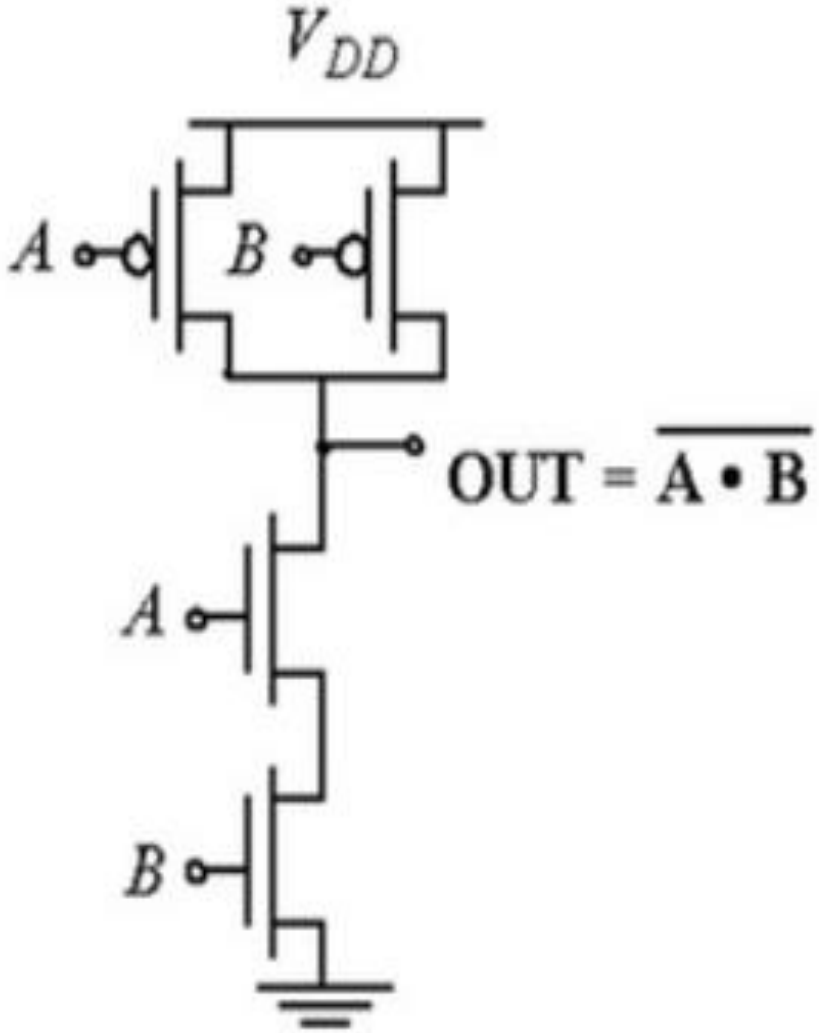
- Complementary MOS logic gates
  - nMOS *pull-down network*
  - pMOS *pull-up network*
  - static CMOS



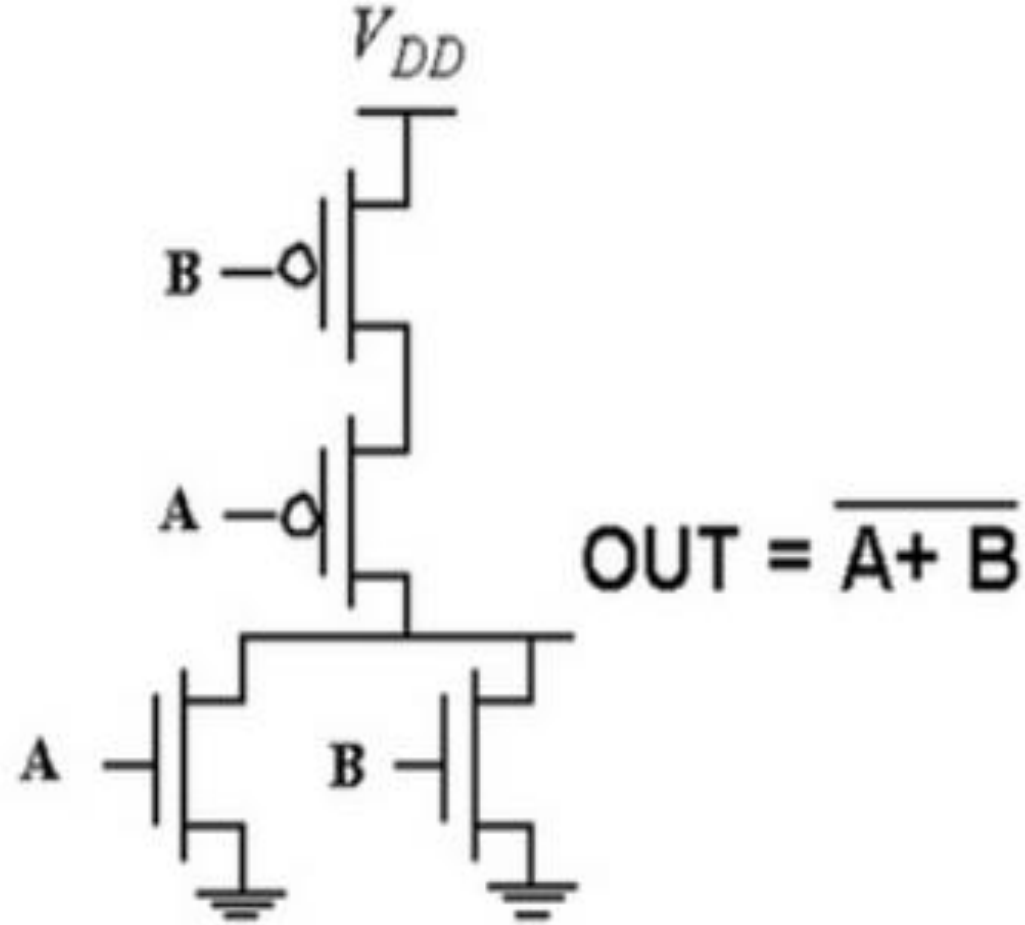
	Pull-up OFF	Pull-up ON
Pull-down OFF	Z (float)	1
Pull-down ON	0	X (crowbar)

- nMOS: 1 = ON
- pMOS: 0 = ON
- *Series*: both must be ON
- *Parallel*: either can be ON





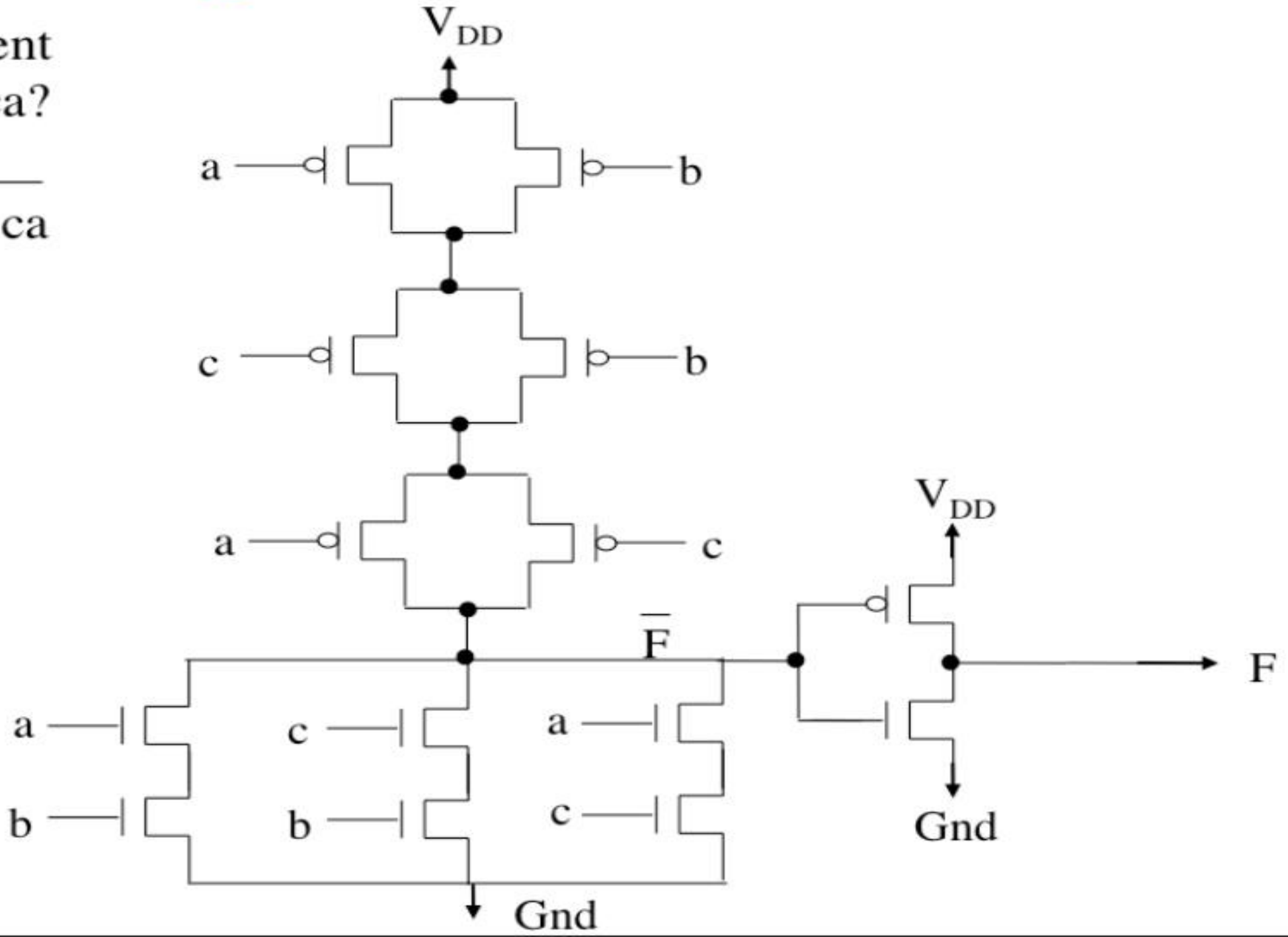
2 input NAND gate (Static Logic)



2 input NOR gate (Static Logic)

How to implement
$F = ab + bc + ca$?

- $\overline{F} = \overline{ab + bc + ca}$



$$Y = \overline{(A + B + C) \cdot D}$$