VIT

Reg. No. :

**Final Assessment Test (FAT) - July/August 2023**

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| Programme | **B.Tech.** | Semester | **Fall Inter Semester 22-23** |
| Course Title | **VLSI SYSTEM DESIGN** | Course Code | **BECE303L** |
| Faculty Name | **Prof. Velmathi G** | Slot | **A1+TA1** |
| | | Class Nbr | **CH2022232500109** |
| Time | **3 Hours** | Max. Marks | **100** |

**Section-I (10 X 8 Marks)**
**Answer All questions**

01. How does a MOSFET operate as a capacitor, and for a MOSFET with an n-type substrate, how do the capacitance-voltage (CV) characteristics vary across the accumulation, depletion, and inversion regions? Furthermore, explain the concepts of gate capacitance, overlap capacitance, and diffusion capacitance in a MOSFET, along with their corresponding equations. [8]

02. Consider an n- channel MOSFET with the following characteristics: $t_{ox}$= 10nm, $\mu$=520cm$^2$/V-sec, $W/L$ = 8, $V_{th}$ = 0.7, calculate the drain current for i) $V_{gs}$= 2 V and $V_{ds}$ = 1.2 , ii) $V_{gs}$ = 2 V and $V_{ds}$= 2 V. Assume the relative permittivity of the gate oxide is 3.9. [8]

03. With a neat circuit diagram, explain the voltage transfer characteristics (VTC) of a CMOS inverter. Mark the different regions and transition points in the VTC. Derive the expressions for input and output transition points that occur in different regions of operation of the inverter. Comment on what will happen if the PMOS transistor is used as a pull-down device and the NMOS transistor as a pull-up device. [8]

04. A positive edge-triggered register on a Master-Slave configuration is shown in Fig.1 below. Implement the same using transmission gates and explain its operation. [8]

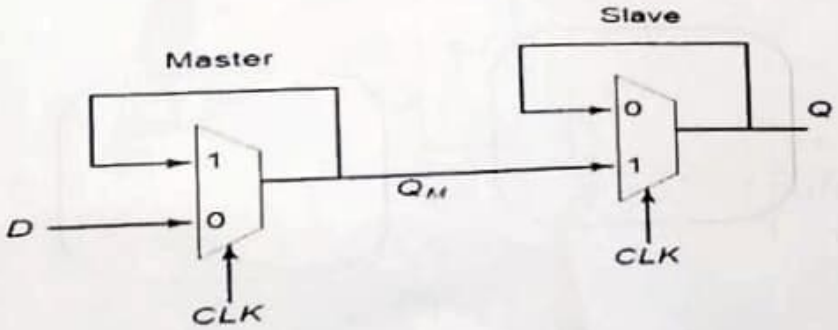


**Fig.1.**

05. Sketch a color-coded stick diagram for the circuit that implements the function [8]

$$\mathbf{F = \overline{(A + BC + D)}.}$$

Using Euler's method, organize the layout so that the transistors can be implemented on a continuous strip.

06. Estimate the minimum delay of the path from A to B in Fig.2 and choose the transistor Sizes (Y and Z) to achieve this delay. [8]

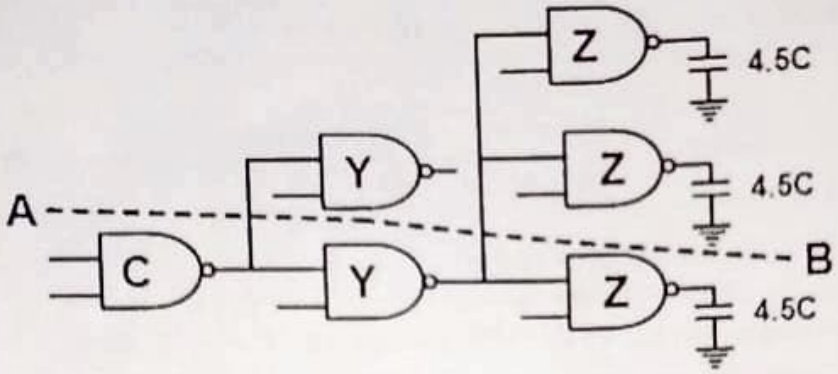


Fig. 2

07. State the advantages and disadvantages of pass transistor and Pseudo-NMOS logic styles. Also, implement 2:1 multiplexer logic with pass transistor and Pseudo-NMOS logic styles. [8]

08. What is the difference between dynamic logic and domino logic? Implement the following Boolean function using dynamic and domino logic styles. [8]

$$F = \overline{(A\,(B + C) + DE)}$$

Explain the timing diagram with neat sketches.

09. a) For the given RTL circuit in Fig.3, check whether any Setup Violation or Hold Violation exists; if so, kindly suggest a measure to rectify it. [8]

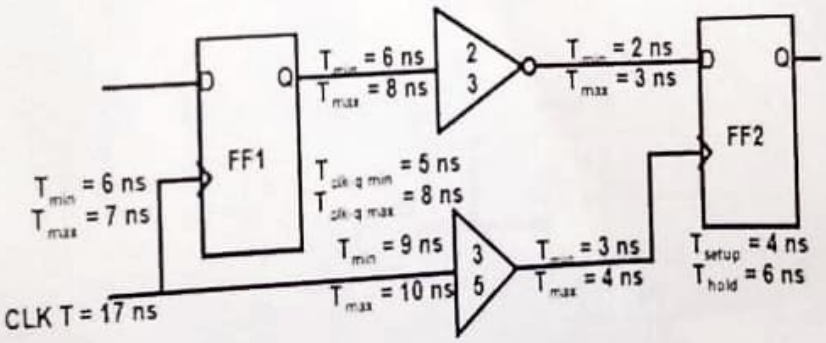


Fig.3

b) With a neat sketch of the waveform, elaborate the Setup Time calculation for an RTL circuit with Launch FF & Latch FF.

10. Explain the "write operation" of a 6T CMOS SRAM cell with neat sketches. Mention the operating region of all the transistors of the SRAM cell during write operation. Derive for the W/L ratio of the transistors for proper "write" operation. [8]

## Section-II (4 X 5 Marks)

**Answer All questions**

11. With neat cross-sectional sketches, explain the fabrication process flow of Fig.4 is shown below. How many masks are required for the fabrication? Draw the masks assuming positive photoresist for the metallization step and negative photoresist for all other steps. [5]

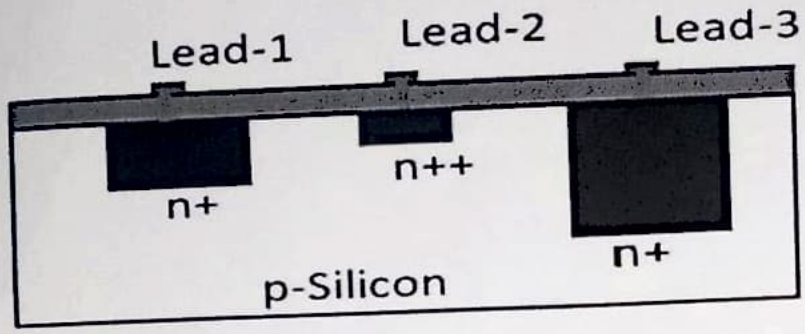


**Fig. 4**

12. Evaluate the dynamic power dissipated for a VLSI circuit that works with the clock frequency of 3 MHz and has gate capacitance and diffusion capacitance of 2.0 fF/μm with a supply voltage of 1.0 V. [5]

13. What is the concept of row and column addressing in DRAM? Explain their significance in VLSI design. [5]

14. What are the various limitations of the low-voltage, low-power design of VLSI circuits? [5]

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