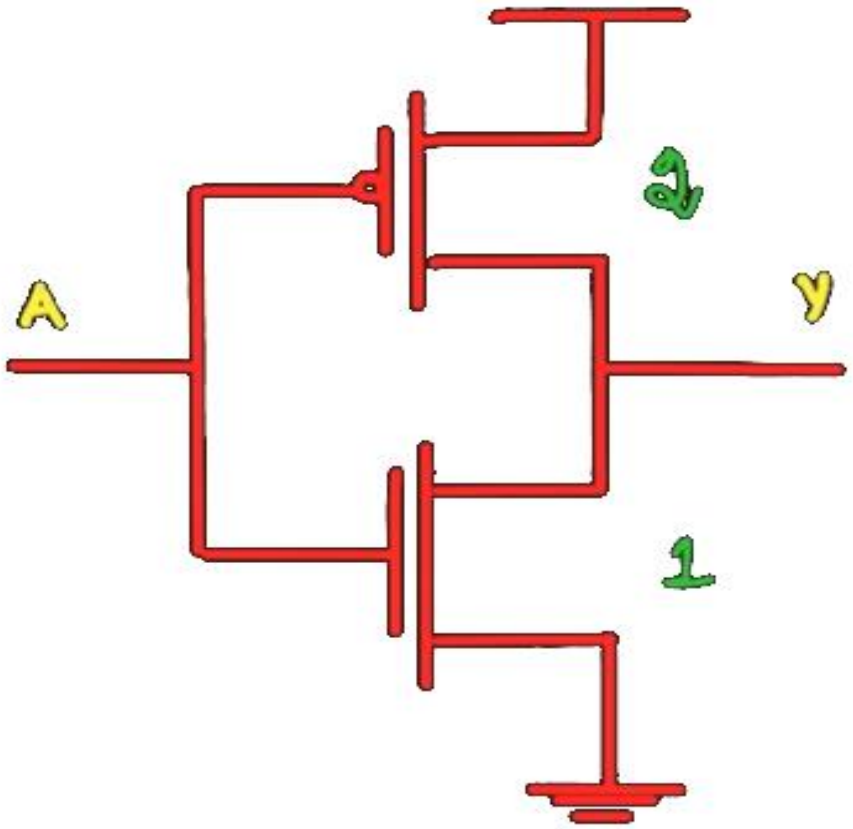
CMOS Circuits Performance Analysis

Unit -4

by
Dr. SAKTHIVEL.S.M

Transistor Sizing

Unskewed - CMOS INVERTER



$$\left(\frac{W}{L}\right)_{PMOS} \simeq 2\text{-}3 \text{ TIMES } \left(\frac{W}{L}\right)_{NMOS}$$

$$\beta = 1$$

where $\beta = \dfrac{\beta_p}{\beta_n}$

SKEWED DESIGN

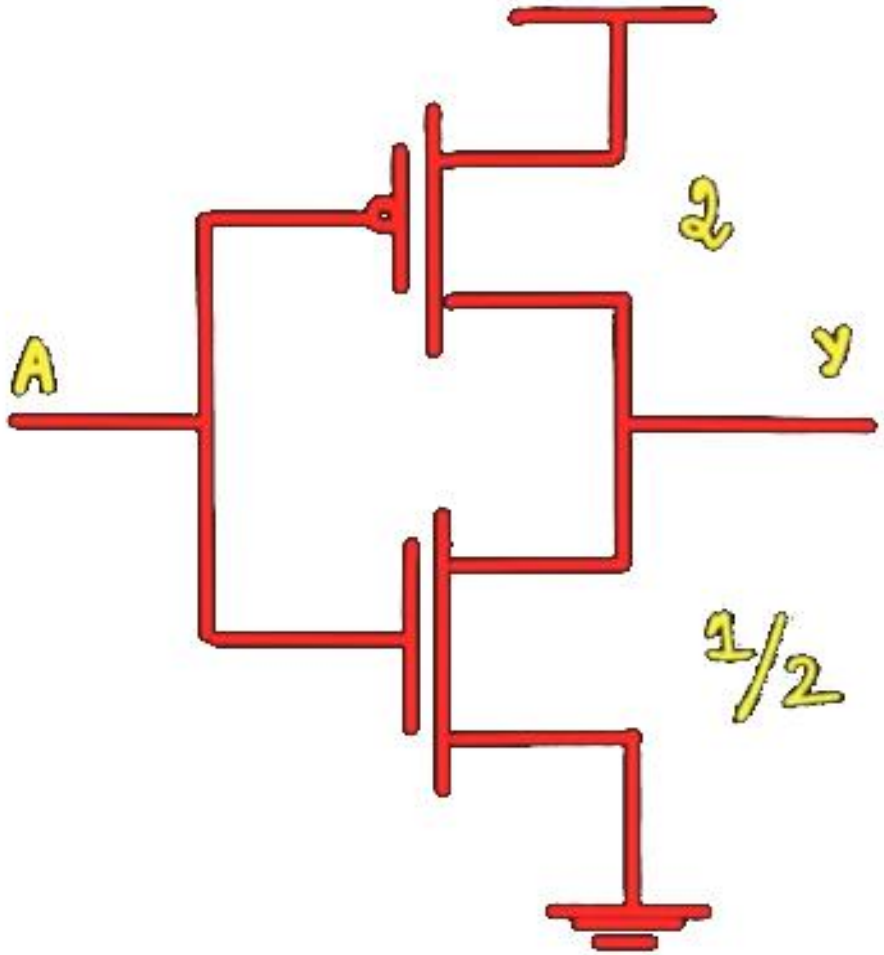
(i) <u>HI - SKEW</u> ; $\beta > 1$

$$\therefore \quad \beta_p > \beta_n \quad \therefore \left(\frac{W}{L}\right)_p > \left(\frac{W}{L}\right)_n$$

(ii) <u>LO - SKEW</u> ; $\beta < 1$

$$\therefore \quad \beta_n > \beta_p \quad \therefore \left(\frac{W}{L}\right)_n > \left(\frac{W}{L}\right)_p$$

HI - Skew - CMOS INVERTER



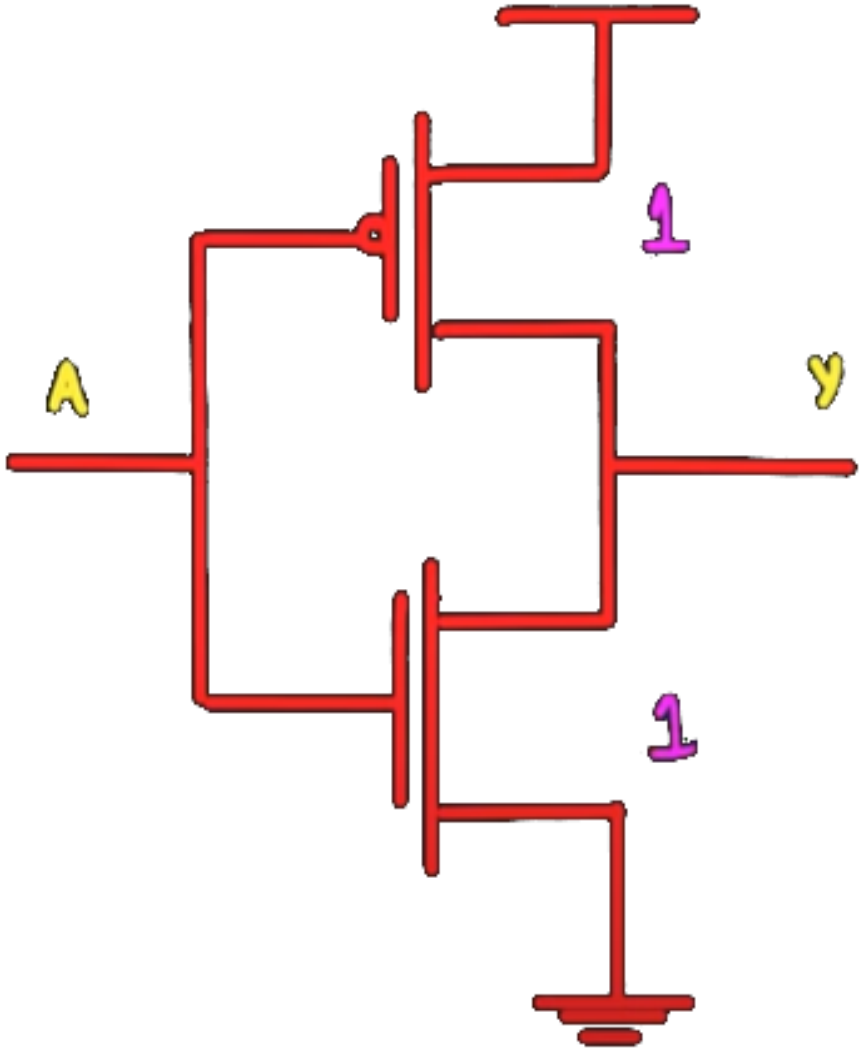
$$\left(\frac{W}{L}\right)_p > \left(\frac{W}{L}\right)_n$$

$$\left.\begin{aligned} W_{p,inv} &= 2 \\ W_{n,inv} &= 1 \end{aligned}\right\} \text{UNSKEWED DESIGN}$$

$$W_{p,inv} = 2$$

$$W_{n,inv} = 1/2$$

LO - Skew - CMOS INVERTER



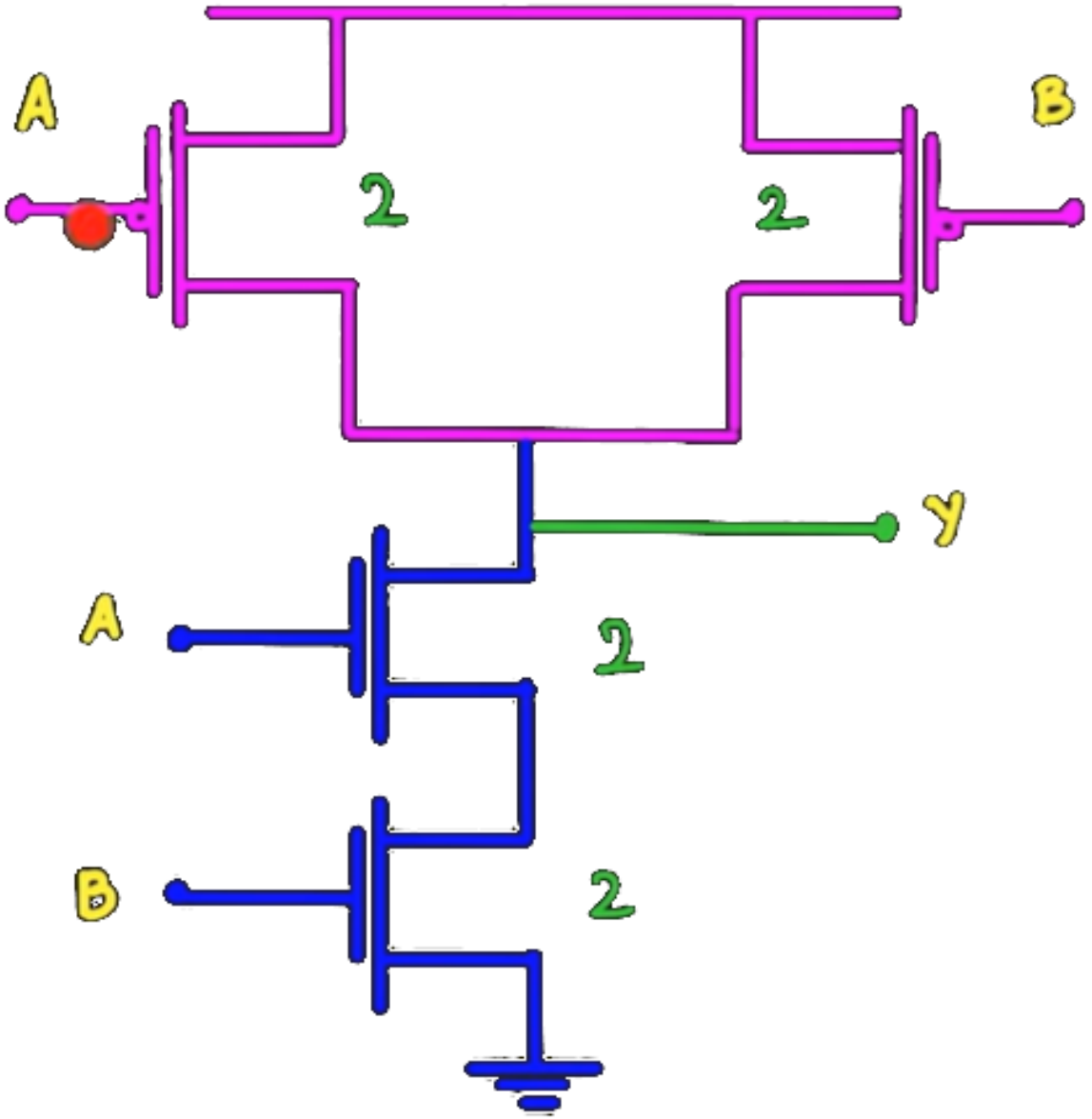
$$\left(\frac{W}{L}\right)_p < \left(\frac{W}{L}\right)_n$$

$$W_{p,inv} = 2 \; ; \; W_{n,inv} = 1$$

$$W_{p,inv} = 2/2 = 1$$

$$W_{n,inv} = 1$$

Unskewed - CMOS NAND2 GATE



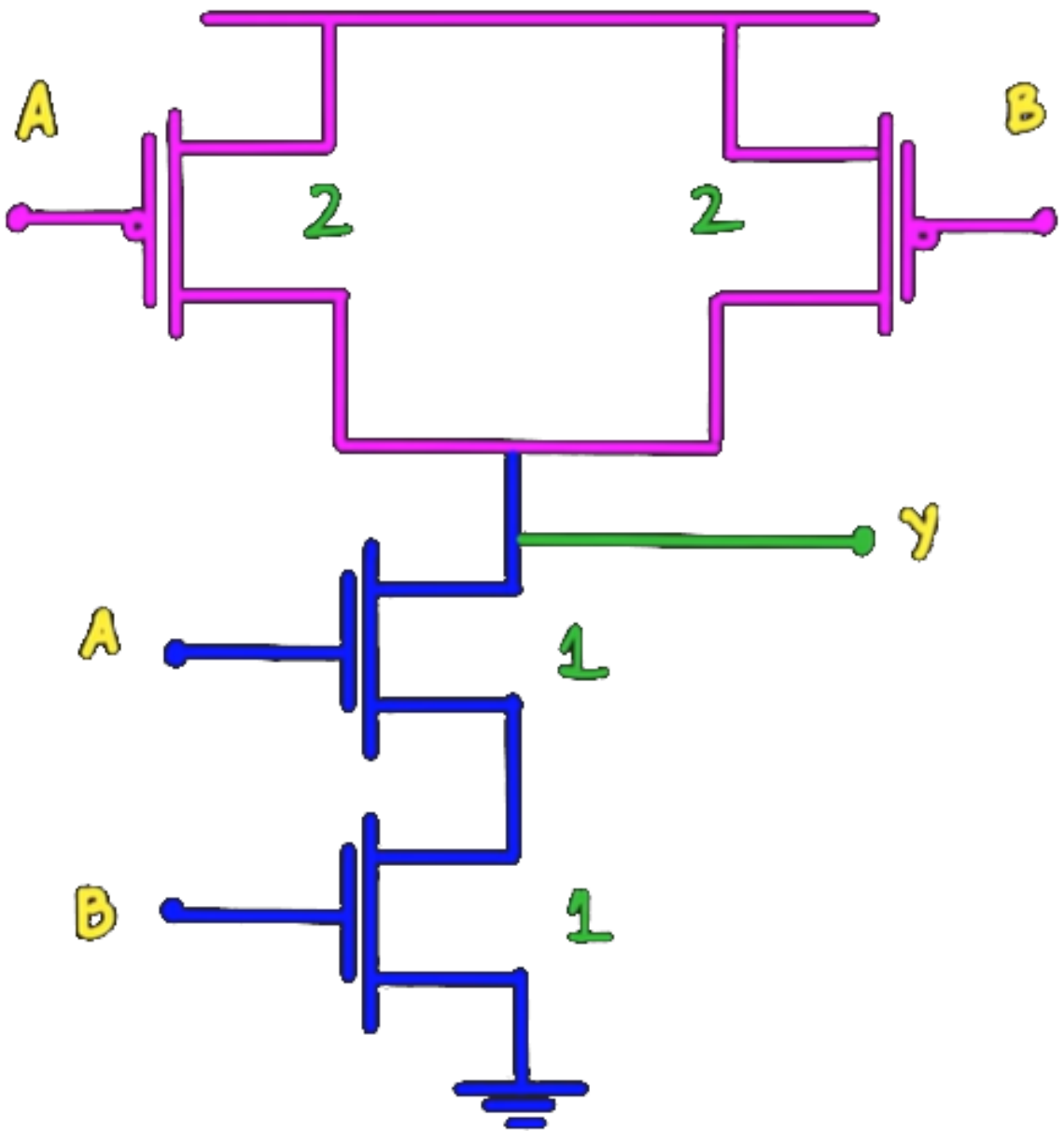
$$\left.\begin{aligned} W_{p,inv} &= 2 \\ W_{n,inv} &= 1 \end{aligned}\right\} \text{unskewed CMOS Inverter design}$$

$$W_{p,NAND} = 2$$

$$W_{n,NAND} = 2 \times W_{n,inv}$$

$$= 2 \times 1 = 2$$

HI - Skew - CMOS NAND2 GATE



$W_{p,NAND} = 2$

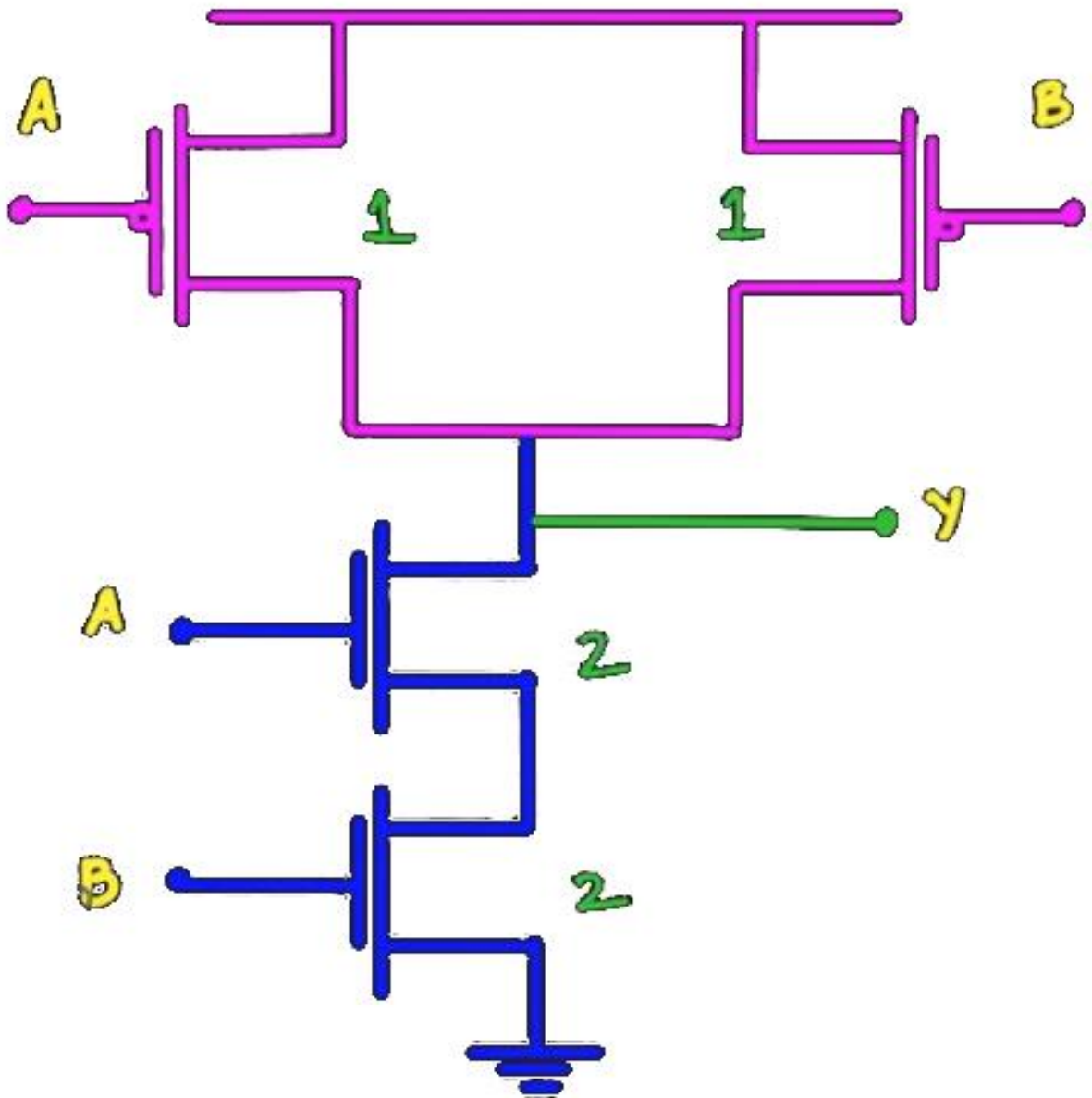
$W_{n,NAND} = 2$

UNSKEWED 2-INPUT CMOS NAND

$W_{p,NAND} = 2$

$W_{n,NAND} = 2/2 = 1$

LO - Skew - CMOS NAND2 GATE

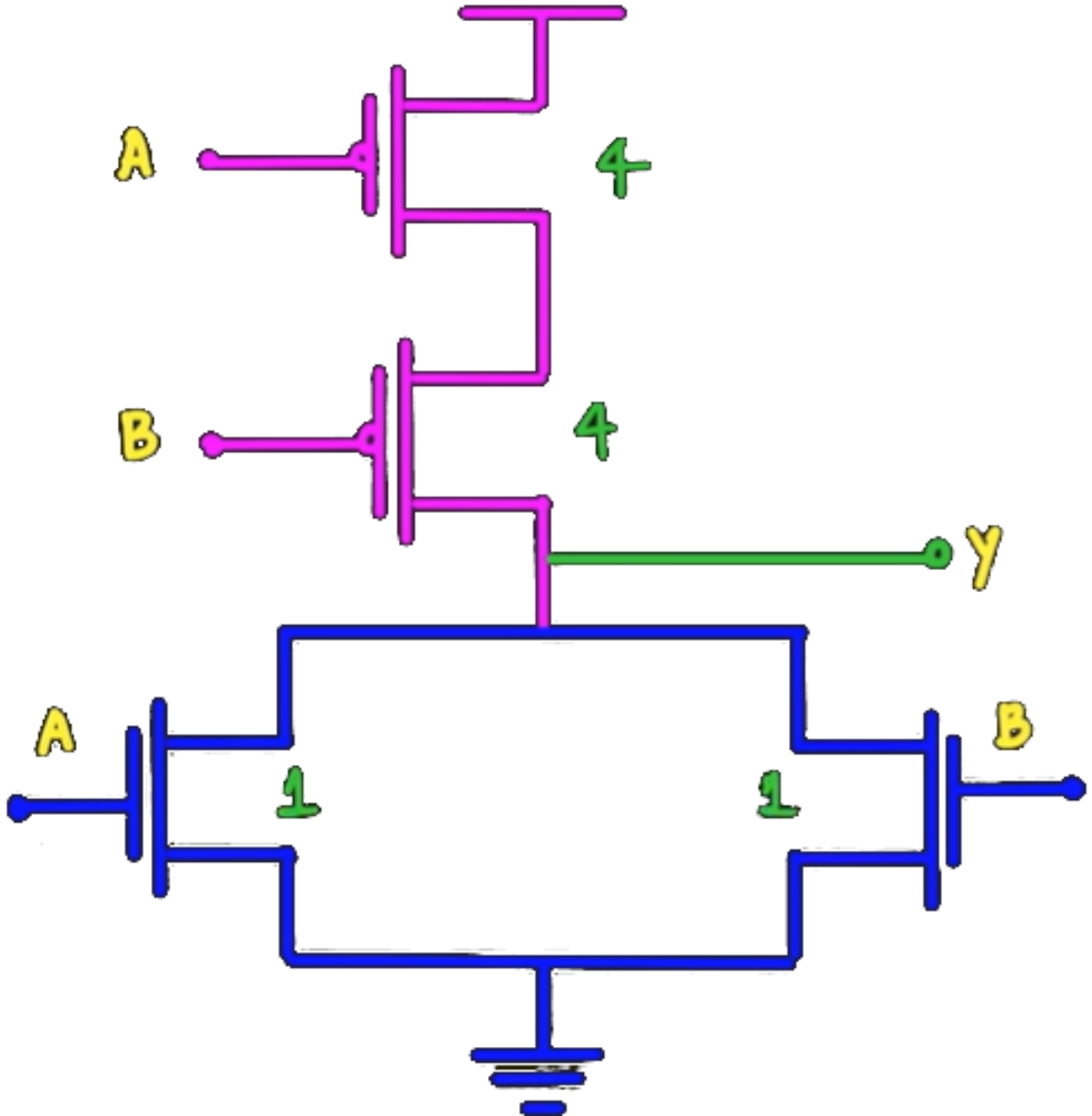


$W_{p,NAND} = 2$
$W_{n,NAND} = 2$
} UNSKEWED 2-INPUT CMOS NAND

$\therefore W_{p,NAND} = 2/2 = 1$

$W_{n,NAND} = 2$

Unskewed - CMOS NOR2 GATE



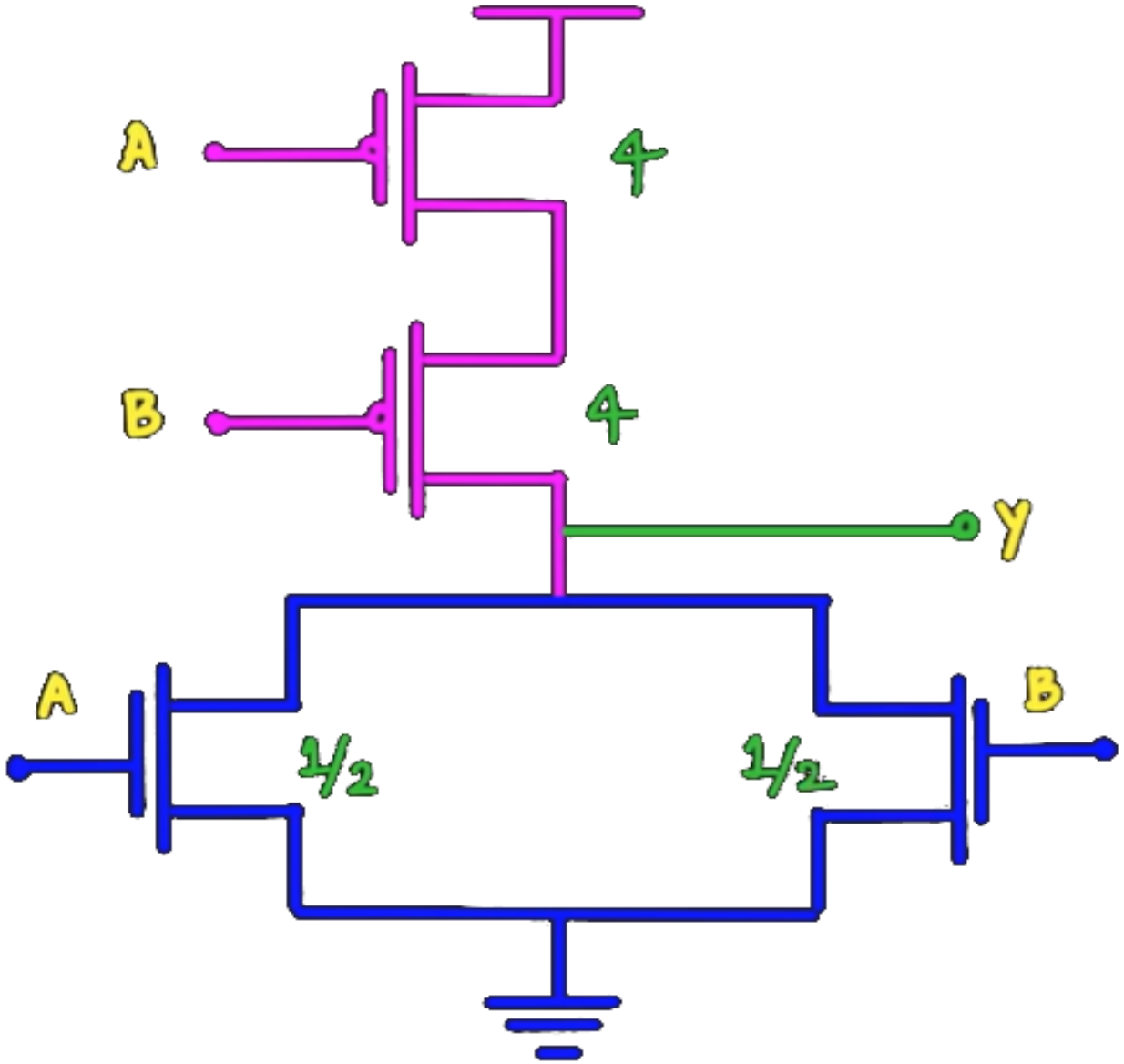
$$\left.\begin{aligned} W_{p,inv} &= 2 \\ W_{n,inv} &= 1 \end{aligned}\right\} \text{unskewed CMOS Inverter design}$$

$$W_{p,NOR} = 2\, W_{p,inv}$$

$$= 2 \times 2 = 4$$

$$W_{n,NOR} = W_{n,inv} = 1$$

HI - Skew - CMOS NOR2 GATE



$W_{p,\,NOR} = 4$

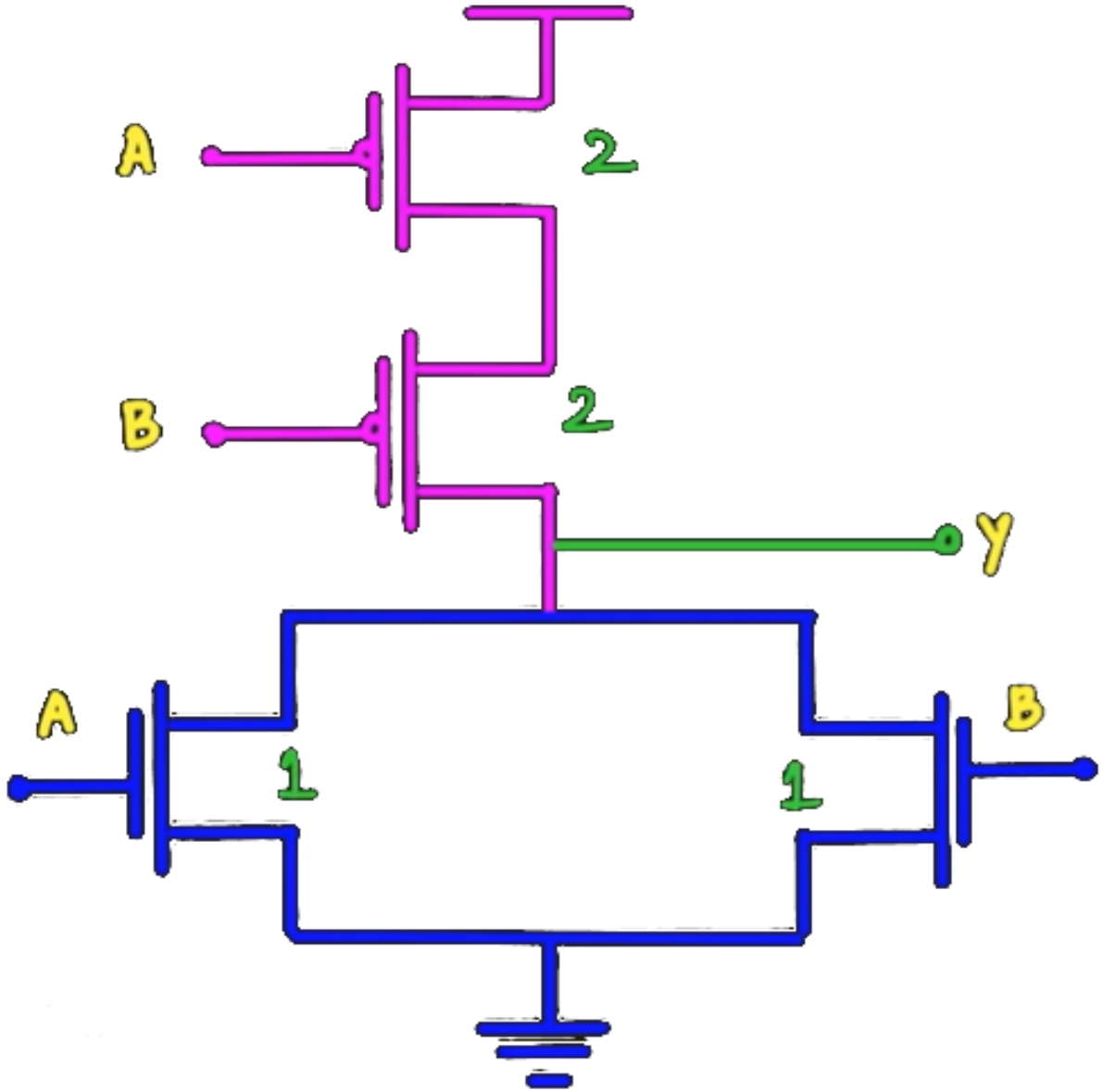
$W_{n,\,NOR} = 1$

} UNSKEWED 2-INPUT CMOS NOR

$W_{p,\,NOR} = 4$

$W_{n,\,NOR} = 1/2$

LO - Skew - CMOS NOR2 GATE



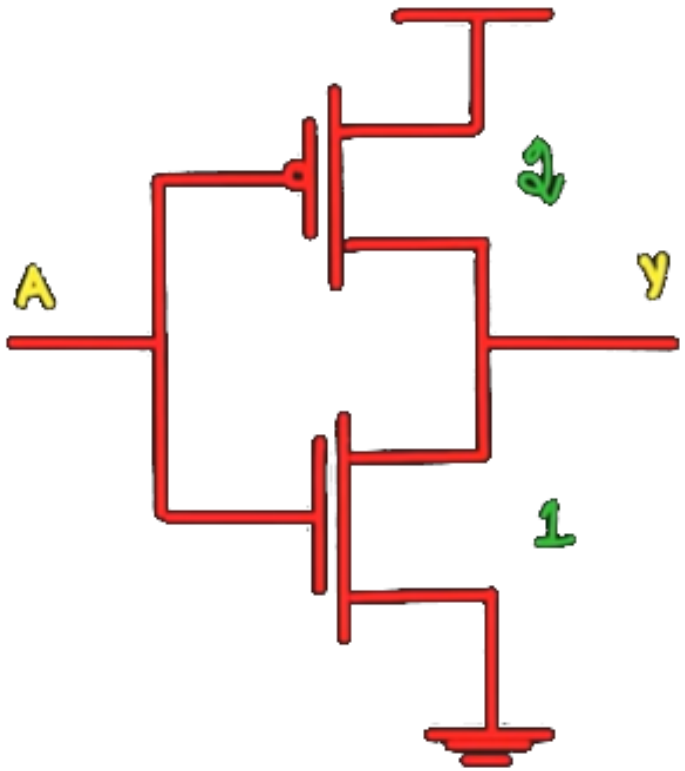
$W_{p,NOR} = 4$
$W_{n,NOR} = 1$

UNSKEWED 2-INPUT CMOS NOR

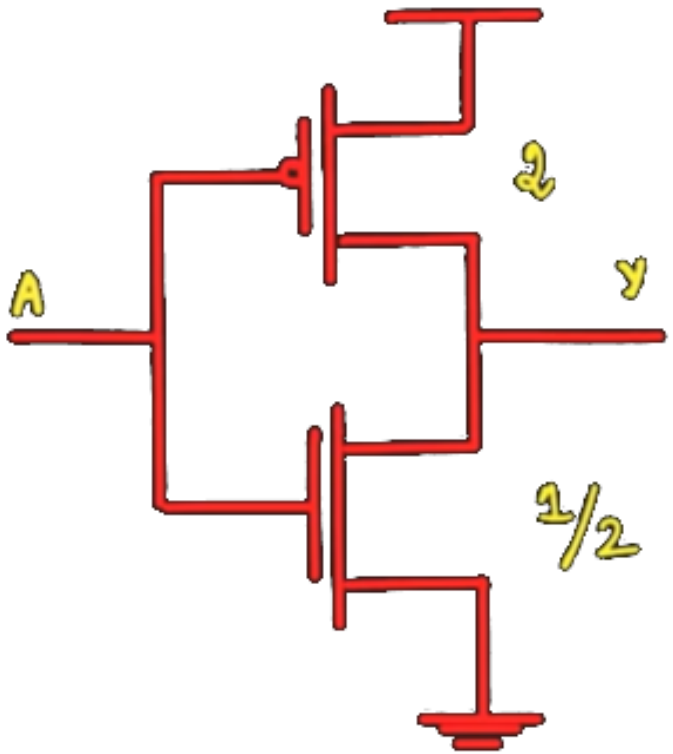
$W_{p,NOR} = 4/2 = 2$

$W_{n,NOR} = 1$

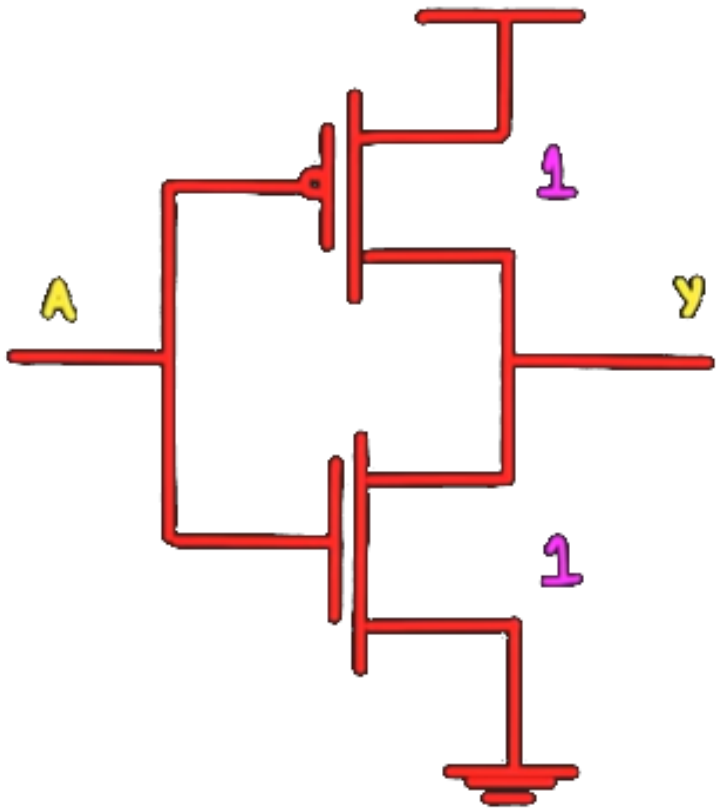
SUMMARY OF CMOS INVERTER



UNSKEWED

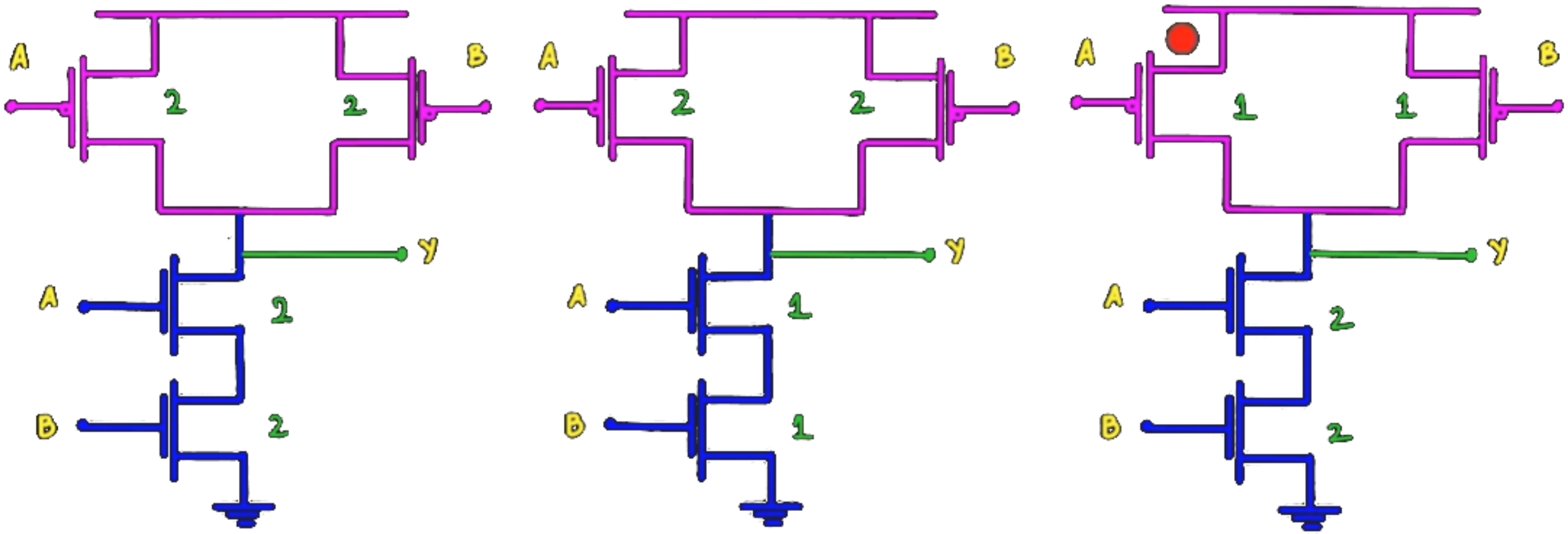


HI - SKEW



LO - SKEW

SUMMARY OF CMOS NAND2 GATE

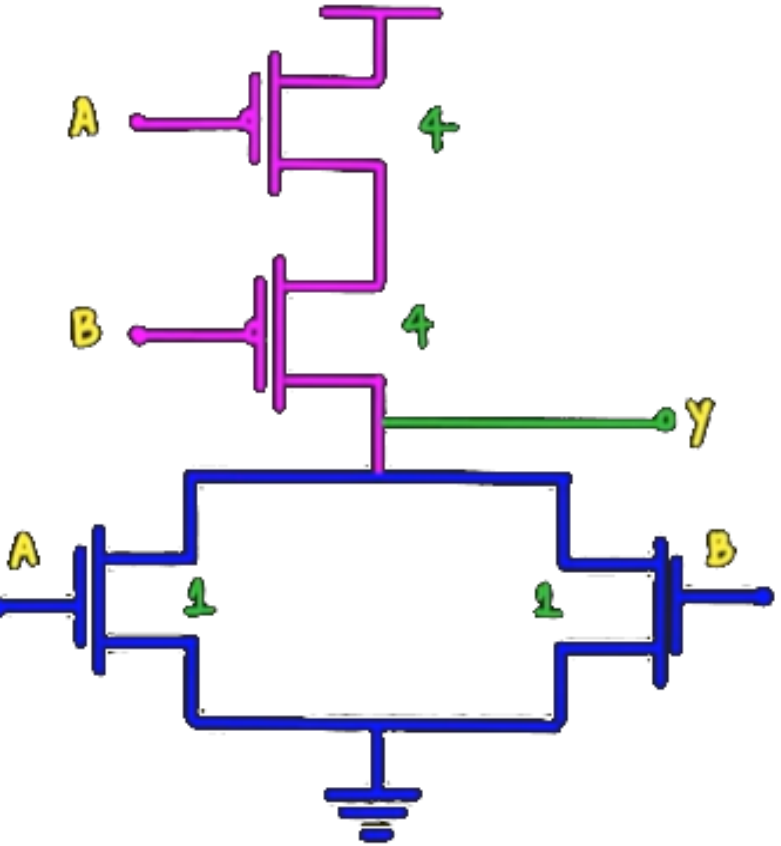


UNSKEWED

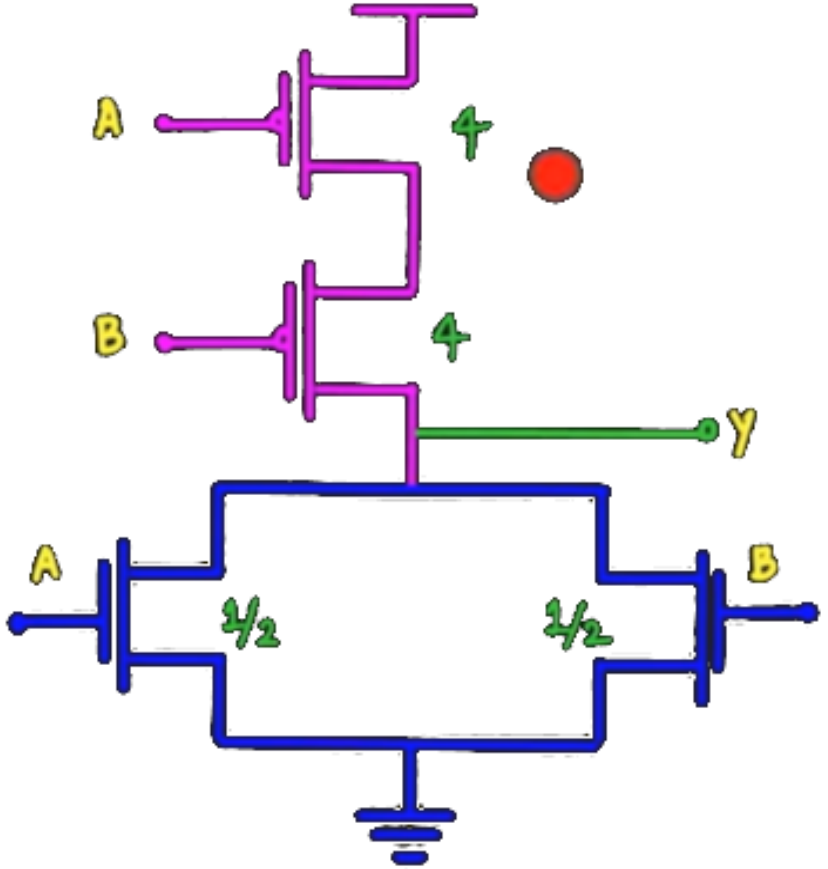
HI - SKEW

LO - SKEW

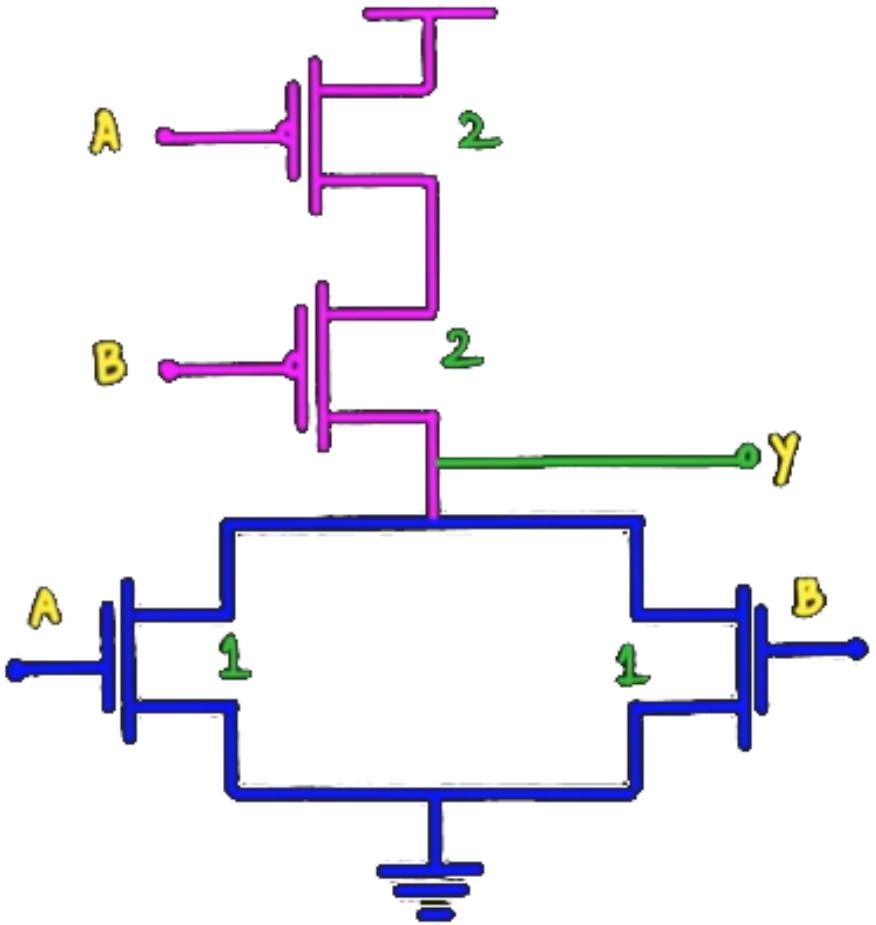
SUMMARY OF CMOS NOR2 GATE



UNSKEWED



HI - SKEW



LO - SKEW

STATIC CMOS DESIGN - OAI22

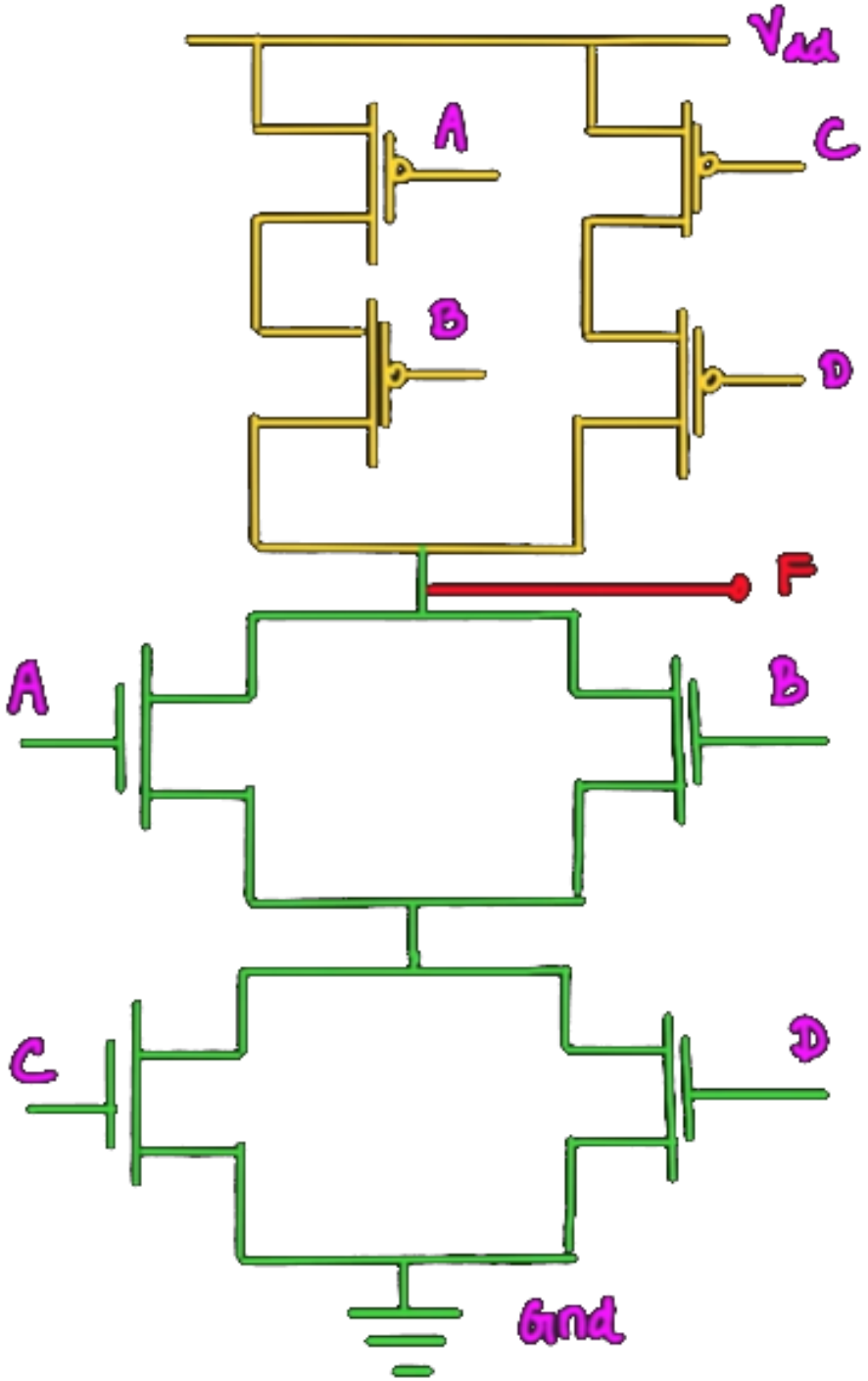
$$F = \overline{(A+B).(C+D)}$$

$$F_n = (A+B).(C+D)$$

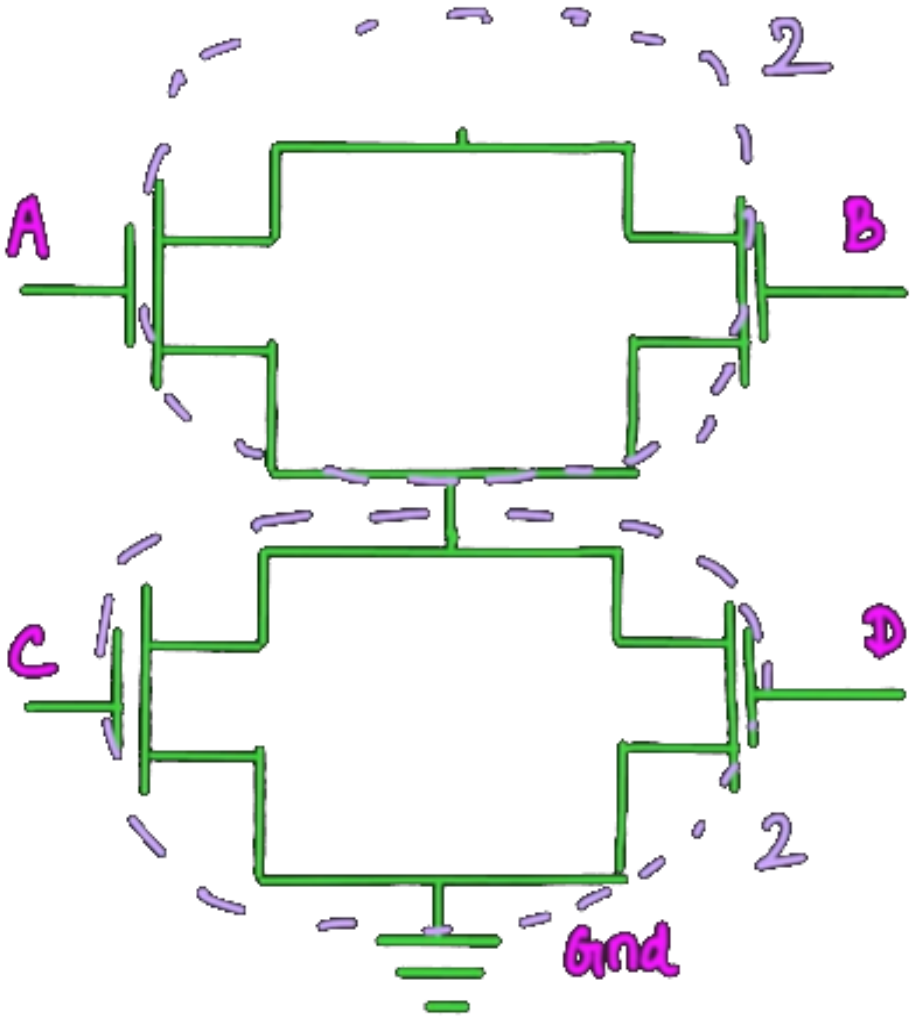
$$F_p = \overline{(A+B)} + \overline{(C+D)}$$

$$= (\bar{A}.\bar{B}) + (\bar{C}.\bar{D})$$

$$F_p = A.B + C.D$$



PDN SIZING



$(W/L)_p = 2$

$(W/L)_n = 1$

$(W/L)_{eq} = 2 \times W_{n,inv}$

$= 2$

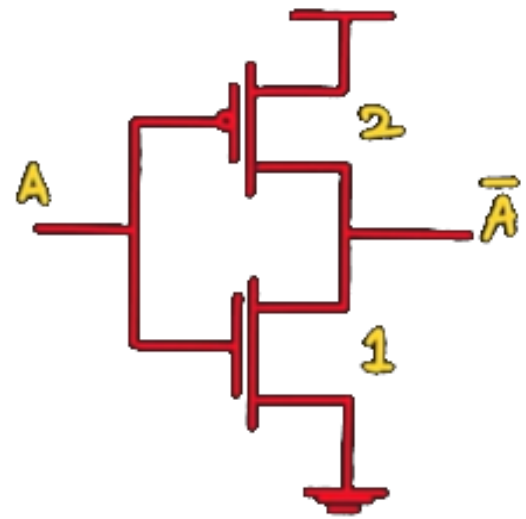
$(W/L)_A = (W/L)_B = 2$

$(W/L)_C = (W/L)_D = 2$

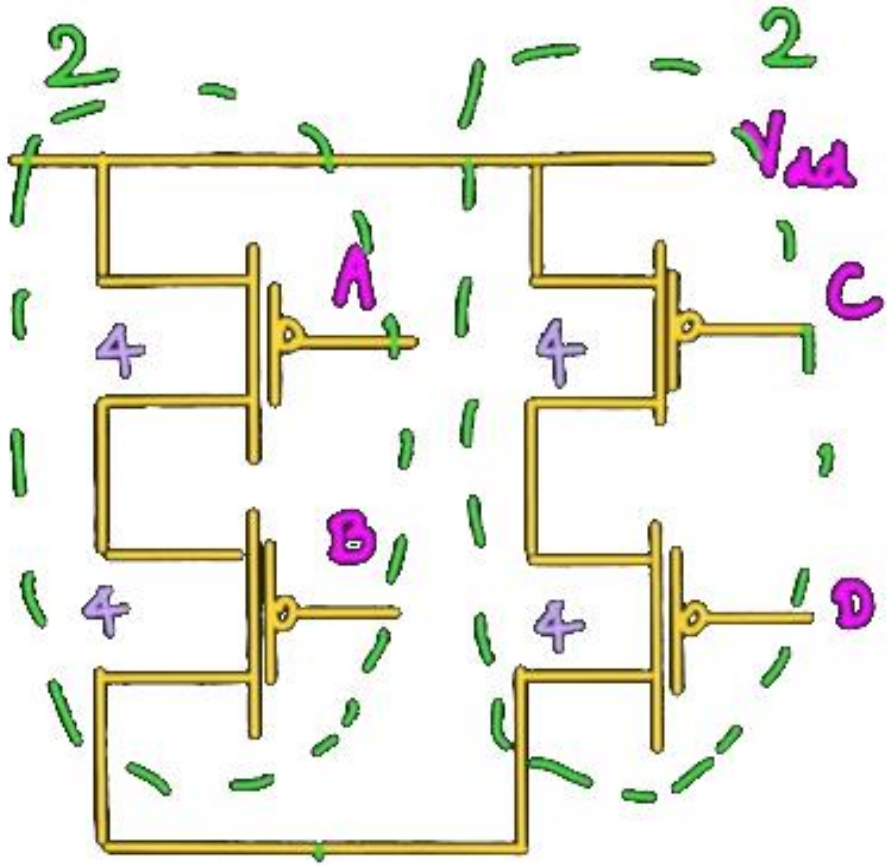
$$(W/L)_{eq} = \frac{1}{(L/W)+(L/W)} = \frac{1}{2L/W}$$

$$1 = 1/\,2L/W \quad \therefore \; (W/L) = 2/1 = 2$$

UNIT CMOS INVERTER

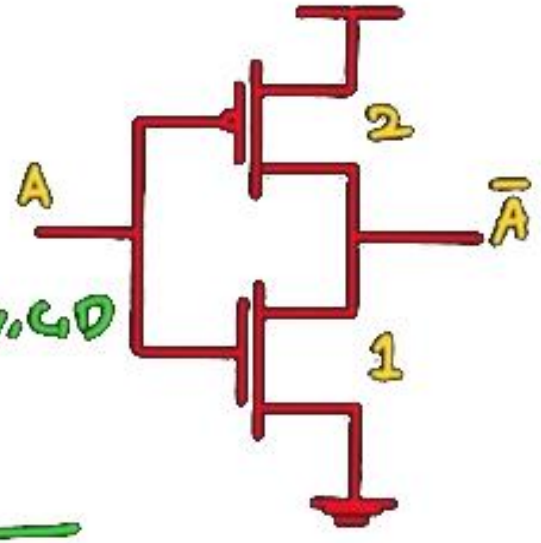


PUN SIZING



$$(W/L)_p = W_{p,inv} = 2$$

UNIT CMOS INVERTER



$$\therefore (W/L)_{eq,A,B} = 2 = (W/L)_{eq,C,D}$$

$$(W/L)_{eq,A,B} = \frac{1}{L/W + L/W}$$

$$2 = \frac{1}{2L/W}$$

$$\therefore (W/L)_A = (W/L)_B = 4 \; ; \; \left(\frac{W}{L}\right)_C = \left(\frac{W}{L}\right)_D = 4$$

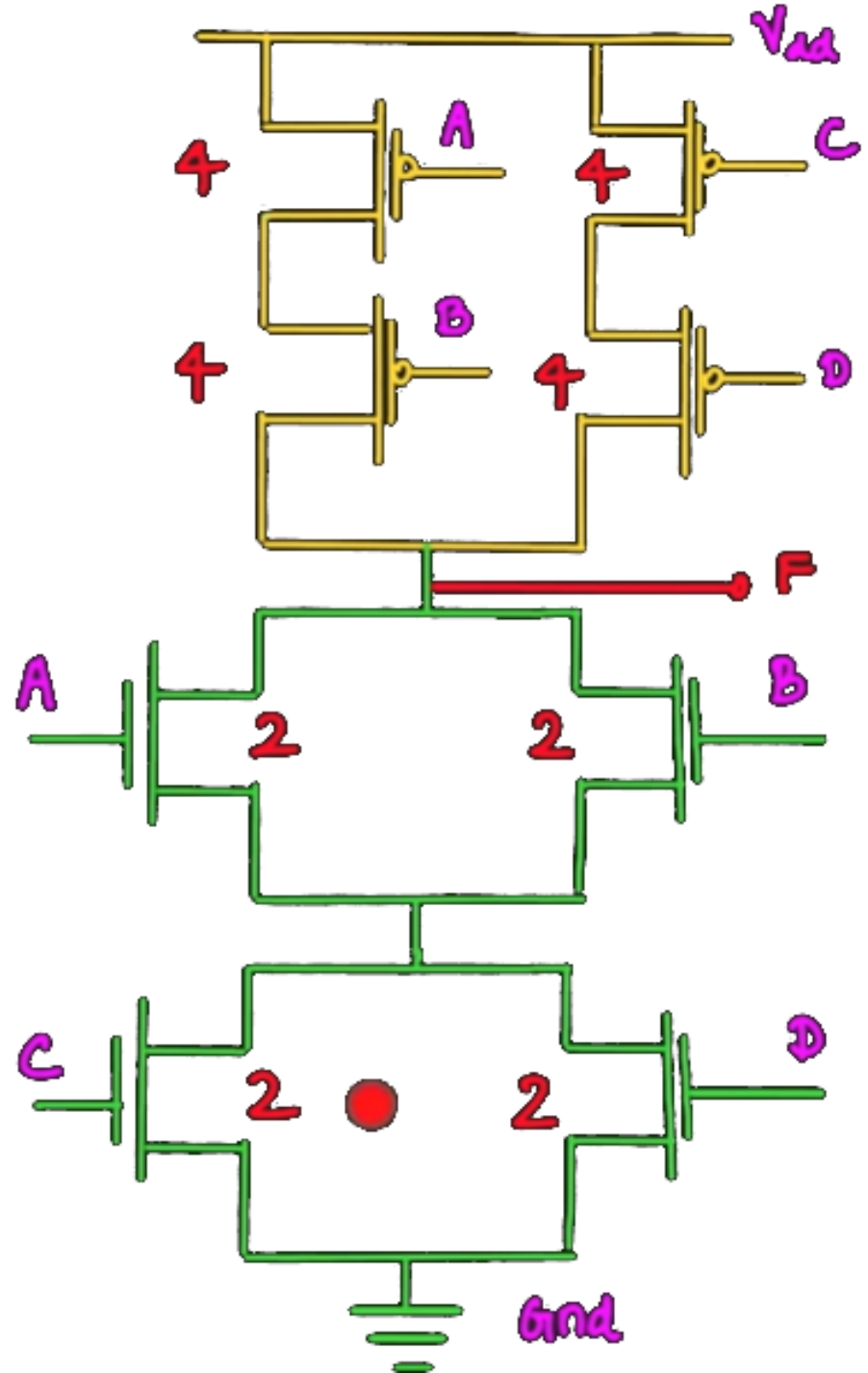
STATIC CMOS - SIZING

PDN:

$$(W/L)_A = (W/L)_B = (W/L)_C = (W/L)_D = 2$$

PUN:

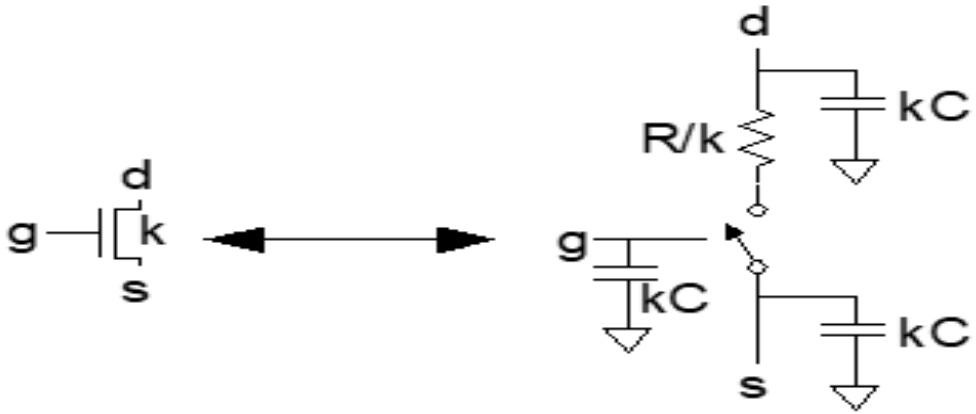
$$(W/L)_A = (W/L)_B = (W/L)_C = (W/L)_D = 4$$

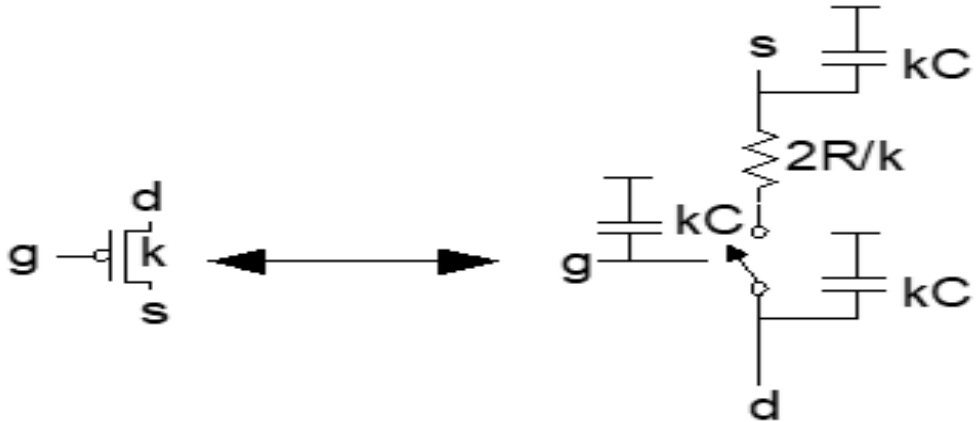


Delay Estimation

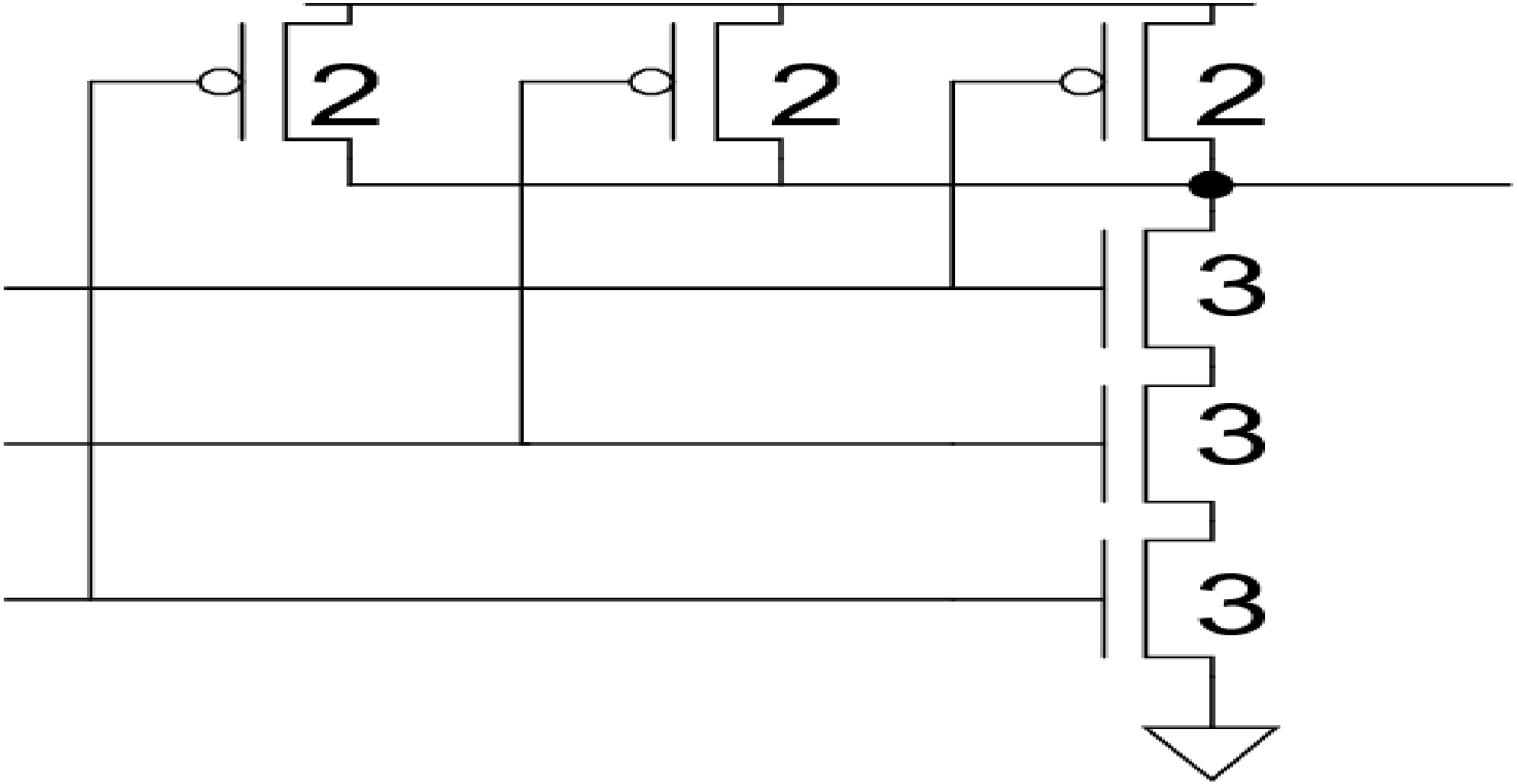
RC Delay Model

- Use equivalent circuits for MOS transistors
  - Ideal switch + capacitance and ON resistance
  - Unit nMOS has resistance R, capacitance C
  - Unit pMOS has resistance 2R, capacitance C
- Capacitance proportional to width
- Resistance inversely proportional to width

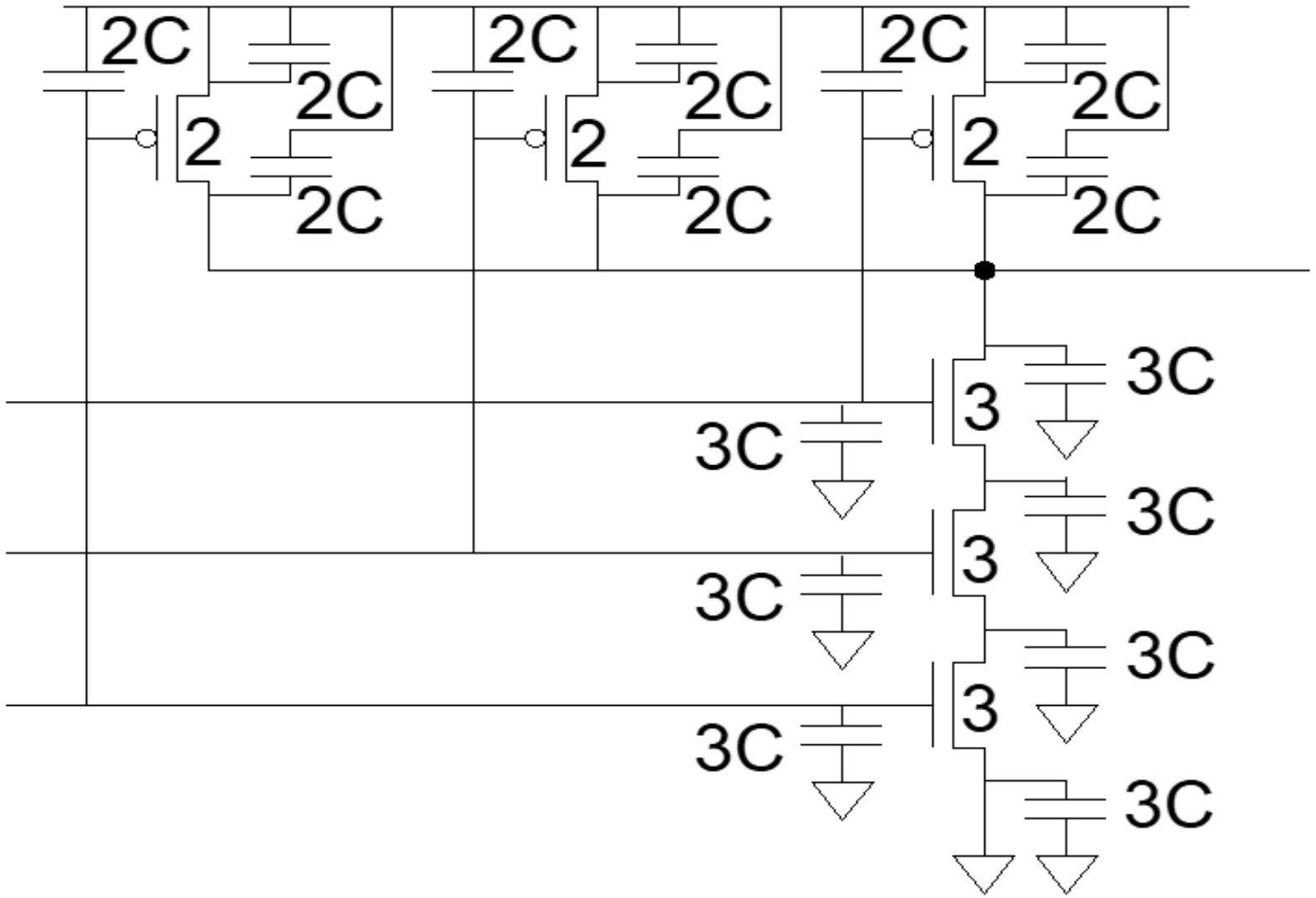


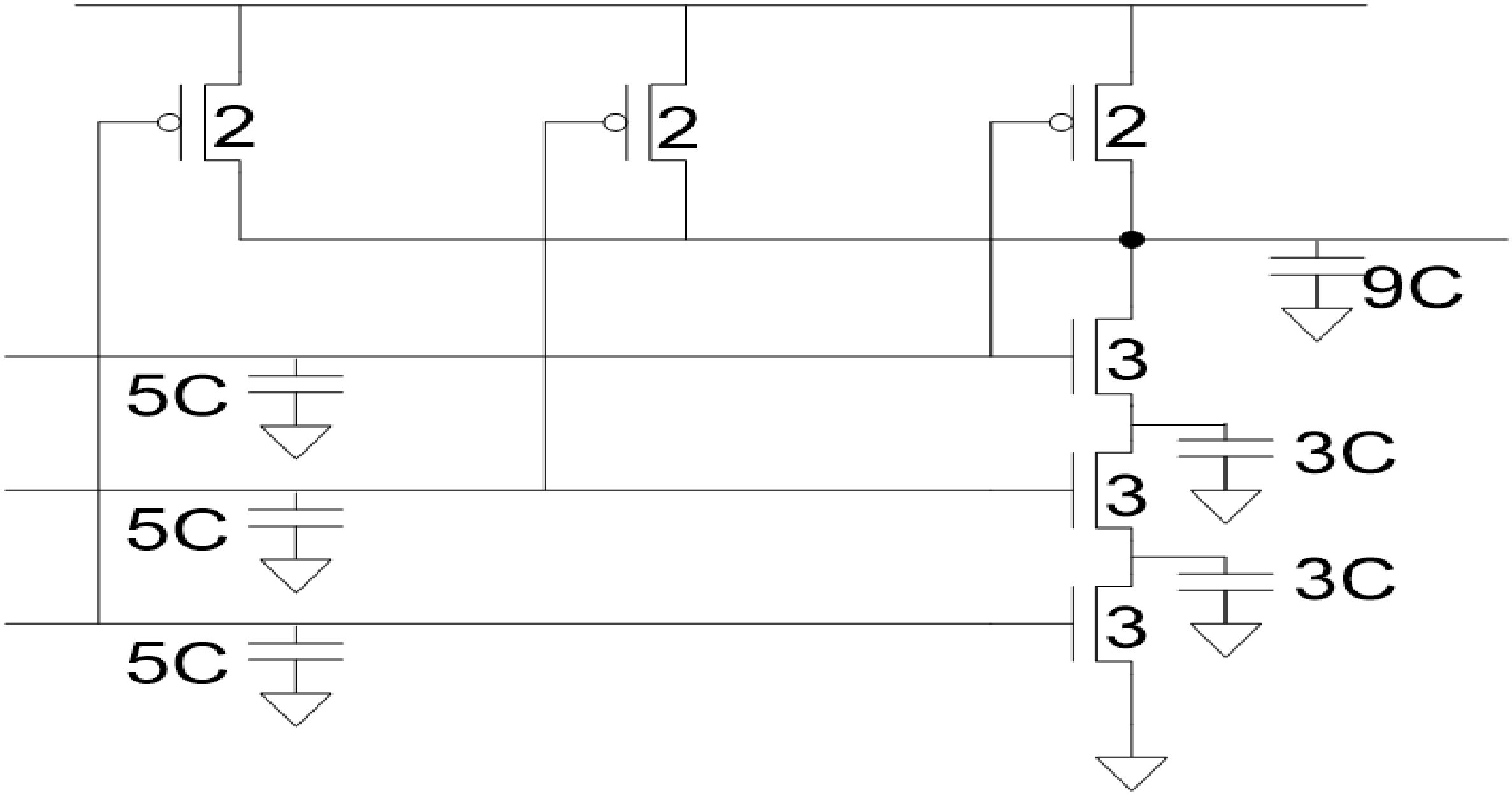


Delay Estimation



Annotate the 3-input NAND gate with gate and diffusion capacitance.

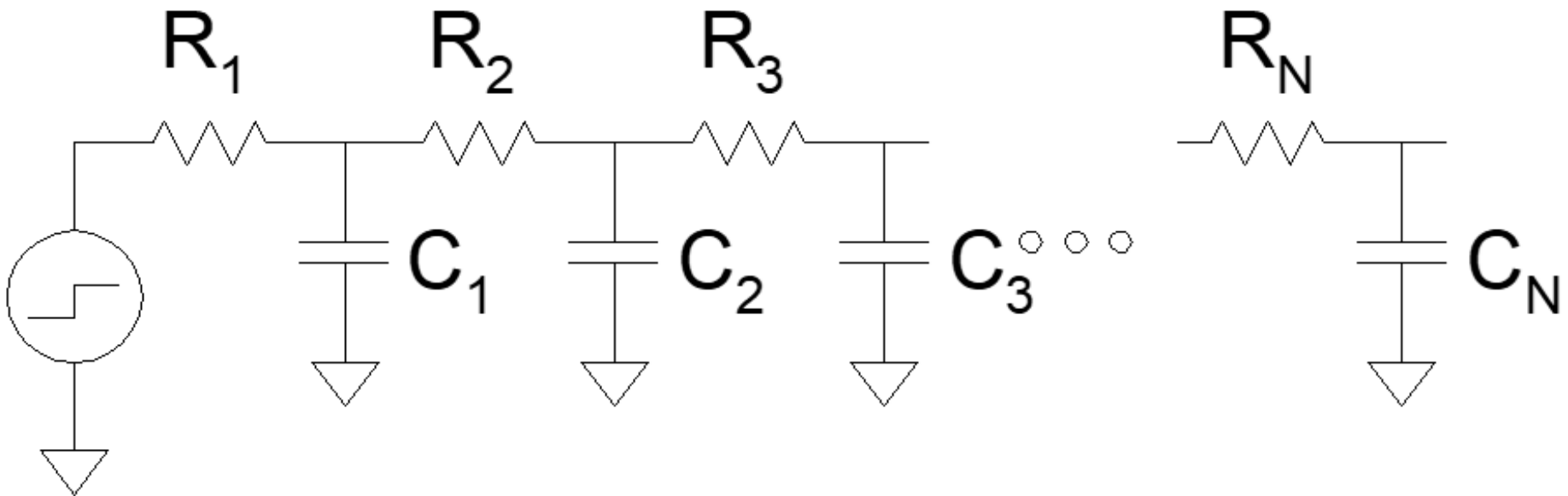



2
2
2
9C
3
5C
3C
3
5C
3C
3
5C

- ON transistors look like resistors
- Pullup or pulldown network modeled as *RC ladder*
- Elmore delay of RC ladder

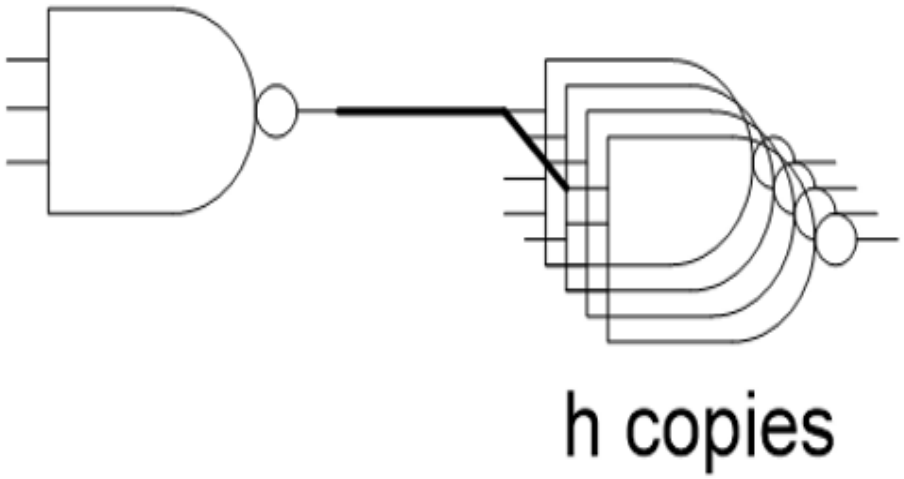
$$t_{pd} \approx \sum_{\text{nodes } i} R_{i-to-source} C_i$$

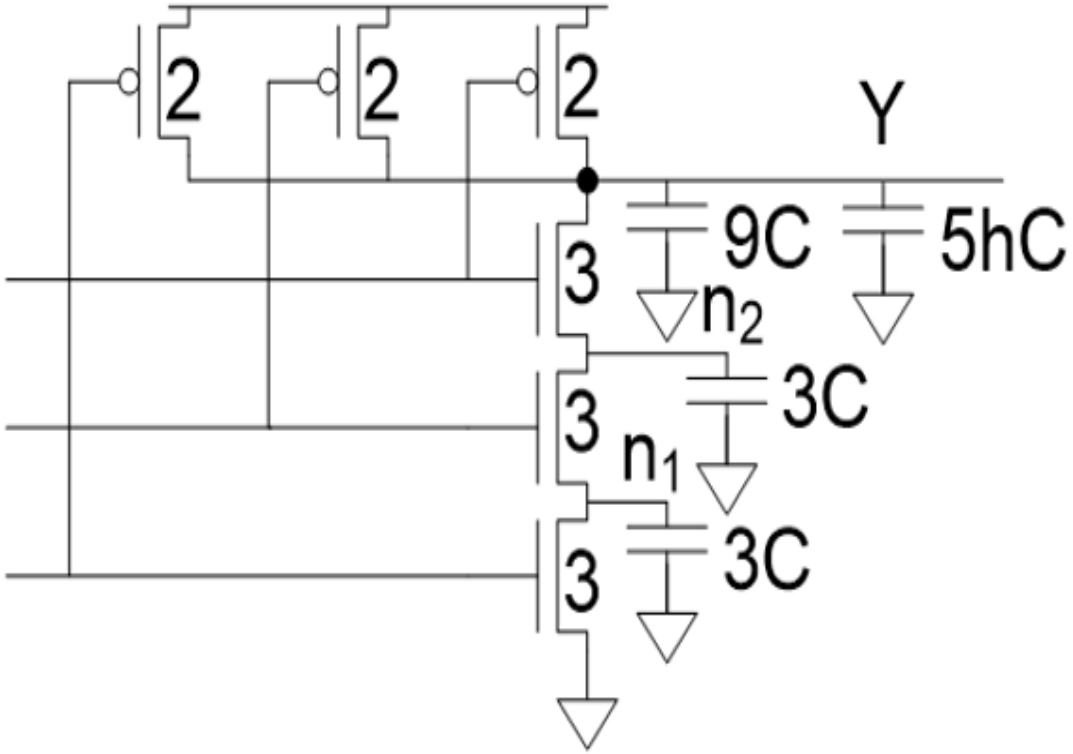
$$= R_1 C_1 + \left(R_1 + R_2\right) C_2 + \ldots + \left(R_1 + R_2 + \ldots + R_N\right) C_N$$



Example: 3-input NAND

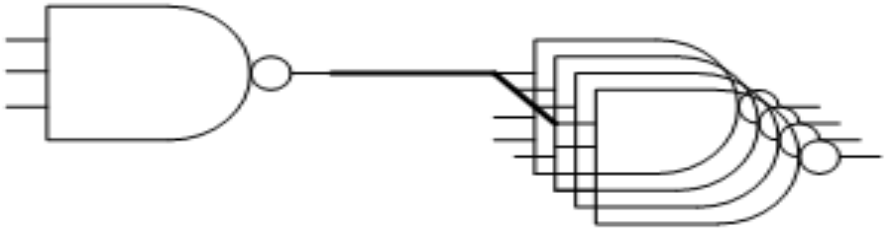
- Estimate worst-case rising and falling delay of 3-input NAND driving *h* identical gates.

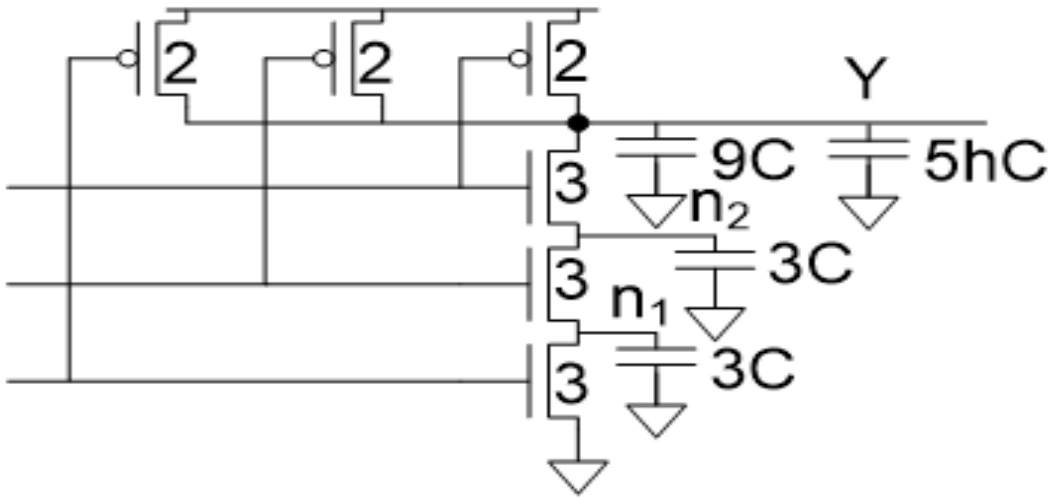


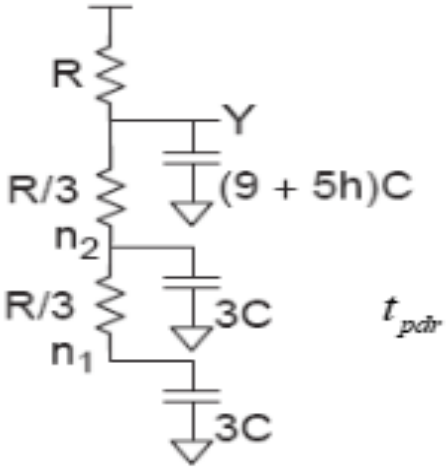


Example: 3-input NAND

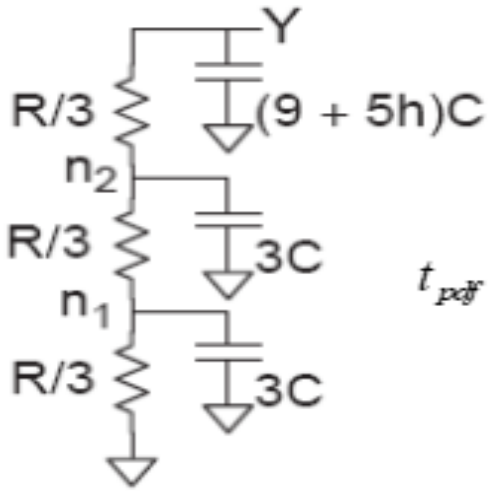
- Estimate worst-case rising and falling delay of 3-input NAND driving *h* identical gates.







$$t_{pdr} = (9+5h)RC$$



$$t_{pdf} = (3C)\left(\tfrac{R}{3}\right) + (3C)\left(\tfrac{R}{3}+\tfrac{R}{3}\right) + \left[(9+5h)C\right]\left(\tfrac{R}{3}+\tfrac{R}{3}+\tfrac{R}{3}\right)$$
$$= (12+5h)RC$$

EFFORT DELAY, LOGICAL EFFORT, ELECTRICAL EFFORT, PARASITIC DELAY

DELAY IN A LOGIC GATE

Delay has two components, namely Effort delay, Parasitic delay

1. Effort Delay (f) = g . h

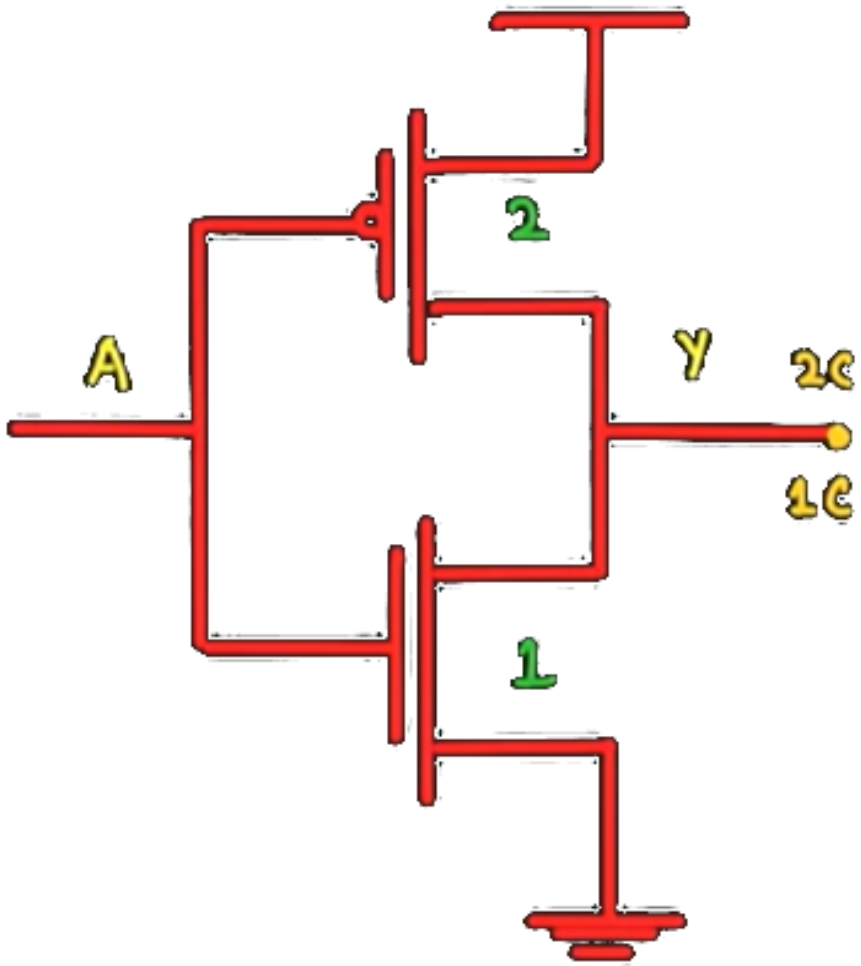
2. Logical Effort (g) - Measures the relative ability of gate to deliver current

3. Electrical Effort (h) - Ratio of output to input capacitance

4. Parasitic Delay - Set by internal parasitic capacitance

$$\text{Delay (d)} = f + p$$

Unskewed - CMOS INVERTER



$$g = \frac{C_{in,gate}}{C_{in,inverter}}$$

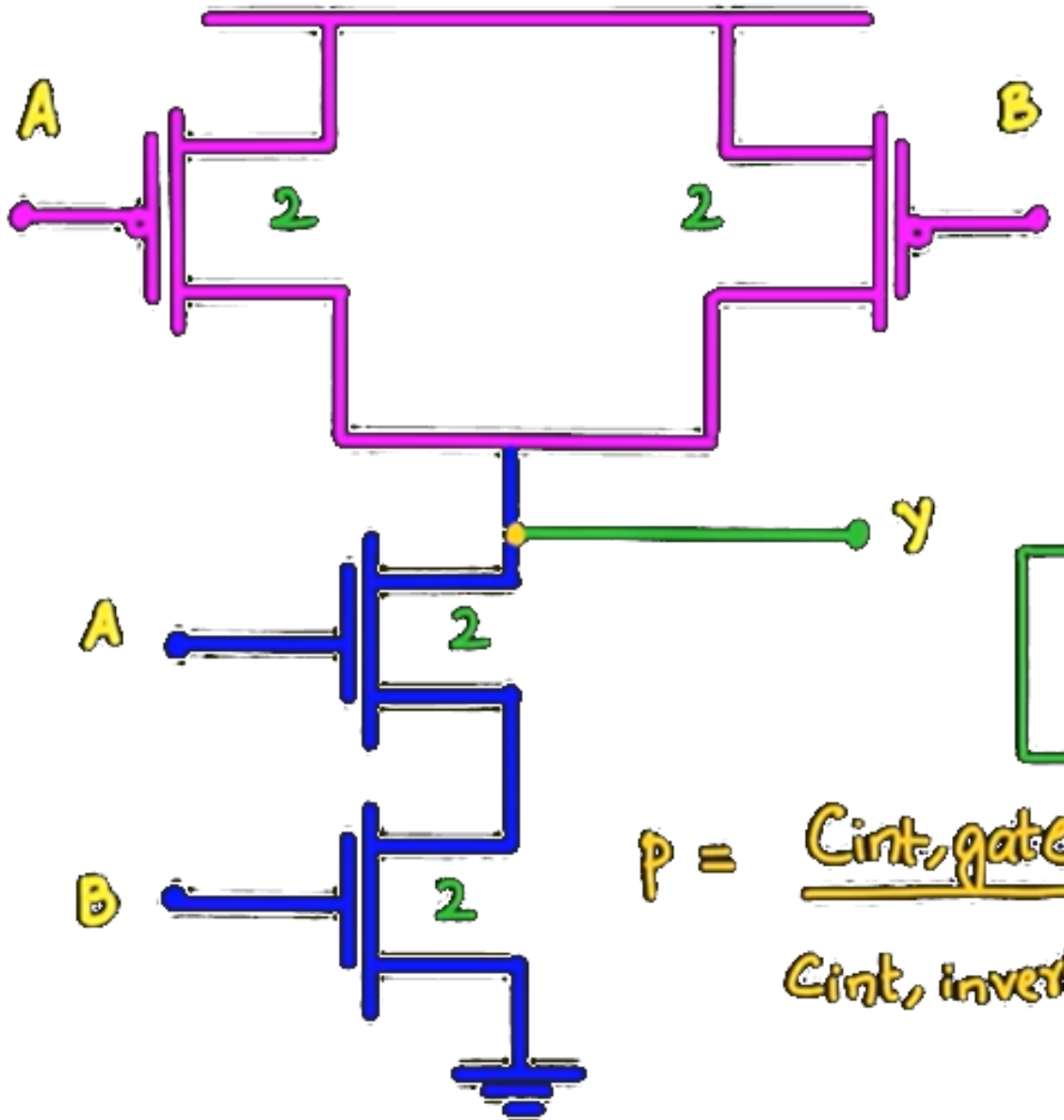
$$C_{in,inverter} = 2C + C = 3C$$

$$C_{in,gate} = 3C$$

$$\boxed{g = 1}$$

$$p = \frac{C_{int,gate}}{C_{int,inverter}} \quad @ \text{ o/p NODE} \qquad p = 1$$

Unskewed - CMOS NAND2 GATE



$$g = \frac{C_{in,\,gate}}{C_{in,\,inverter}}$$

$$C_{in,\,NAND} = 2C + 2C = 4C$$

$$C_{in,\,Inverter} = 2C + 1C = 3C$$

$$\boxed{g = \frac{4}{3}}$$

$$g = \frac{n+2}{3}$$

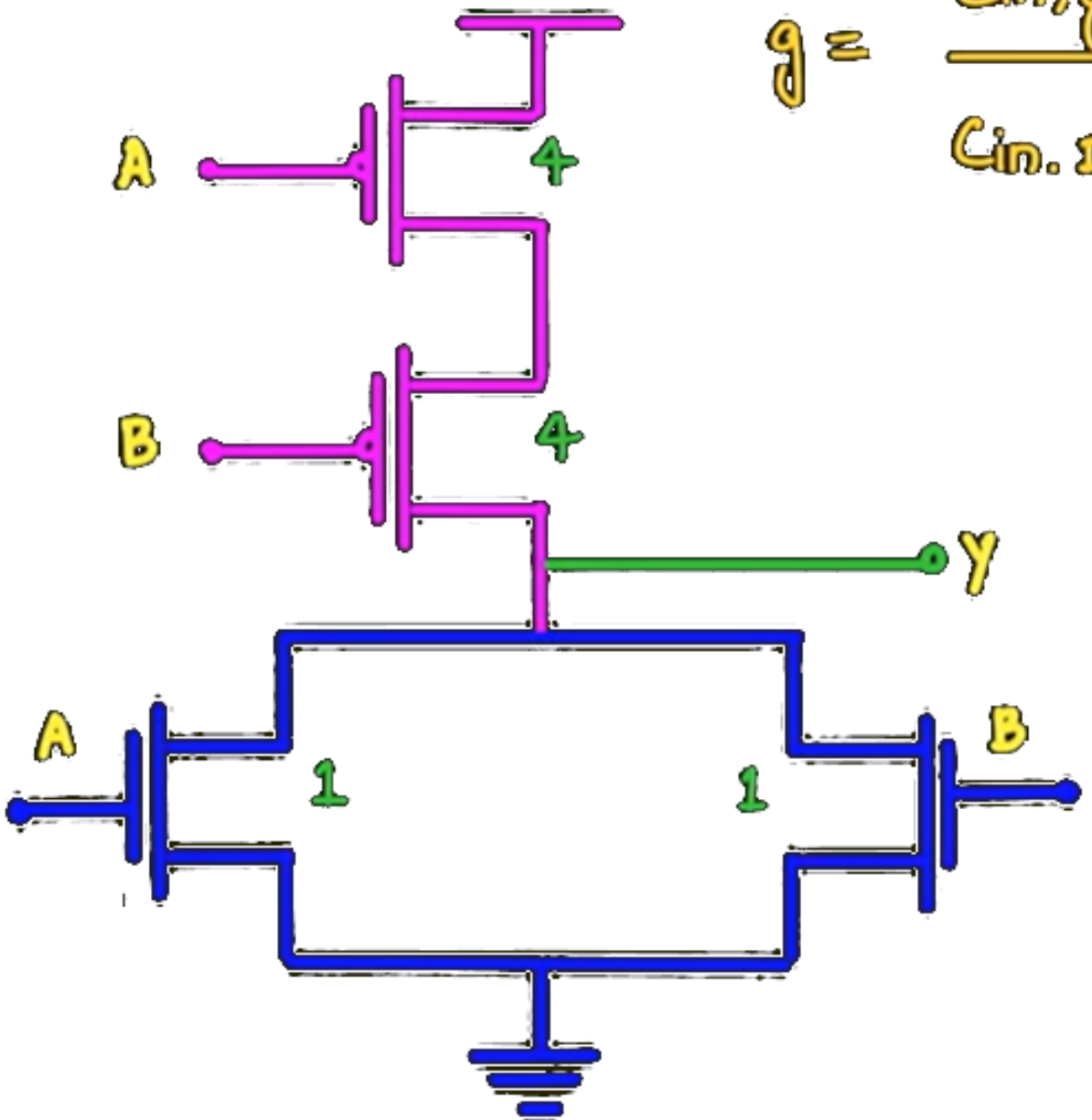
$$p = \frac{C_{int,\,gate}}{C_{int,\,inverter}} \quad @ \text{ o/p NODE}$$

$$C_{int,\,gate} = 6C$$

$$\therefore p = \frac{6C}{3C} = 2 \quad \therefore p = 2$$

$$p = n$$

Unskewed - CMOS NOR2 GATE



$$g = \frac{C_{in,gate}}{C_{in,inverter}} = \frac{5C}{3C} = \frac{5}{3}$$

$$g = \frac{(2n+1)}{3}$$

$$p = \frac{C_{int,gate}}{C_{int,inverter}} \text{ @ o/p NODE}$$

$$= \frac{6C}{3C} \Rightarrow \therefore p = 2 \qquad p = n$$

LOGICAL EFFORT OF COMMON GATES

Gate Type	Number of Inputs				
	1	2	3	4	n
Inverter	1				
NAND		4/3	5/3	6/3	(n + 2) / 3
NOR		5/3	7/3	9/3	(2n + 1) / 3

PARASITIC DELAY OF COMMON GATES

Gate Type	Number of Inputs				
	1	2	3	4	n
Inverter	1				
NAND		2	3	4	n
NOR		2	3	4	n

DELAY IN MULTISTAGE NETWORK

1. PATH LOGICAL EFFORT $G = \prod g_i$

2. PATH ELECTRICAL EFFORT $H = \dfrac{C_{OUT\text{-}path}}{C_{IN\text{-}path}}$

3. PATH EFFORT $F = \prod f_i = \prod g_i h_i$

BRANCHING EFFORT

$$B = \prod b_i$$

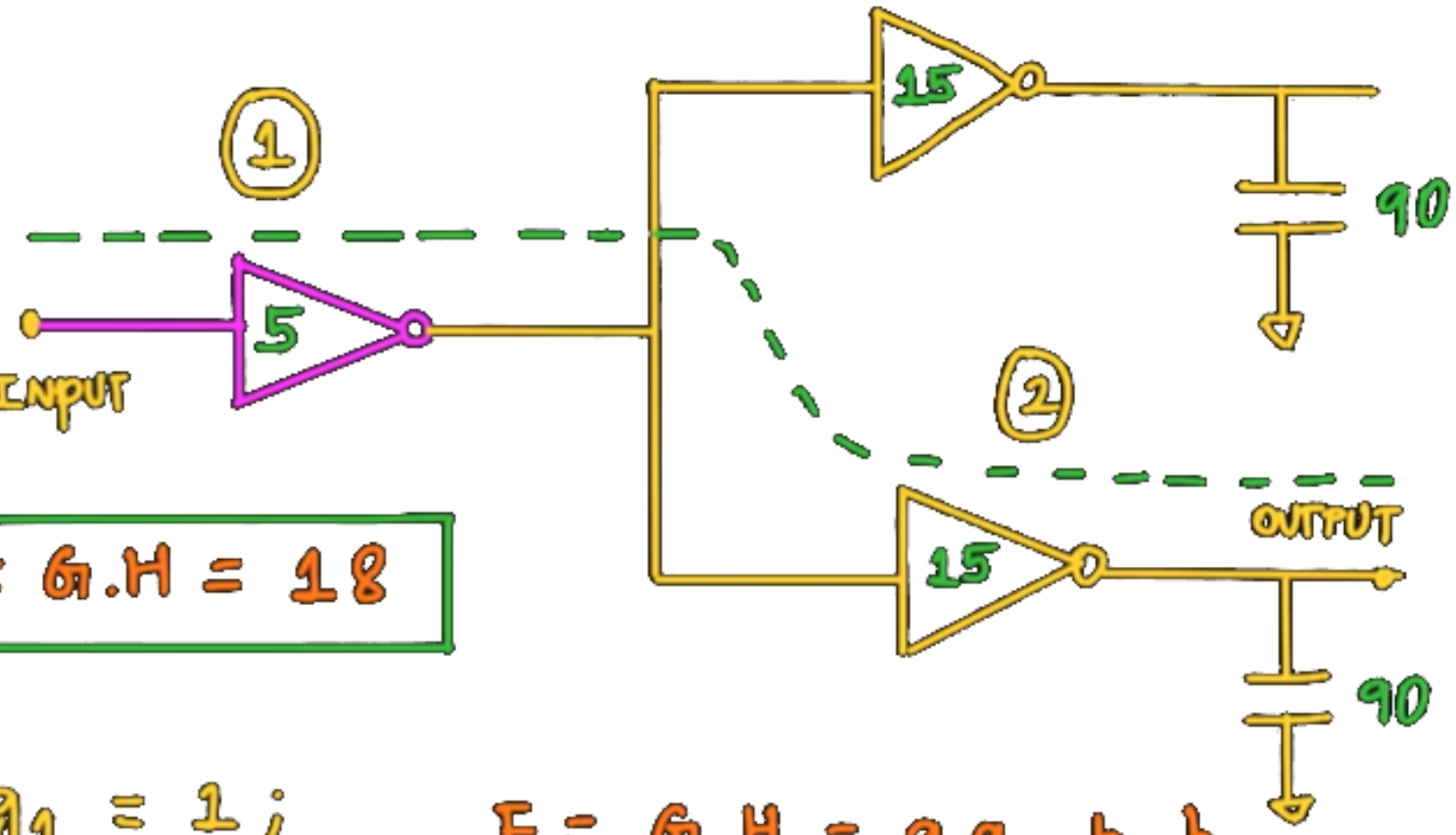
where;

$$b = \frac{C_{ON,path} + C_{OFF,path}}{C_{ON,path}}$$

PATH EFFORT (F) = G.B.H.

BRANCHING EFFORT

$$H = \frac{C_{out,path}}{C_{in,path}} = \frac{90}{5} = 18$$



$$G = \prod g_i = g_1 \cdot g_2 = 1$$

$$G.H = 18 \qquad \therefore \boxed{F = G.H = 18}$$

$$h_1 = \frac{15+15}{5} = 6 \; ; \quad g_1 = 1 \; ;$$

$$h_2 = \frac{90}{15} = 6 \; ; \quad g_2 = 1 \; ;$$

$$F = G.H = g_1 g_2 . h_1 . h_2$$

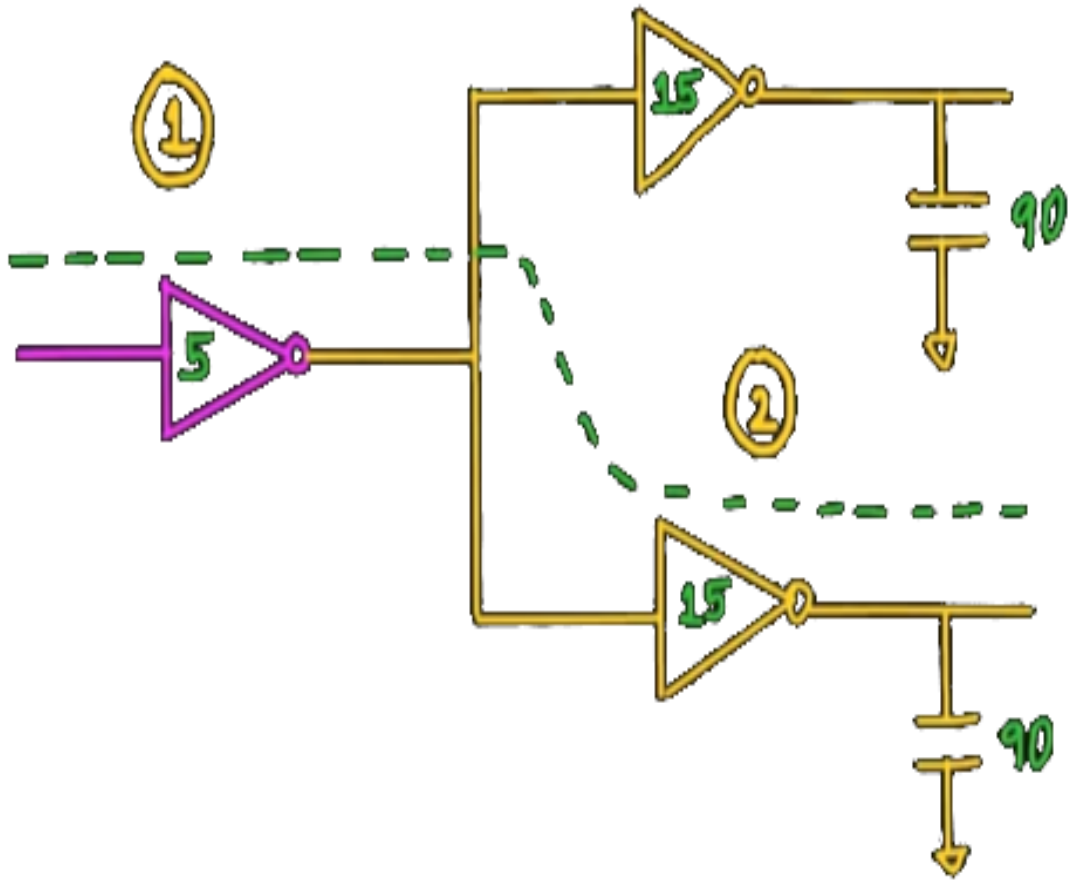
$$= 6.6 = 36$$

$$\boxed{F = 36} \qquad = 2GH$$

BRANCHING EFFORT

$$B = \prod b_i$$

where; $$b = \frac{C_{ON,path} + C_{OFF,path}}{C_{ON,path}}$$

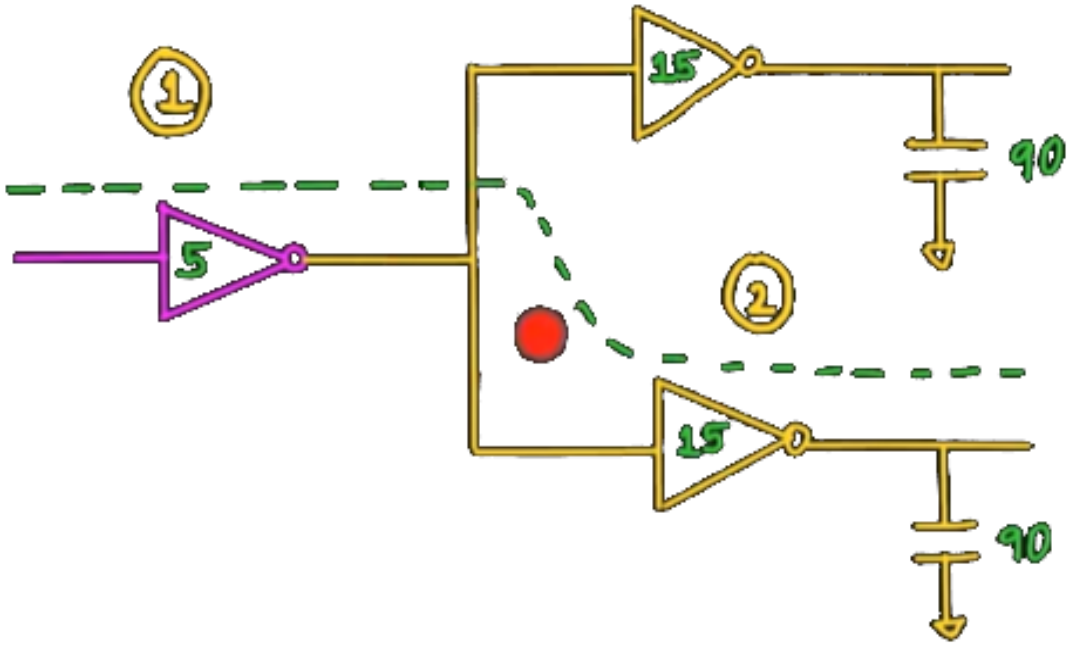


PATH EFFORT (F) = G.B.H.

BRANCHING EFFORT

$$B = \prod b_i$$

where; $$b = \frac{C_{ON,path} + C_{OFF,path}}{C_{ON,path}}$$



PATH EFFORT (F) = G.B.H.

$$b_1 = \frac{15 + 15}{15} = 2 \quad \therefore \boxed{B = 2}$$

$G = 1$; $H = 18$

$$F = G.B.H = 2.18 = 36$$

DELAY IN MULTISTAGE NETWORK

1. PATH EFFORT DELAY $D_F = \sum f_i$

2. PATH PARASITIC DELAY $P = \sum p_i$

3. PATH DELAY $D = \sum d_i = D_F + P$

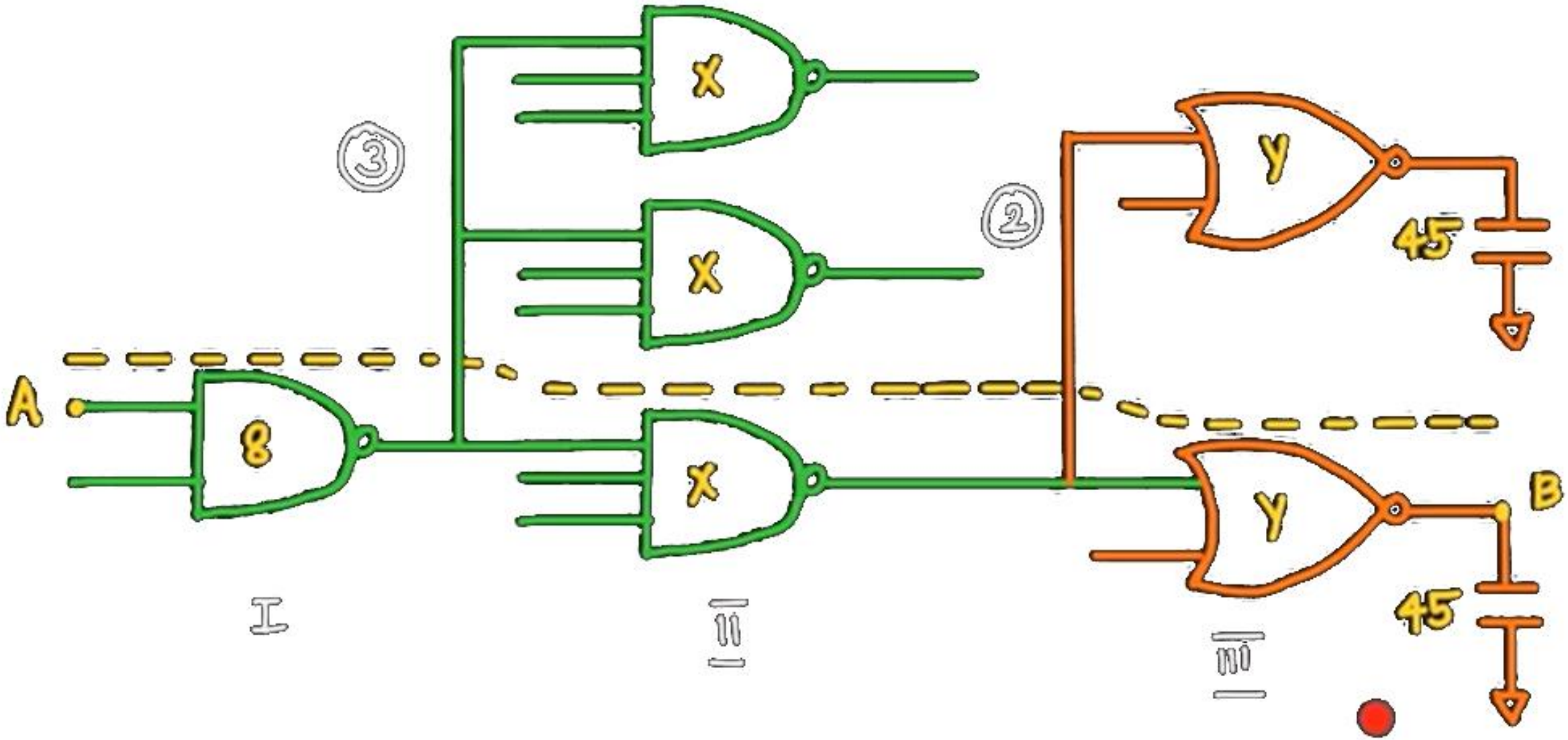
Delay is smallest, when each stage bears same effort.

$$\therefore \hat{f} = g_i h_i = F^{1/N}$$

Hence, the minimum delay of "N" stage path :

$$D = NF^{1/N} + P$$

BEST STAGE EFFORT



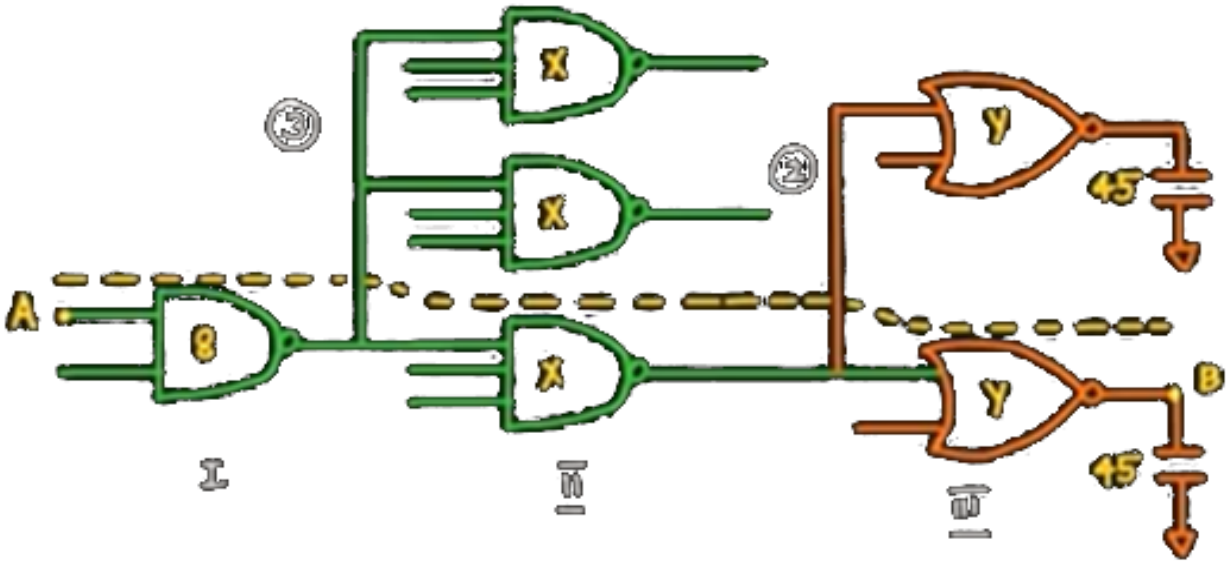
$$H = \frac{C_{out,path}}{C_{in,path}} = \frac{45}{8}$$

$$G = \prod g_i = g_1 . g_2 . g_3$$

$$G = \frac{4}{3} \times \frac{5}{3} \times \frac{5}{3} = \frac{100}{27}$$

$$B = \prod b_i = b_1 . b_2$$

$$b_1 = \frac{x + 2x}{x} = \frac{3x}{x} = 3 ;$$



$$b_2 = \frac{y + y}{y} = \frac{2y}{y} = 2$$

$$\therefore \quad B = b_1 . b_2 = 6 .$$

$$F = G . B . H = \frac{100}{27} \times 6 \times \frac{45}{8}$$

$$\therefore F = 125$$

$$\therefore \quad \hat{f} = f_{opt} = (F)^{1/N} \qquad (N = 3) \qquad \therefore F = 125$$

$$\therefore \quad \hat{f} = (125)^{1/3} = 5. \qquad \therefore \hat{f} = 5$$

$$D = N(F)^{1/N} + P$$

$$P = \sum P_i = P_1 + P_2 + P_3 = 2 + 3 + 2 = 7$$

$$D = (3 \times 5) + 7 \qquad \therefore \quad \boxed{D = 22}$$

BEST STAGE EFFORT

$\hat{f} = 5 \qquad (\because f = g.h)$

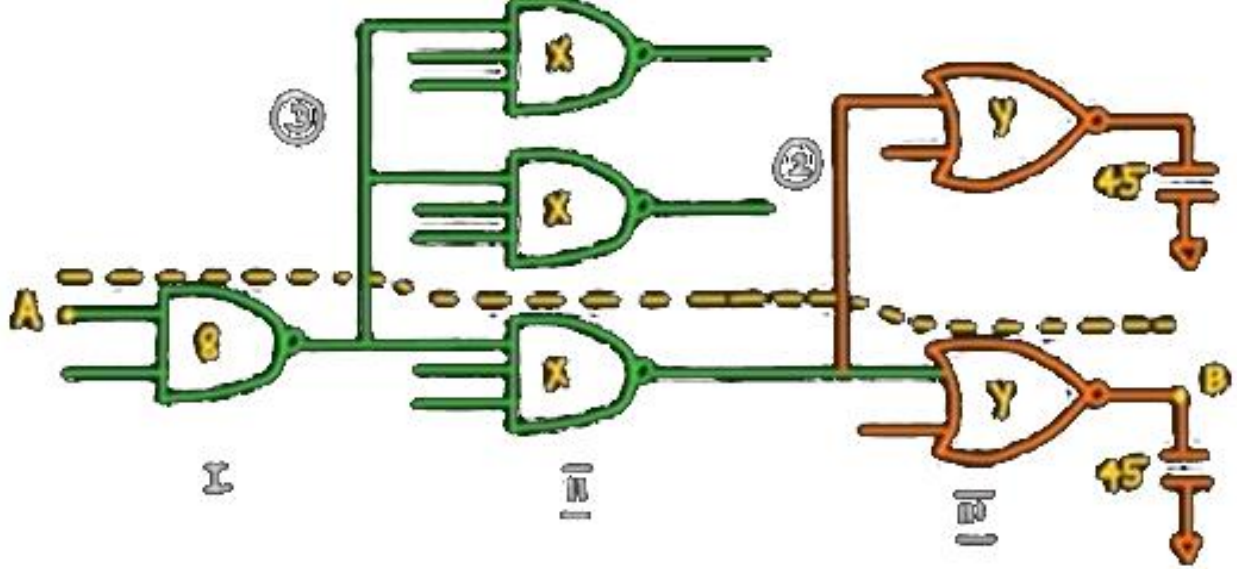
$g = 5/3 \; ; \; h = 45/y$

$f = g.h$

$5 = 5/3 \times 45/y$

$\therefore \quad y = \frac{5}{3} \times \frac{45}{5} = 15$

$\therefore \quad y = 15$



$f = g.h$

$5 = 5/3 \times \frac{2y}{x}$

$x = \frac{5}{3} \times \frac{2 \times 15}{5} = 10$

$\therefore \quad x = 10$

$f = g.h$

$5 = \frac{4}{3} \times \frac{3x}{8}$

$5 = \frac{4}{3} \times \frac{30}{8}$

$5 = 5$

VERIFIED

Stage - I - NAND2

$$d = f + p \quad (f = g \cdot h)$$

$$d = \left(\frac{4}{3} \times \frac{30}{8}\right) + 2$$

$$\therefore \; d = 7$$

Stage - II - NAND3

$$d = g \cdot h + p$$

$$d = \left(\frac{5}{3} \times \frac{2 \times 15}{10}\right) + 3$$

$$\therefore \; d = 8$$

Stage - III - NOR2

$$d = g \cdot h + p$$

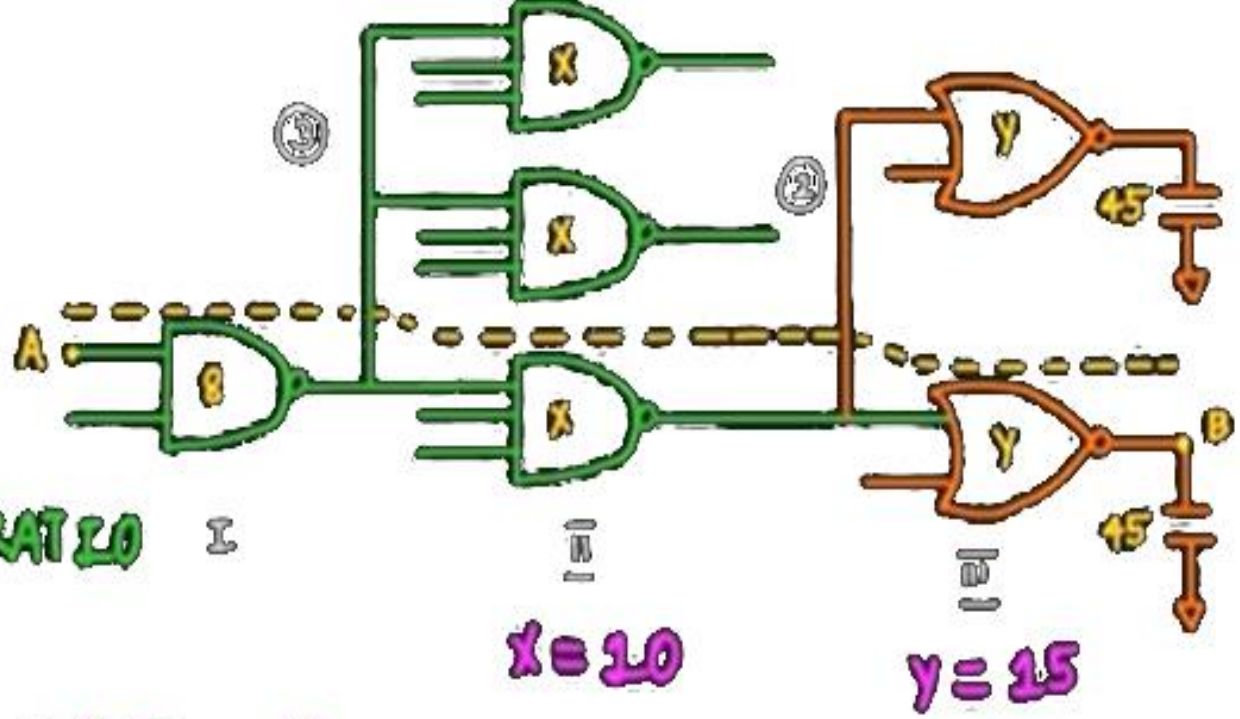
$$d = \left(\frac{5}{3} \times \frac{45}{15}\right) + 2$$

$$\therefore \; d = 7$$

$$D = \sum d_i = 7 + 8 + 7 = 22$$

Verified

BEST STAGE EFFORT



STAGE - III - NOR2 :

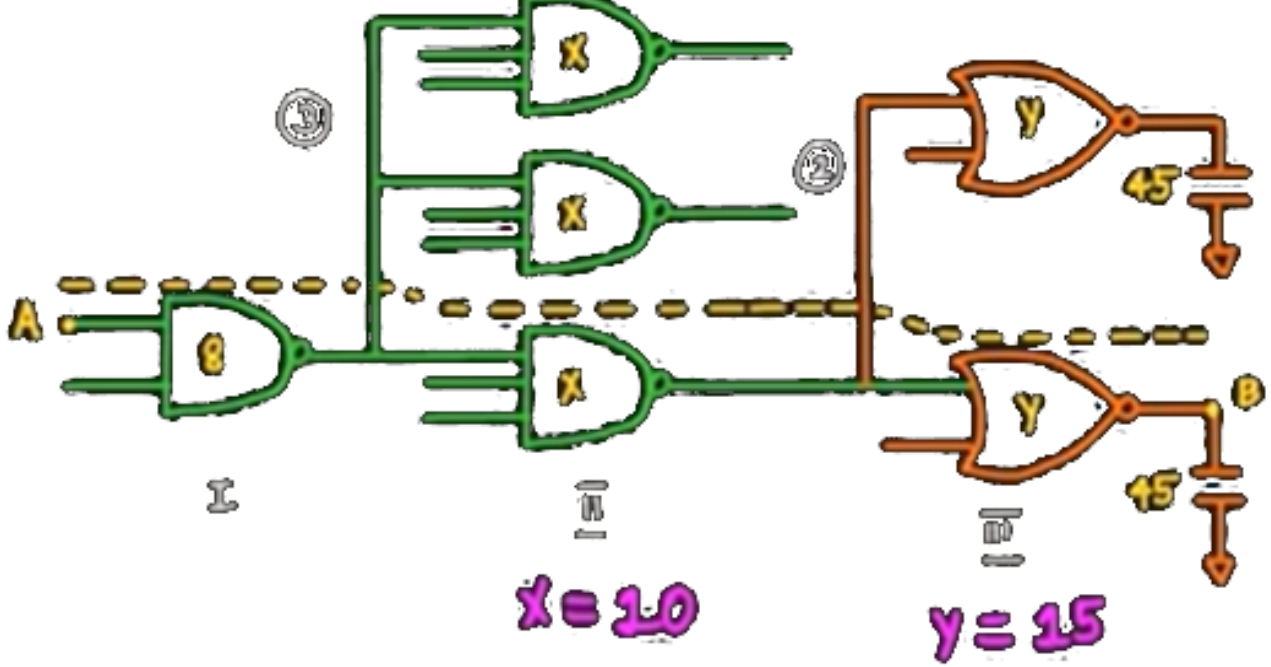
PMOS : 4 & NMOS : 1 (W/L) RATIO

$$NMOS = \frac{1}{5} \text{ of } Y = \frac{1}{5} \times 15 = 3$$

N : 3

$$PMOS = \frac{4}{5} \text{ of } Y = \frac{4}{5} \times 15 = 12 \Rightarrow P : 12$$

BEST STAGE EFFORT



STAGE - II - NAND 3 :

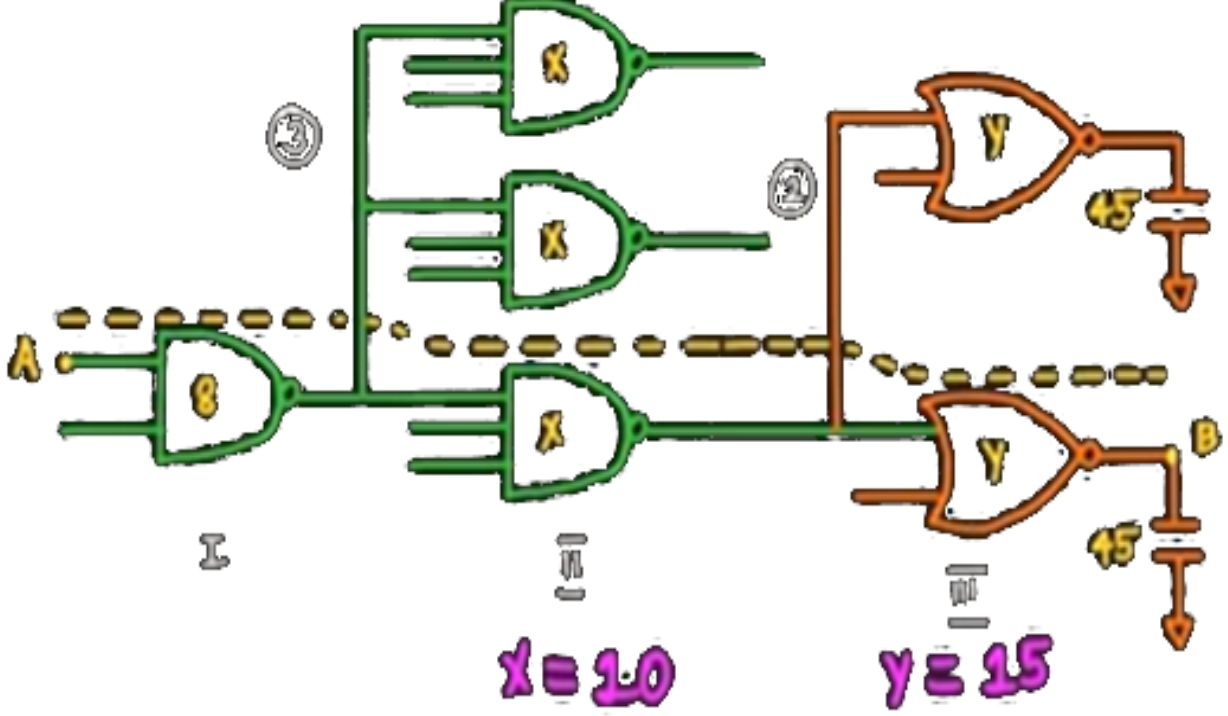
PMOS = 2; NMOS = 3; W/L ratio

NMOS = 3/5 of X = 3/5 × 10 = 6

⇒ N: 6

PMOS = 2/5 of X = 2/5 × 10 = 4 ⇒ P: 4

BEST STAGE EFFORT



STAGE - I - NAND 2 :

PMOS = 2; NMOS = 2 (W/L RATIO)

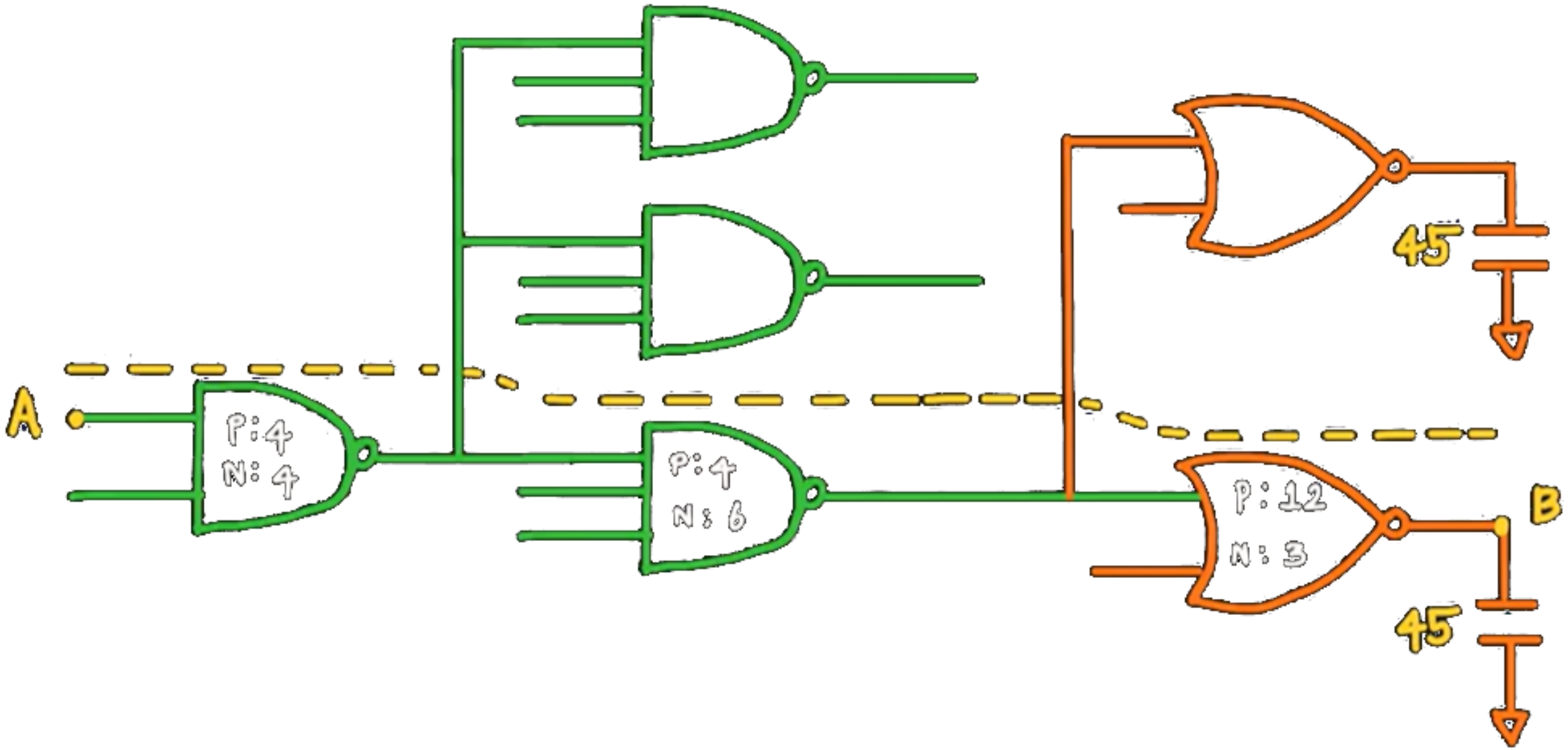
NMOS = 2/4 of 8 = 4

⇒ N: 4

PMOS = 2/4 of 8 = 4

⇒ P: 4

BEST STAGE EFFORT



Power Dissipation (Static Dissipation)

STATIC :-

- Subthreshold cond^n
- Tunneling current
- Leakage through RB diodes

$P_{avg(static)} \cong 0$

$I_{Leakage}$

$P_T = P_{static} + P_{dyn}$

Dynamic

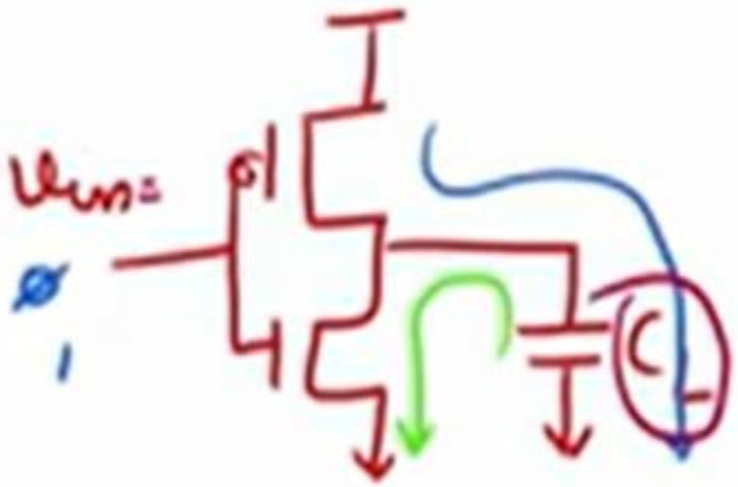
1. Charging and discharg of Load Cap
2. "Short ckt" current

NMOS - PMOS

both are partially ON

in 5 minutes

Power Dissipation (Dynamic Dissipation)



i/p = 0 , $C_L = V_{DD}$

i/p = 1, $C_L = 0$

1 Charge + 1 discharge = charge moves V_{DD} to GND ✓✓

C_L is switched between V_{DD} and GND @ avg freq of 'F_{sw}'

$Q = C_L V_{DD}$

Total charge moved from V_{DD} to GND via char & disch of C_L in 1 sec

$= 1 \cdot \boxed{F_{sw} \cdot C_L \cdot V_{DD}}$

'T'

$= T \cdot F_{sw} \cdot C_L \cdot V_{DD}$

Power Dissipation (Dynamic Dissipation)

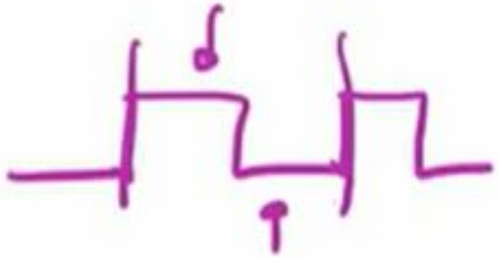
$$P_{dyn} = \frac{1}{T}\int_0^T i_{dd}(t) \cdot V_{DD} \cdot dt$$

$$= \frac{V_{DD}}{T}\int_0^T i_{dd}(t)\, dt$$

$$= \frac{V_{DD}}{T}\left[F_{sw} \cdot V_{DD} \cdot C_L\right)\left[T\right]$$

$$= V_{DD}^2 \cdot F_{sw} \cdot C_L$$

$$P_{dynamic} = V_{DD}^2 \cdot \alpha \cdot F \cdot C_L$$



α = 1 for one clock cycle switching

$F_{sw} = \alpha F$

activity factor

in 3 minutes