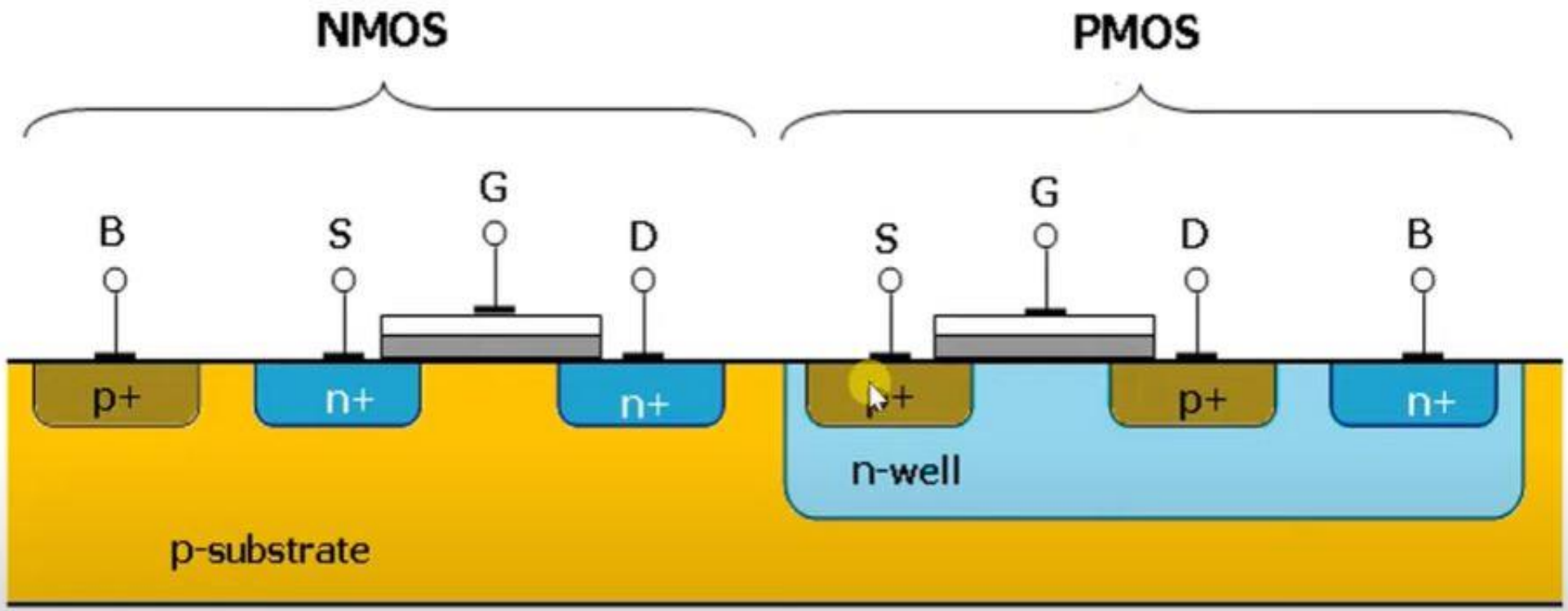
CMOS Fabrication & Layout

Unit -3

by
Dr. SAKTHIVEL.S.M

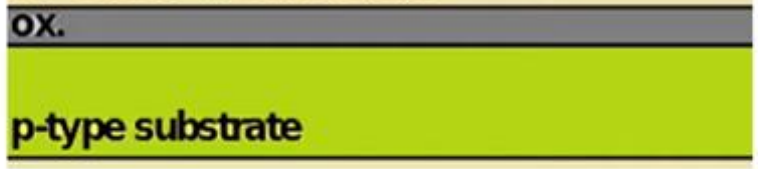
CMOS Structure

nMOS and pMOS structure on P Type Substrate

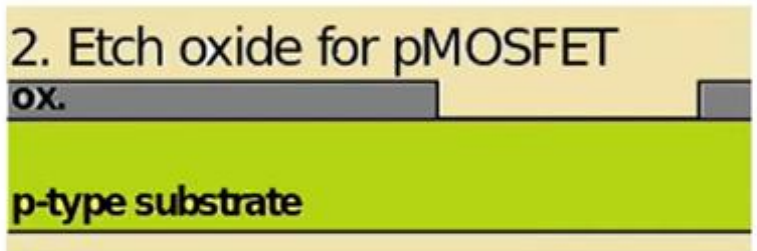


nMOS and pMOS on P Type Substrate - N WELL PROCESS

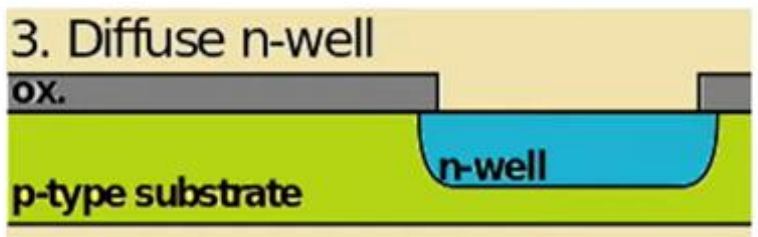
1. Grow field oxide



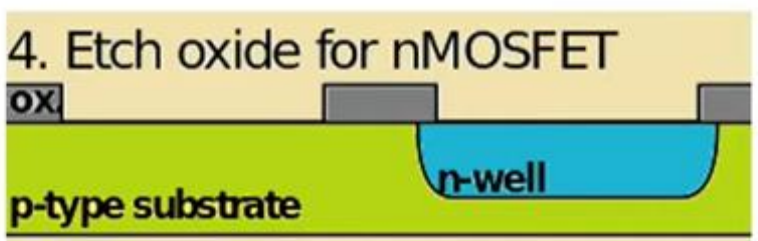
2. Etch oxide for pMOSFET



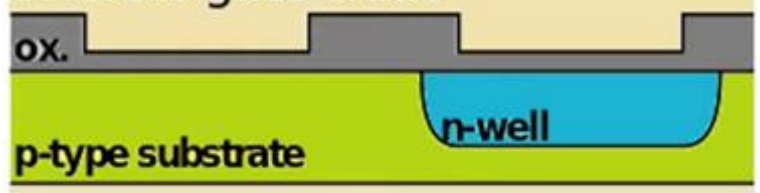
3. Diffuse n-well



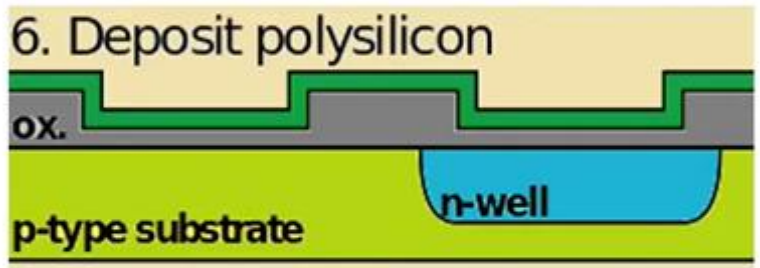
4. Etch oxide for nMOSFET



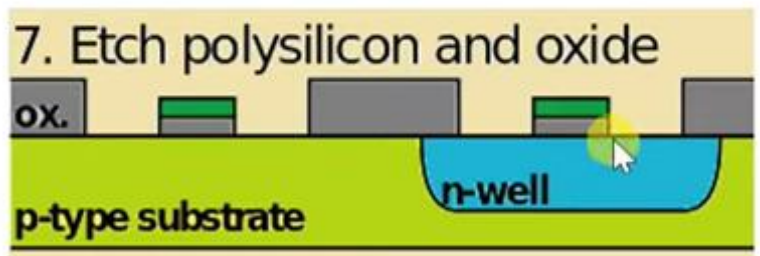
5. Grow gate oxide



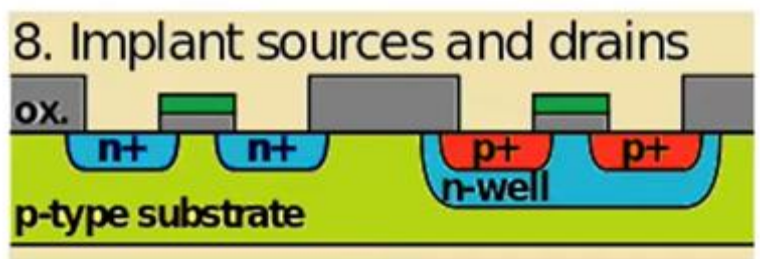
6. Deposit polysilicon



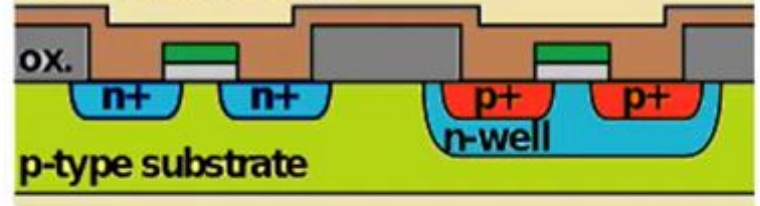
7. Etch polysilicon and oxide



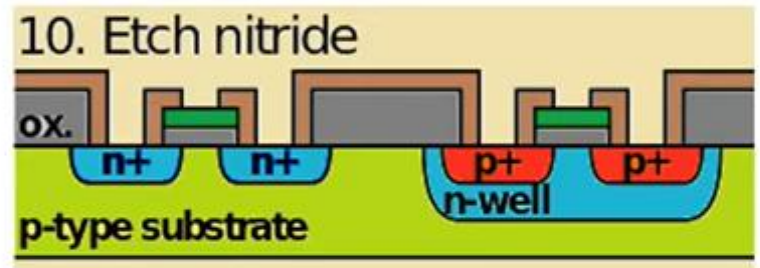
8. Implant sources and drains



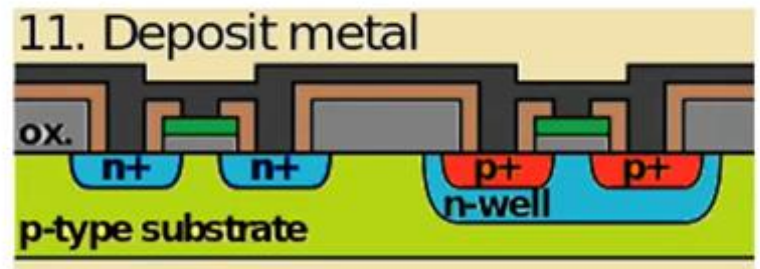
9. Grow nitride



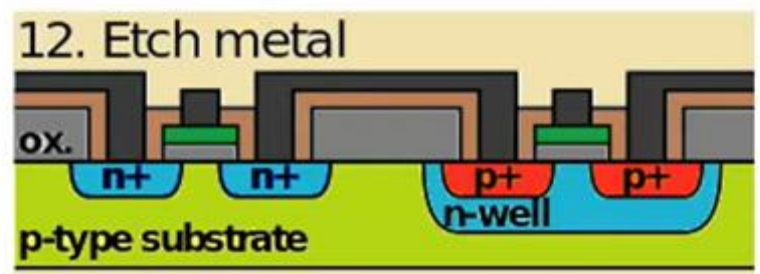
10. Etch nitride



11. Deposit metal

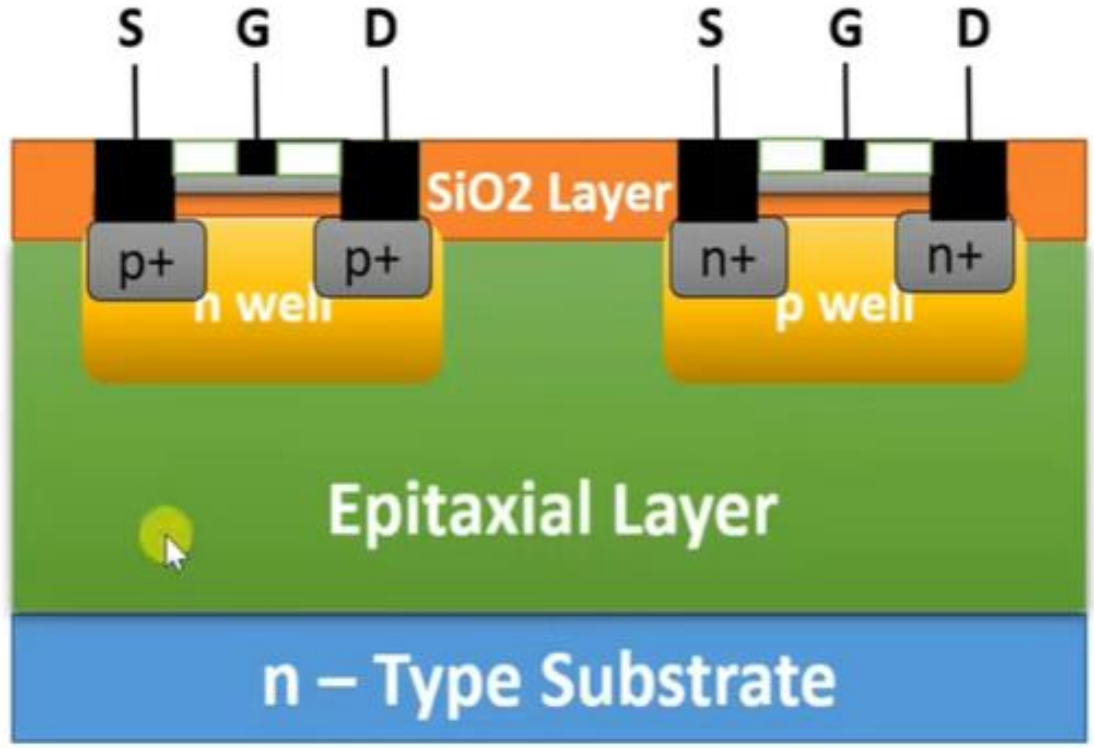


12. Etch metal

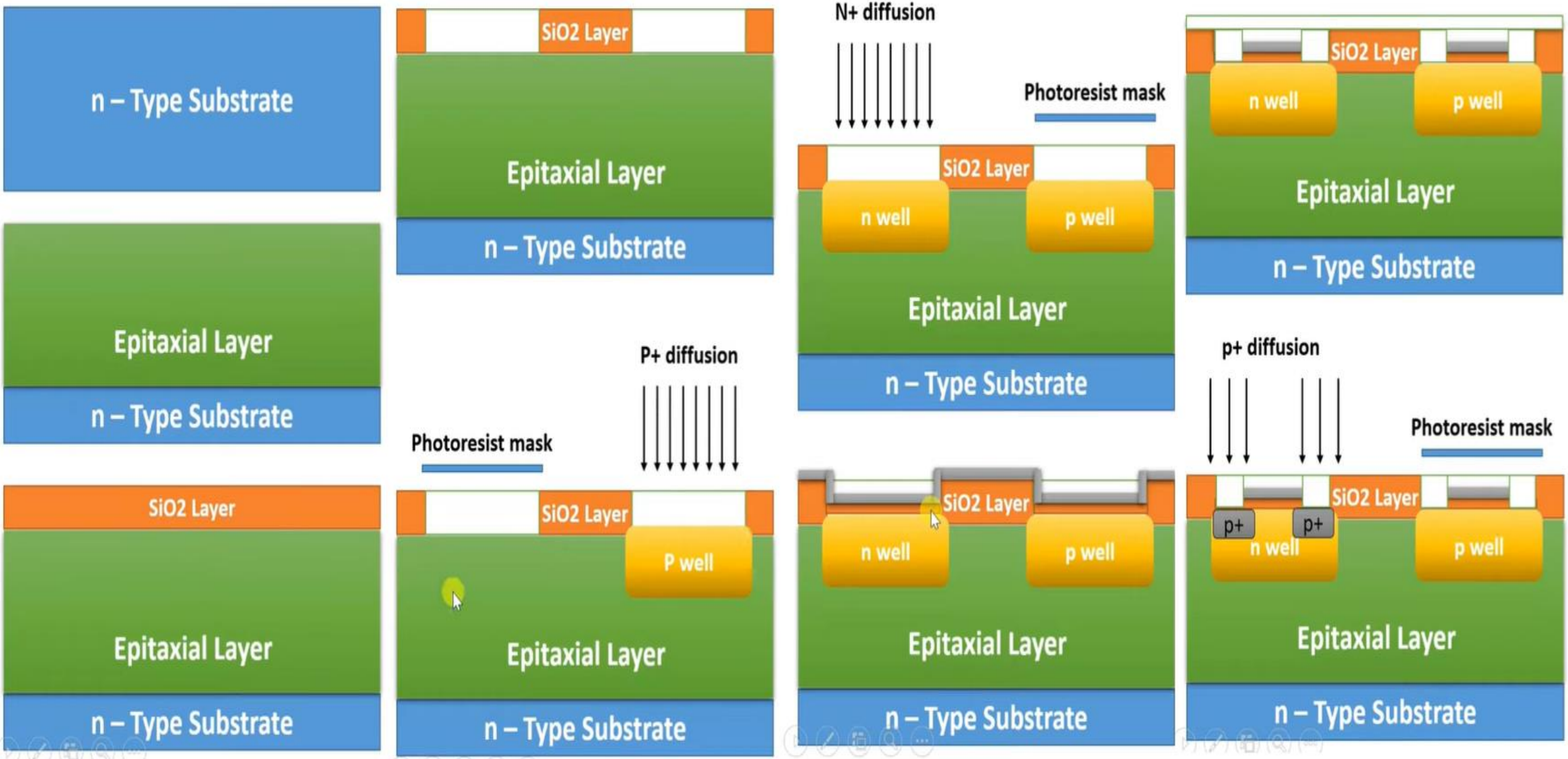


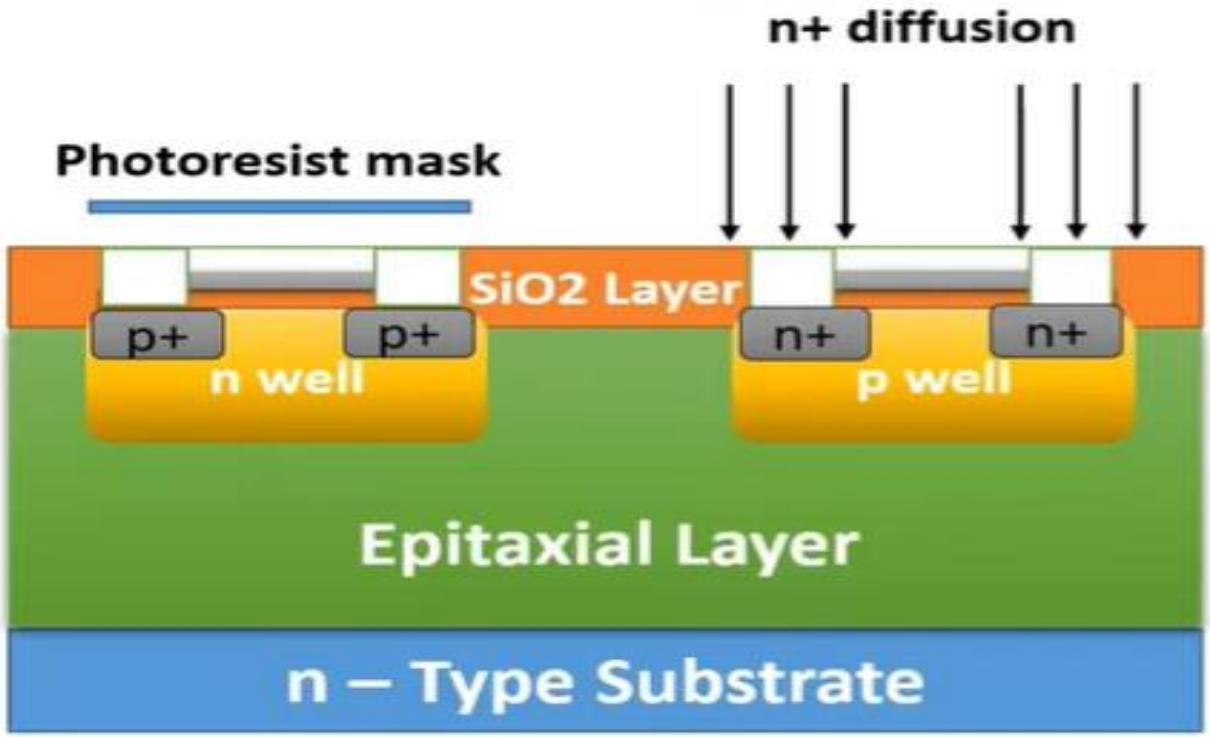
Basics of Twin tube fabrication process

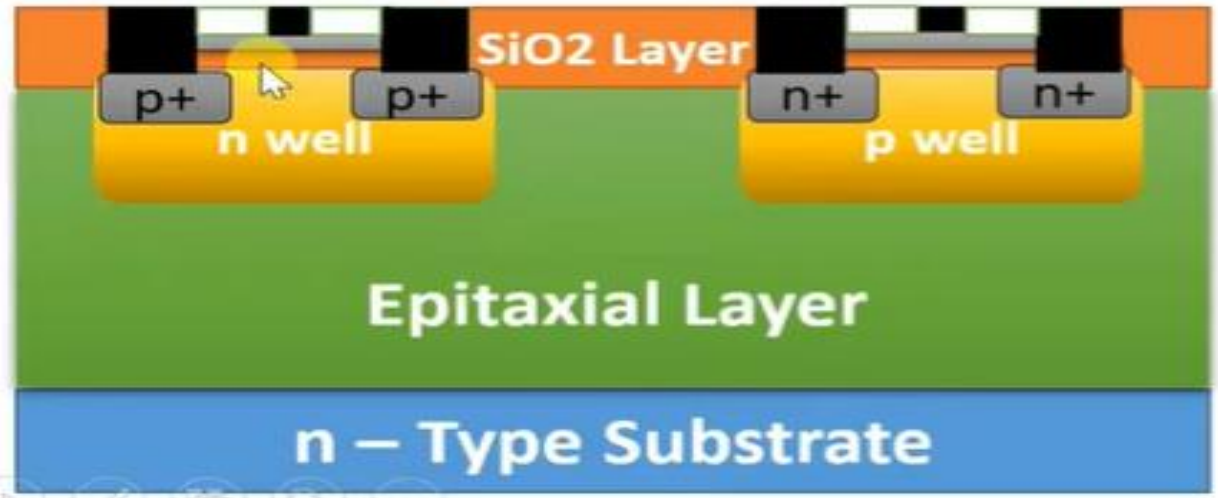
- In our previous video, I have explained nMOS and pMOS structure on P Type Substrate.
- In that, there can be issues regarding, mutual coupling in between nMOS and pMOS.
- There can be major issues regarding, Latch up for CMOS fabrication.
- To avoid those issues, we should fabrication nMOS and pMOS by twin tube fabrication process.

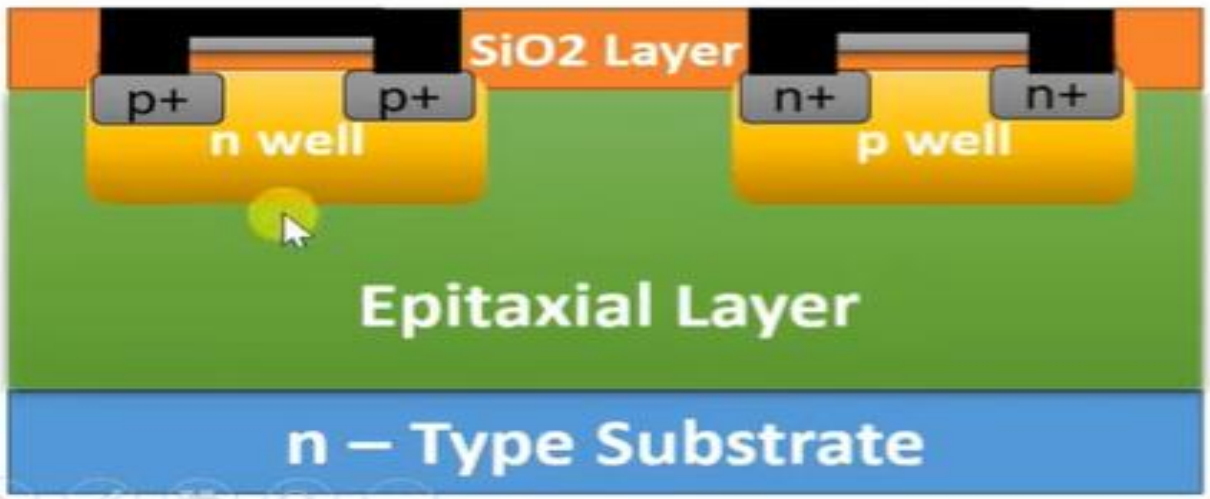


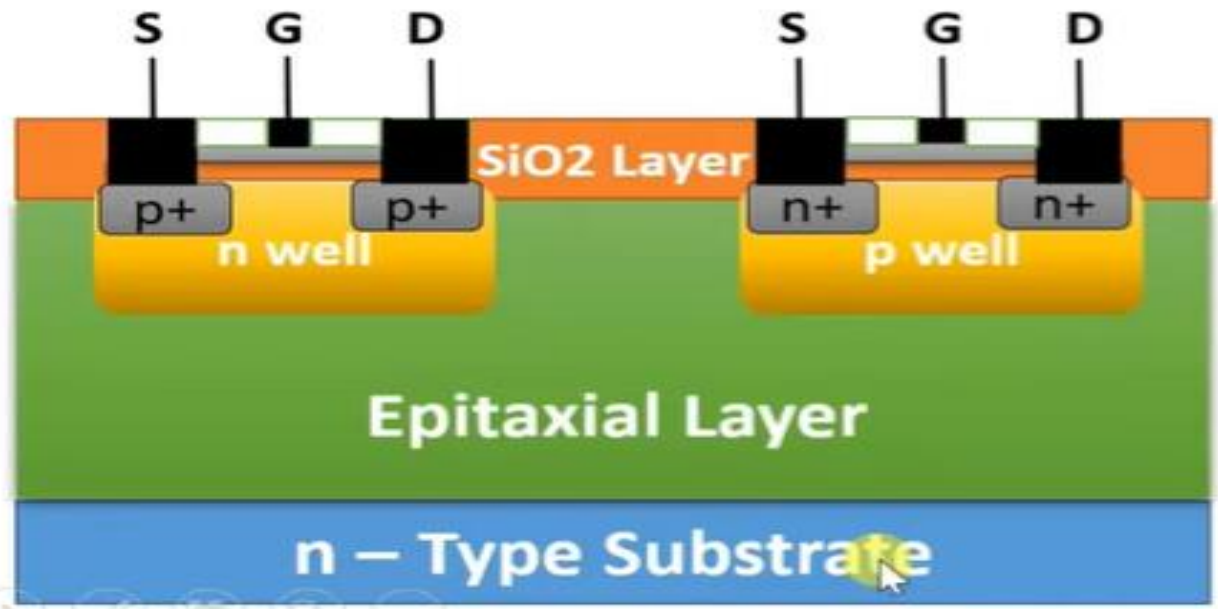
TWIN TUB PROCESS




n+ diffusion
Photoresist mask
SiO2 Layer
p+
p+
n+
n+
n well
p well
Epitaxial Layer
n – Type Substrate


SiO2 Layer
p+
p+
n+
n+
n well
p well
Epitaxial Layer
n – Type Substrate


SiO2 Layer
p+
p+
n+
n+
n well
p well
Epitaxial Layer
n – Type Substrate


S
G
D
S
G
D
SiO2 Layer
p+
p+
n+
n+
n well
p well
Epitaxial Layer
n – Type Substrate

1. Latch-up issue in CMOS

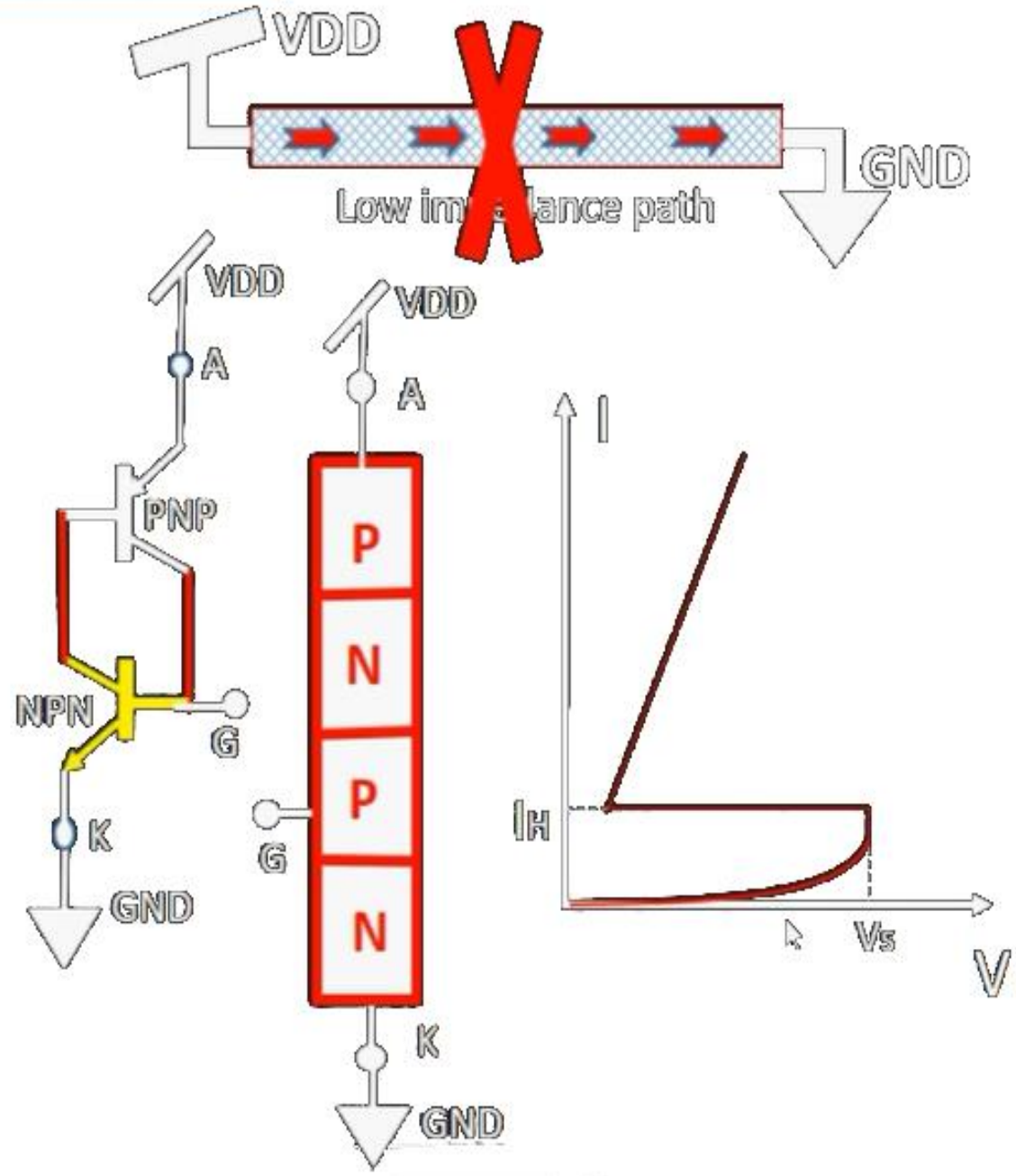
What is Latch-up ?

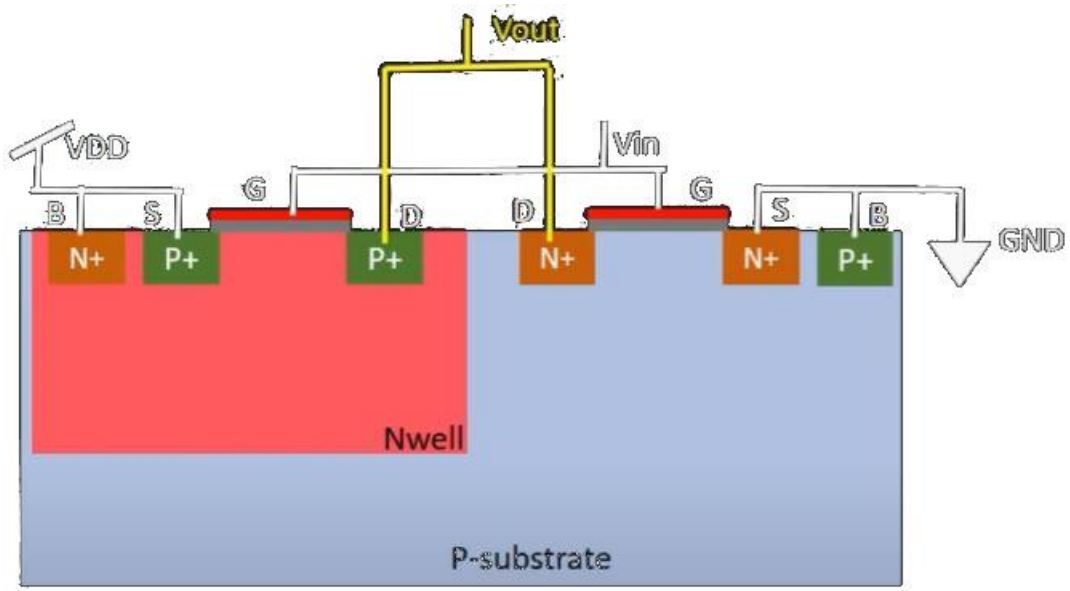
- In simplest words, Latch-up is a formation of direct current path between VDD and GND. Which cause large current flow between Power supply terminal to Ground terminal

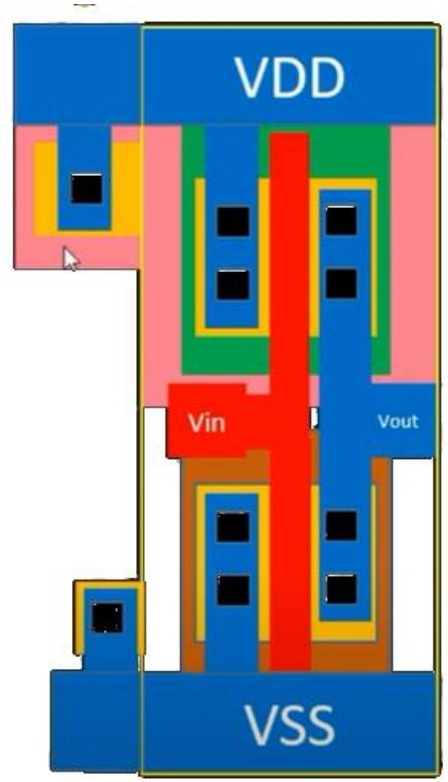
- Technically, Latch-up is a phenomena of activation of **parasitic BJTs** in CMOS circuit which form **a low impedance path** between Power supply and Ground. This low impedance path draw **large current** which heat up the IC and cause **permanent damage**

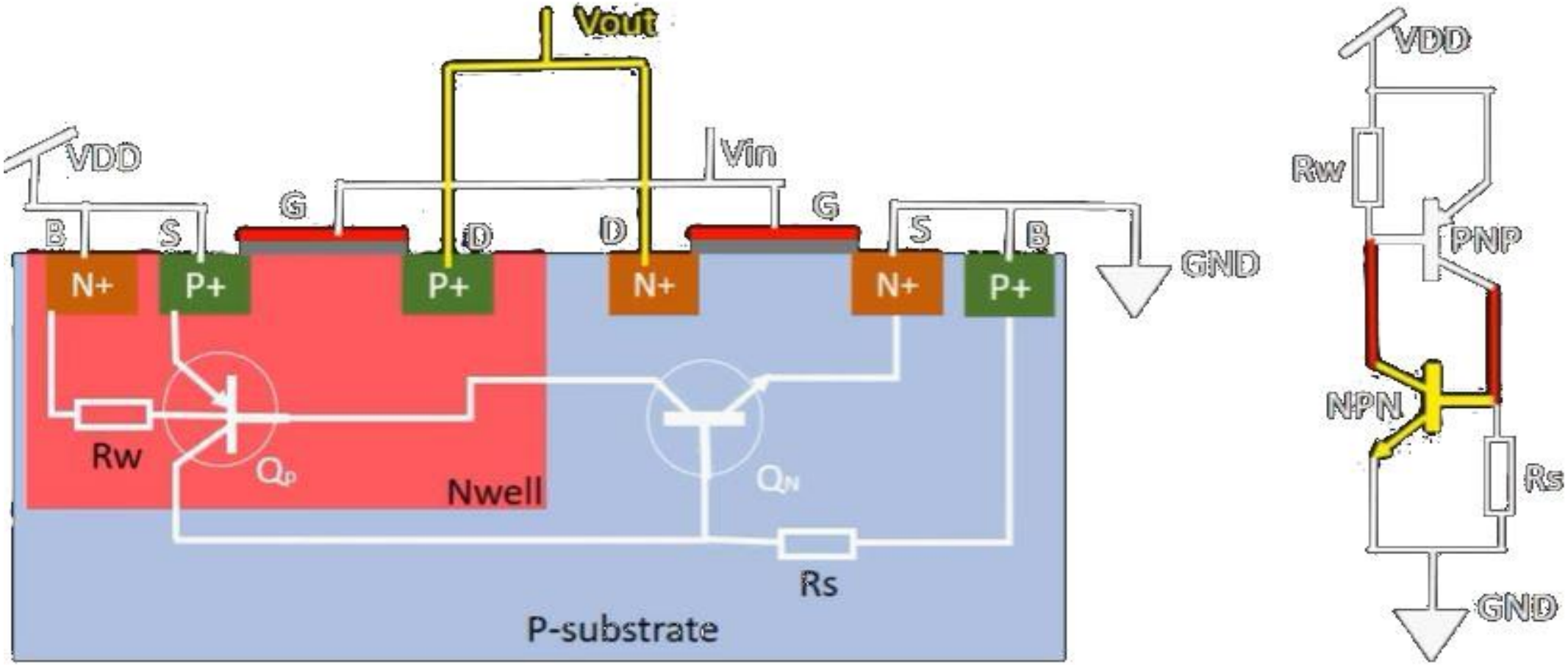
- In CMOS circuit, two parasitic BJT get formed and connected in such a way that it forms a PNPN device / SCR / Thyristor

- A PNPN device is normally on OFF stage with minimal current flow but once it get triggered by Gate signal, it continue to flow large current even if the triggered gate signal has been removed. This phenomena is actually called latched up




Vout
VDD
Vin
G
G
B
S
D
D
S
B
N+
P+
P+
N+
N+
P+
GND
Nwell
P-substrate


VDD
Vin
Vout
VSS



- Unless SCR is triggered, there is no low impedance path formed
- Each BJT has here low current gain, so large current spike is needed to activate them

STICK DIAGRAM

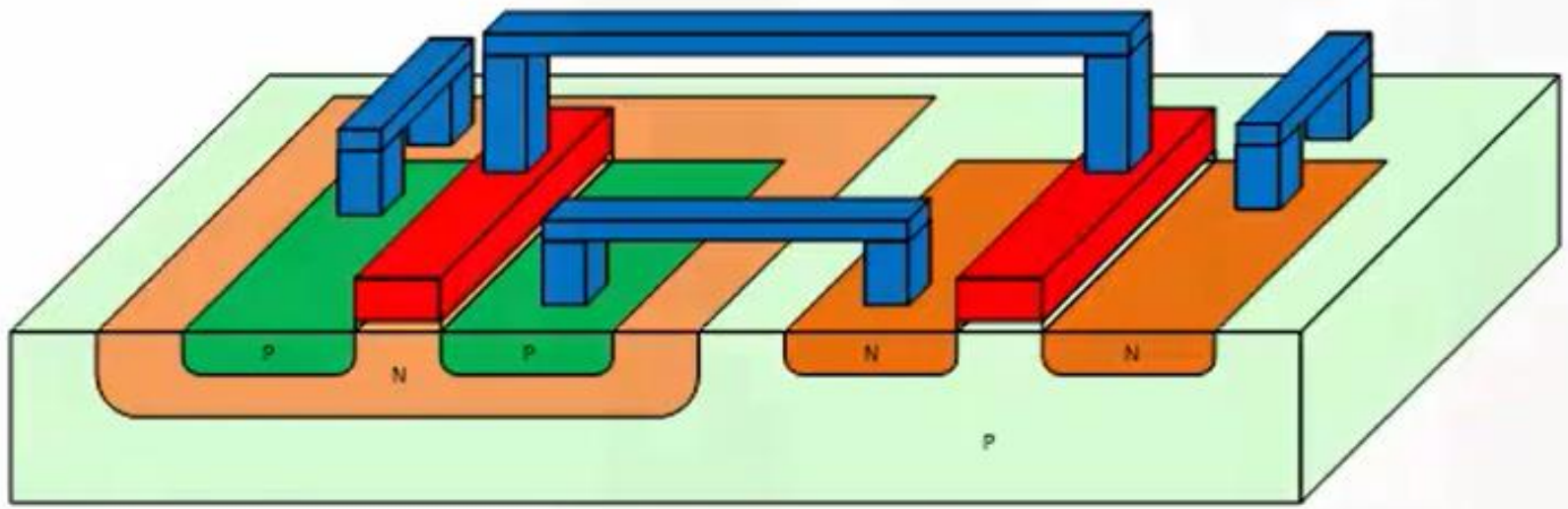
- **Stick diagrams convey layer information**
- **Interface b/w ckt & layout**
- **Size of transistor, width of layers, wire length etc.., are not mentioned**
- **For a chip designer, all CMOS design consists of the following layers**
  - ❖ **substrate or wells of p-type for NMOS & n-type for PMOS**
  - ❖ **diffusion layers, generally called as active area**
  - ❖ **polysilicon layers forms the gate terminal**
  - ❖ **metal & interconnect layers**
  - ❖ **contact & via layers**

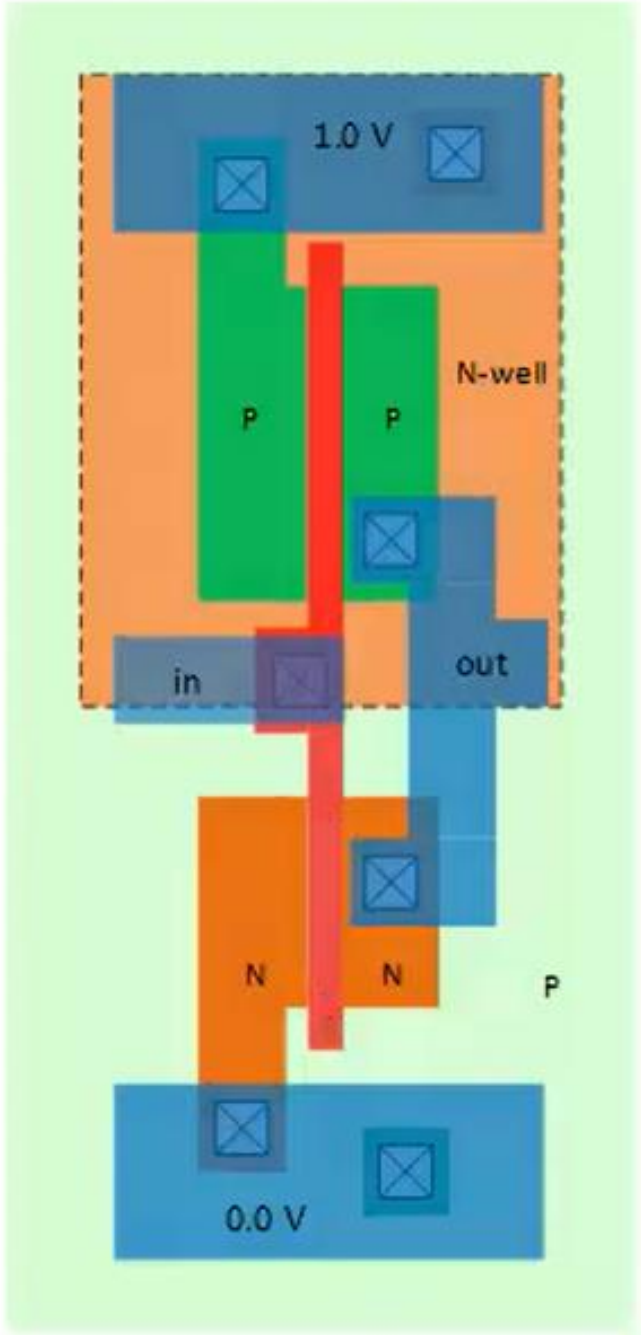
Colour Codes & Patterns

Layers	Colour	Patterns
N diffusion	Green	
P diffusion	Yellow/Brown	
Polysilicon	Red	
Metal 1	Blue	
Metal 2	Magenta	
Contact & Taps	Black	

V_{DD} and V_{ss} - metal layers - Blue

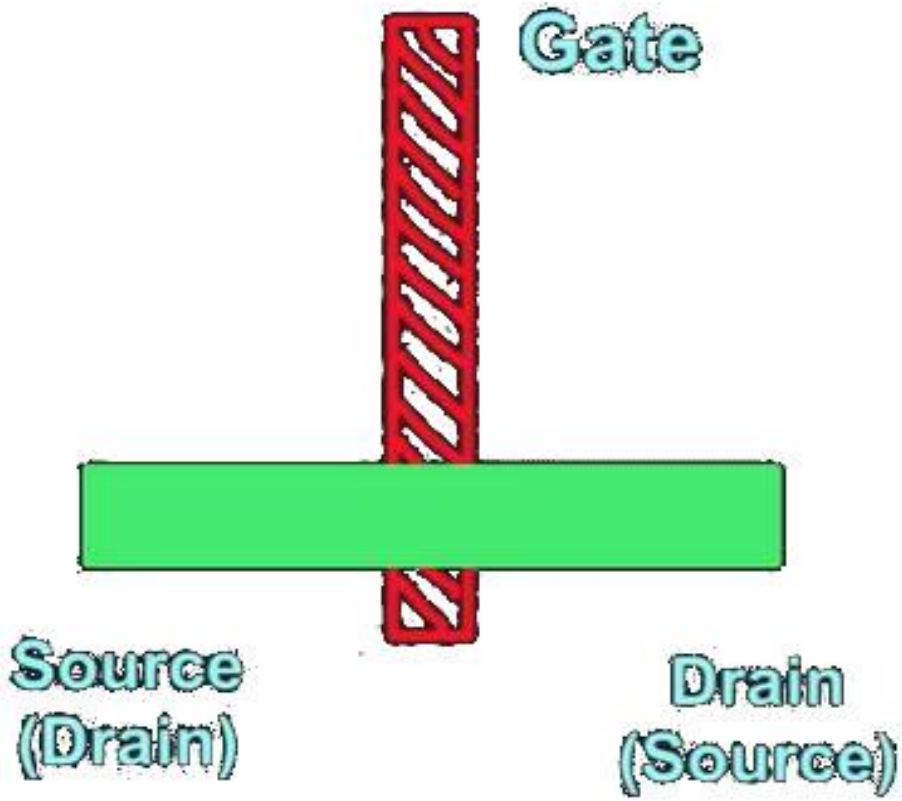
CMOS Technology: Layout



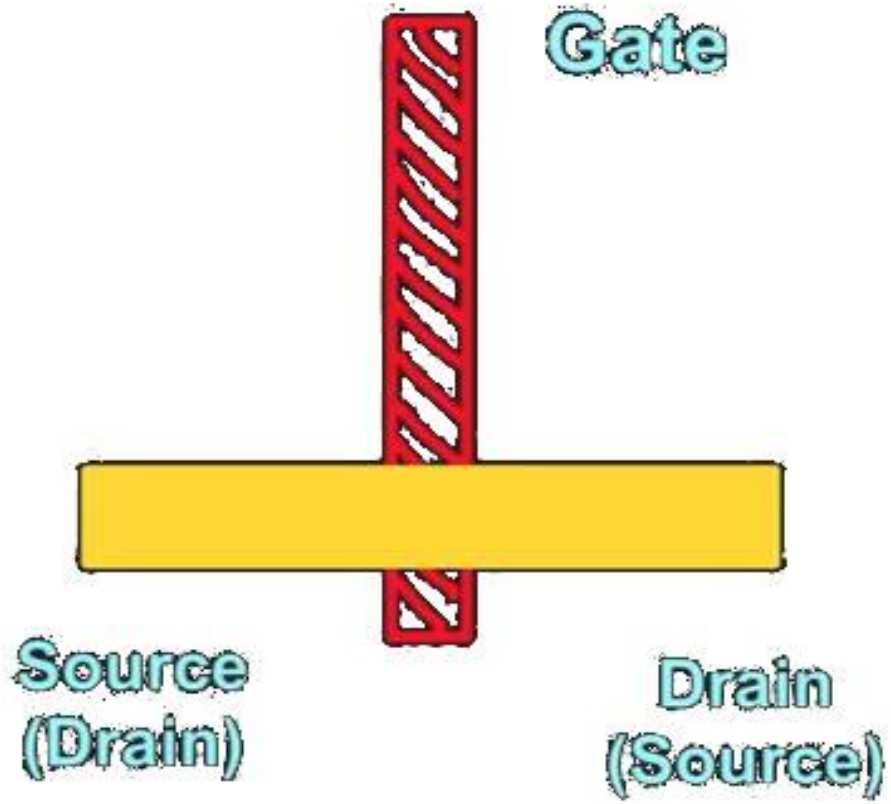


Transistors using Colour Code

NMOS Transistor



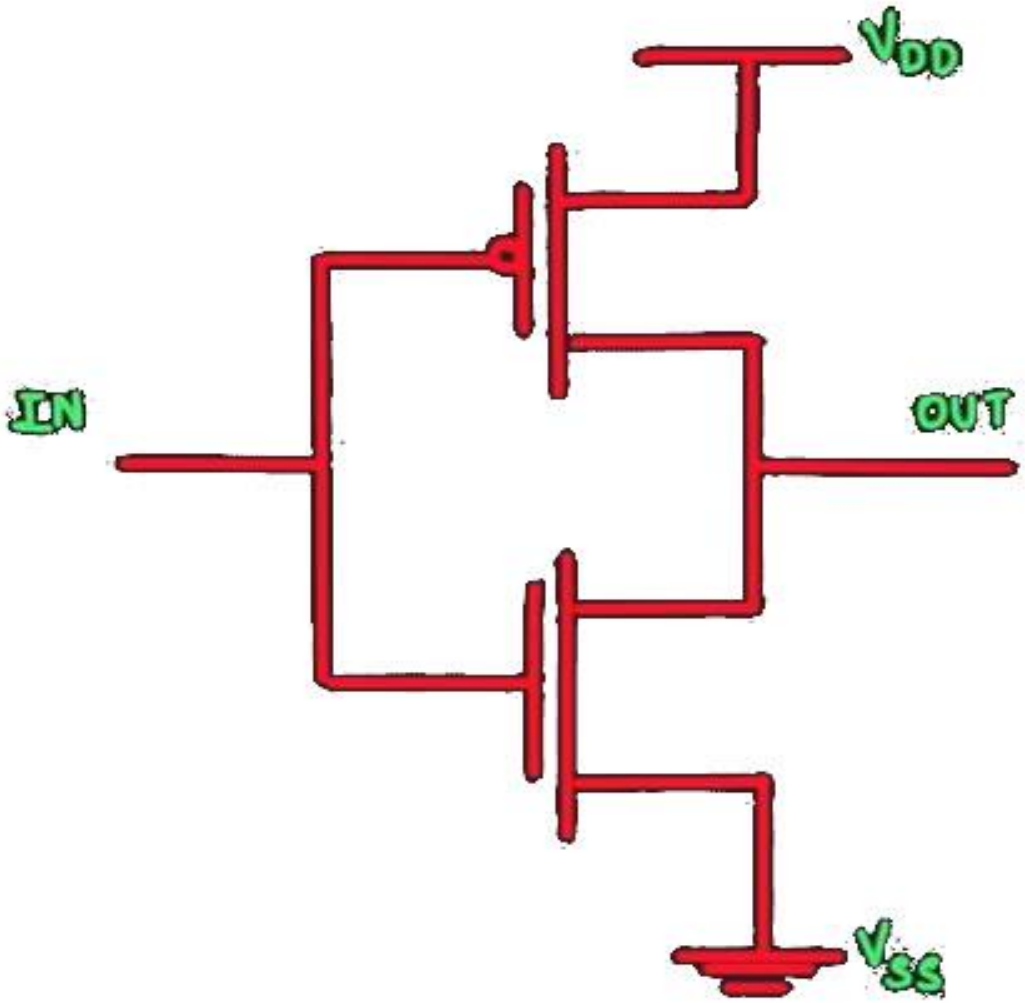
PMOS Transistor

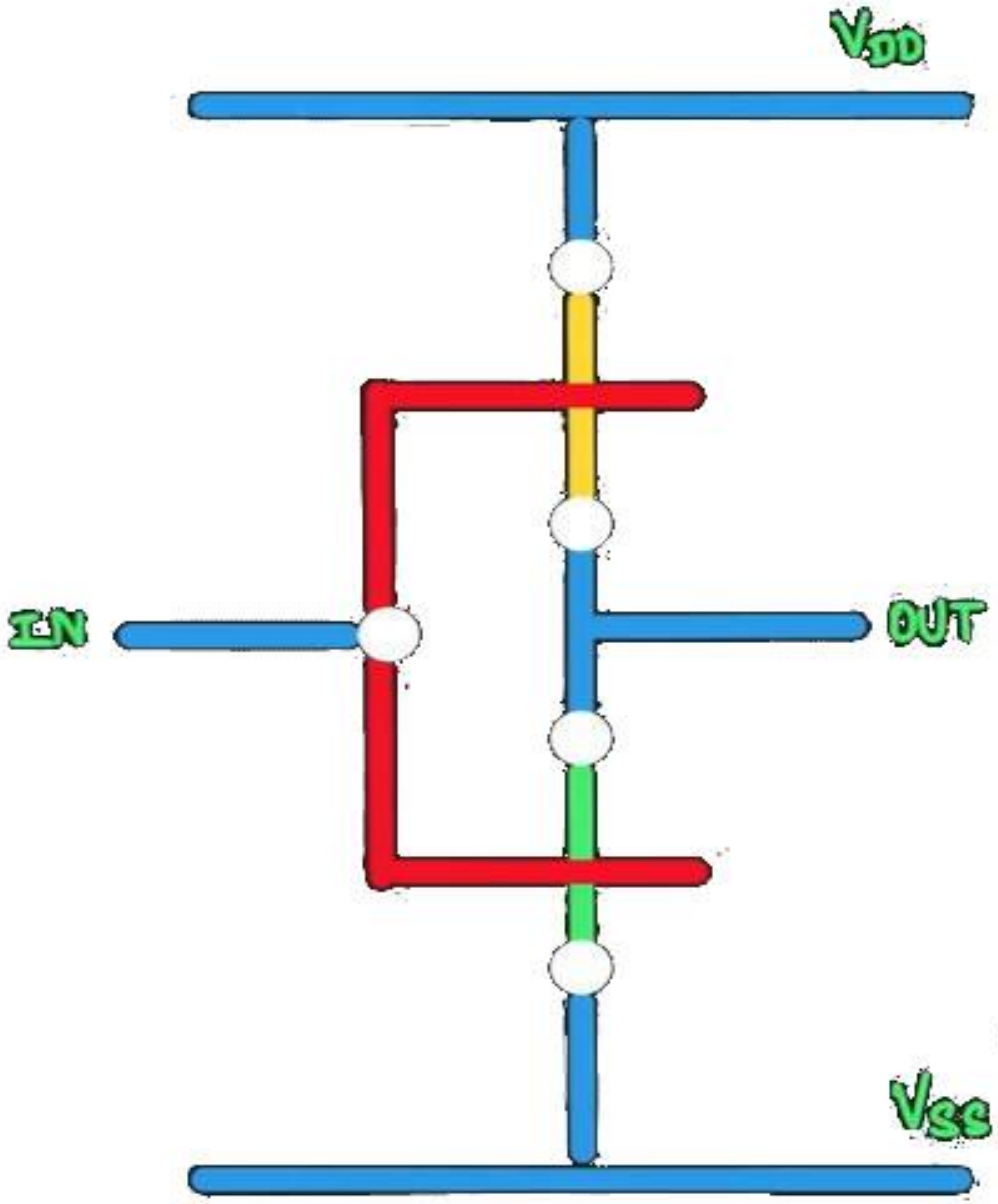


STICK Diagram STEP by STEP Procedure

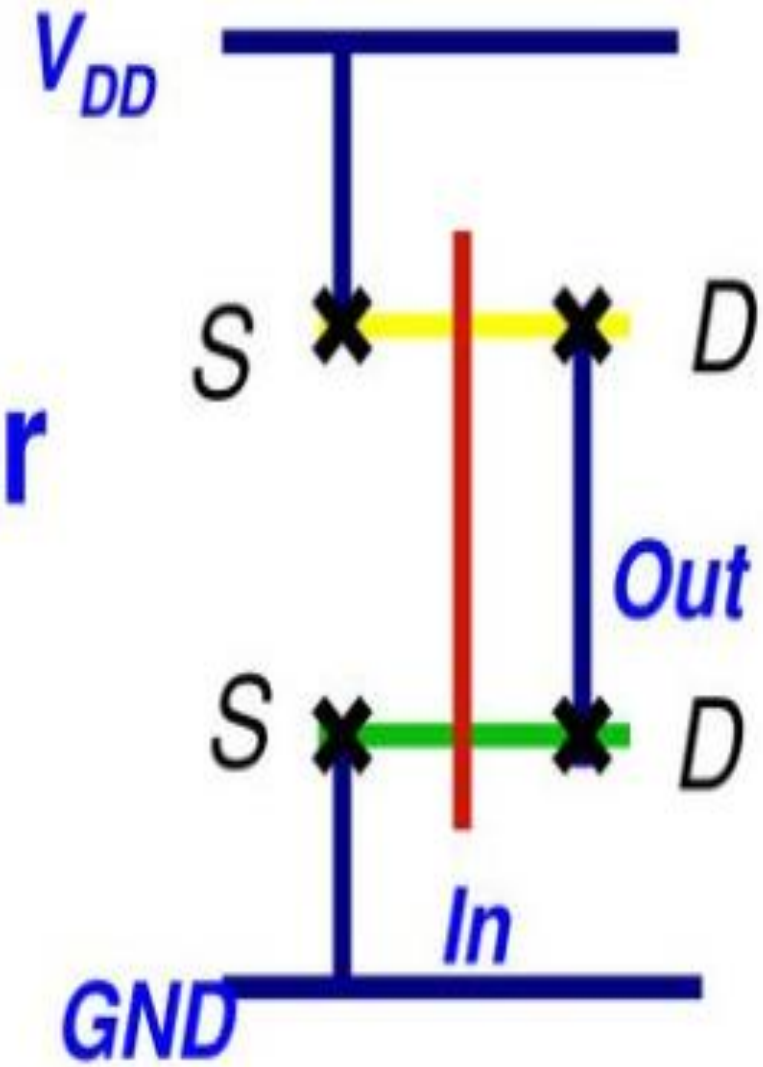
- Draw VDD & VSS rail with sufficient space as per ckt
- Draw PMOS & NMOS diffusion layers
- Form the NMOS & PMOS transistors by placing poly layer
- Connect the terminals of NMOS & PMOS using appropriate layers.
- Connect Source of PMOS to VDD & NMOS to VSS using a metal
- For inputs & outputs use metal layers
- Place a contact cut at points where two different layers are connected

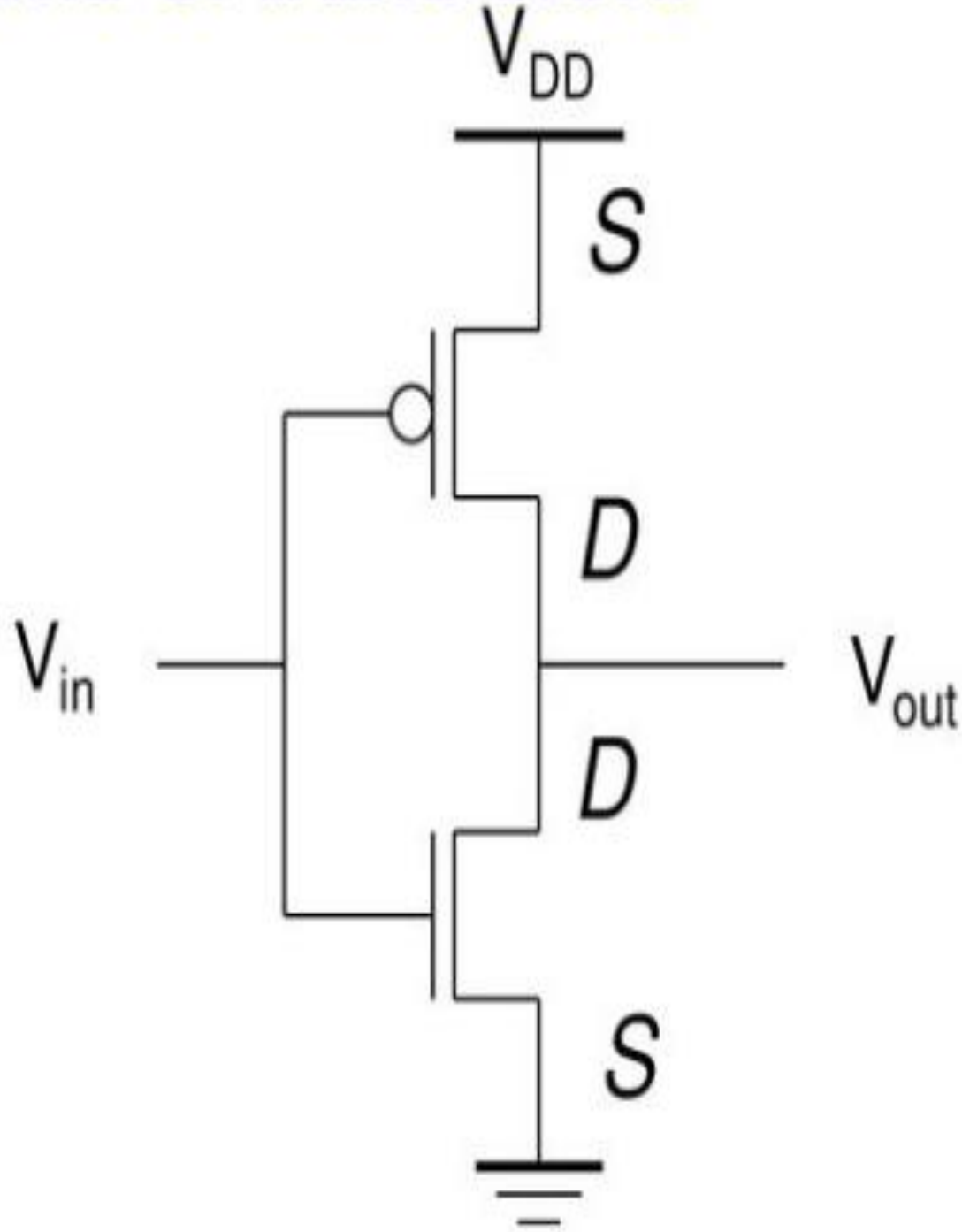
Example - CMOS Inverter



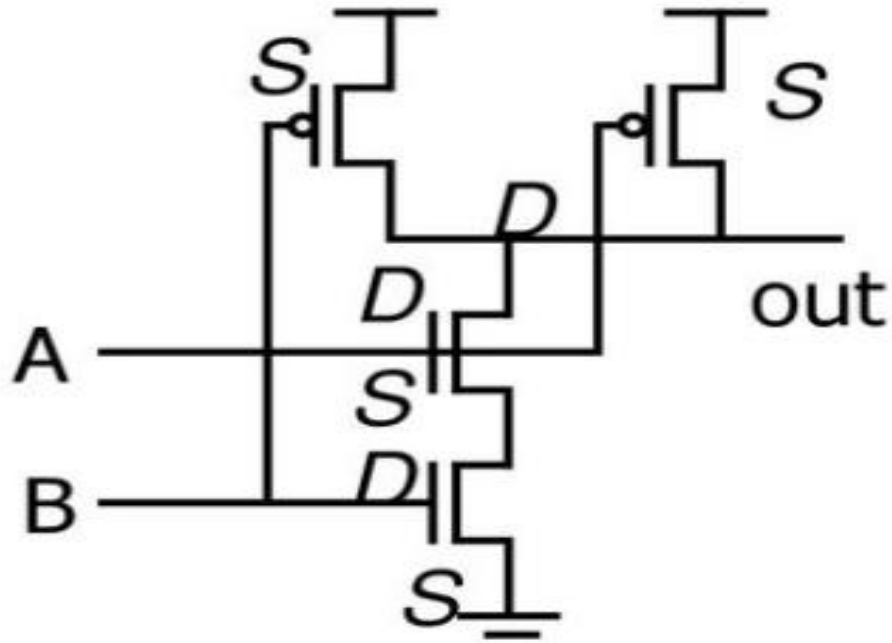


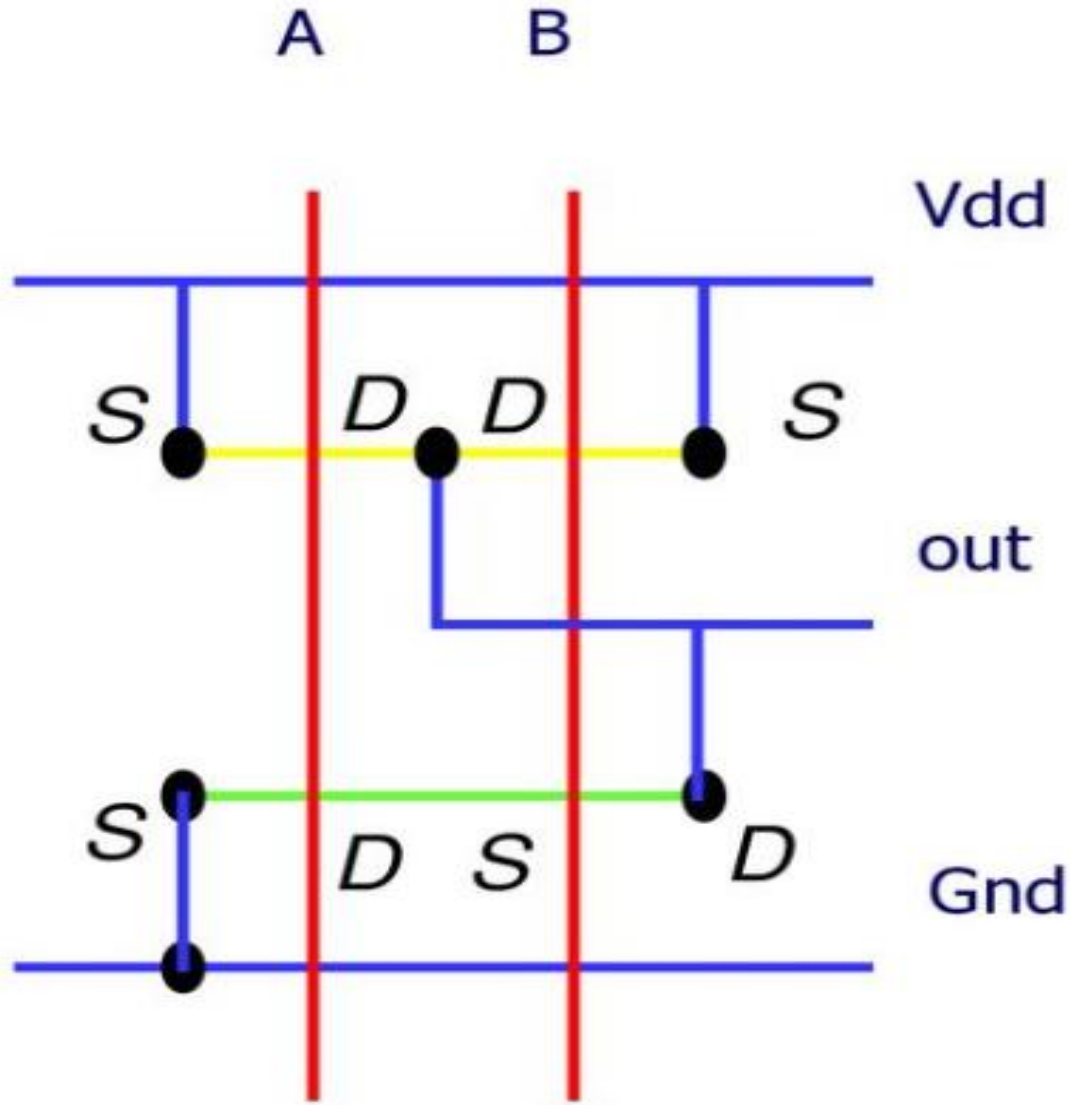
Inverter



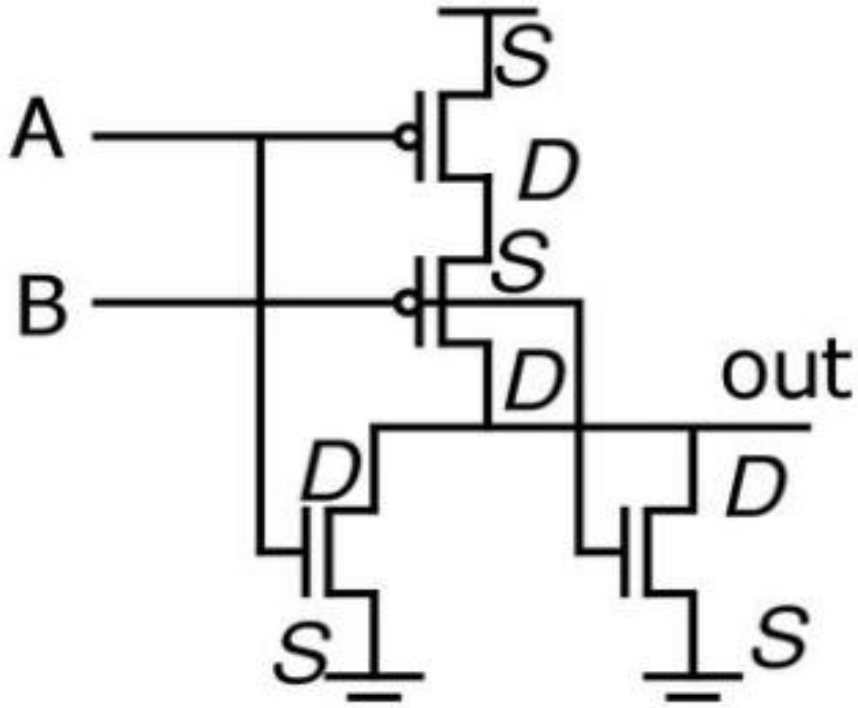


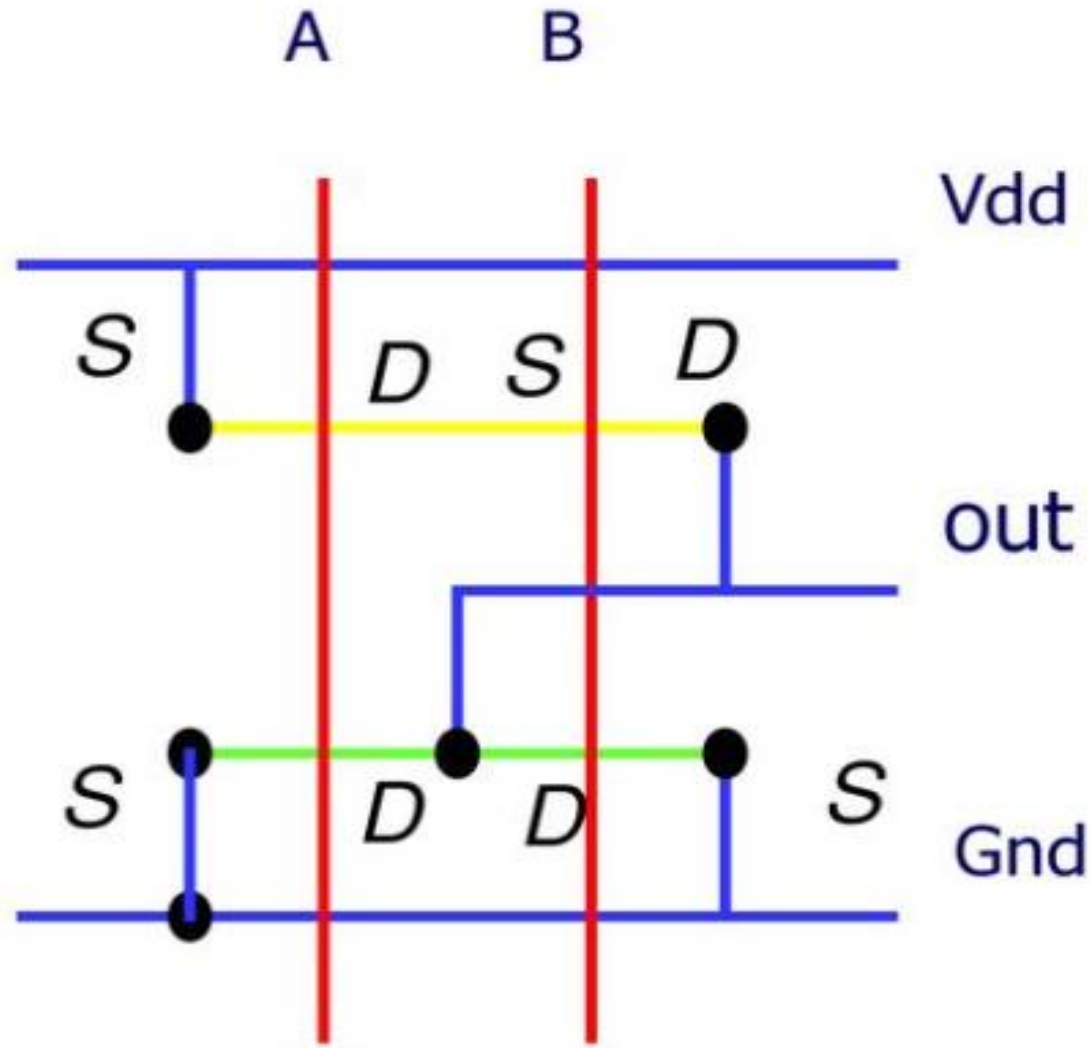
CMOS NAND



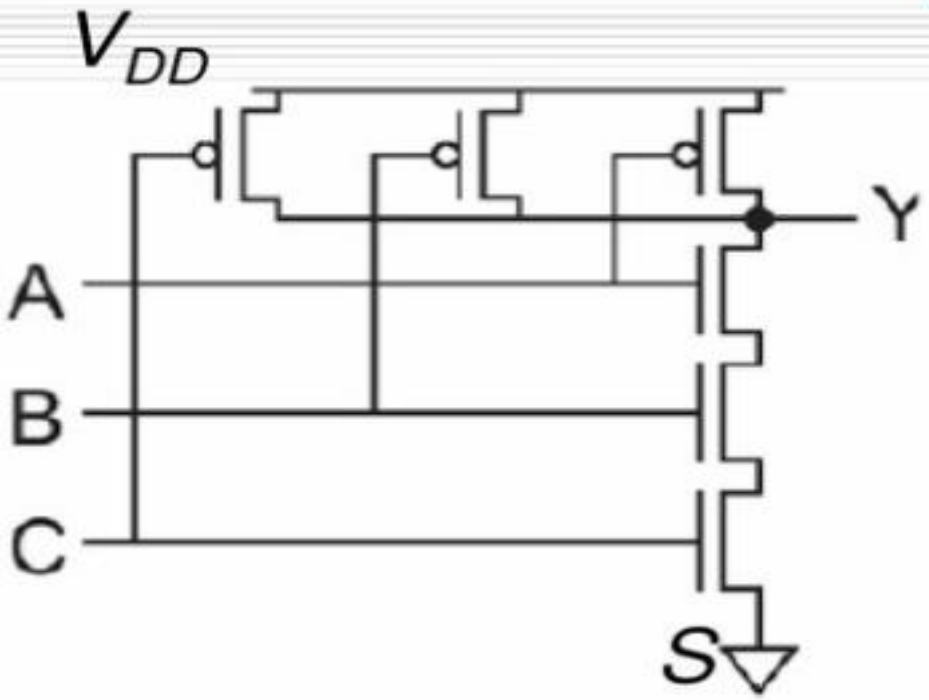


Stick Diagram for CMOS NOR



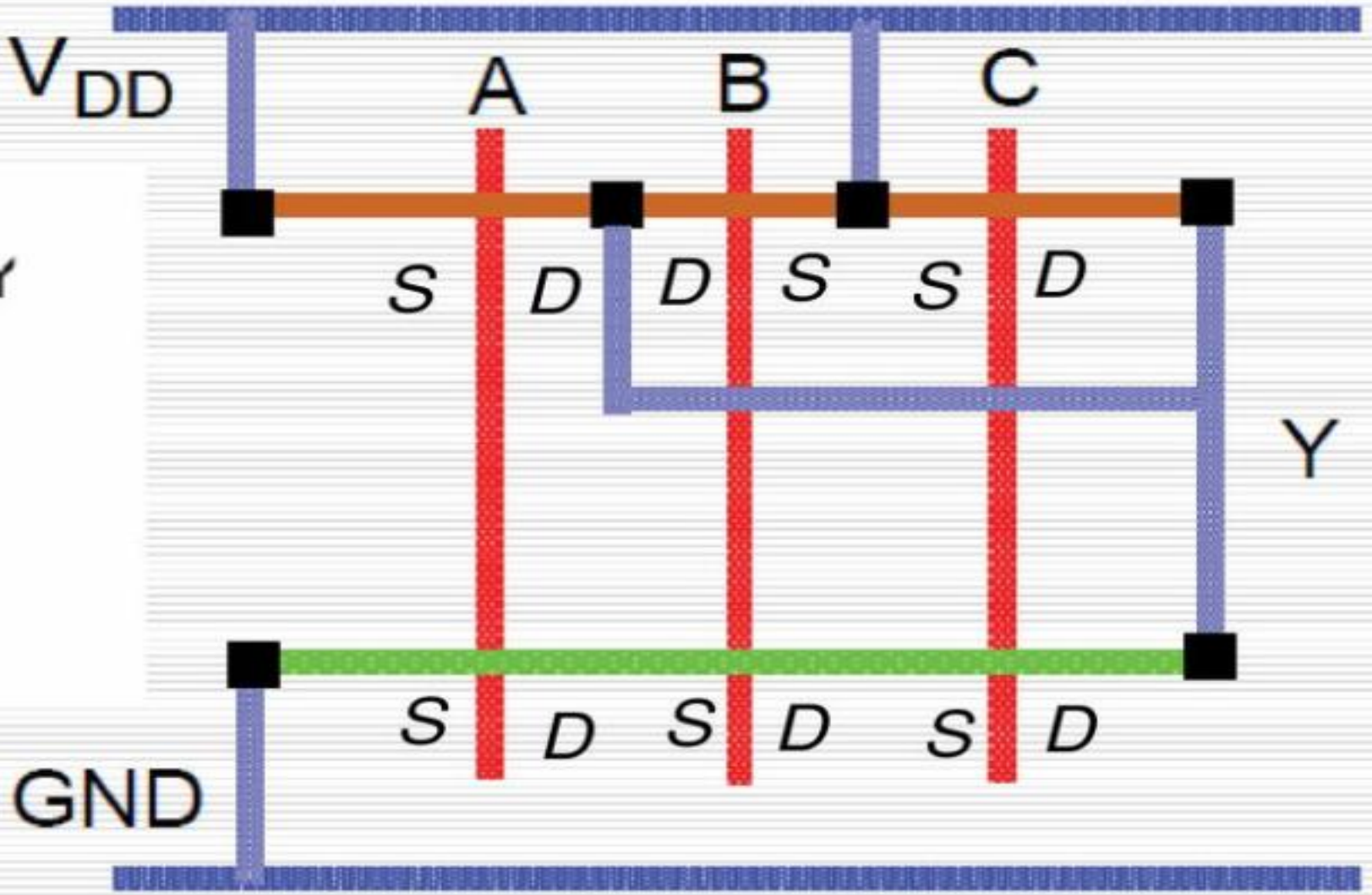


NAND3 Stick Diagram



3-input NAND gate schematic

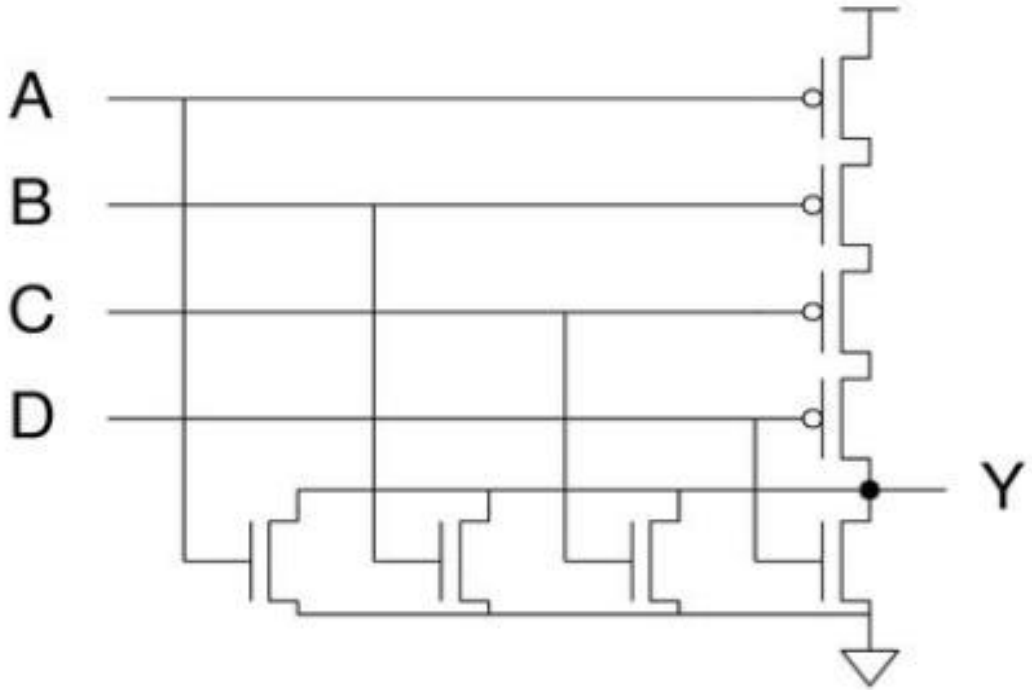
$$Y = \overline{A \bullet B \bullet C}$$

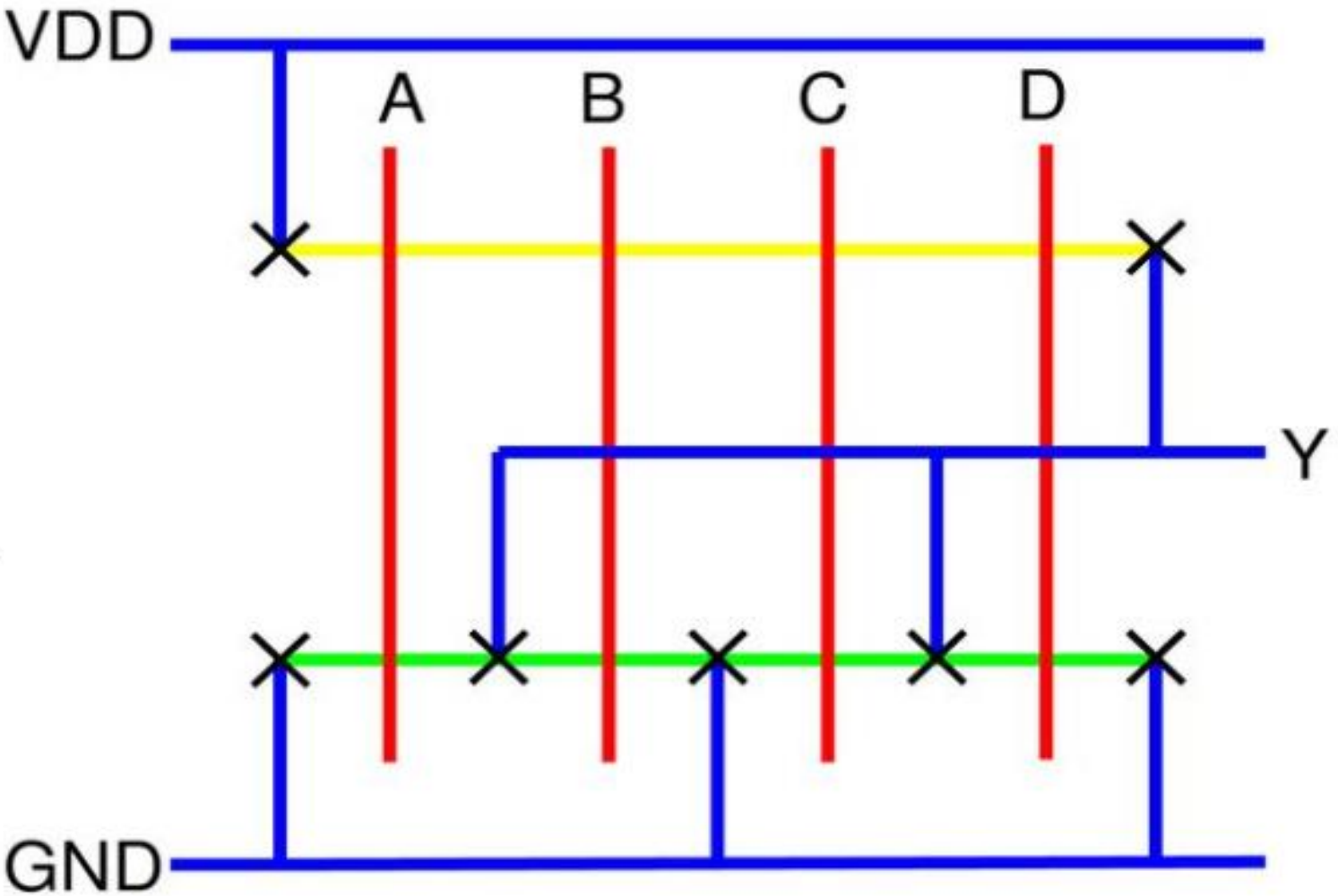


Stick diagram of NAND3

4-input NOR gate

$$Y=\overline{A+B+C+D}$$





EULER GRAPH BASED STICK DIAGRAM

Construction of Logic Graph - Euler's Method

- Convert CMOS circuit into graph
  - Vertices - Source / Drain connections
  - Edges - Transistor Gates
- Two graphs will result:
  - Pull - Up Network (PUN)
  - Pull - Down Network (PDN)

EULER GRAPH BASED STICK DIAGRAM

Euler Path

"Traverses each branch of the graph EXACTLY ONCE"

- ✅ Find a Euler path in both pull-up & pull-down tree graphs with IDENTICAL REORDERING OF INPUTS.
- ✅ By reordering the input gates, we can obtain an optimum layout of the given CMOS gate.

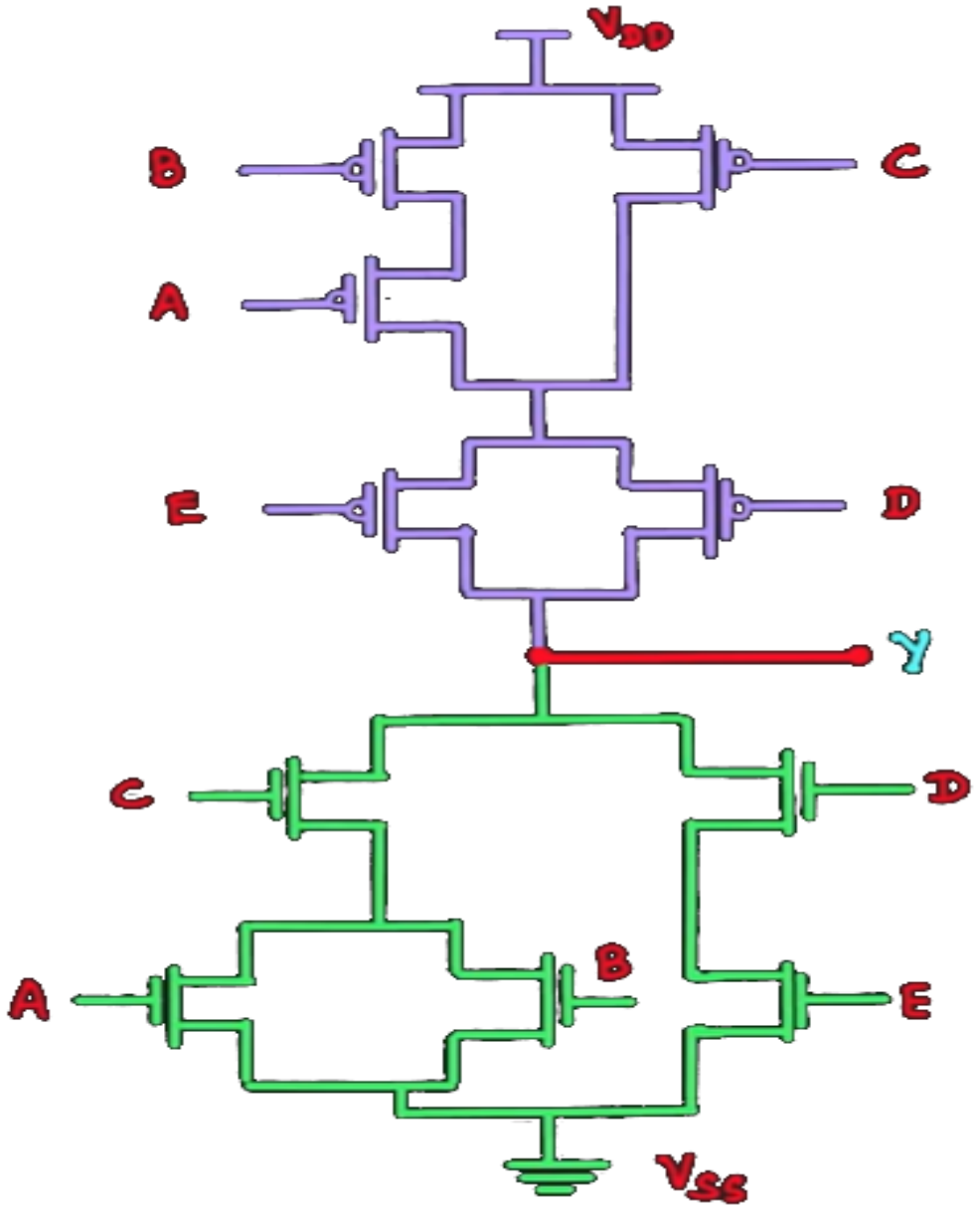
EULER GRAPH BASED STICK DIAGRAM

Stick Diagram: $\overline{Y = [(A + B).C + DE]}$

Step I: Draw the schematic of the given Boolean logic.

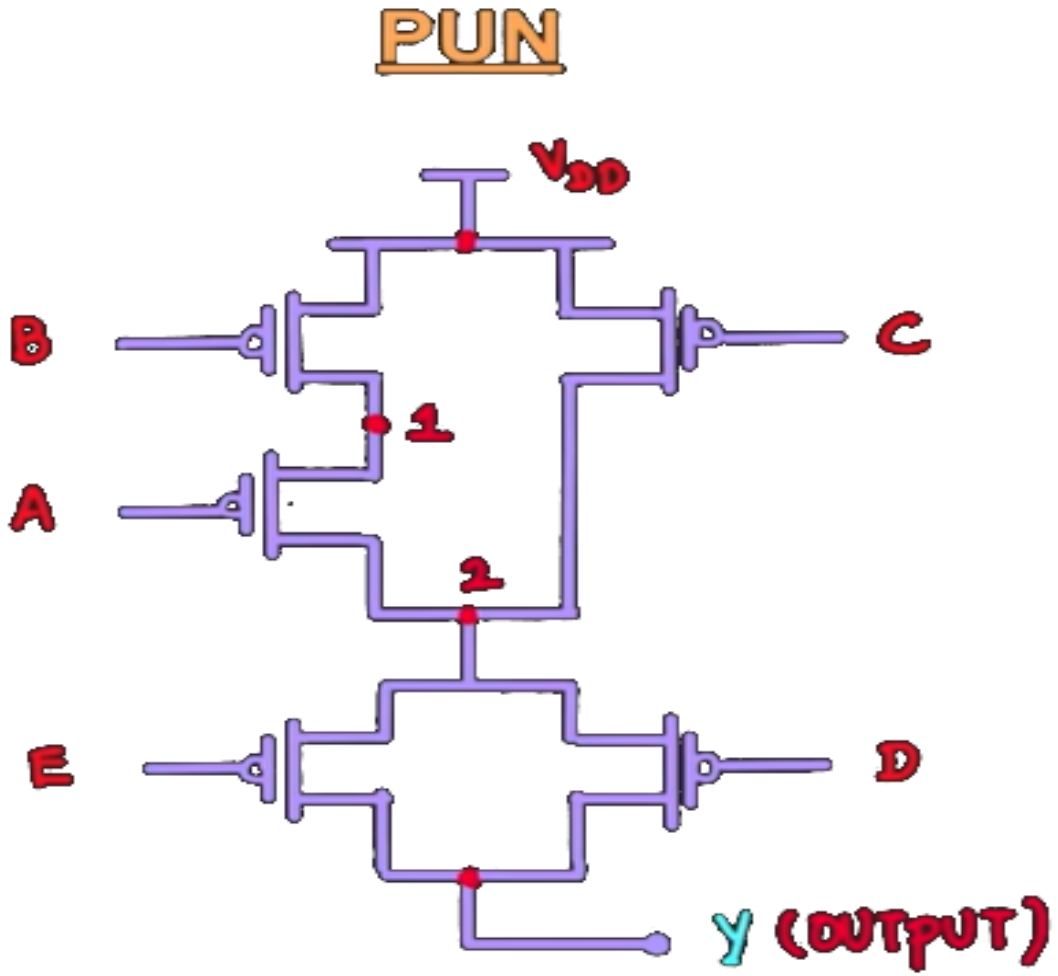
For PUN : $Y = (A.B) + C . (D + E)$

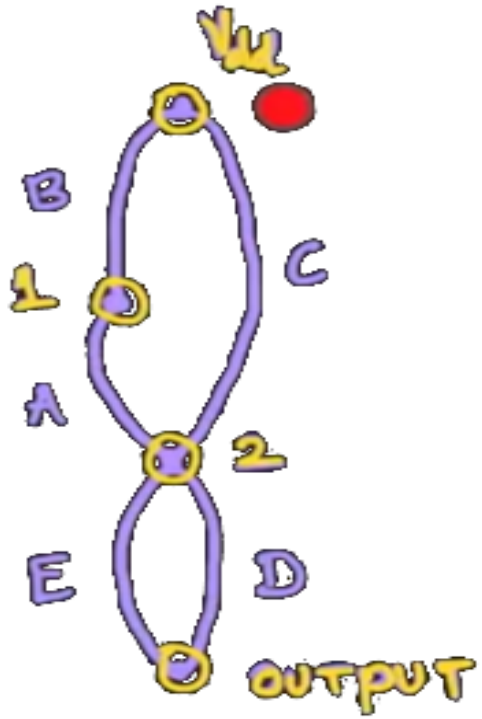
For PDN : $Y = (A + B).C + DE$



EULER GRAPH BASED STICK DIAGRAM

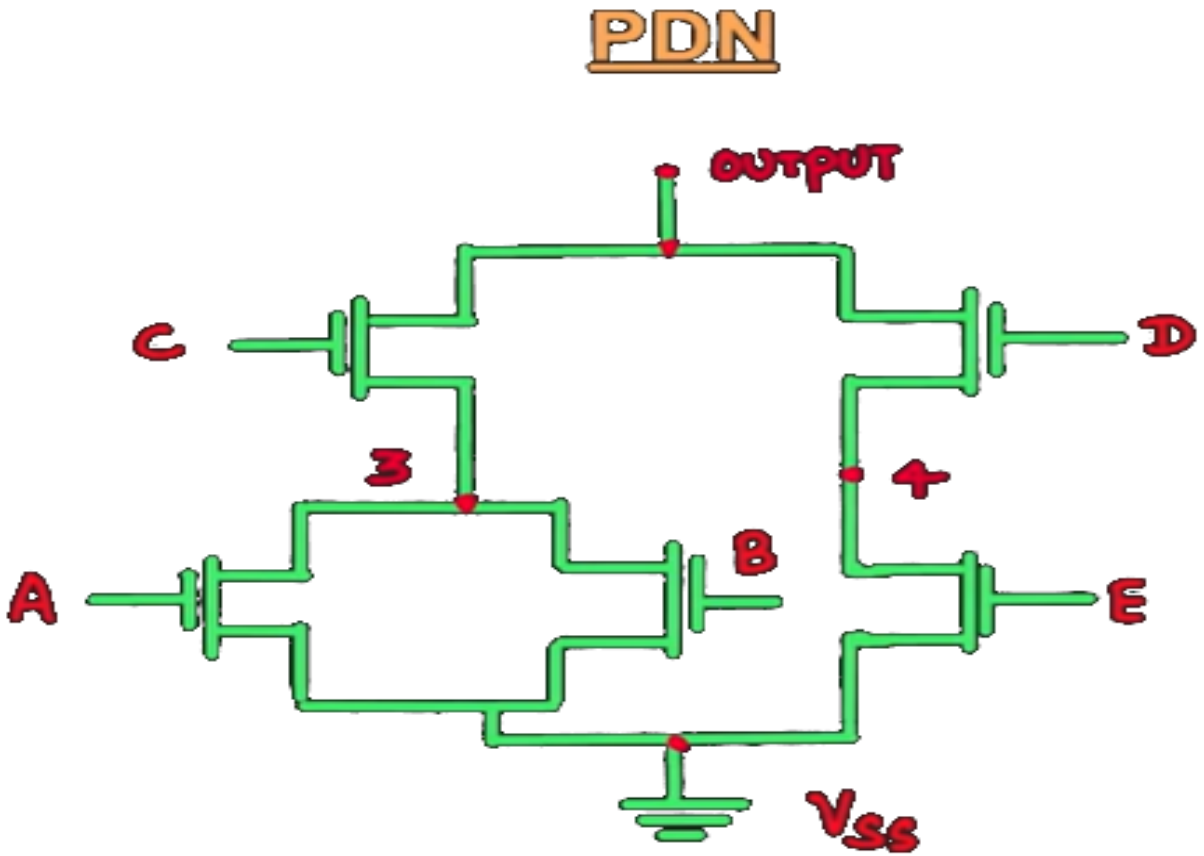
Step II: Draw the Euler Graph.

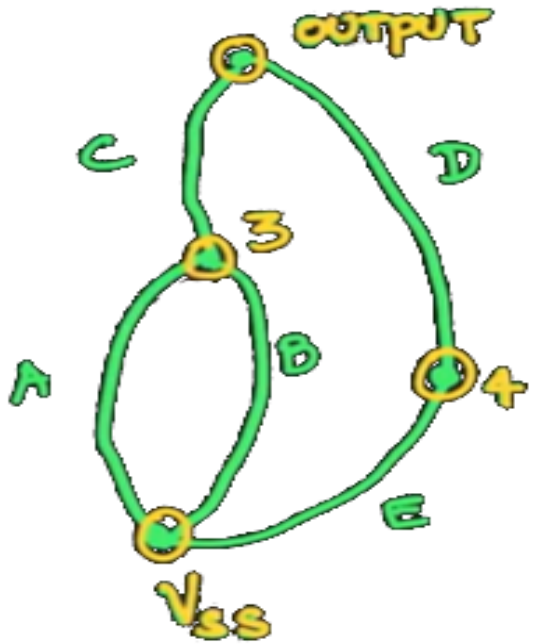




EULER GRAPH BASED STICK DIAGRAM

Step II: Draw the Euler Graph.

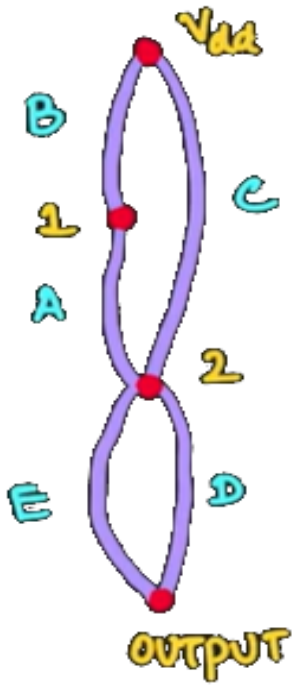




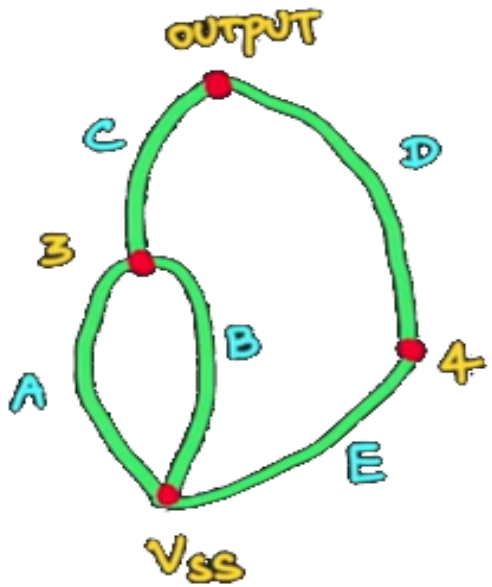
EULER GRAPH BASED STICK DIAGRAM

Step III: Traverse the Euler path.

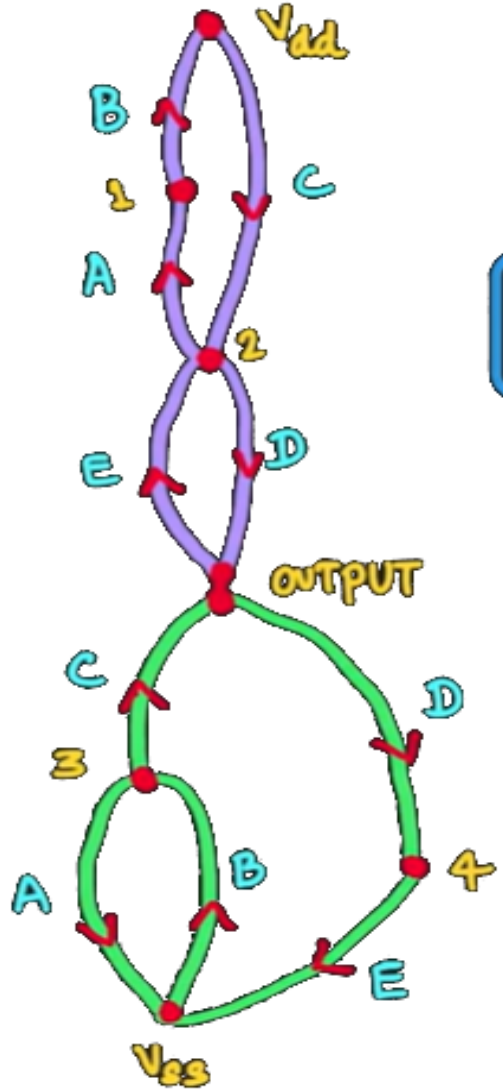
PUN



PDN



Euler Graph



A → B → C → D → E

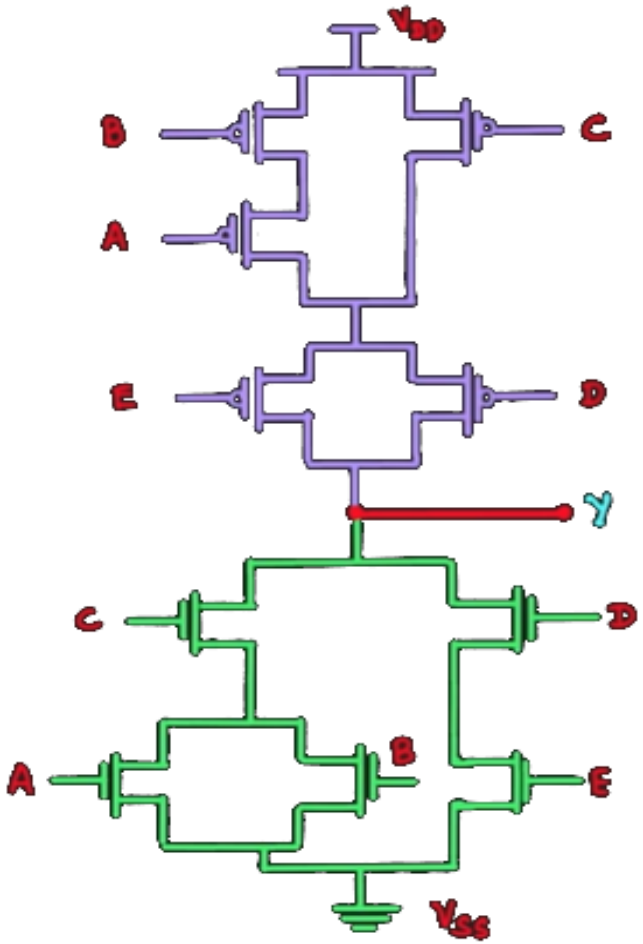
Euler Path

A - B - C - D - E

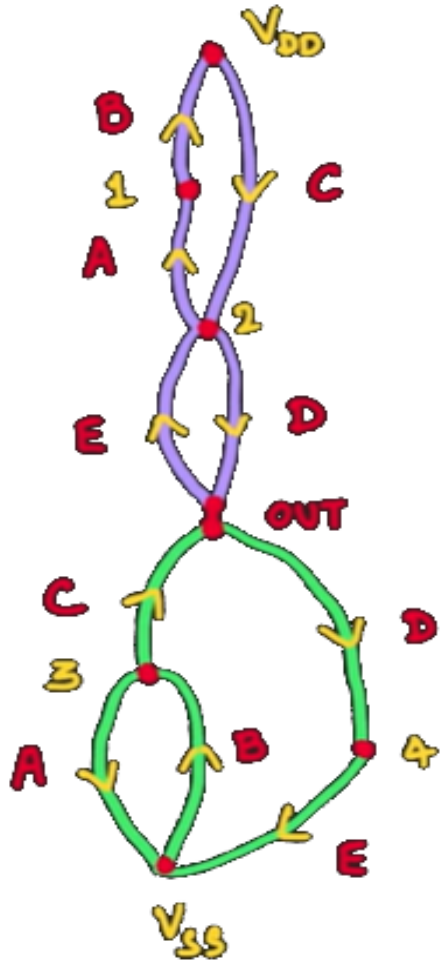
EULER GRAPH BASED STICK DIAGRAM

Stick Diagram: Y = [(A + B).C + DE]

Step I: Schematic



Step II: Euler Graph

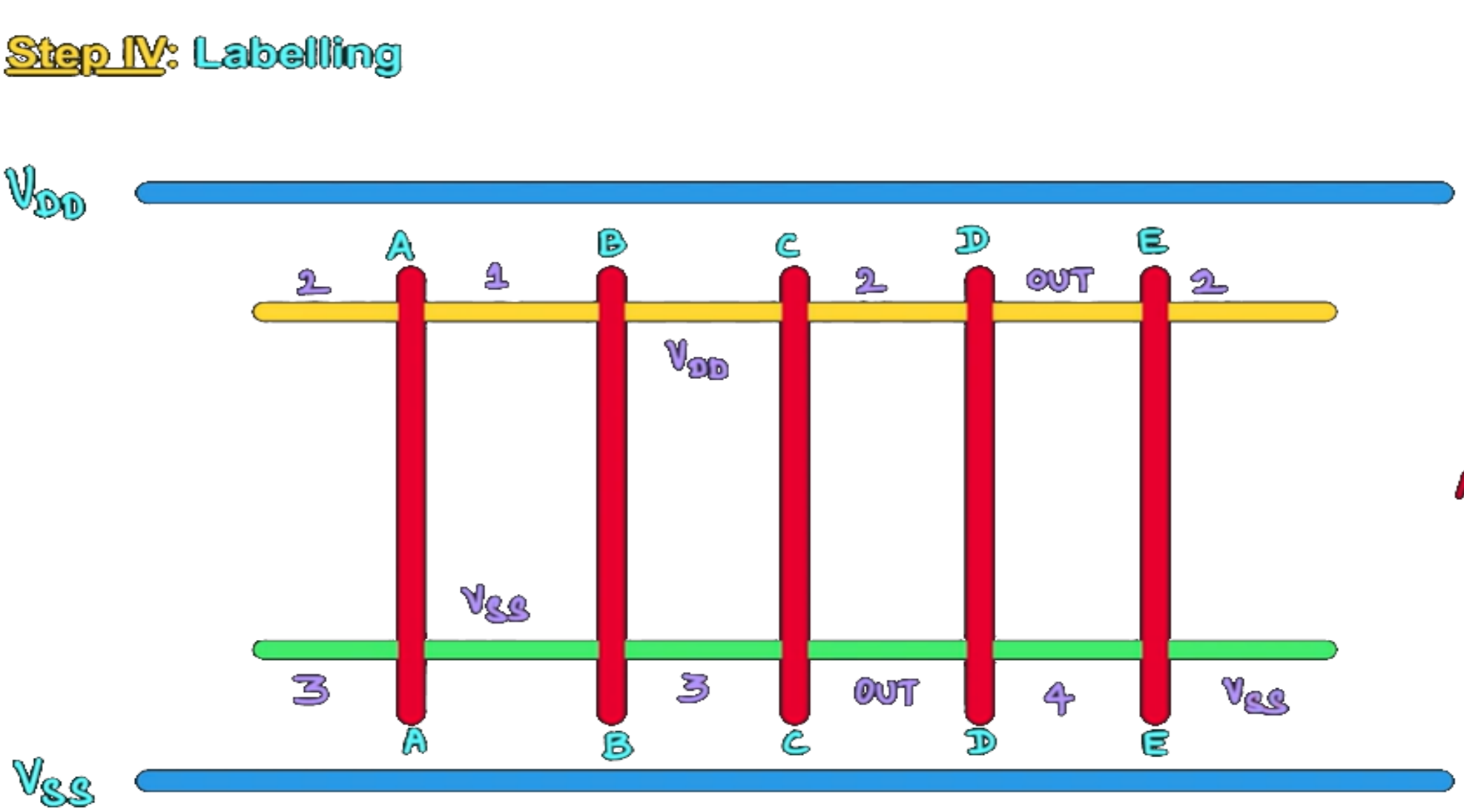


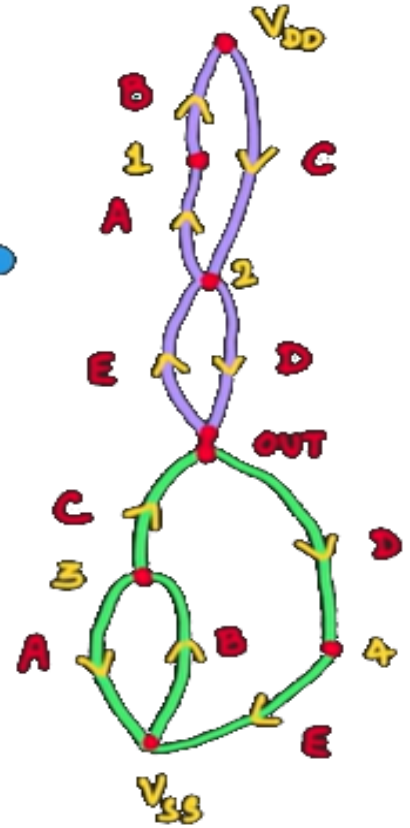
Step III: Euler Path

A - B - C - D - E

EULER GRAPH BASED STICK DIAGRAM

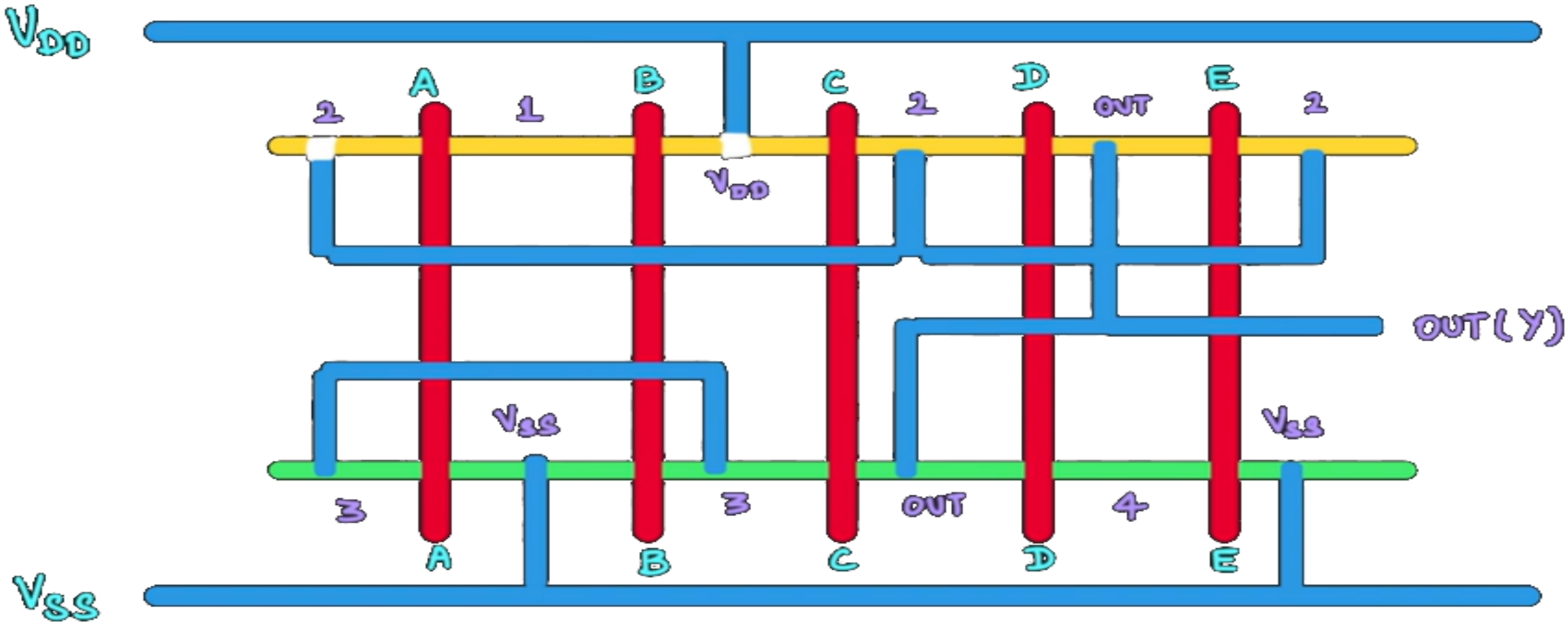
Step IV: Labelling



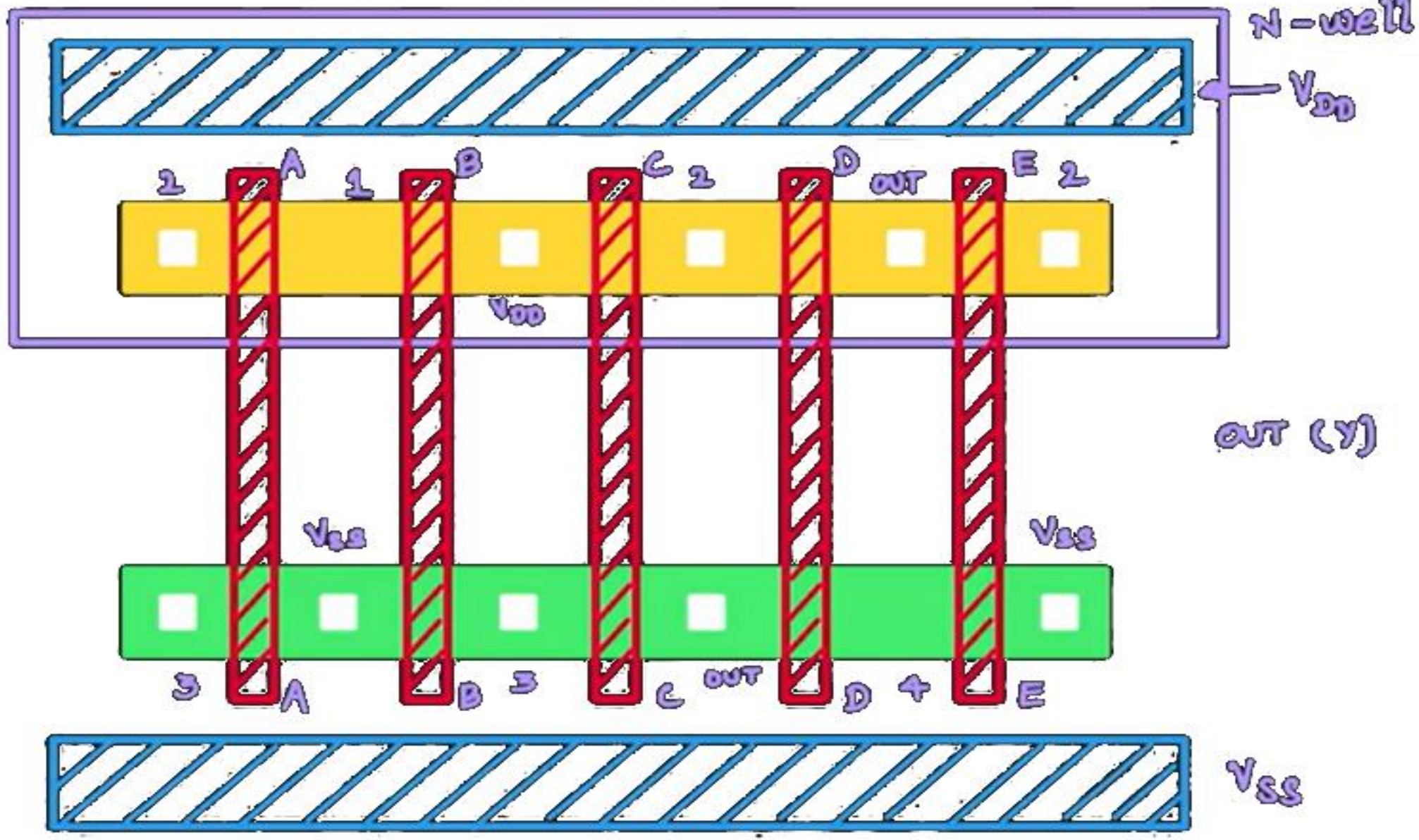


EULER GRAPH BASED STICK DIAGRAM

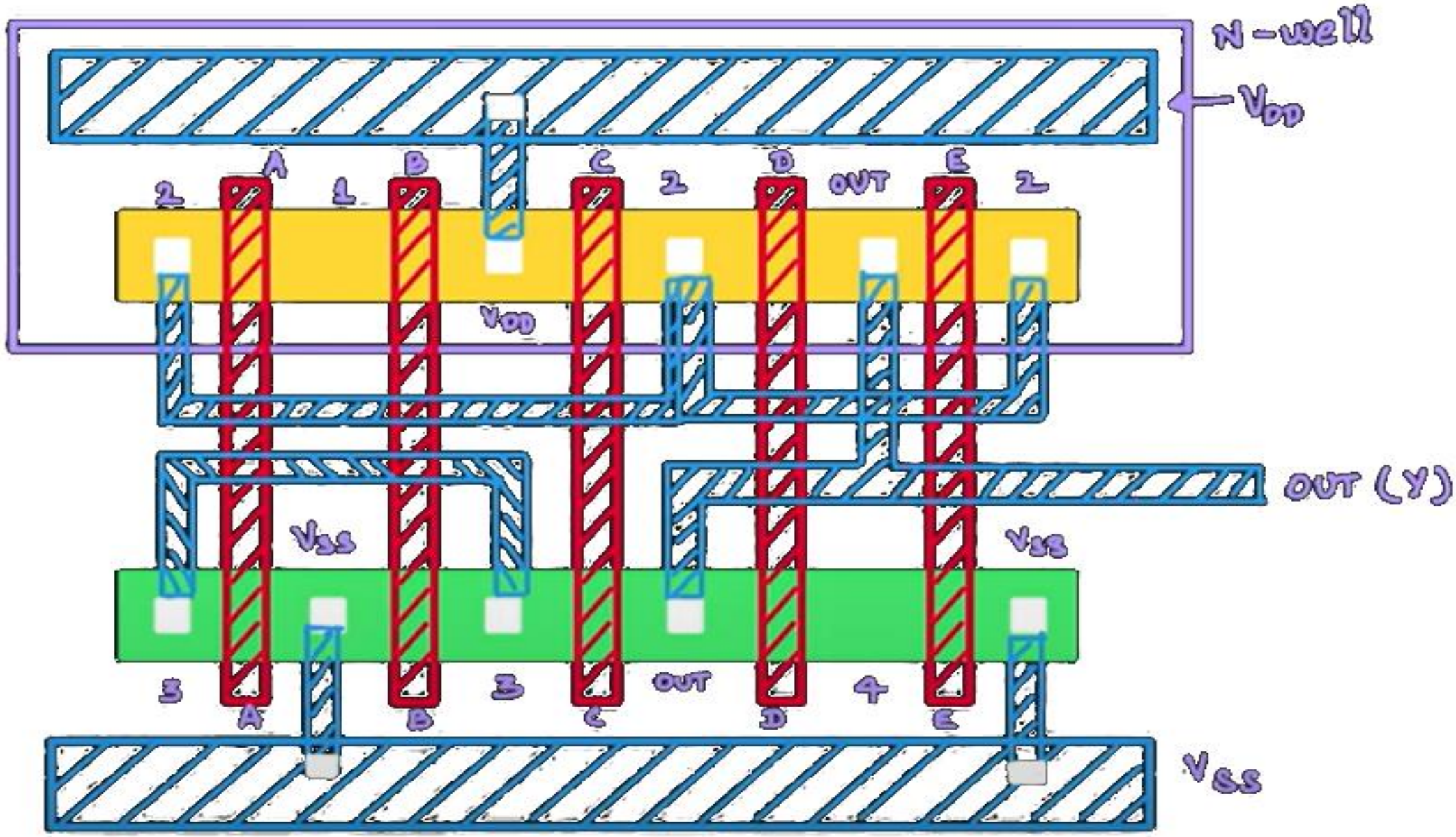
Step V: STICK DIAGRAM



Layout Diagram: $Y = \overline{[(A + B).C + DE]}$



Layout Diagram: $Y = [(A + B).C + DE]$

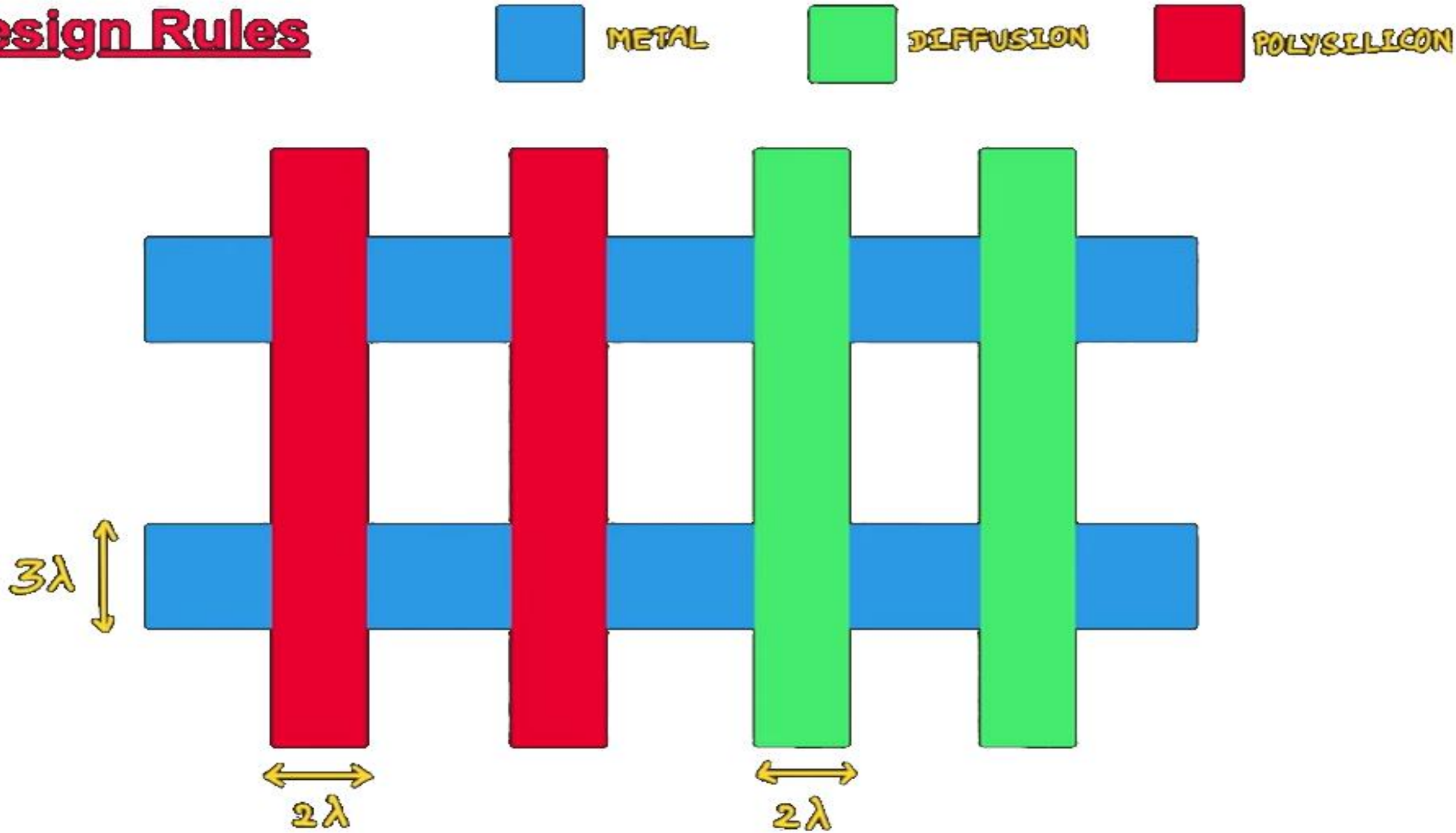


Layout Design Rules

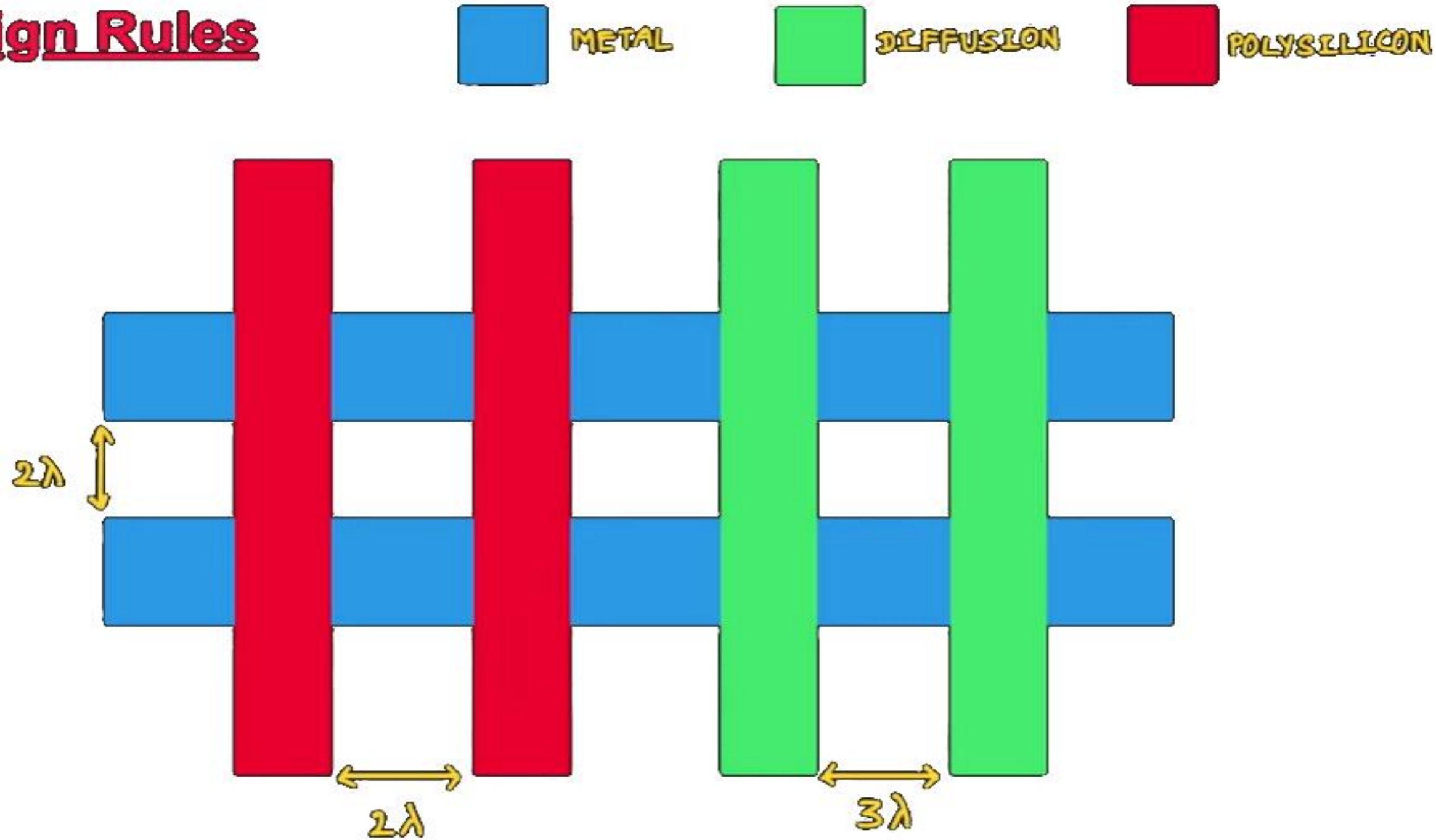
- **Width** - the minimum width of a rectangle
- **Spacing** - the minimum spacing between two rectangles on the same or different layers
- **Overlap** - specifies how much a rectangle must surround another on another layer

$$\lambda = \frac{\text{channel length (L)}}{2}$$

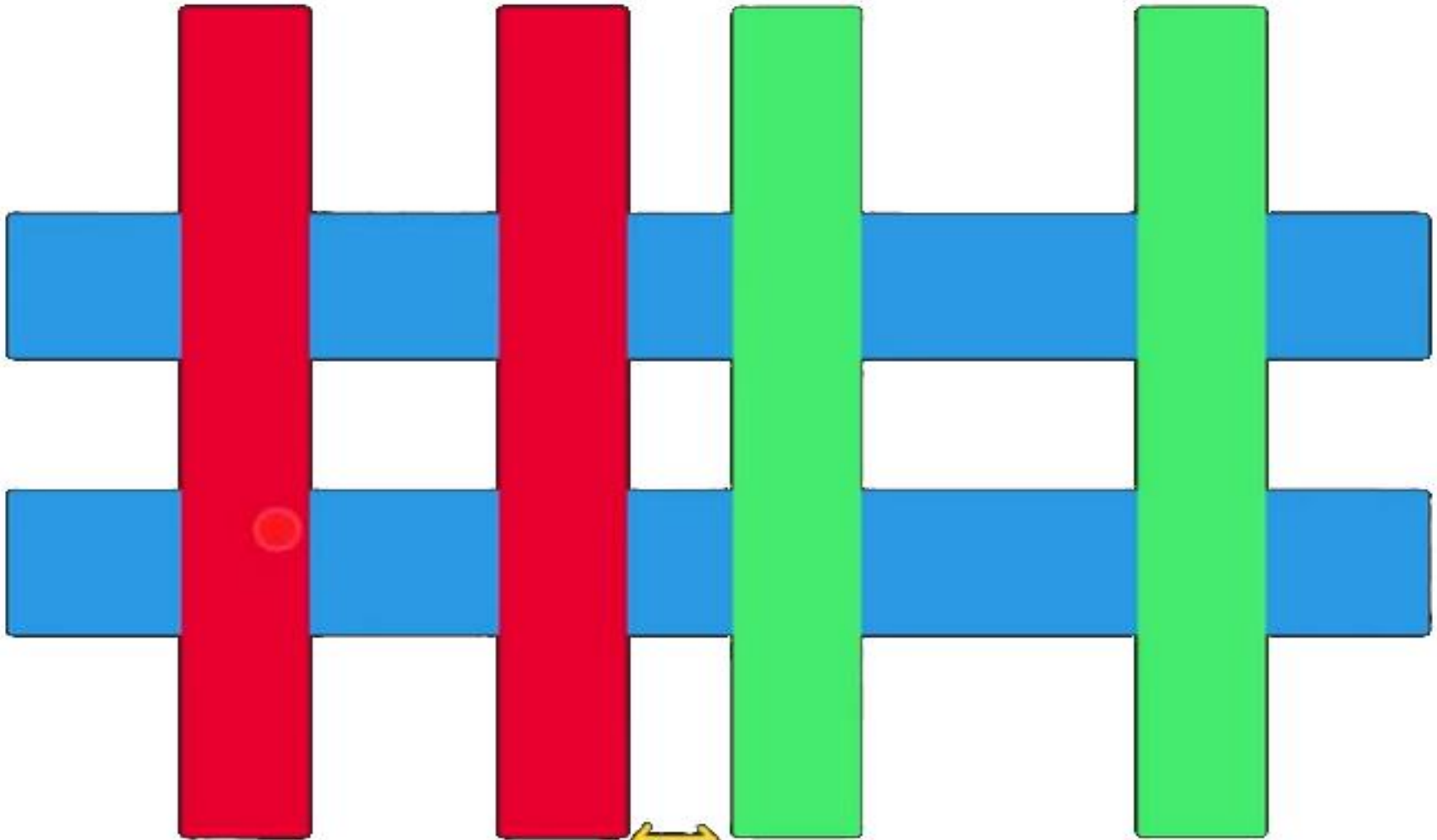
Design Rules



Design Rules



Design Rules

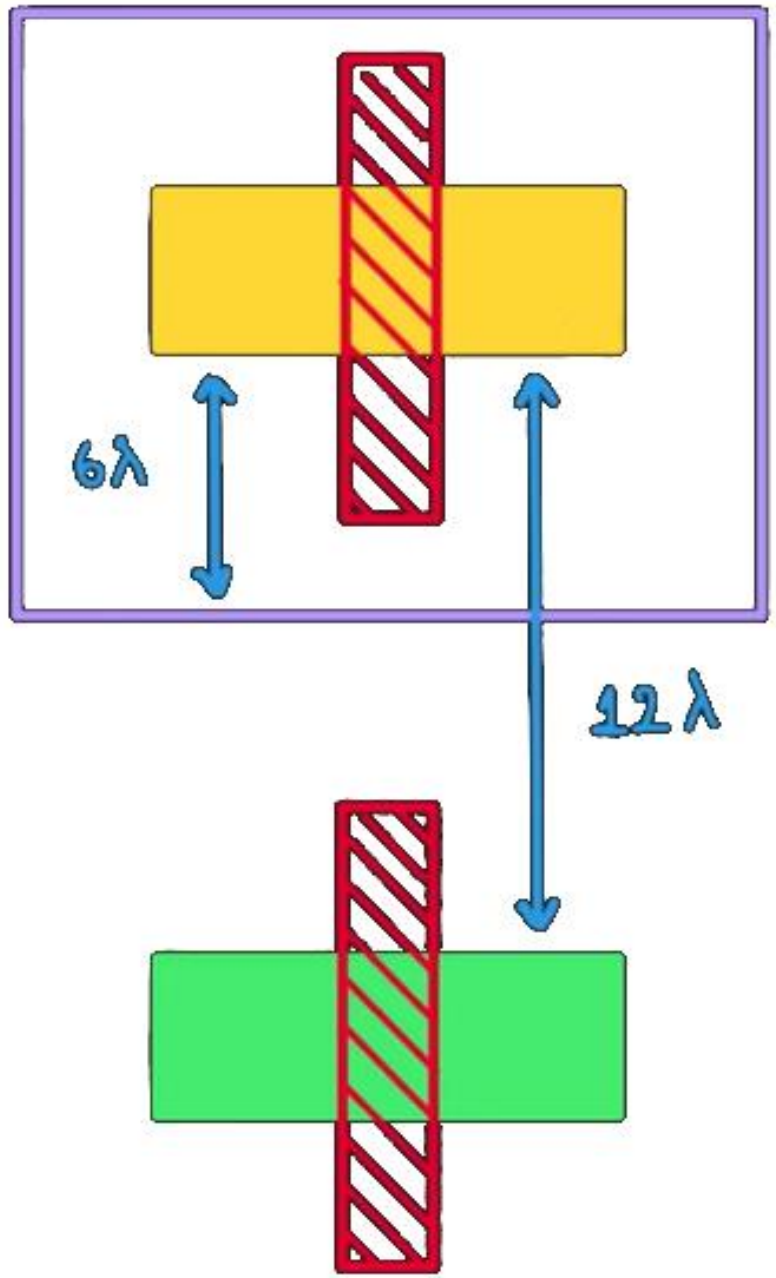


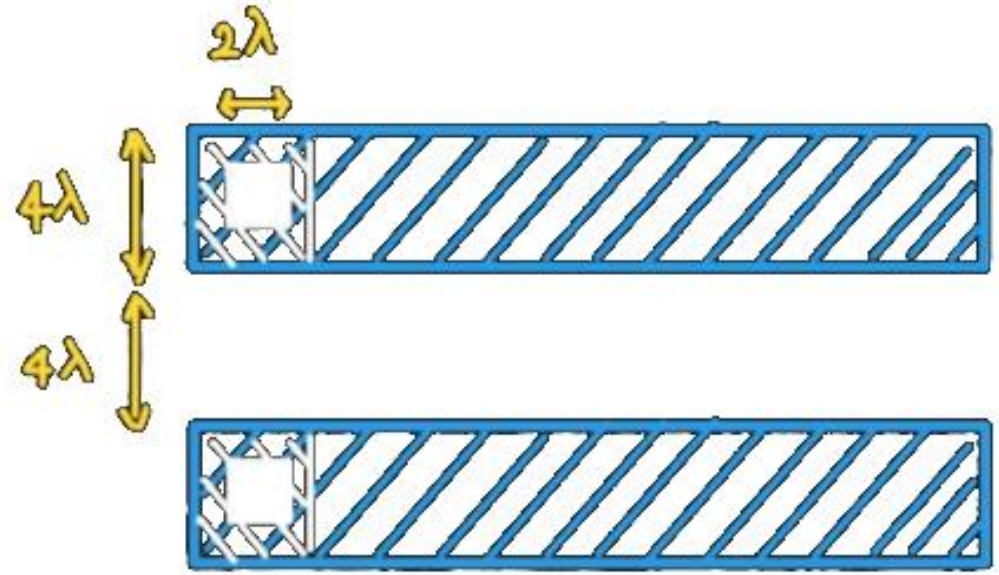
Design Rules

METAL

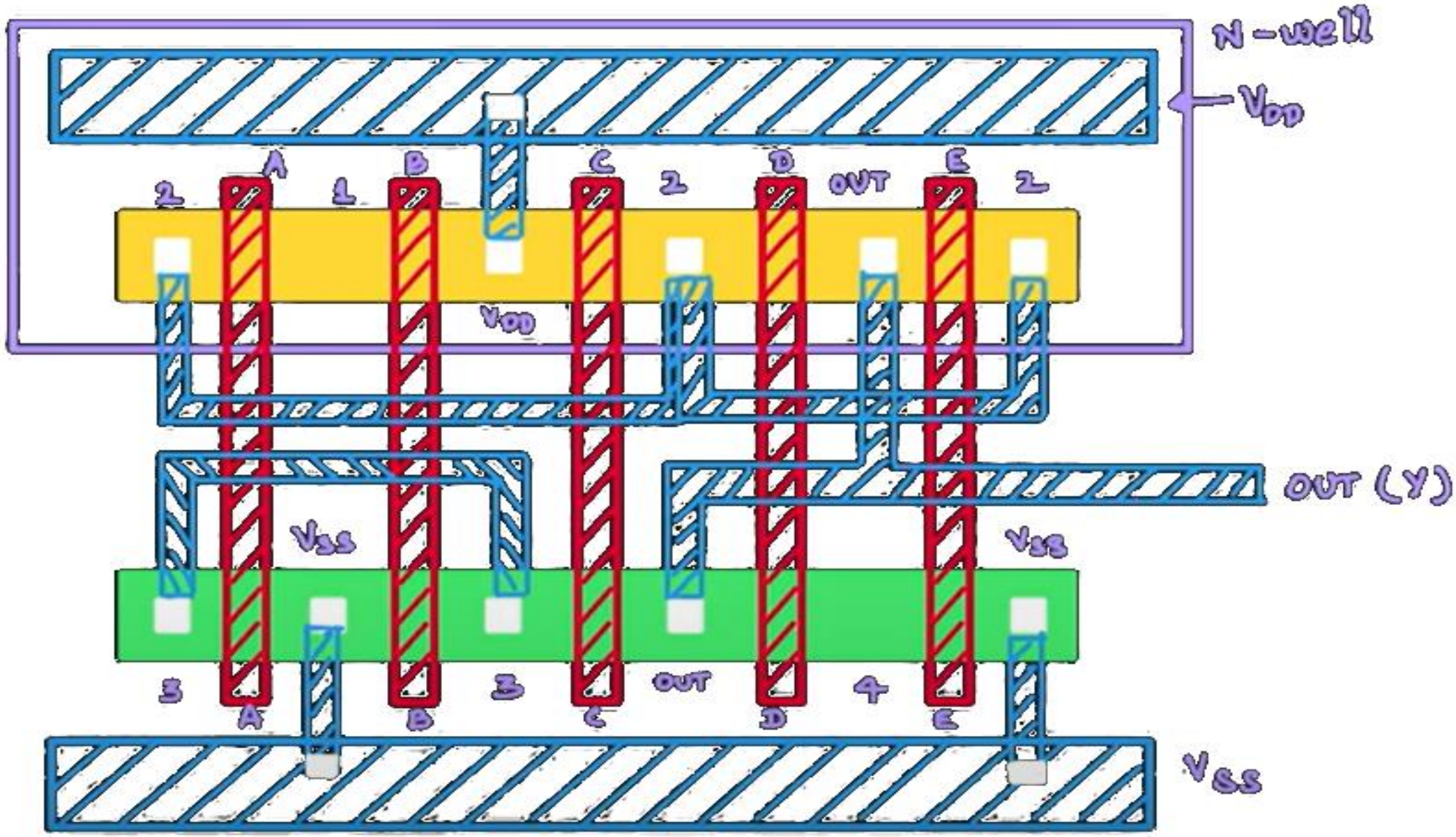
POLYSILICON

Design Rules



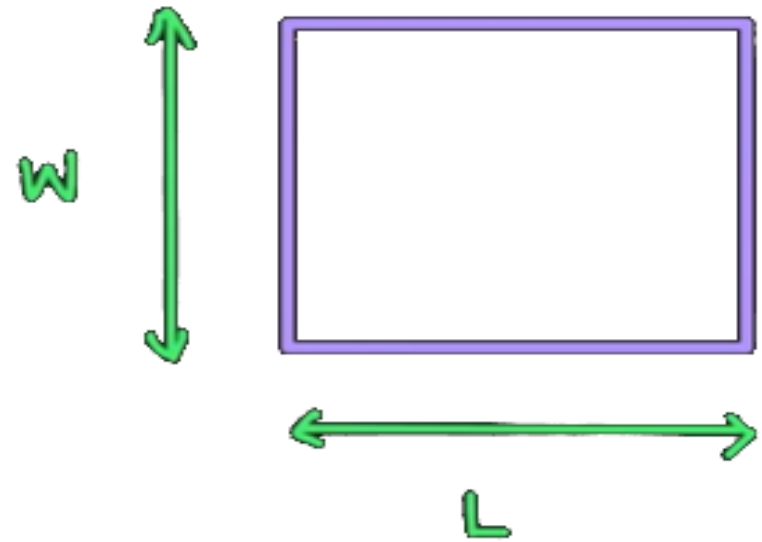


Layout Diagram: $Y = [(A + B).C + DE]$



Estimation of Layout Area:

$$Area = L * W$$

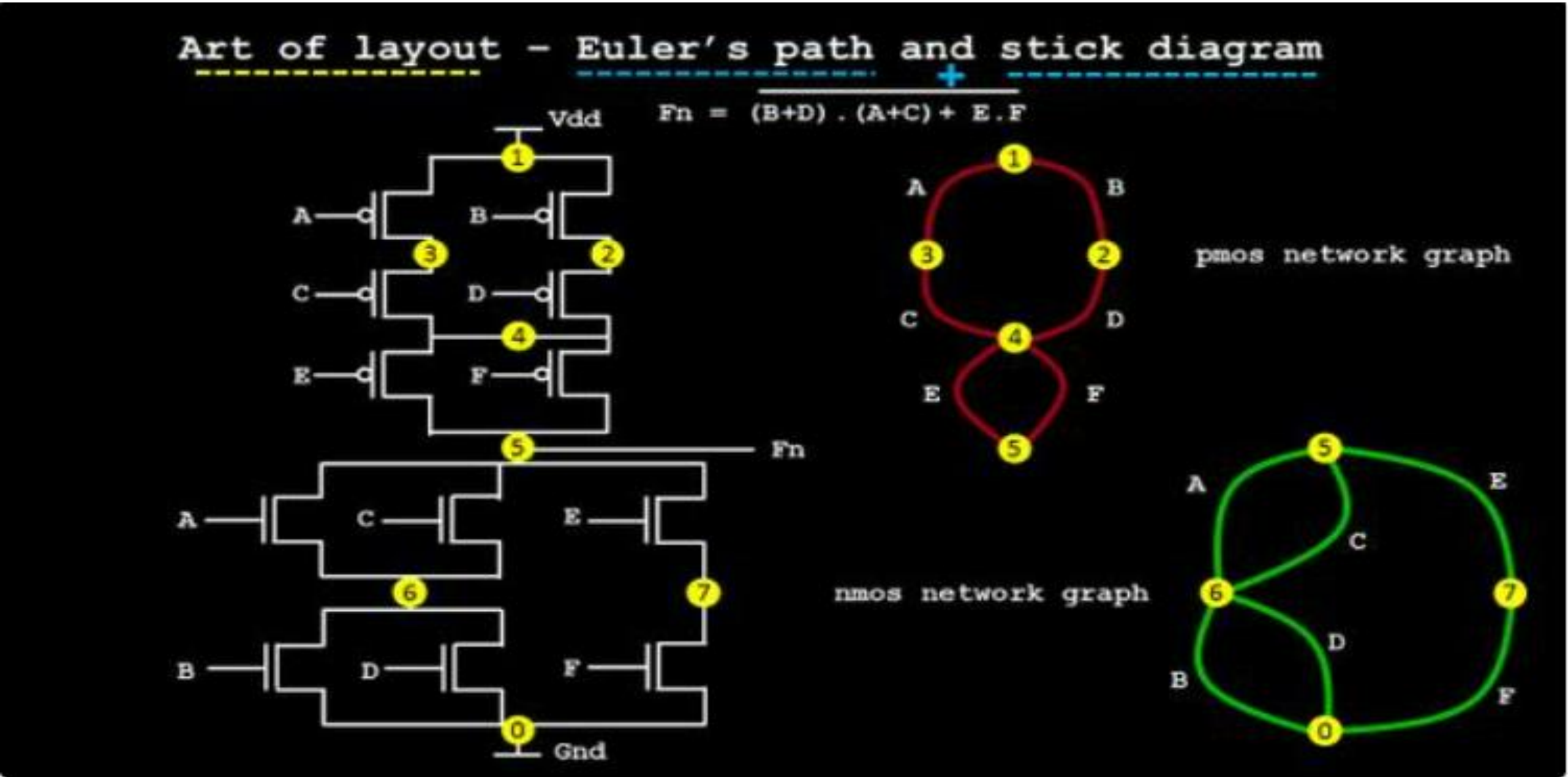


Horizontal Tracks (L) = $(4+1)\lambda = 5\lambda$

Vertical Tracks (W) = $(5+1)\lambda = 6\lambda$

$$Area = 5\lambda \times 6\lambda = 30\lambda^2$$

EULER GRAPH BASED STICK DIAGRAM

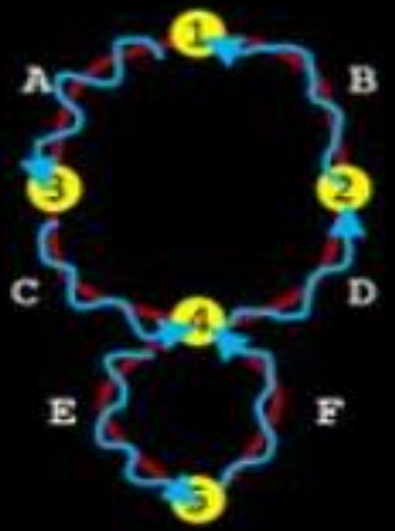


EULER GRAPH BASED STICK DIAGRAM

Art of layout - Euler's path and stick diagram

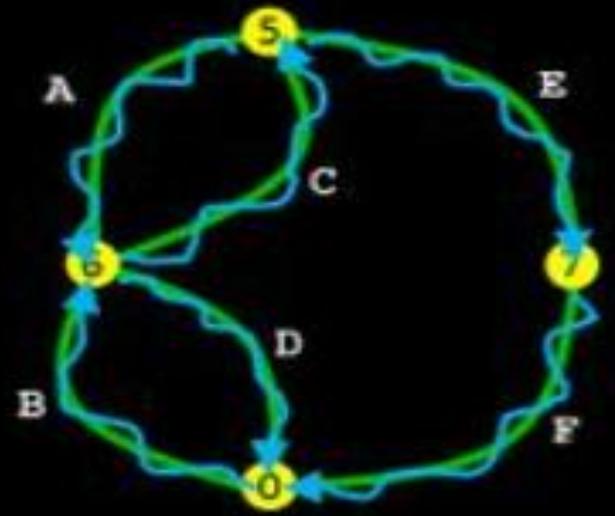
$$Fn = \overline{(B+D).(A+C)+E.F}$$

A – C – E – F – D – B

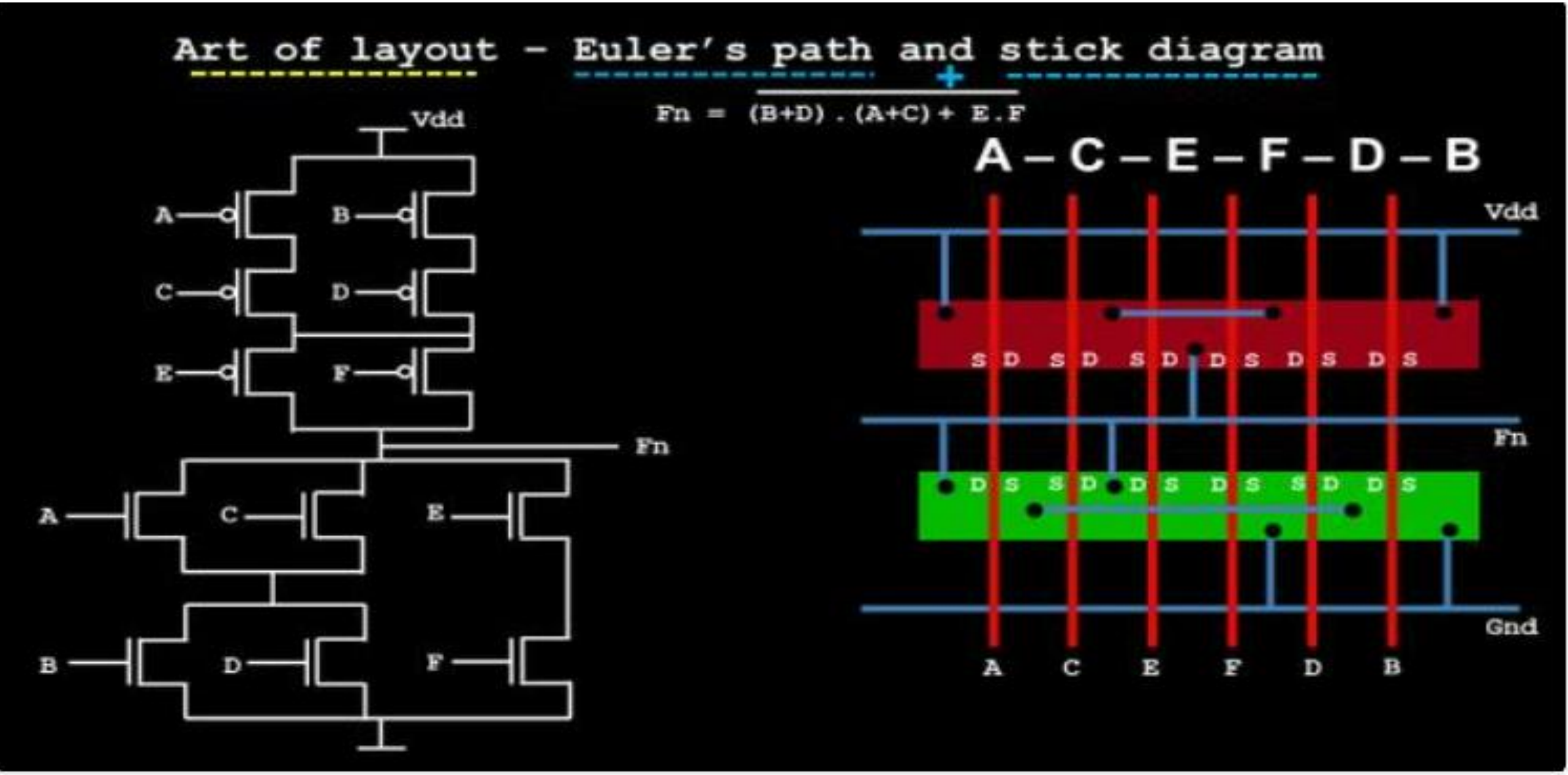


pmos network graph

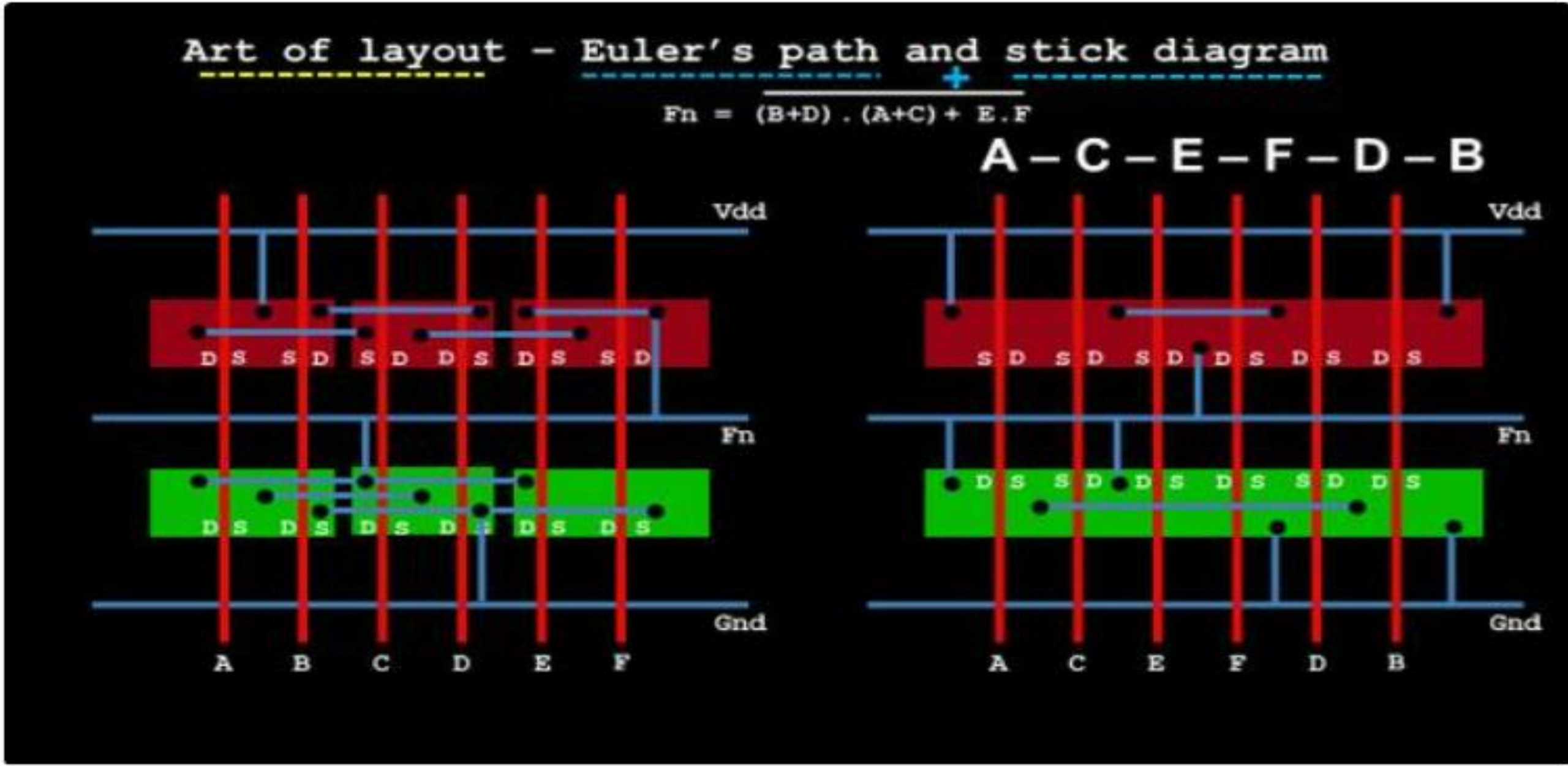
nmos network graph



EULER GRAPH BASED STICK DIAGRAM



EULER GRAPH BASED STICK DIAGRAM



EULER GRAPH BASED STICK DIAGRAM