Unit – 2 & 5

by
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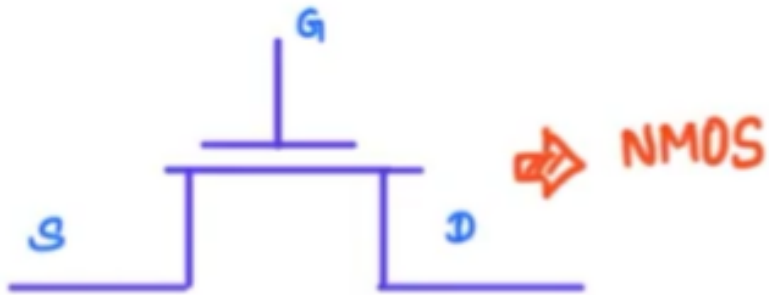
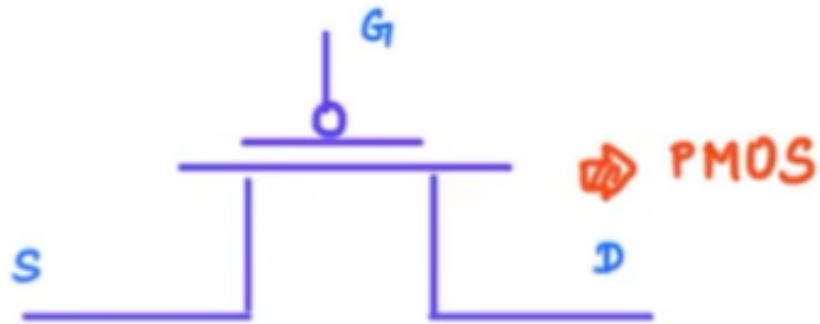
SYMBOLS OF "NMOS" and "PMOS"





applied Gate - to - Source voltage, $V_{gs} \geq V_t$

↙

Threshold voltage.

CONDITIONS :

nMOS $\Rightarrow$ $V_{gs} \geq V_{tn}$

pMOS $\Rightarrow$ $V_{sg} \geq |V_{tp}|$

NMOS – PASS TRANSISTOR LOGIC

case(i): $V_g = V_{dd} = 5V$, also $V_{tn} = 1V$.

$V_g = 0V$ (low input voltage) $\Rightarrow$ OFF

$V_g = 5V$ (high I/P voltage) $\Rightarrow$ ON $\rightarrow$ closed state switch.

$V_S = 0V$; $V_D = ??$

$V_{gs} \geq V_{tn}$; $V_{gs} = V_g - V_S = 5 - 0 = 5V$

$V_{tn} = 1V$; $V_{gs} > V_{tn}$ (i.e $5 > 1$)

$\therefore$ nMOS $\Rightarrow$ ON

$$\boxed{V_D = V_S = 0V}$$ $\Rightarrow$ strong '0'

case (ii): Let $V_S = 2V$; $V_D = ??$

$$V_{gs} = V_g - V_s = 5 - 2 = 3V$$

$$V_{tn} = 1V$$

$V_{gs} > V_{tn} \Rightarrow$ nMOS $\Rightarrow$ ON state

$\therefore$ $\boxed{V_D = V_S = 2V}$

case (iii): Let $V_S = 4V$; $V_D = ??$

$V_{gs} = V_g - V_s = 5V - 4V = 1V$; $V_{tn} = 1V$

$\therefore$ $V_{gs} = V_{tn}$ (i.e. $1 = 1V$)

nMOS $\Rightarrow$ ON state

$\boxed{V_D = V_S = 4V}$

$V_D = V_{dd} - V_{tn}$ (i.e $V_{dd} = 5V$, $V_{tn} = 1V$)

$= 5 - 1$

$\therefore$ $V_D = 4V$

NMOS – PASS TRANSISTOR LOGIC

case (iv) : $V_s = 5V$ (≈ high voltage)

$V_{gs} = V_g - V_s = 5V - 5V = 0V$; $V_{tn} = 1V$

$V_{gs} < V_{tn}$ ⇒ nMOS = OFF

$V_d = V_{dd} - V_{tn}$ ⇒ Threshold voltage drop / V_t drop problem

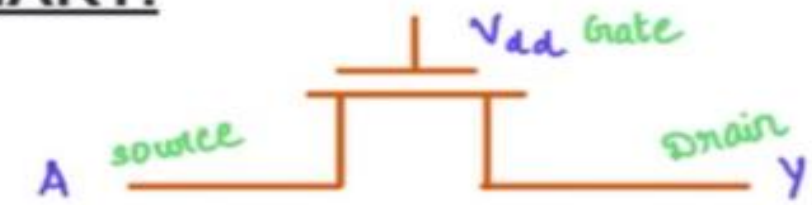
$V_d = 4V$

⇓

weak "1"

NMOS – PASS TRANSISTOR LOGIC

SUMMARY:



case(i): $V_g = V_{dd} = 5V$; $V_{tn} = 1V$

$V_s = V_A = 0V$ and $V_y = ?? = V_d = ??$

$V_{gs} = V_g - V_s = 5 - 0 = 5V$;

$V_{gs} > V_{tn} \Rightarrow 5 > 1 \therefore$ nMOS $\Rightarrow$ ON

$\therefore V_y = V_d = 0V$ (strong 0)

case(ii): $V_A = 2V$; $V_y = V_d = ???$

$V_{gs} = V_g - V_s = V_g - V_A = 5 - 2 = 3V$

$V_{gs} > V_{tn} \Rightarrow 3 > 1 \therefore$ nMOS $\Rightarrow$ ON

$\therefore V_y = V_d = 2V$

case(iii): $V_s = V_A = 4V$; $V_y = V_d = ???$

$V_{gs} = V_g - V_s = 5 - 4 = 1V$

$V_{gs} = V_{tn} \Rightarrow 1 = 1V \therefore$ nMOS $\Rightarrow$ ON

whenever $V_{gs} \geq V_{tn}$

$\therefore V_y = V_d = 4V$

case(iv): $V_s = V_A = 5V = V_{dd}$; $V_y = V_d = ??$

$V_{gs} = V_g - V_s = 5 - 5 = 0V$

$\therefore V_{gs} < V_{tn}$ ($\because 0 < 1V$) $\therefore$ nMOS $\Rightarrow$ OFF

$\therefore V_y = V_d = 4V$ (weak 1)

PMOS – PASS TRANSISTOR LOGIC

case (i): $V_g = 0V \Rightarrow$ low I/P voltage $\Rightarrow$ ON $\rightarrow$ closed

$V_g = 5V \Rightarrow$ high I/P voltage $\Rightarrow$ OFF

$V_{tp} = -1V$; PMOS: $V_{sg} \geq |V_{tp}|$

$\therefore |V_{tp}| = 1V$

$V_s = 5V$; $V_g = 0V$; $|V_{tp}| = 1V$

$\therefore V_{sg} = V_s - V_g = 5 - 0 = 5V$

$\therefore V_{sg} > |V_{tp}| \Rightarrow$ PMOS $\Rightarrow$ ON

$\therefore \boxed{V_D = V_S = 5V} \Rightarrow$ strong "1".

case (ii): $V_s = 4V$; $V_g = 0V$; $|V_{tp}| = 1V$

$V_{sg} = V_s - V_g = 4 - 0 = 4V$ ($V_{sg} > |V_{tp}|$)

PMOS ⇒ ON ; $\boxed{V_D = V_S = 4V}$

case (iii): $V_s = 1V$

$V_{sg} = V_s - V_g = 1 - 0 = 1V$; $|V_{tp}| = 1V$

$V_{sg} = |V_{tp}|$ ⇒ PMOS = ON

$\boxed{V_D = V_S = 1V}$ ⇒ $|V_{tp}|$

case (iv): $V_s = 0V$;

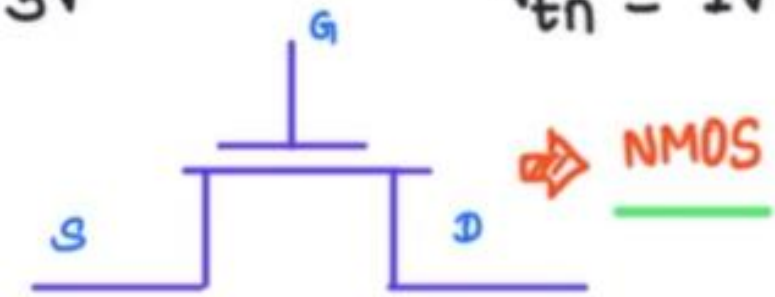
$V_{sg} = V_s - V_g = 0 - 0 = 0V$

$|V_{tp}| = 1V$

$V_{sg} < |V_{tp}|$ ⇒ PMOS - OFF state

$\boxed{1V = V_d = |V_{tp}|}$ → weak "0"

$V_g = 5V$ $V_{tn} = 1V$



(i) $V_S = 0V$;

$V_D = 0V$.

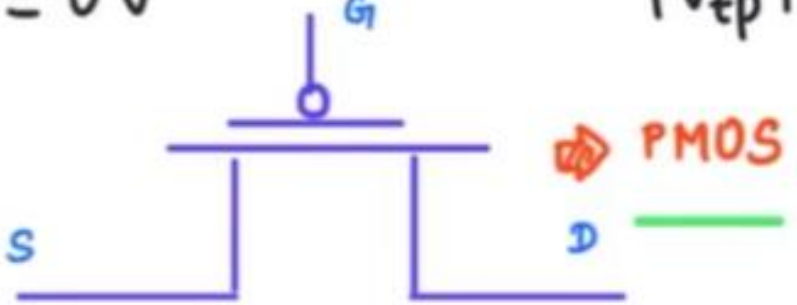
STRONG "0"

(ii) $V_S = V_{dd}$;

$V_D = V_{dd} - V_{tn}$

WEAK "1"

$V_g = 0V$ $|V_{tp}| = 1V$



(i) $V_S = V_{dd}$

$V_D = V_{dd}$

STRONG "1"

(ii) $V_S = 0V$

$V_D = |V_{tp}|$

WEAK "0"

PMOS PASS TRANSISTOR

⇒ PMOS turns "ON" for LOW input at the gate terminal and produces "strong 1" at the drain output.

case(i) $V_B = 0$; $V_A = V_{dd}$

$V_y = ???$

since $V_B = 0V$ (PMOS turns "ON")

$$\therefore \boxed{V_y = V_A = V_{dd}}$$

case(ii) $V_B = 0$; $V_A = 0V$;

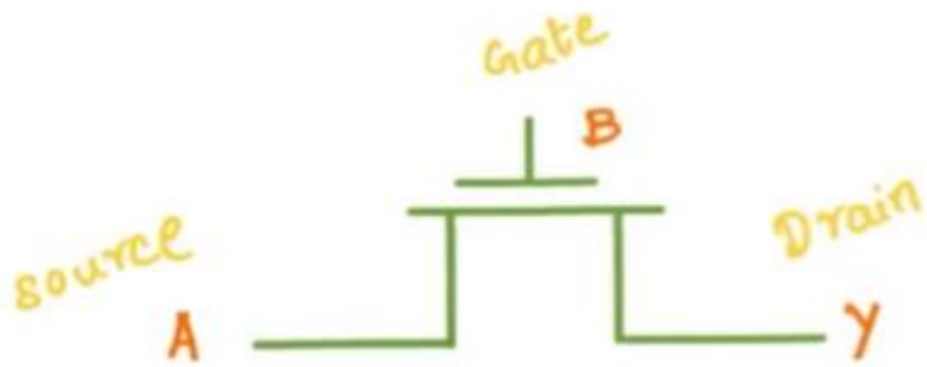
$V_y = ???$

since "PMOS" passes "weak 0"

$\therefore V_A = 0V$ cannot be passed as output to y.

$$\therefore \boxed{V_y = |V_{tp}|}$$

nMOS PASS TRANSISTOR



case (i) $V_B = V_{dd}$; $V_A = 0$

$V_y = ???$

$V_B = V_{dd}$ (Transistor turns ON)

$\therefore$ $\boxed{V_y = V_A = 0}$

$\Rightarrow$ nMOS turns "ON" for high input at the gate terminal and produces "strong 0" at the drain output.

case (ii) $V_B = V_{dd}$; $V_A = V_{dd}$

$V_y = ???$

$V_B = V_{dd}$ (Transistor – ON); But nMOS passes "weak 1" $\therefore$ $V_A = V_{dd}$ cannot be passed as output to y

$\therefore$ $\boxed{V_y = V_{dd} - V_{tn}}$

SUMMARY

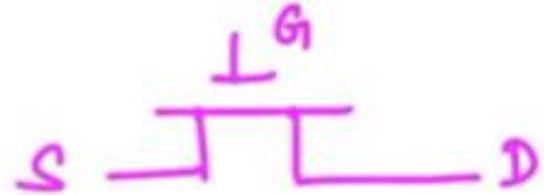
PMOS PASS TRANSISTOR

B Gate	A Source	y Drain
0	0	$\|V_{tp}\|$
0	V_{dd}	V_{dd}
V_{dd}	0	Z
V_{dd}	V_{dd}	Z

NMOS PASS TRANSISTOR

B Gate	A Source	y Drain
0	0	Z
0	V_{dd}	Z
V_{dd}	0	**0**
V_{dd}	V_{dd}	**Vdd - Vtn**

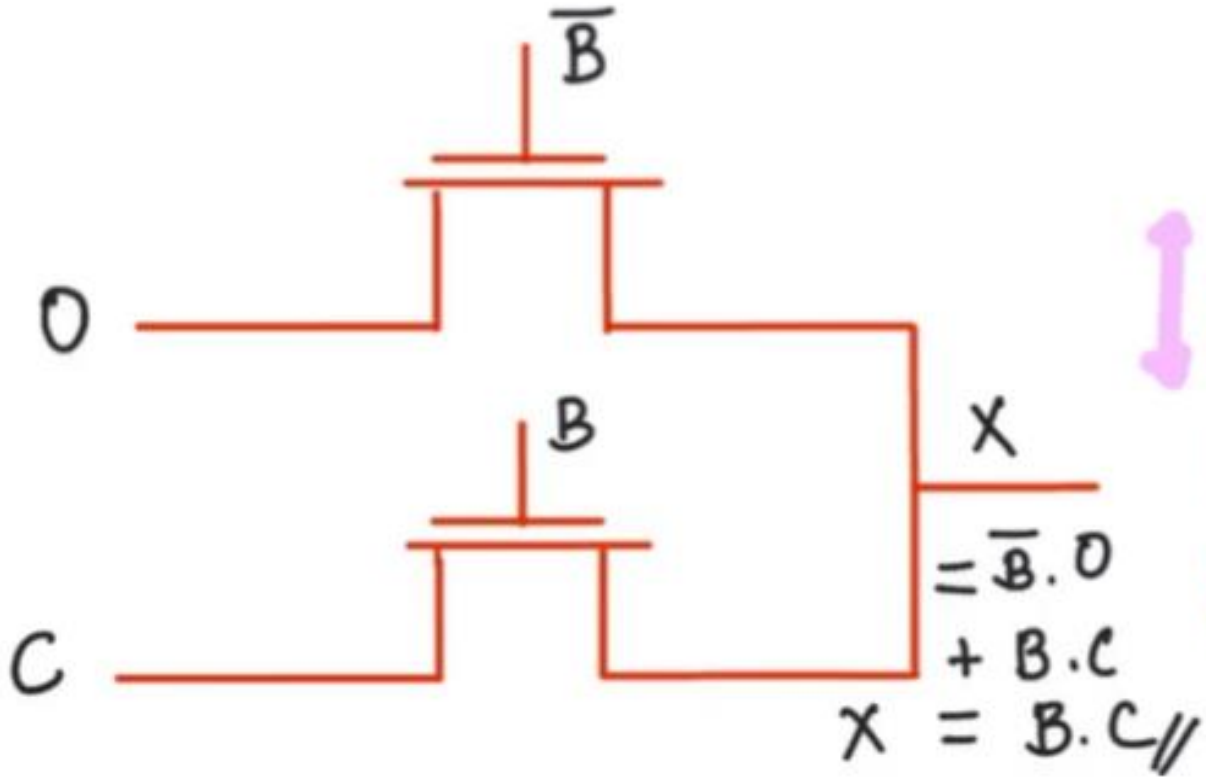
Given: $F = [A + (B.C)]'$ using nMOS pass transistors.



$$F = \overline{A + X}$$

where $X = (B.C) \Rightarrow$ AND

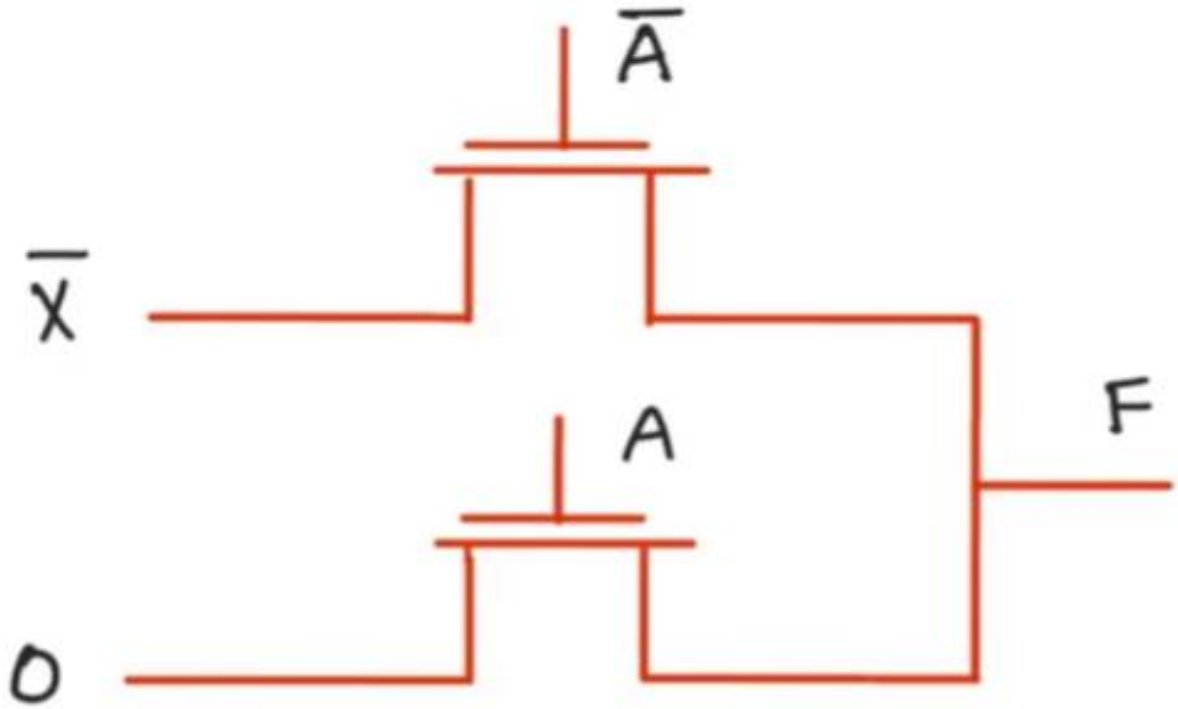
$\overline{A+X} \Rightarrow$ NOR gate



B	C	X
0	0	0
0	1	0
1	0	0
1	1	1

B̄ B̄ B B

$$F = \overline{A + X} = \overline{A + (B.C)}$$



NOR Gate

	A	X	F
$\bar{A}$	0	0	1
$\bar{A}$	0	1	0
A	1	0	0
A	1	1	0

$\bar{X}$

0

$$\therefore \quad F = \bar{A}\,\bar{X} + A.0 = \bar{A}\,\bar{X} = \overline{A + X}$$

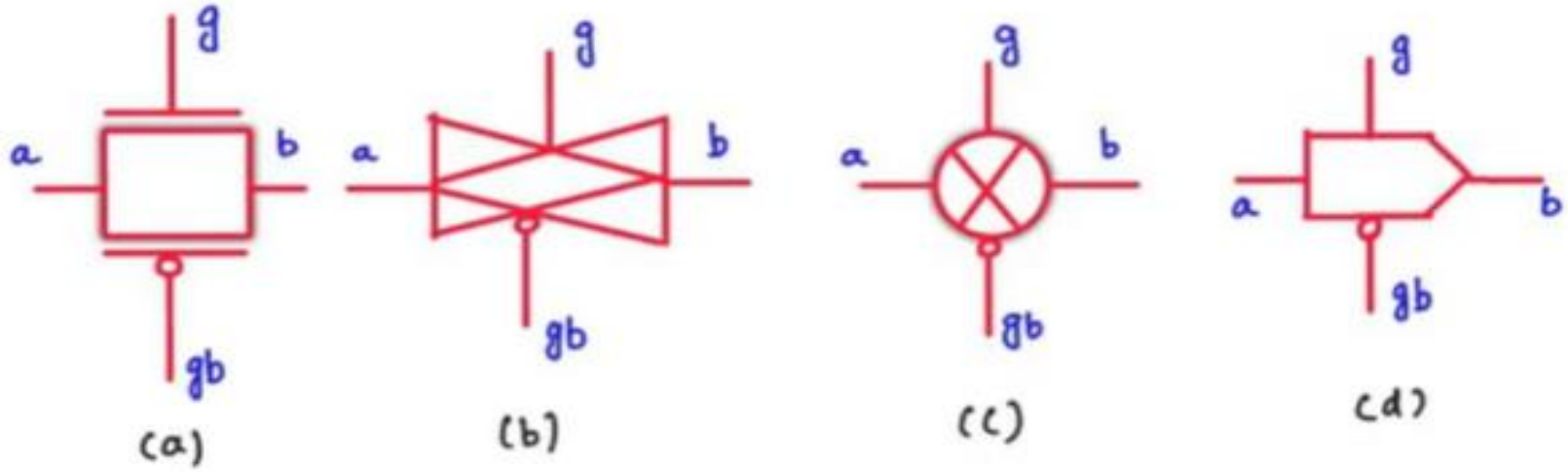
where $X = B.C$

$$\therefore \quad F = \overline{A + (B.C)}$$

No. of transistors = 4

TRANSMISSION GATE

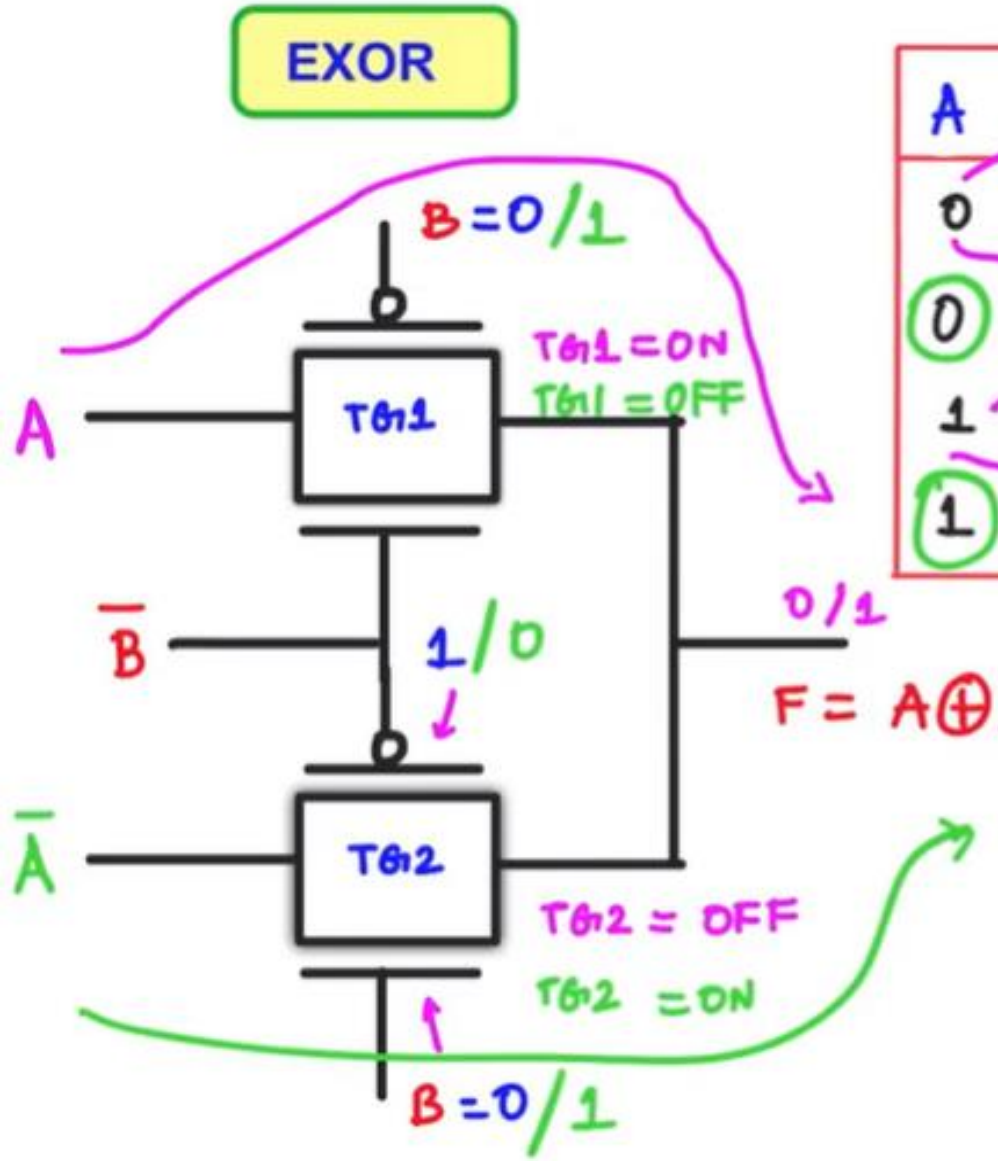
- The transmission gate is a parallel combination of nMOS and pMOS transistors with gates controlled by complementary voltages.
- This is the most widely used solution for the voltage drop problem in pass transistors.
- It uses the complementary properties of pMOS and nMOS transistors.

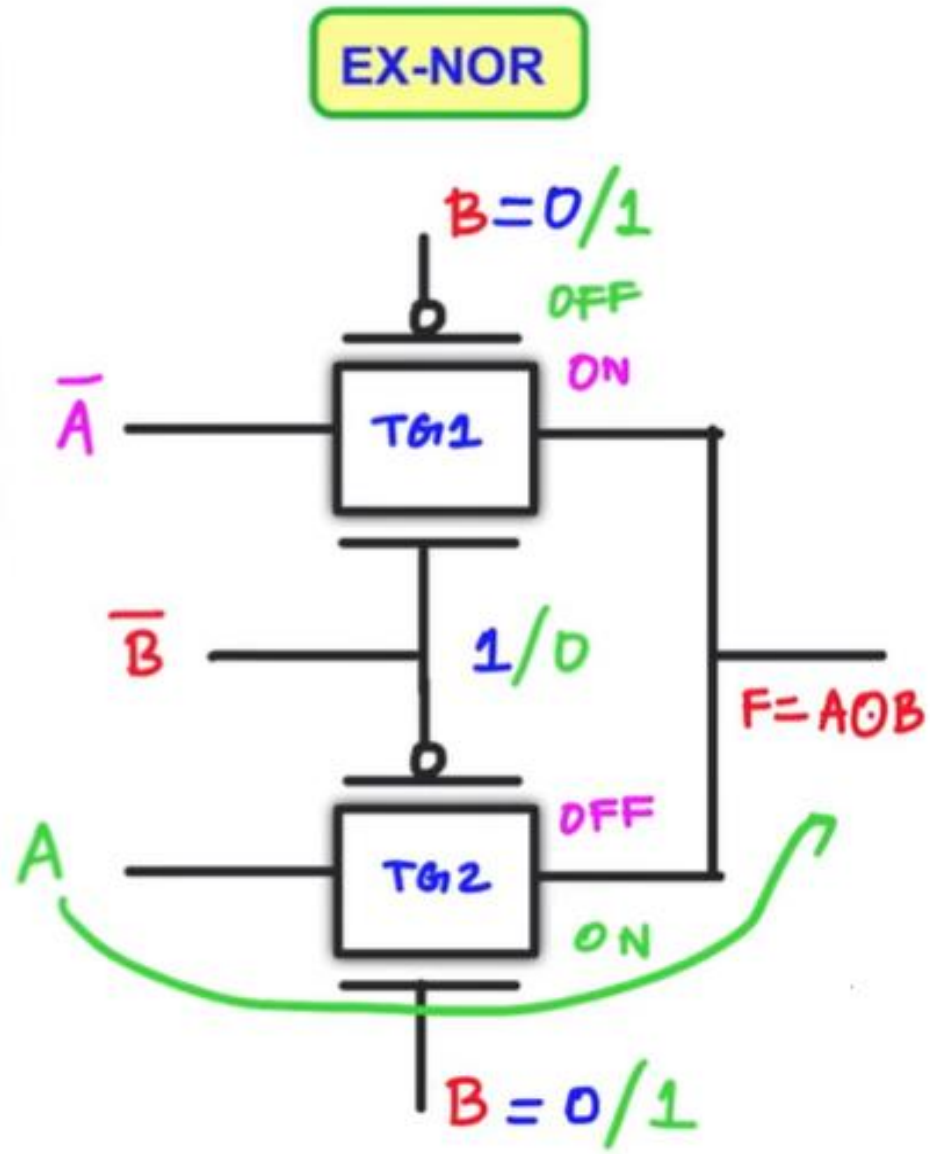


(a), (b), (c), (d) are symbol representations of Transmission Gate

Truth Table:

A	B	XOR	XNOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	0	1



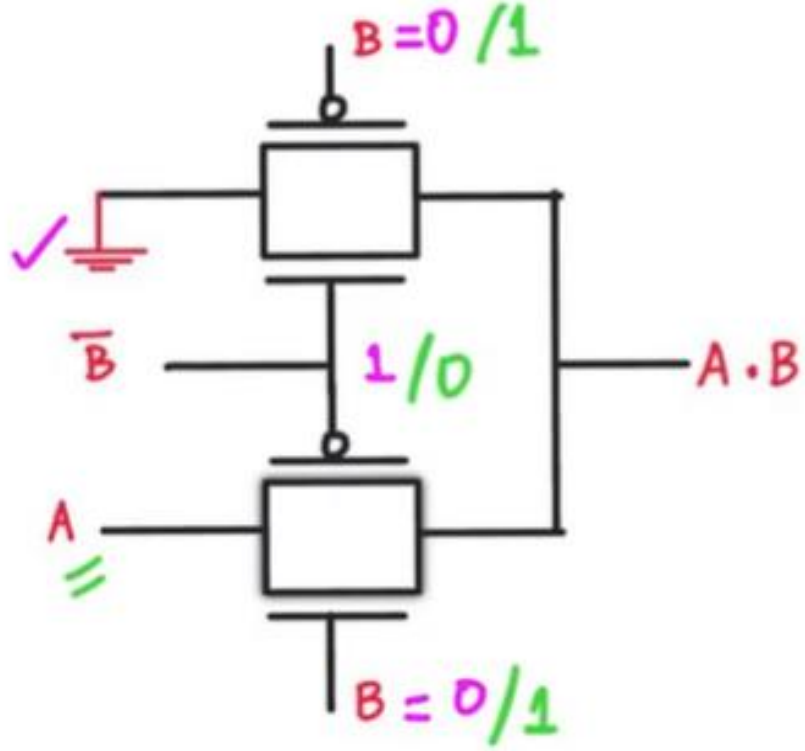


IMPLEMENTATION OF LOGIC GATES USING TG

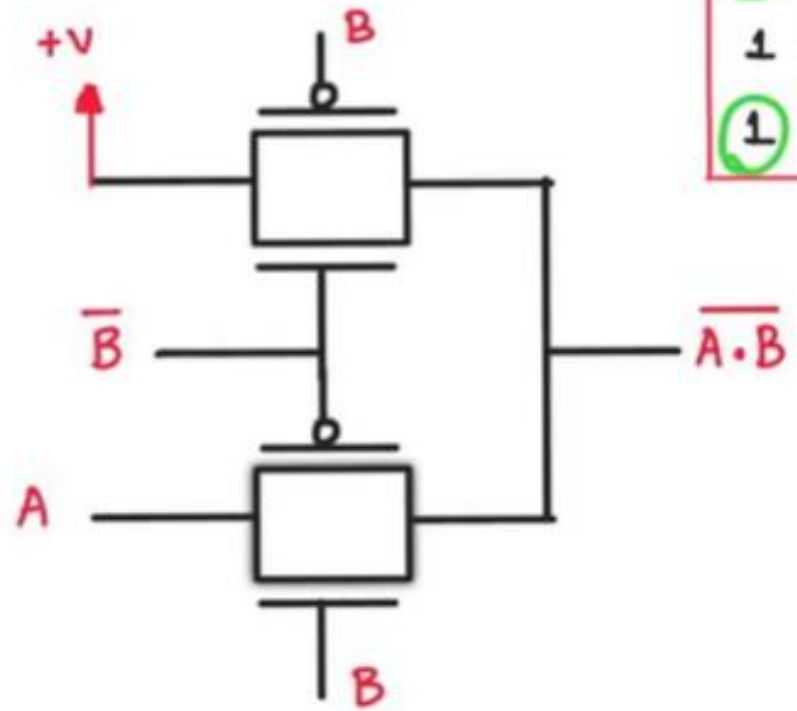
Truth Table:

A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

AND



NAND

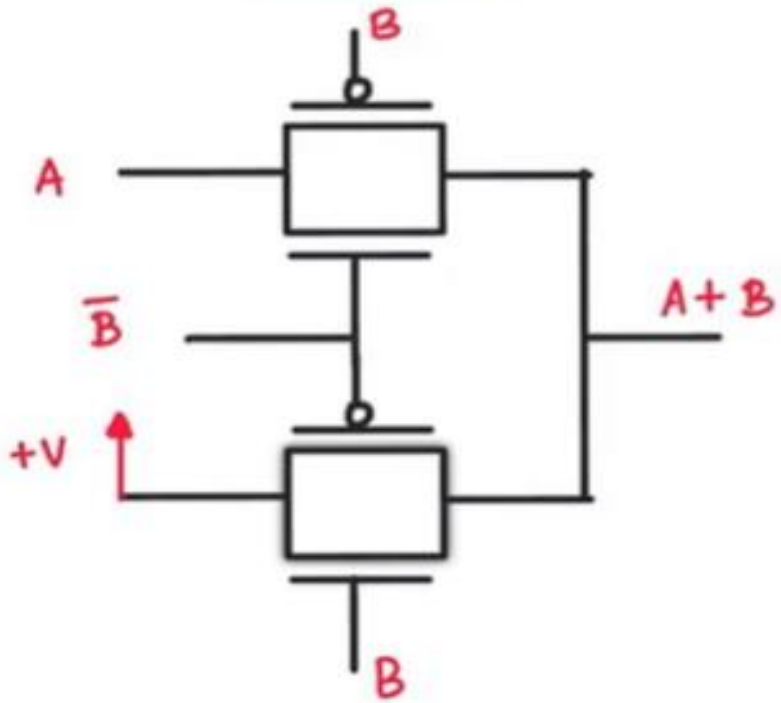


IMPLEMENTATION OF LOGIC GATES USING TG

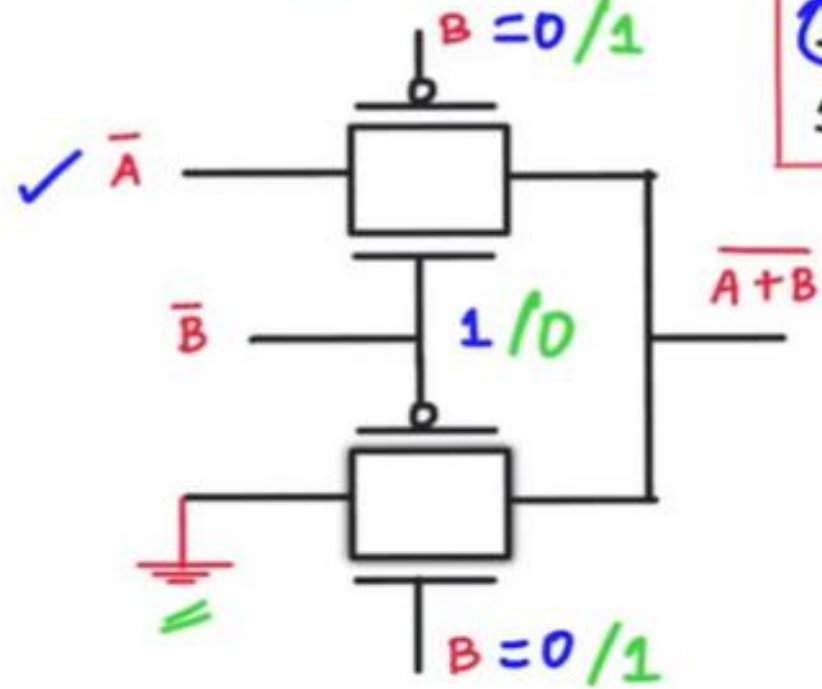
Truth Table:

A	B	OR	NOR
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

OR

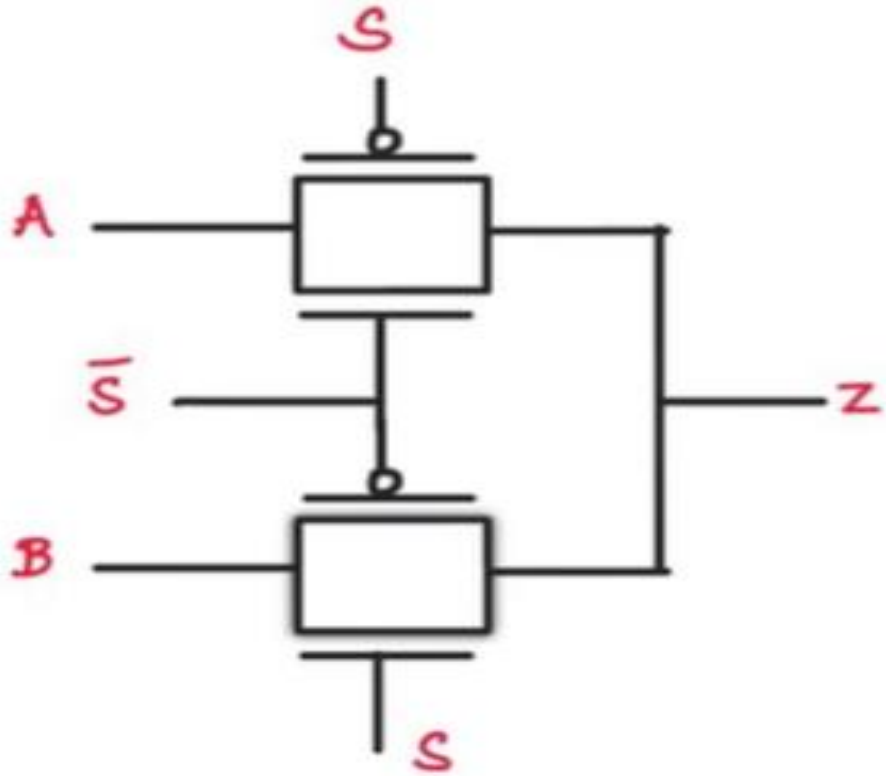


NOR



IMPLEMENTATION OF 2:1 MULTIPLEXER

2 : 1 MUX USING TG



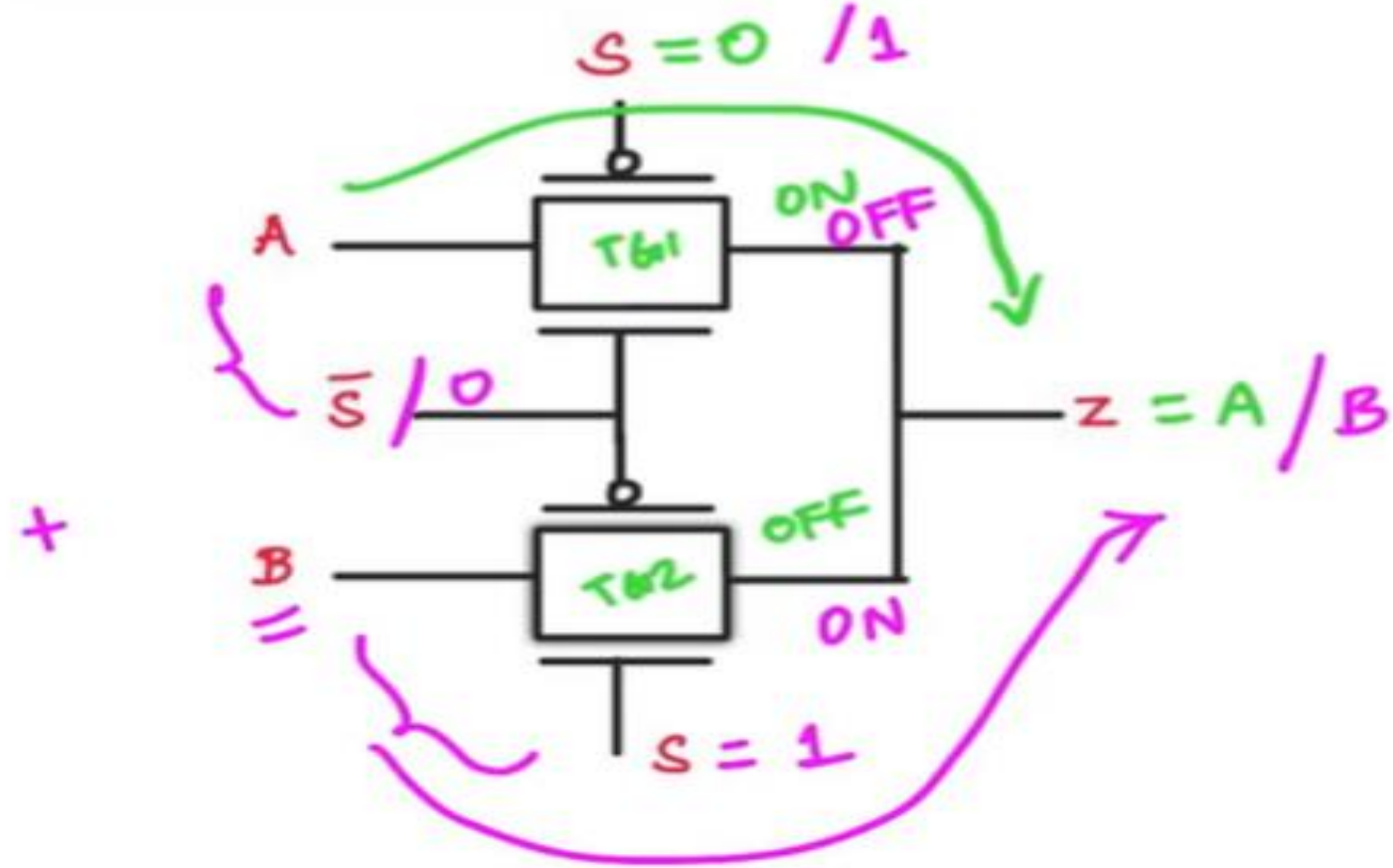
Truth Table:

S	Z
0	A
1	B

$$Z = A.\bar{S} + B.S$$

IMPLEMENTATION OF 2:1 MULTIPLEXER

2 : 1 MUX USING TG



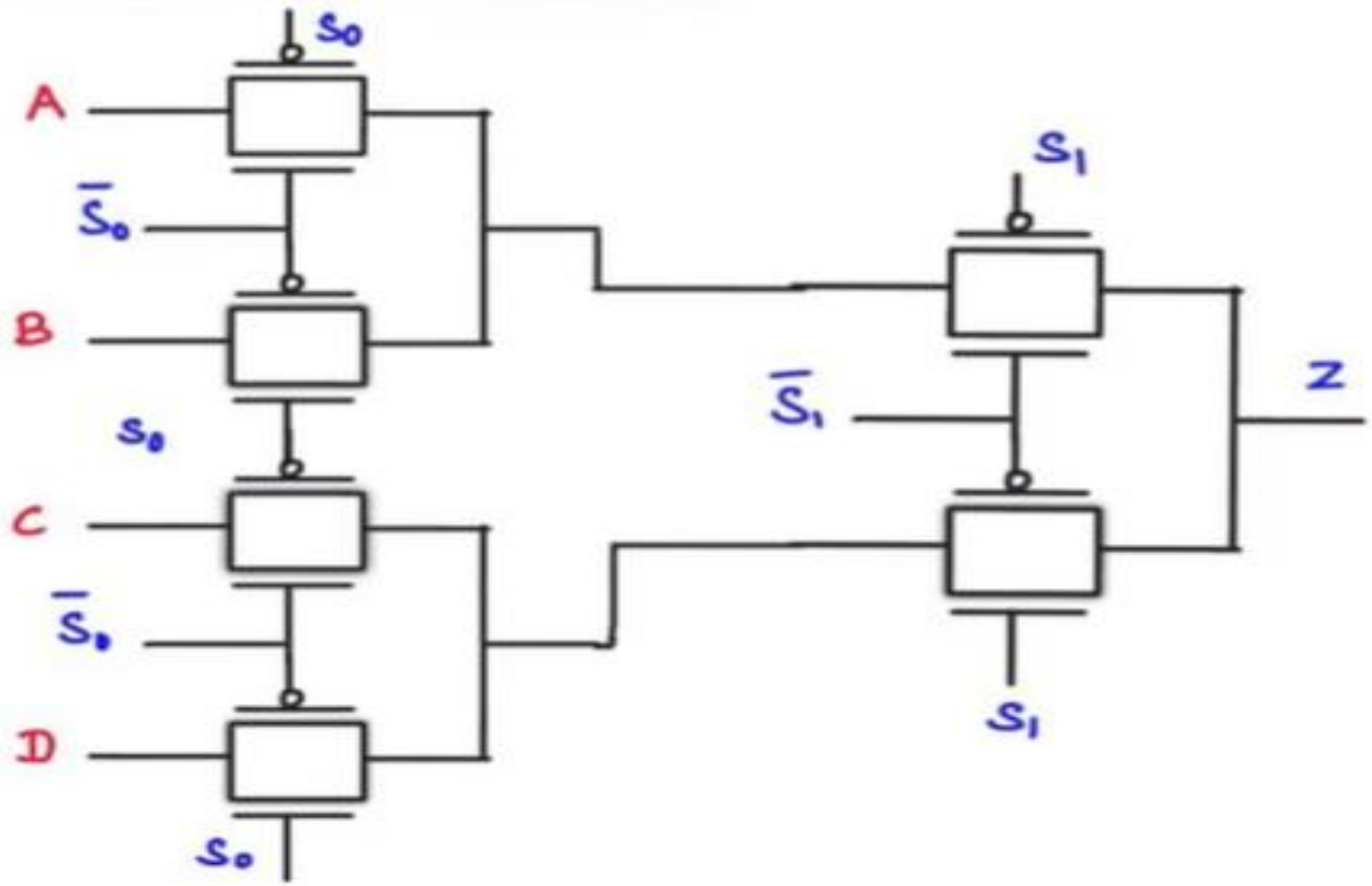
Truth Table:

S	Z
0	A
1	B

$$Z = A.\bar{S} + B.S$$

IMPLEMENTATION OF 4:1 MULTIPLEXER

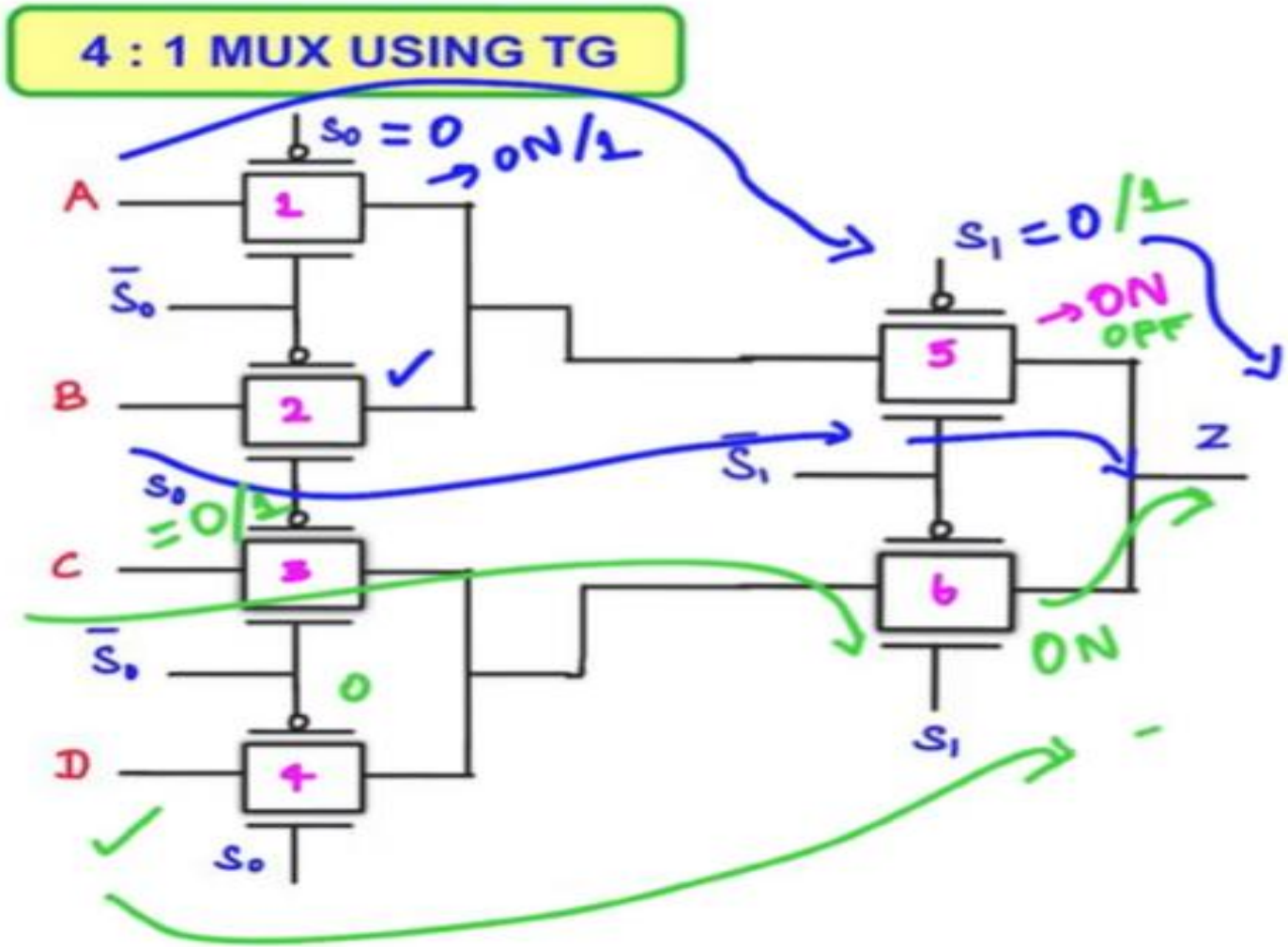
4 : 1 MUX USING TG



Truth Table:

S_1	S_0	Z
0	0	A
0	1	B
1	0	C
1	1	D

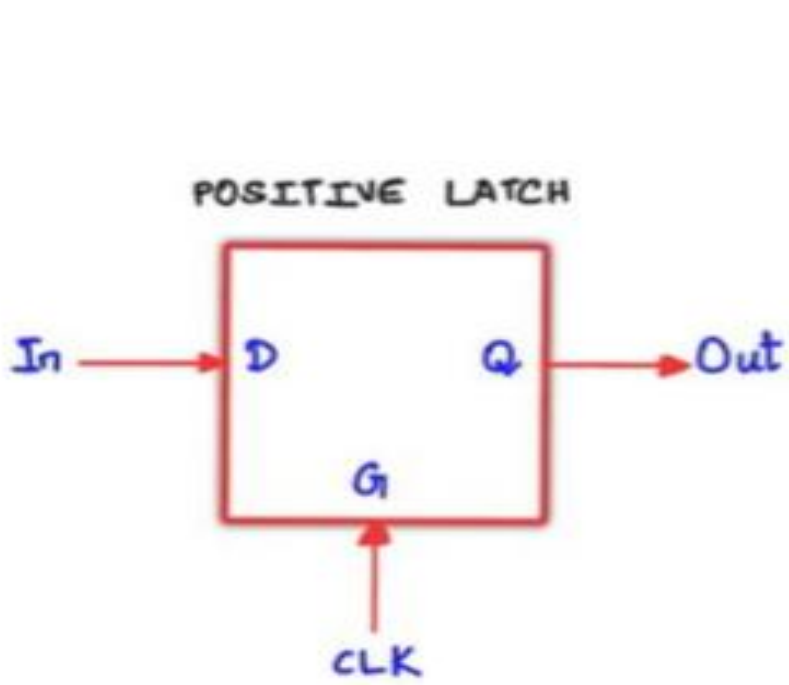
IMPLEMENTATION OF 4:1 MULTIPLEXER

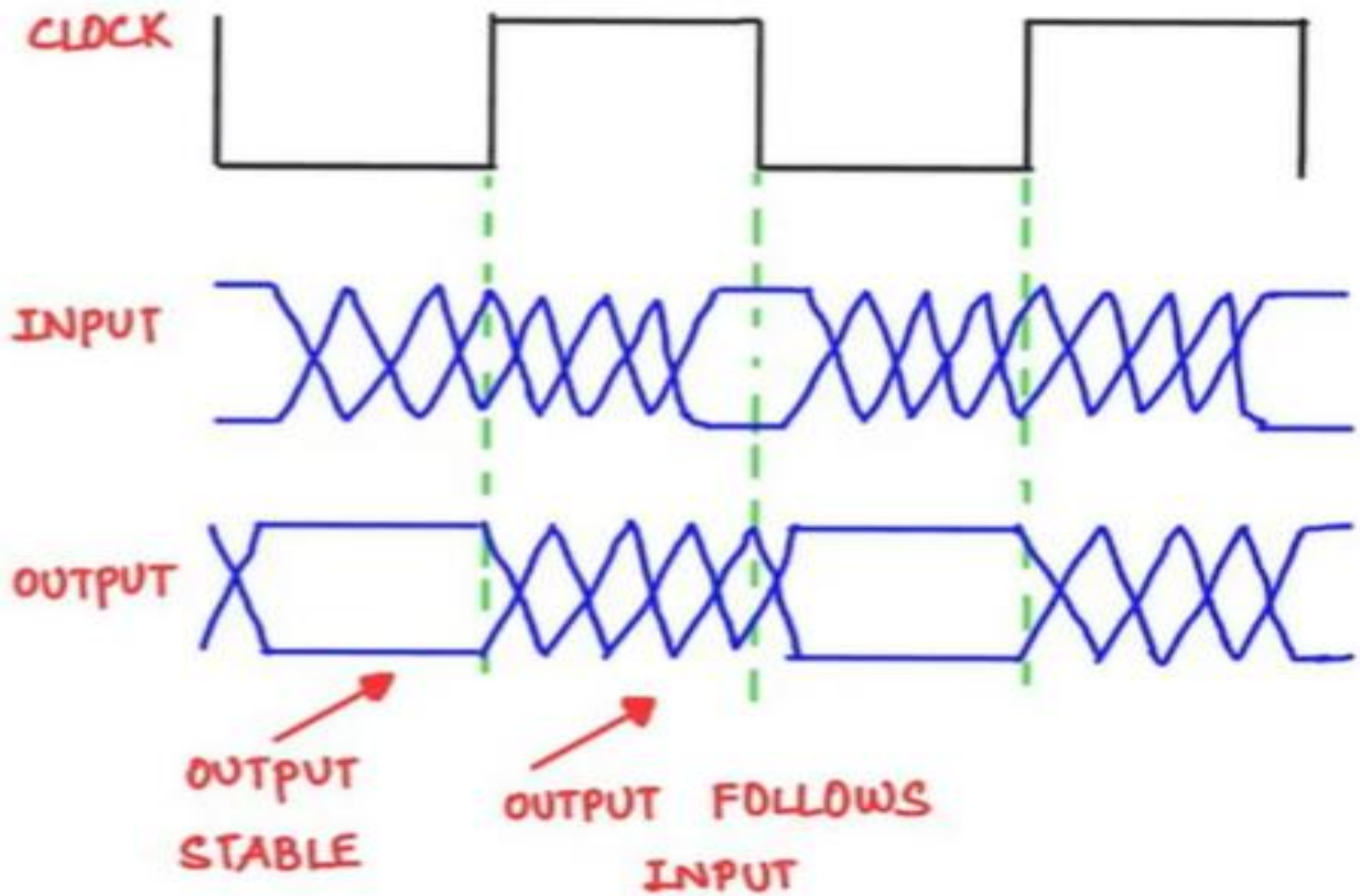


Truth Table:

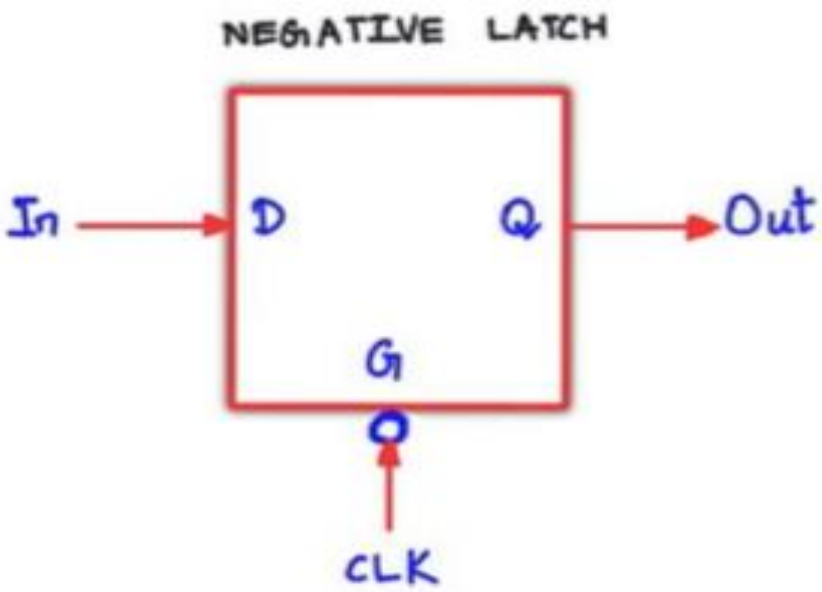
S_1	S_0	Z
0	0	A
0	1	B
1	0	C
1	1	D

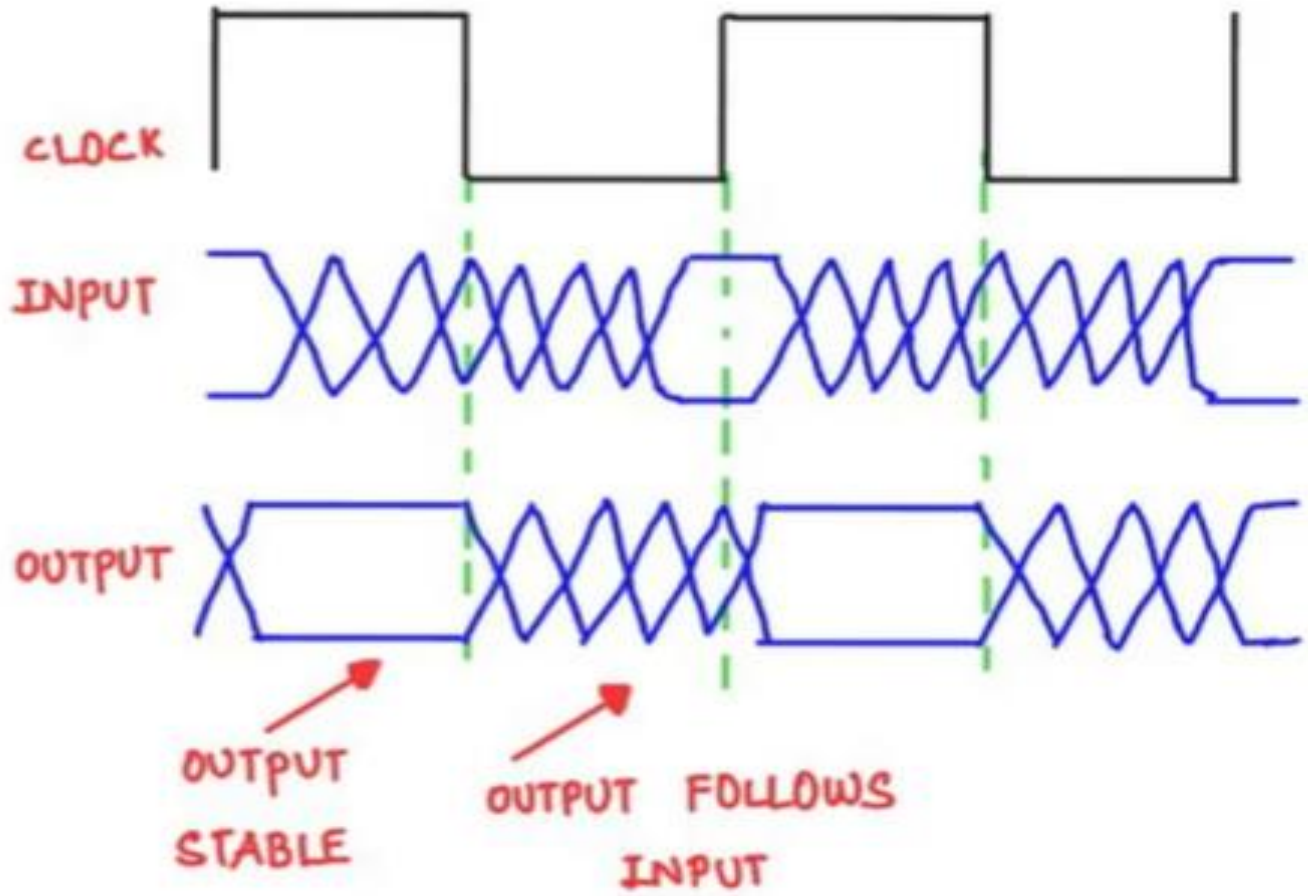
POSITIVE LATCH



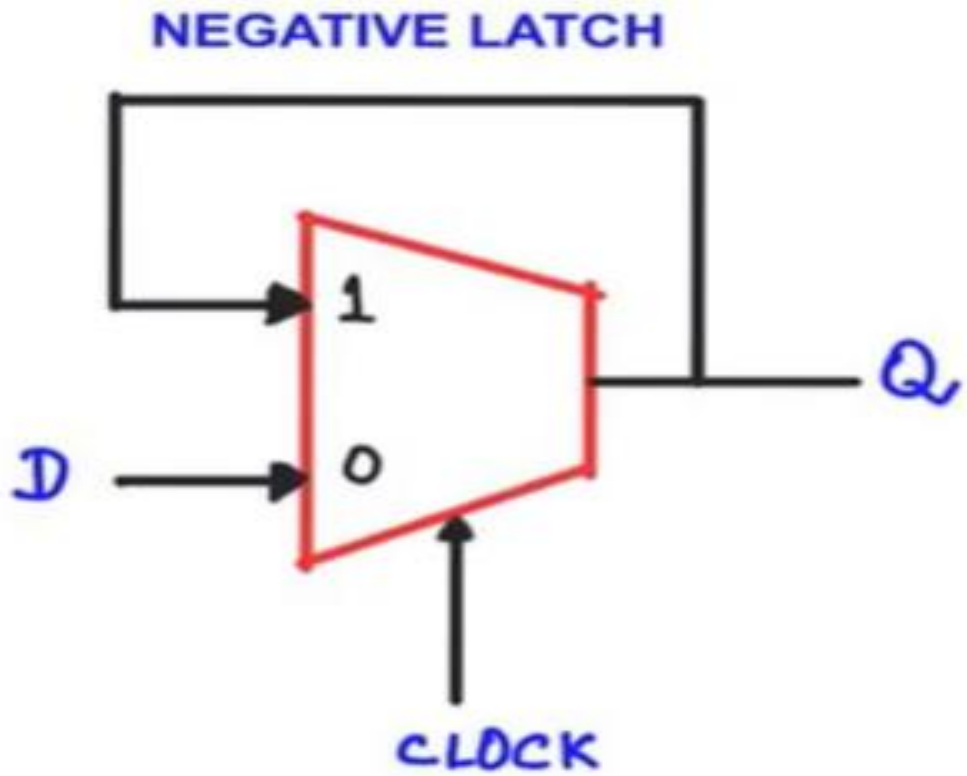


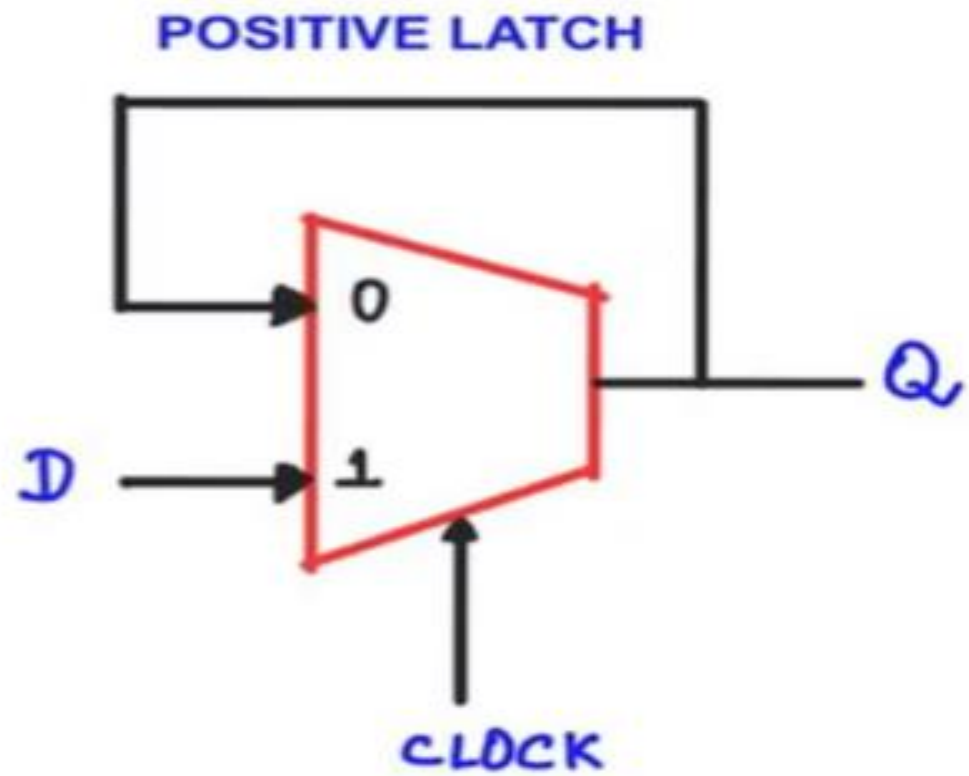
NEGATIVE LATCH



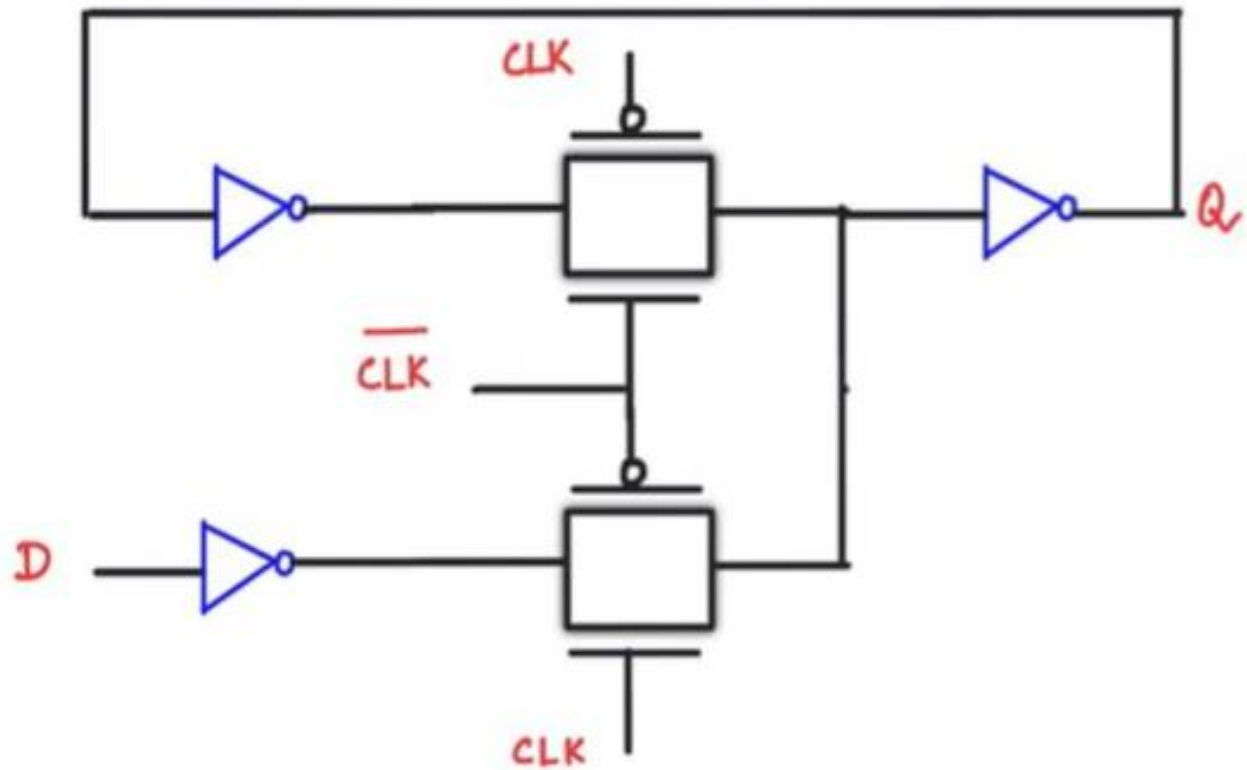


CONSTRUCTION OF STATIC LATCHES



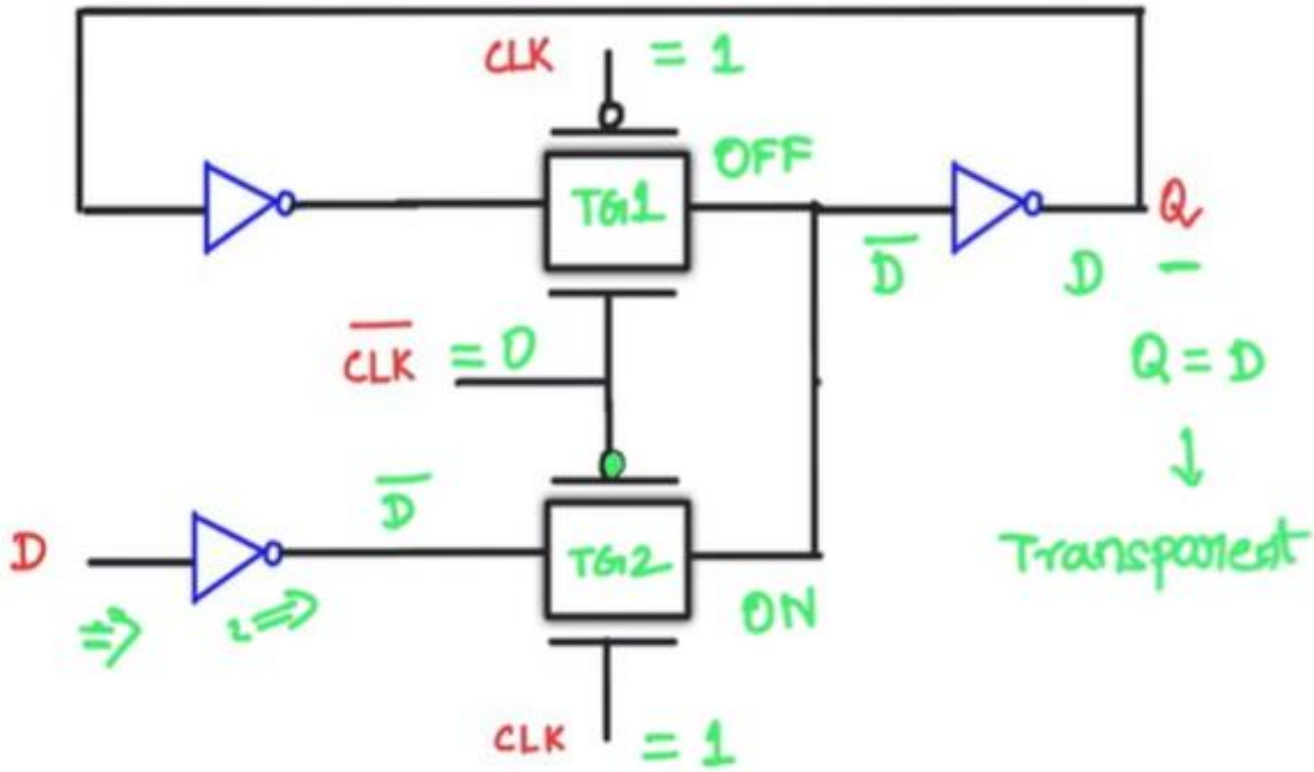


IMPLEMENTATION OF POSITIVE LATCH USING TG



- A transmission gate-based implementation of a positive latch is shown in Figure.
- When CLK is high, the bottom transmission gate is ON, and the D input is copied to the Q output.
- During this period, the feedback loop is open because the top transmission gate is off.

IMPLEMENTATION OF POSITIVE LATCH USING TG



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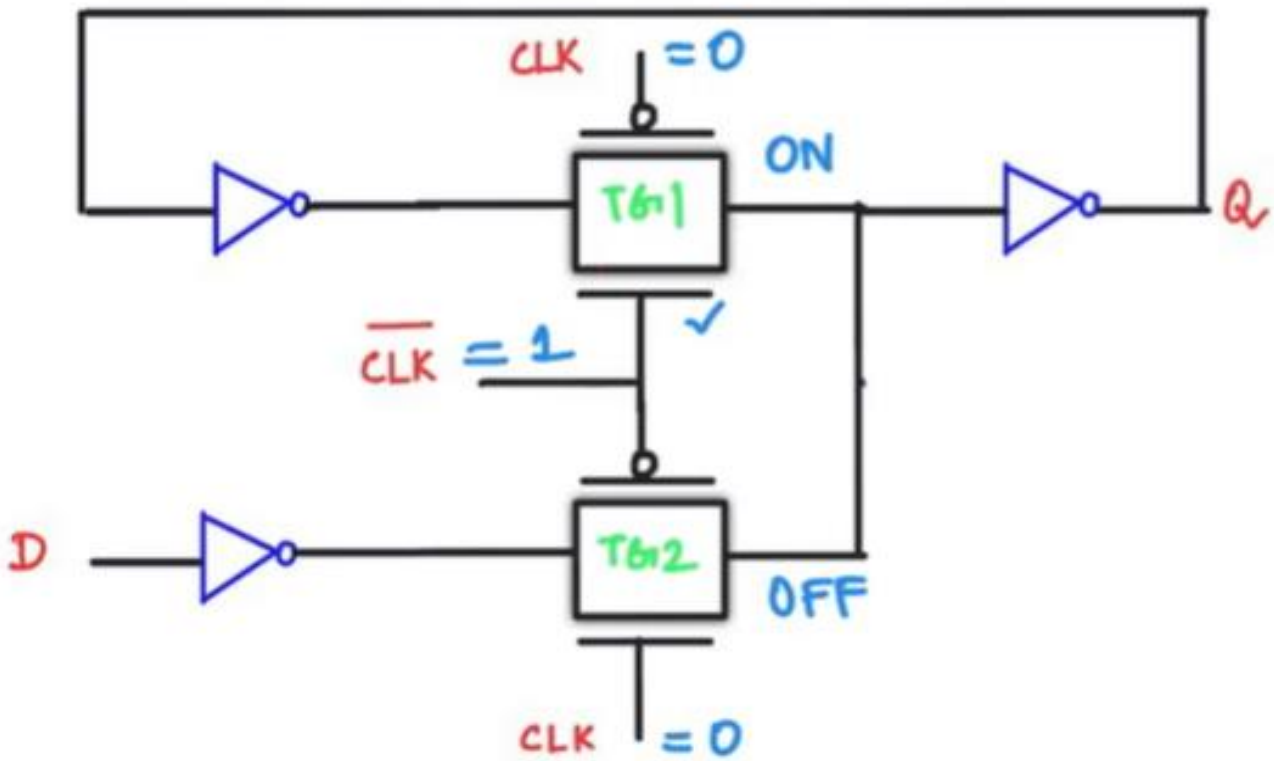
IMPLEMENTATION OF POSITIVE LATCH USING TG



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- When CLK is high, the bottom transmission gate is ON, and the D input is copied to the Q output.
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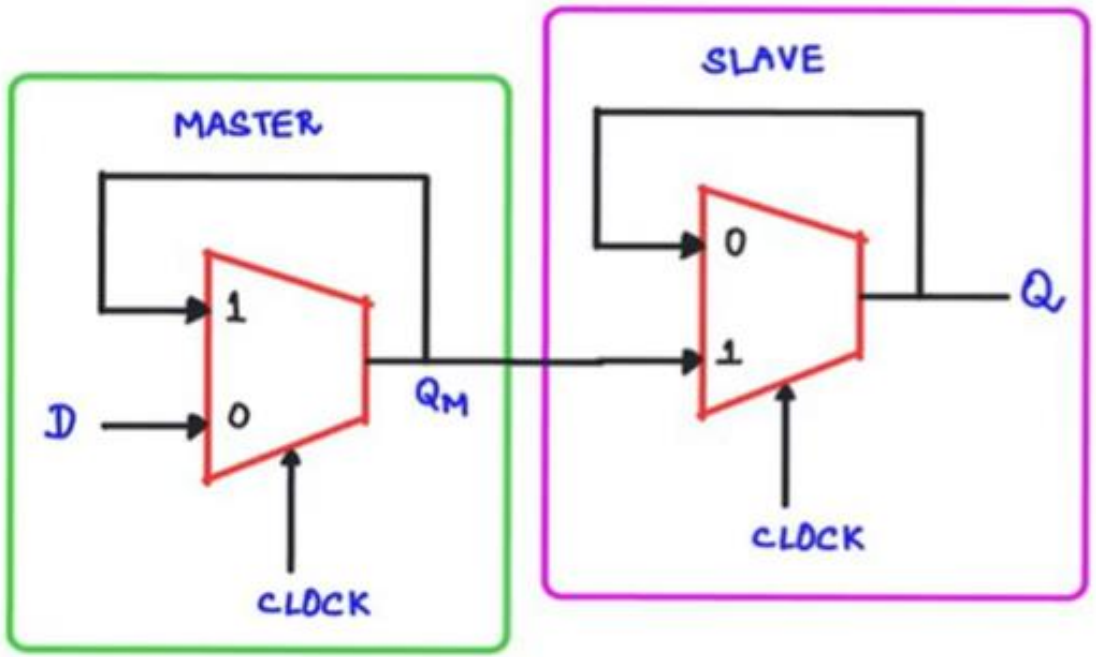
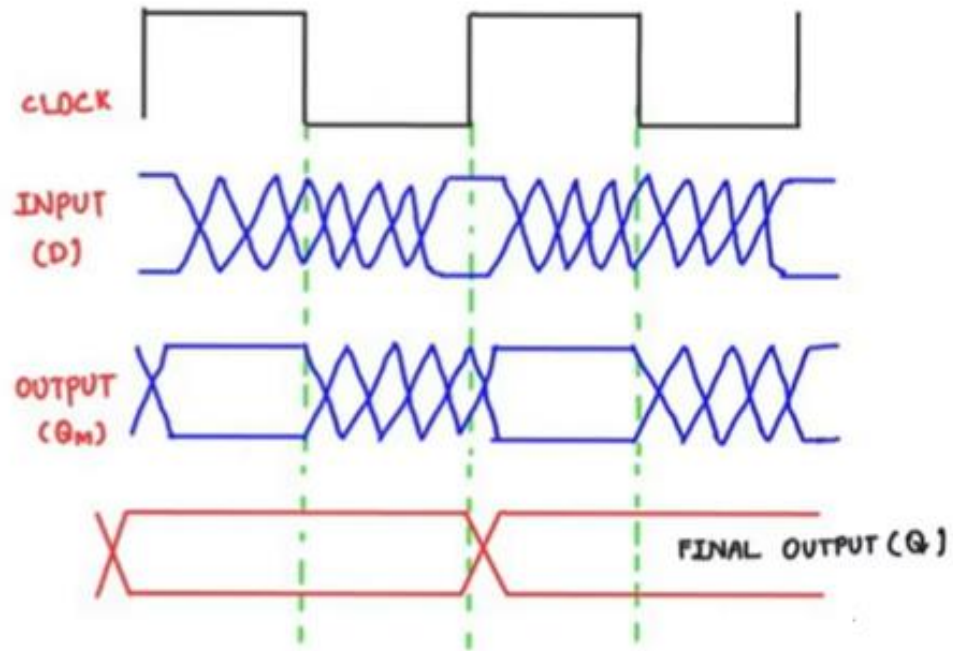
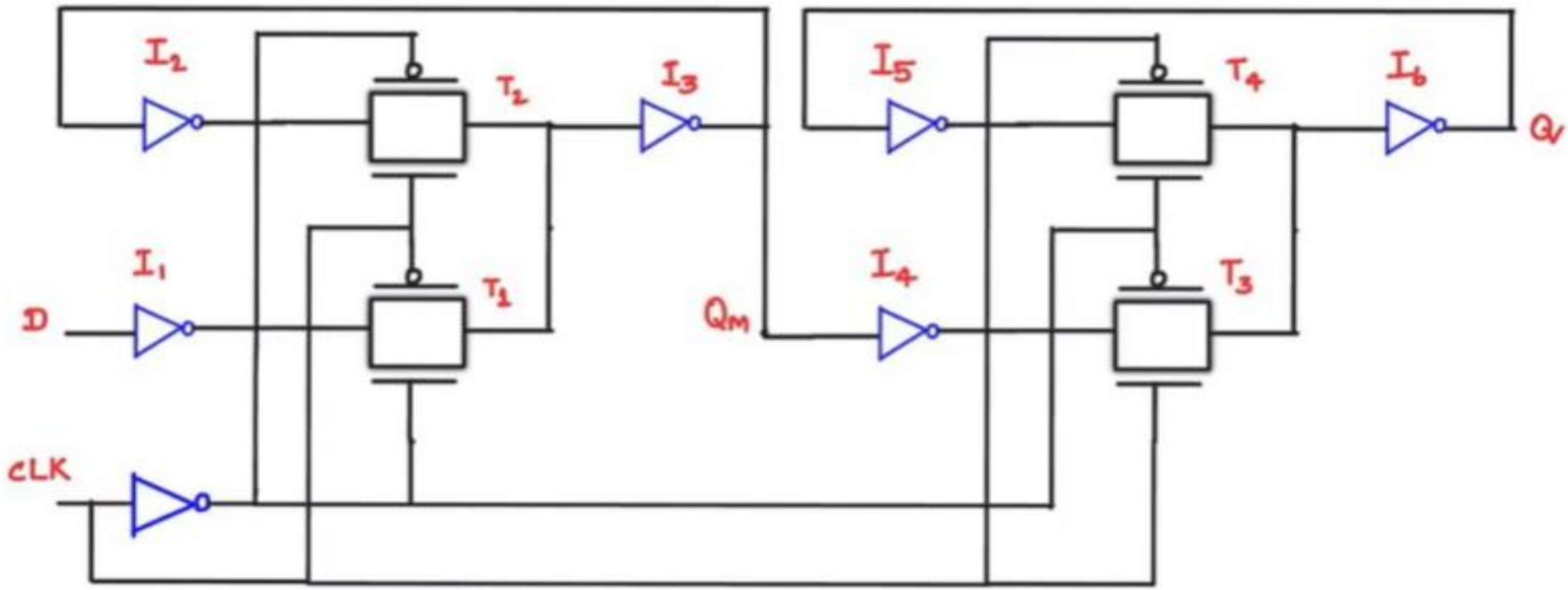
POSITIVE EDGE TRIGGERED REGISTER





MASTER-SLAVE POSITIVE EDGE TRIGGERED REGISTER



A transmission gate level implementation of the complete register is shown in Figure.

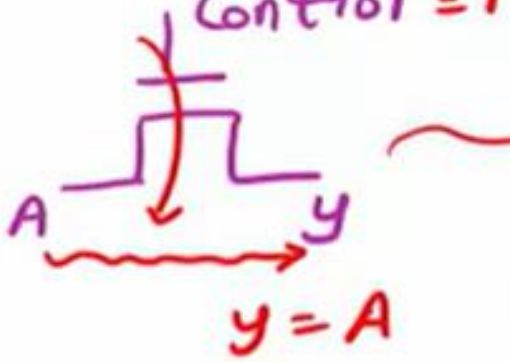
MASTER-SLAVE POSITIVE EDGE TRIGGERED REGISTER

- When CLK=0, T_1 is *on* and T_2 is *off* in the master latch. The D input is sampled into node Q_M.
- During this period, T_3 is *off* and T_4 is *on* and the cross-coupled inverters (I_5, I_6) hold the state of the slave latch.
- When CLK=1, the master stage stops sampling the input and goes into a *hold* mode.
- T_1 is *off* and T_2 is *on*, and the cross coupled inverters I_3 and I_4 holds the state of Q_M.
- Also, T_3 is *on* and T_4 is *off*, and Q_M is copied to the output Q.

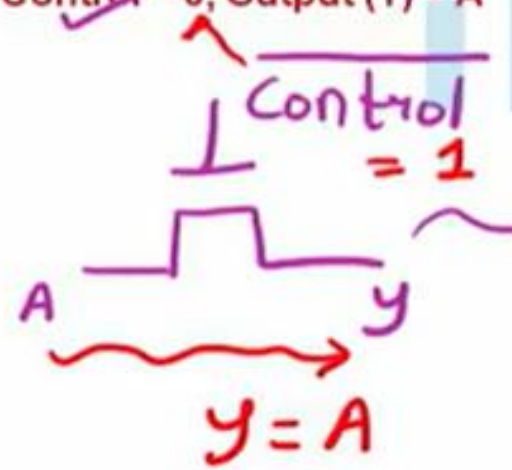
General Concept to implement circuits using Pass Transistor and Transmission Gates

NMOS (PT)

Control = 1, Output (Y) = A

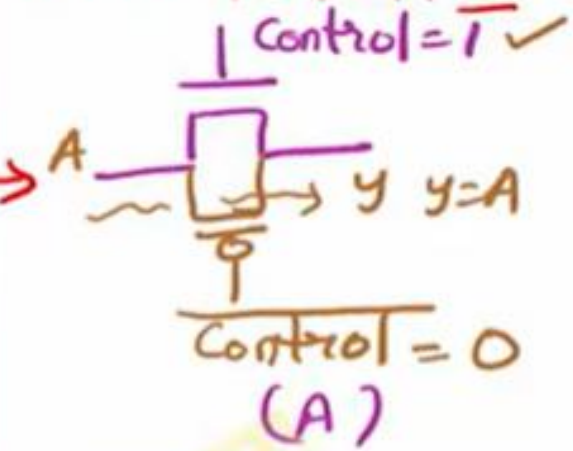


Control = 0, Output (Y) = A



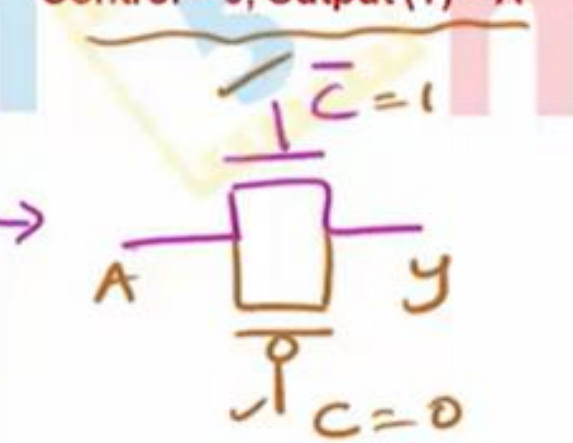
TG

Control = 1, Output (Y) = A



(A)

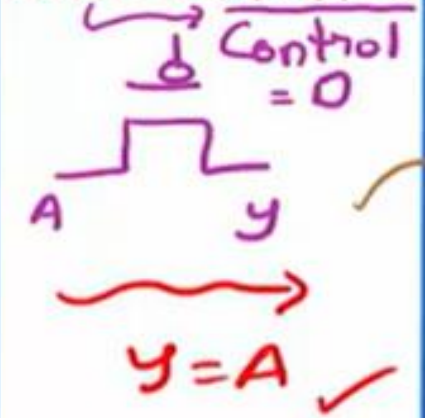
Control = 0, Output (Y) = A



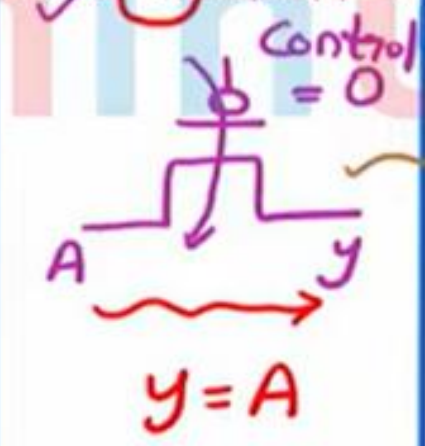
(C)

PMOS (PT)

Control = 1, Output (Y) = A

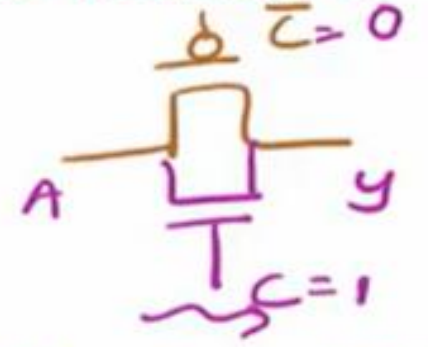


Control = 0, Output (Y) = A



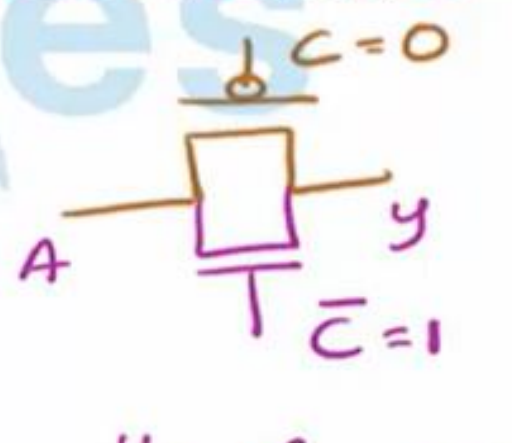
TG

Control = 1, Output (Y) = A



(B)

Control = 0, Output (Y) = A



(D)

Implementation of a 2 input Nand and Nor gate using Pass transistor and Transmission Gates

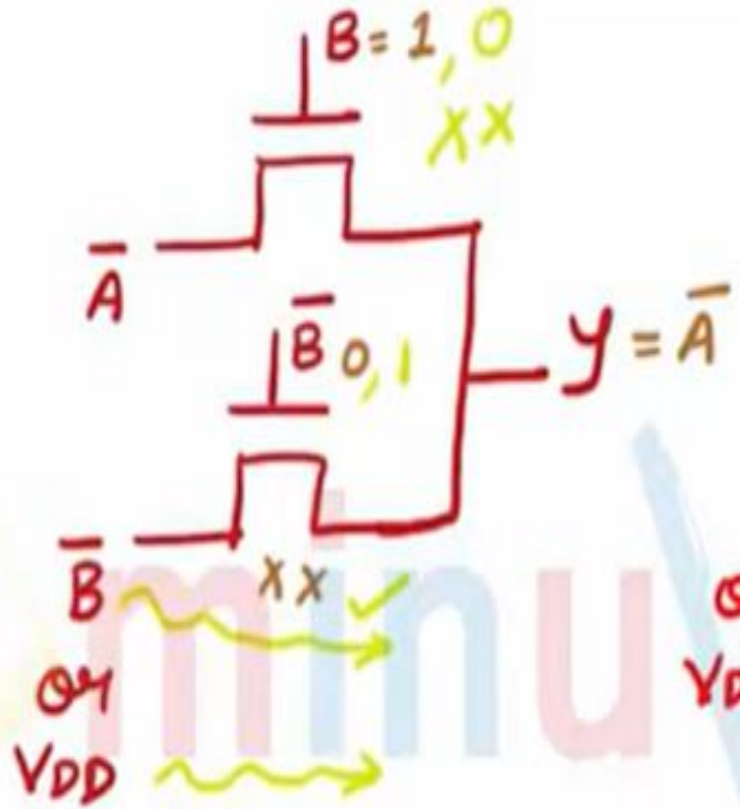
a) 2 i/p NAND Gate:

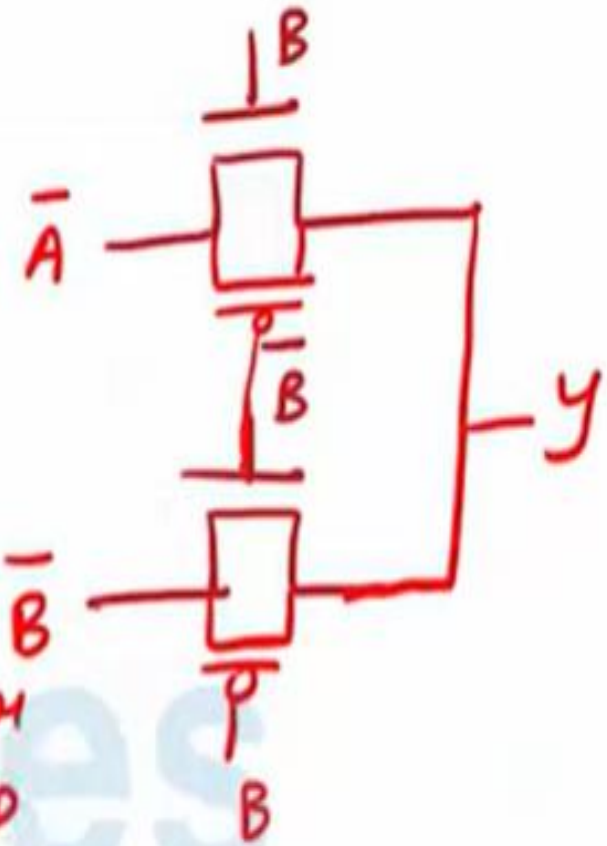
A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

B = 1; $Y = \bar{A}$

B = 0; $Y = \bar{B}$;

$Y = V_{DD}$





Implementation of 2 input NOR gate using Pass Transistor and Transmission Gates

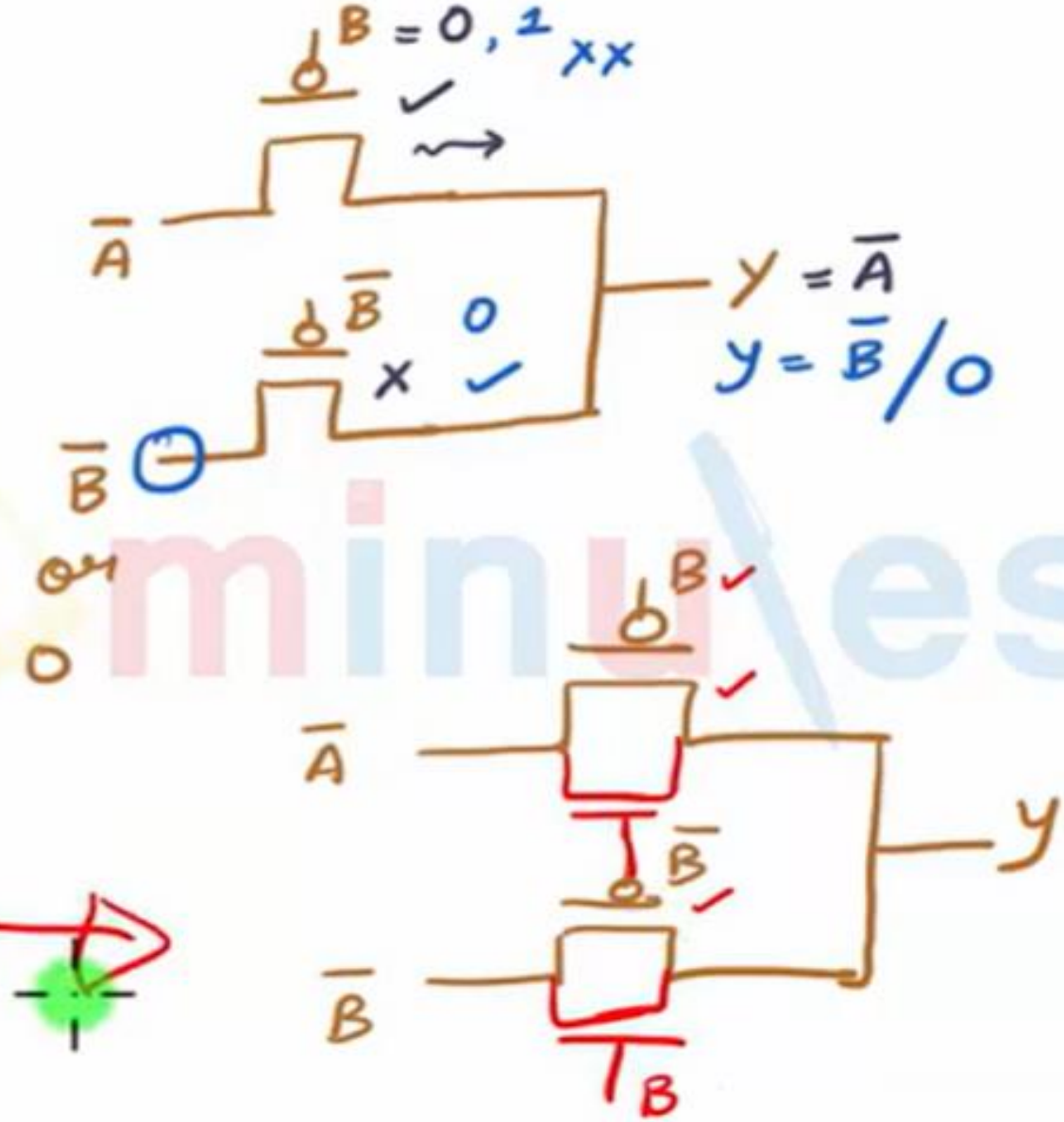
a) 2 i/p NOR gate

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

i/p B = 0, $y = \bar{A}$;

B = 1, $\bar{B} = 0$, $y = \bar{B}$;

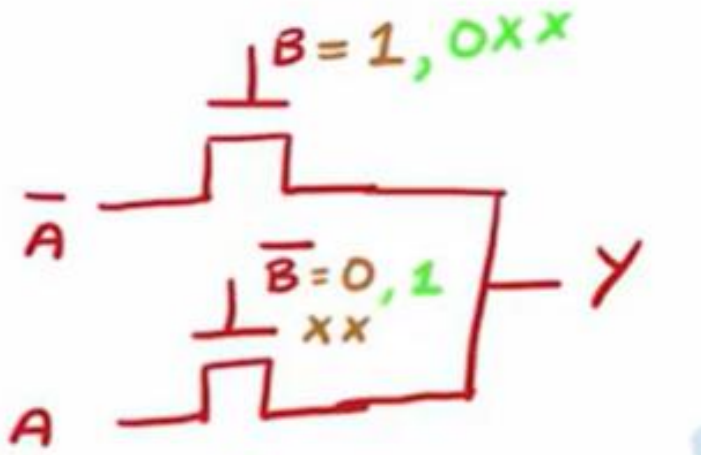
B = 1, y = GND(0)



Implementation of 2 input Ex-OR Gate and Ex- NOR Gate using Pass transistors and Transmission Gates

a) 2 i/p Ex-OR

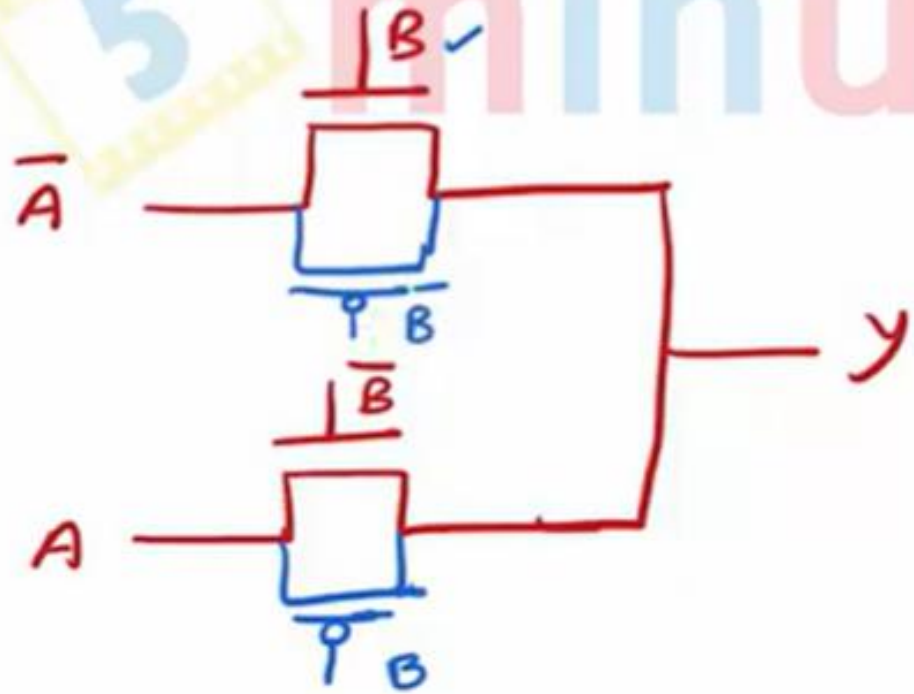
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



B = 1, $Y = \bar{A}$

B = 0, $\bar{B}$ = 1, $Y = A$

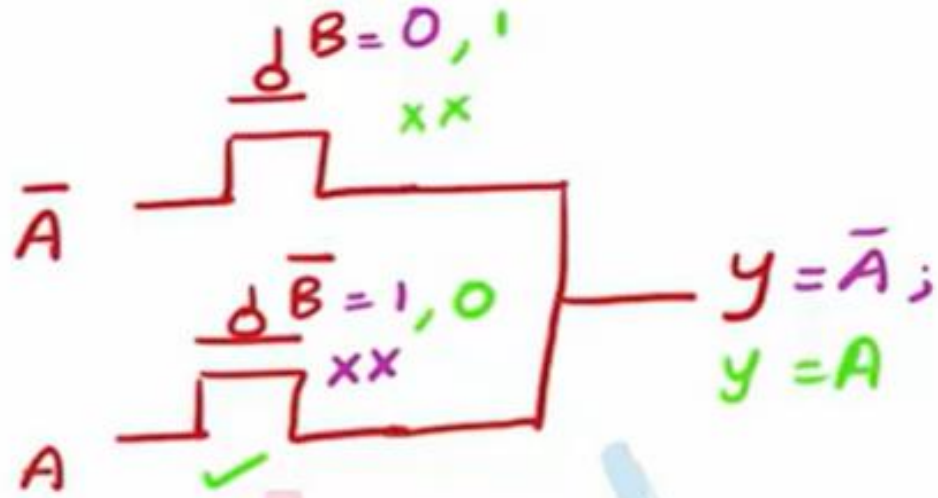
(NMOS PT)

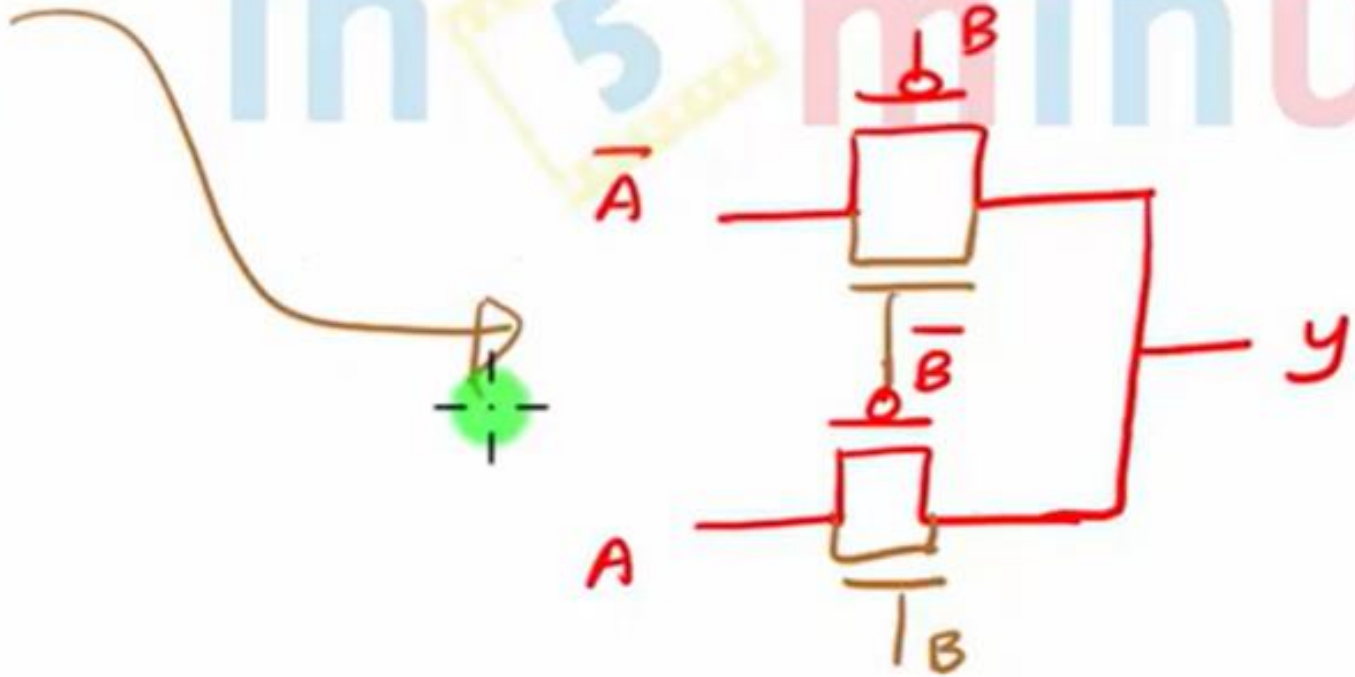


Implementation of 2 input Ex-OR Gate and Ex- NOR Gate using Pass transistors and Transmission Gates

b) 2 i/p Ex-NOR

A	B	y
0	0 ✓	1
0	1 ✓	0 ✓
1	0 ✓	0
1	1 ✓	1 ✓





Implementation of 2:1 muliplexer using Pass Transistor and Tranmission Gates

$$Y = \overline{S}A + S\overline{B}$$

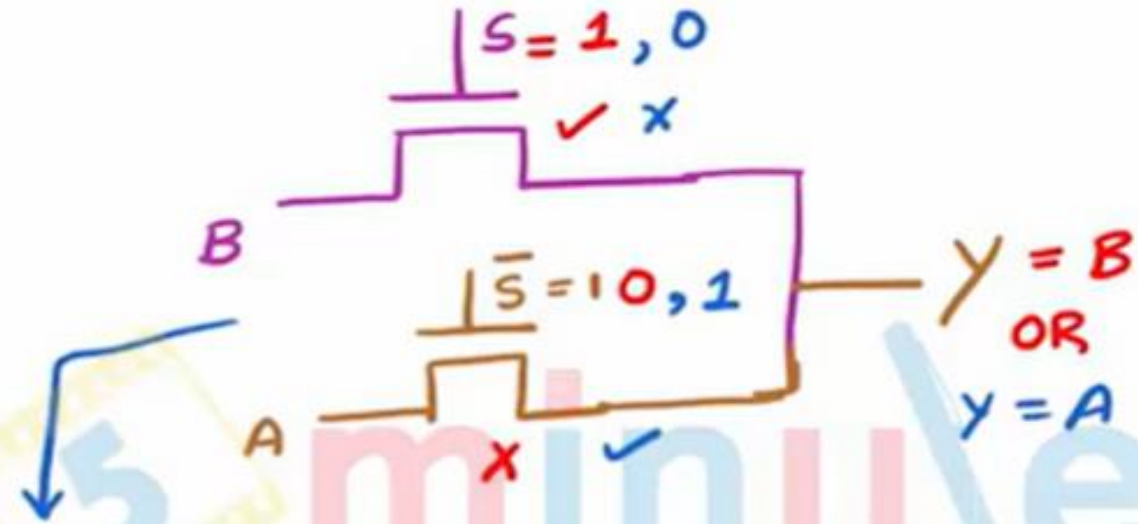
(1) (0)

OR

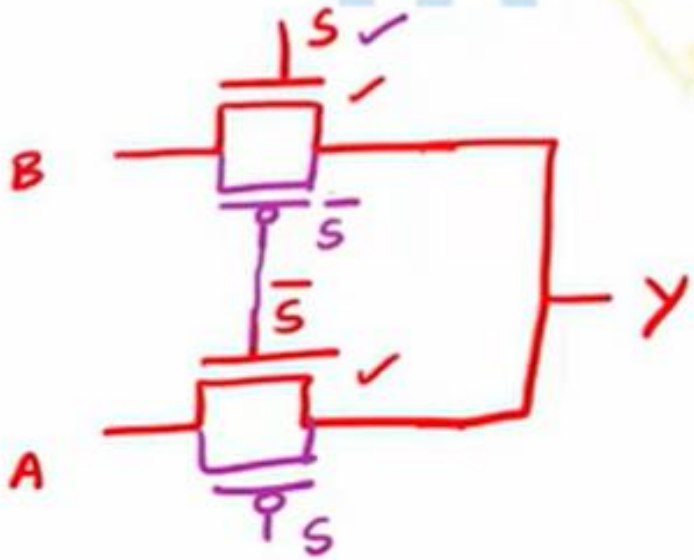
$S = 0, \overline{S} = 1; Y = A$

$S = 1, Y = B$

NMOS Pass trans



2:1 mux



2:1 mux using TG

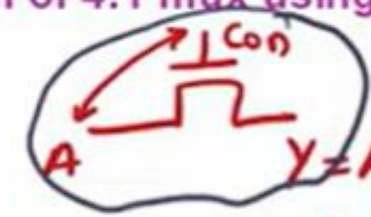
Implementation of 4:1 mux using Pass Transistor and Tranmission Gates

I/P data lines: D_0, D_1, D_2, D_3

Control signal : S_0, S_1

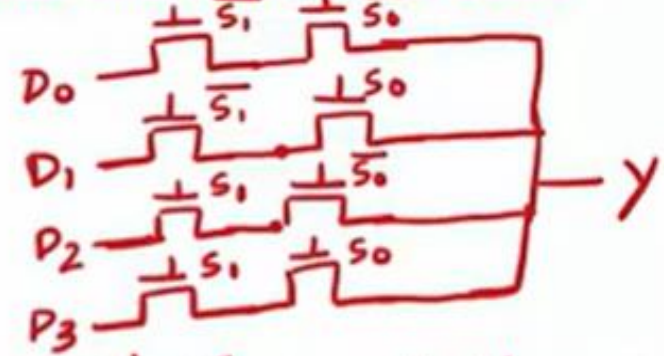
Multiplexed output : Y

$Y = \bar{S}_1\bar{S}_0 D_0 + \bar{S}_1 S_0 D_1 + S_1 \bar{S}_0 D_2 + S_1 S_0 D_3$ ①



$Y = A.\text{Control}$

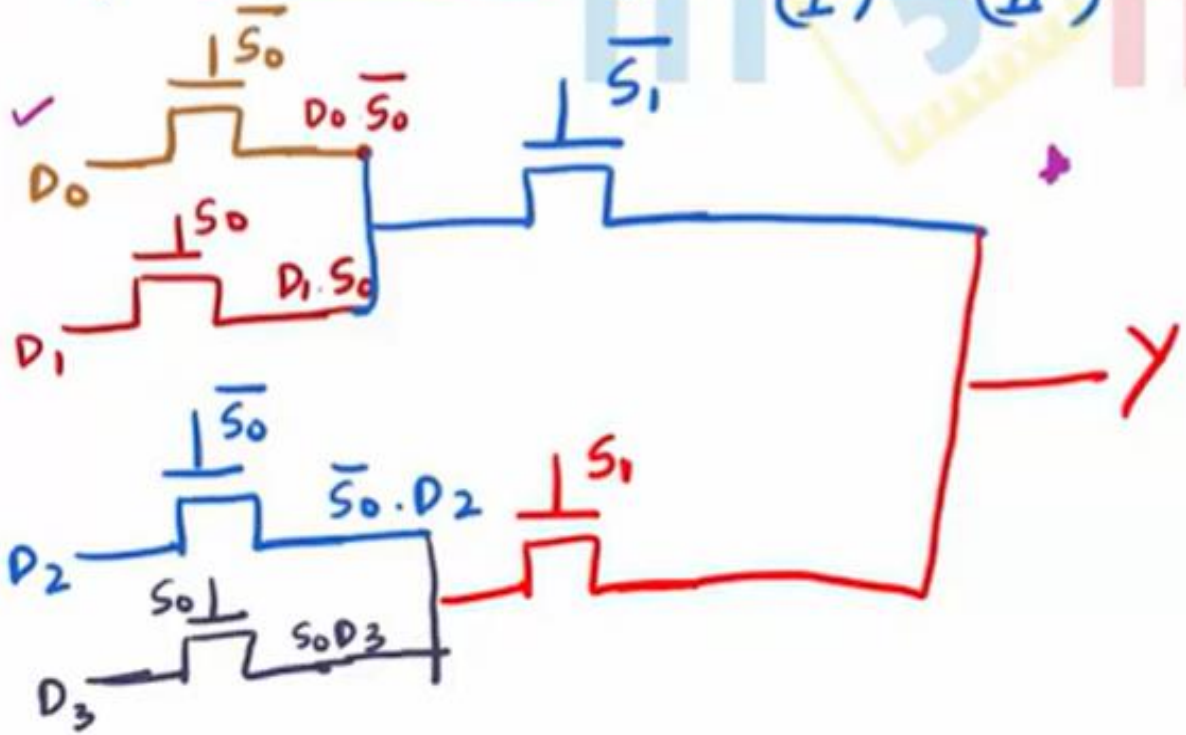
$= A.1$

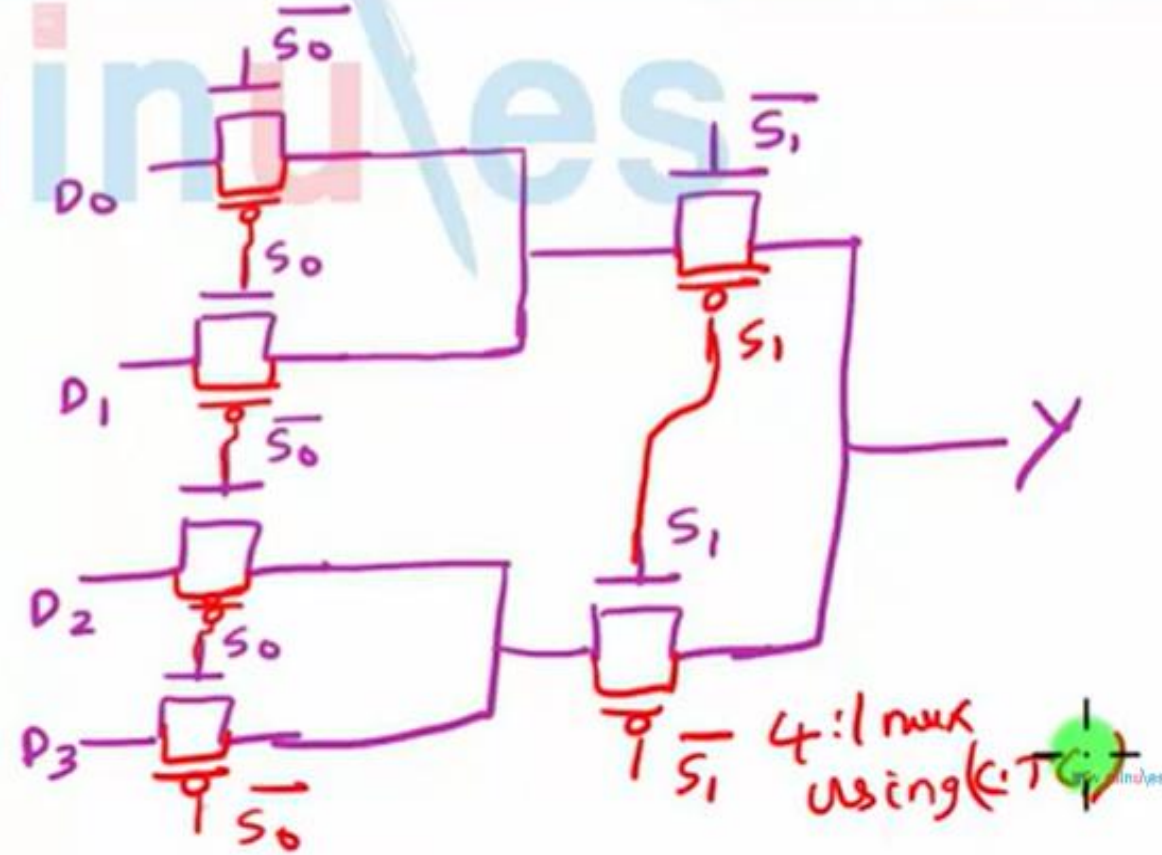


8 transistors 4:1 mux PT(N)

$Y = \left(\bar{S}_1.(\bar{S}_0 D_0 + S_0 D_1)\right) + \left(S_1.(\bar{S}_0 D_2 + S_0 D_3)\right)$

(I) (II)

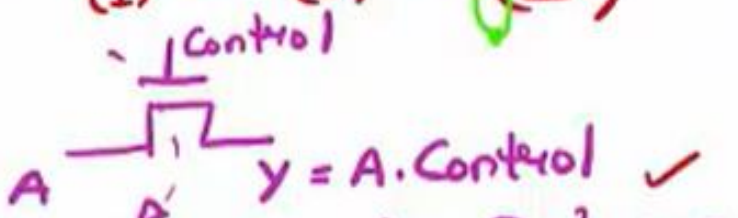


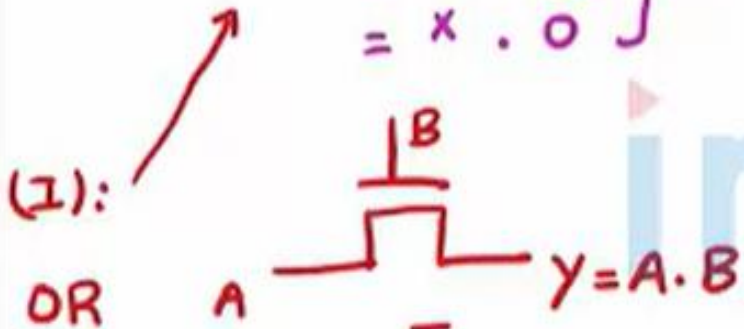


Realize the following Boolean expression using CMOS Transmission Gate design style

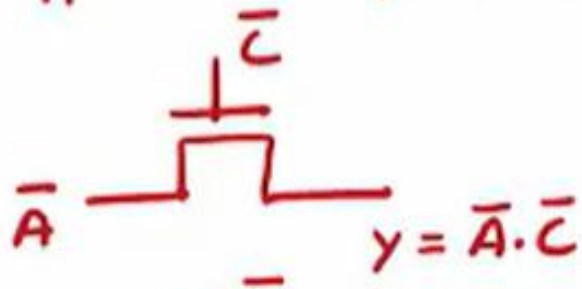
$Y = AB + \bar{A}\bar{C} + A\bar{B}C$

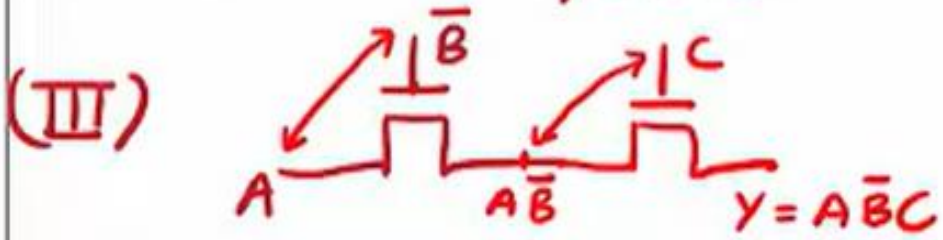
(I) (II) (III)

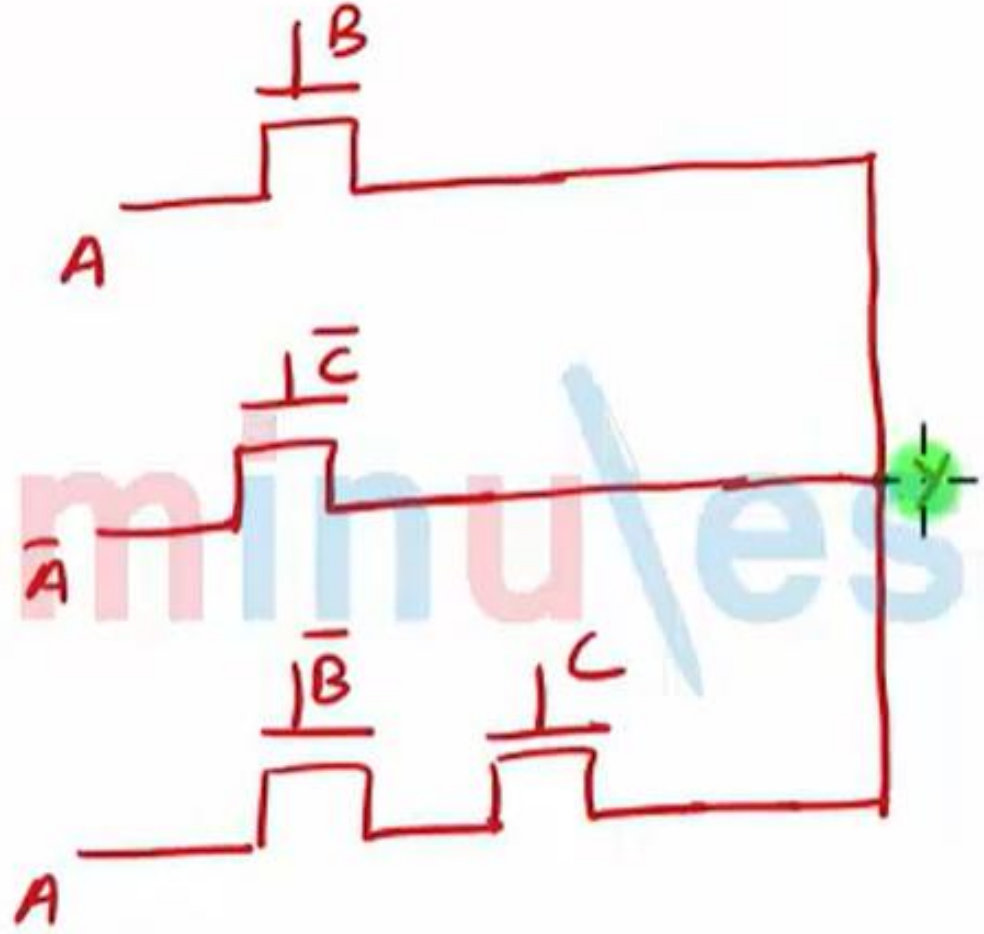


(I): 

OR

(II) 

(III) 



Realize the following Boolean expression using CMOS Transmission Gate design style

$Y = \underbrace{AB}_{(I)} + \underbrace{\bar{A}\bar{C}}_{(II)} + \underbrace{A\bar{B}C}_{(III)}$

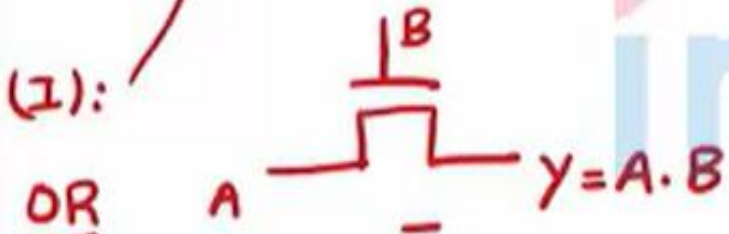
Control

A — y = A.Control ✓

= A (1) } AND

= x . 0 }

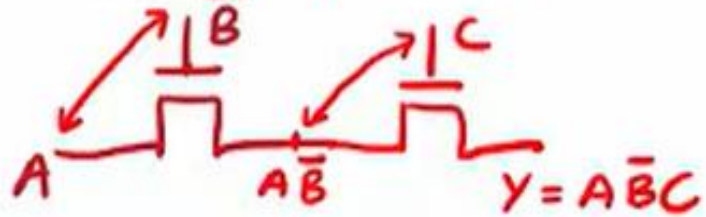
(I):

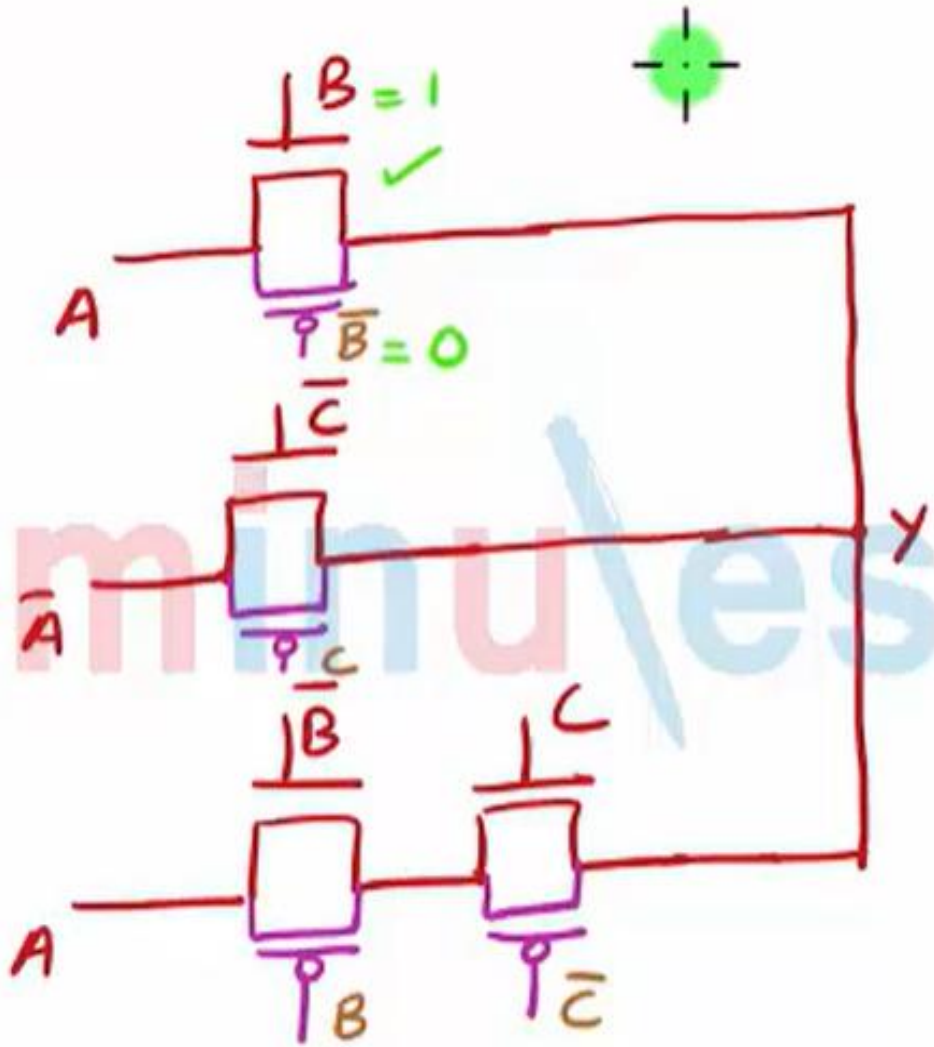


OR

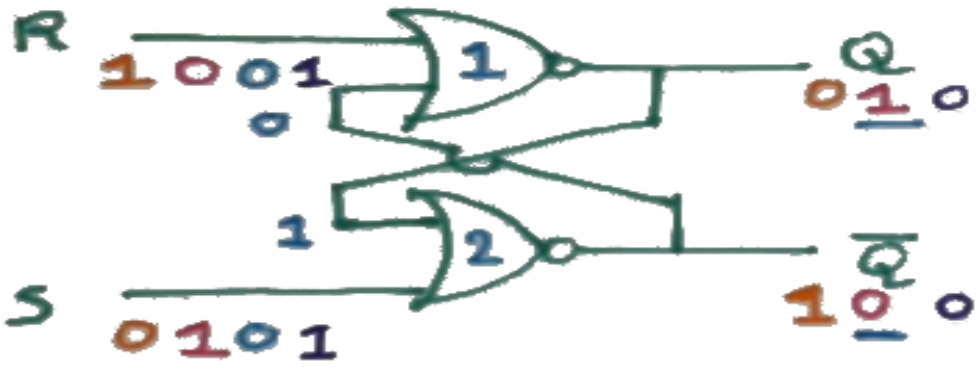
(II)

(III)



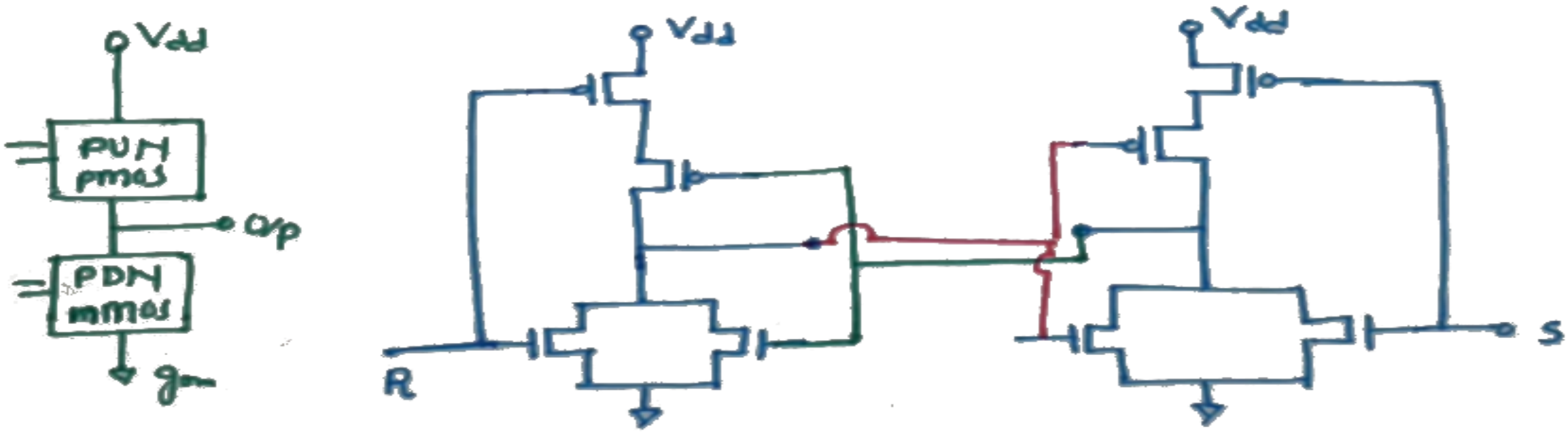


SR LATCH CMOS



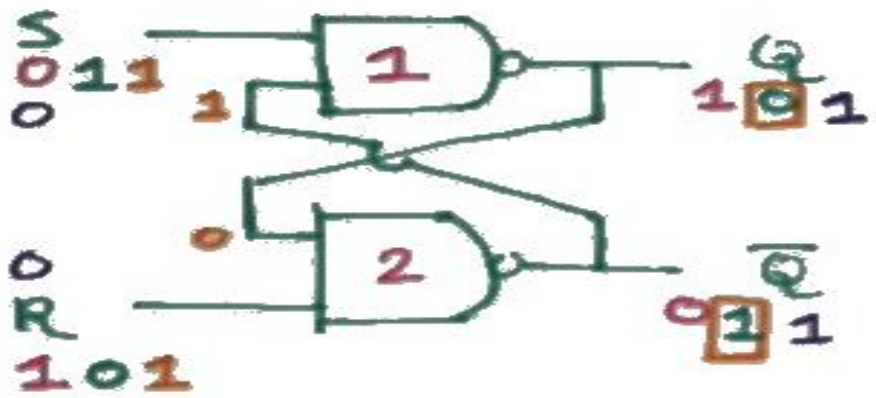
S	R	Q	$\overline{Q}$	Operation
0	0	mem		Hold
0	1	0	1	Reset
1	0	1	0	Set
1	1	0	0	Not allowed

→ (+) Operation → Pmos - Source → NMOS - Parallel



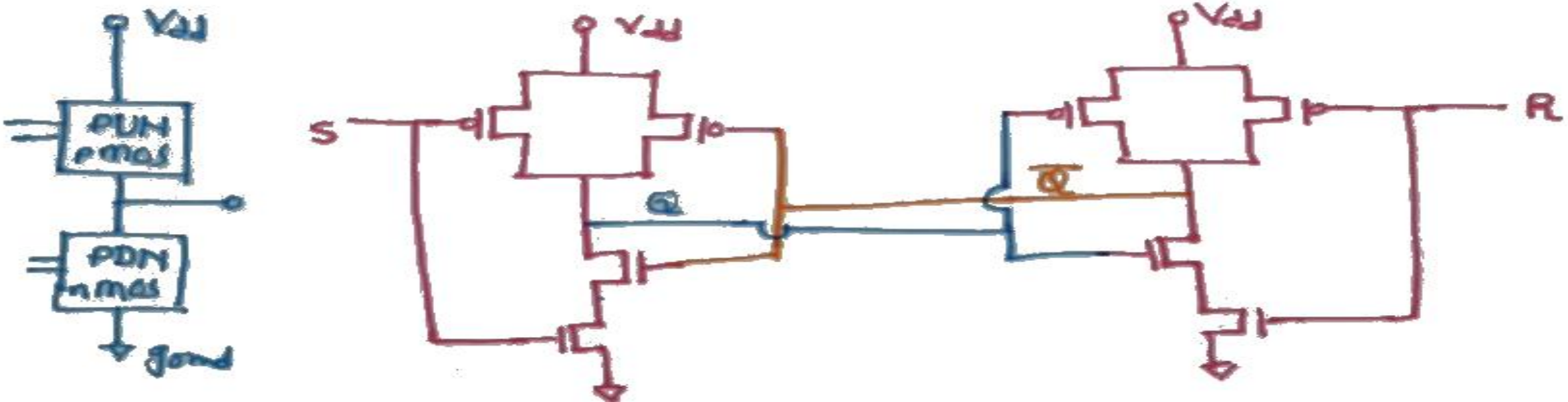
SR LATCH CMOS

CMOS SR latch using NAND gates

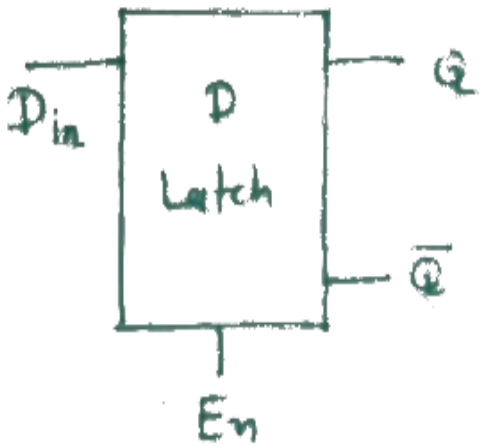


S	R	Q	$\bar{Q}$	Operation
0	0	1	1	Invalid
0	1	1	0	Set
1	0	0	1	Reset
1	1	Mem		Hold

→ (·) Operation → Pmos - Parallel → nmos - Series

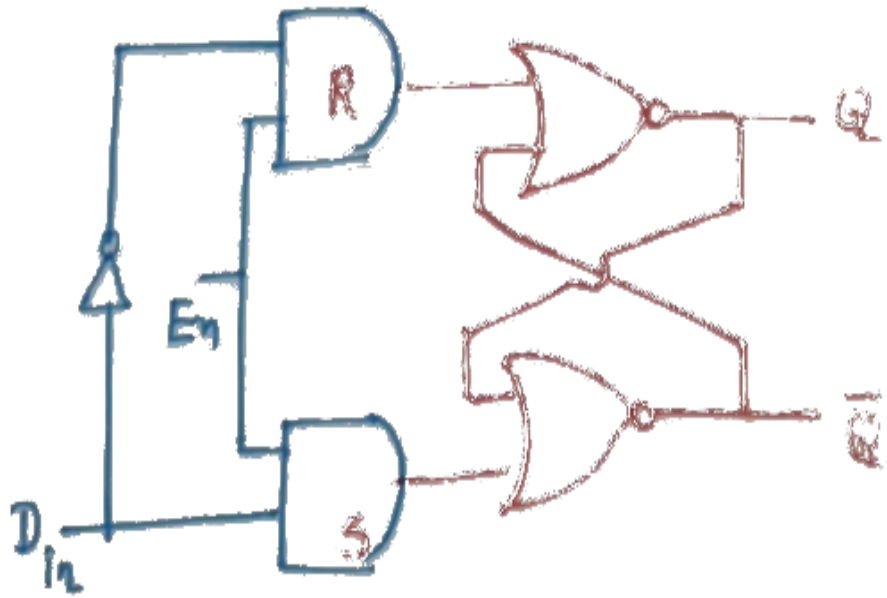


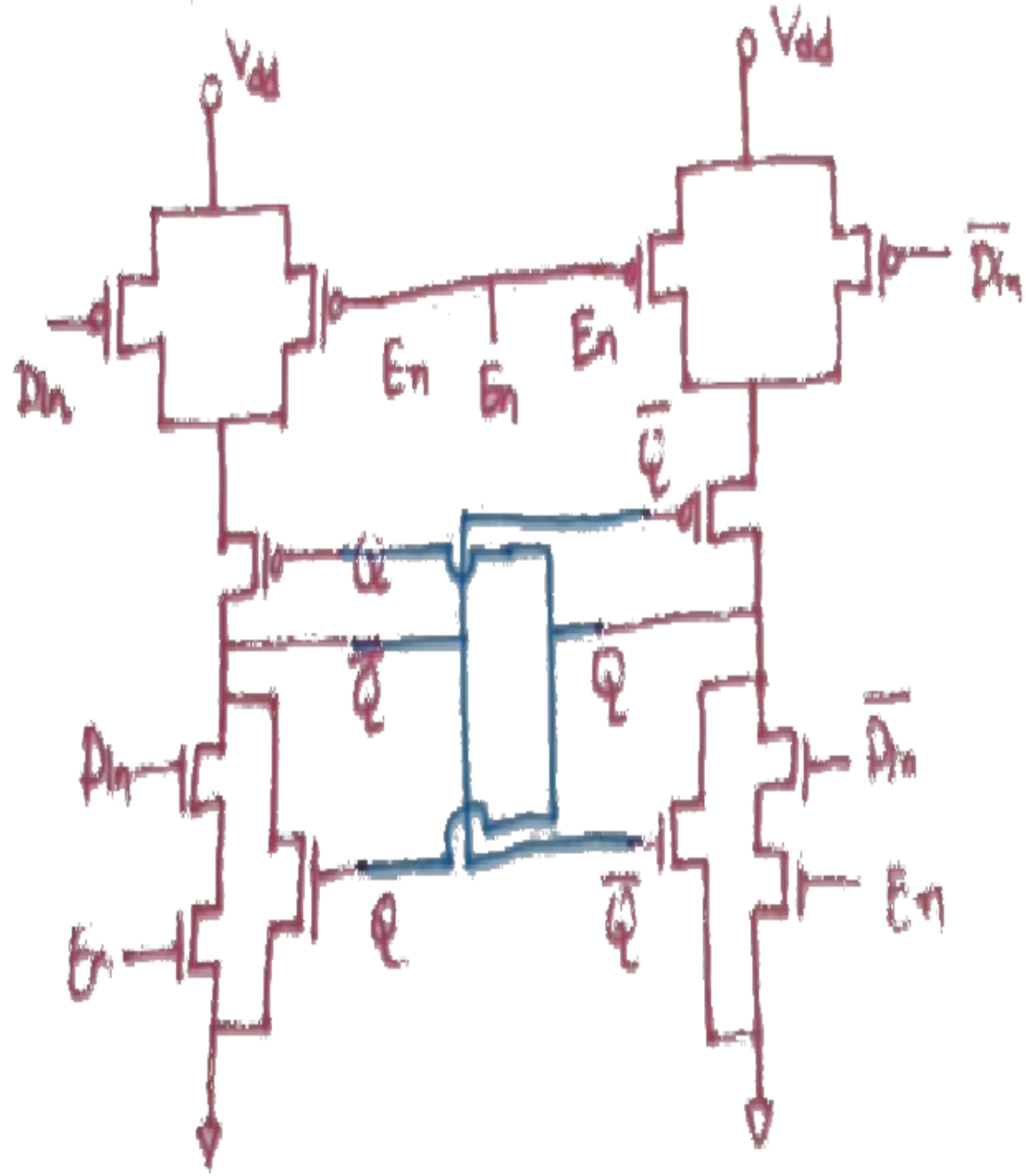
CMOS D Latch



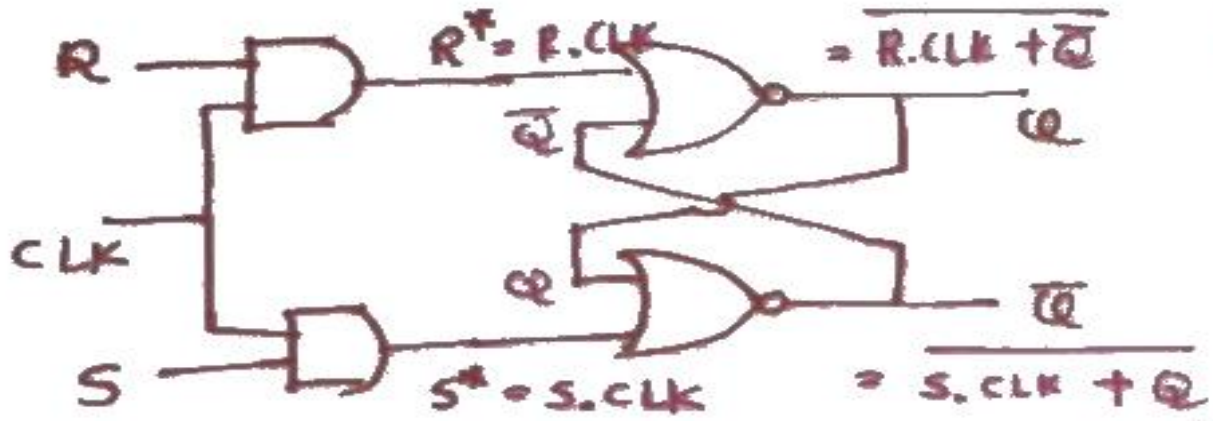
→ If En = 1, Q = D_{in}

→ If En = 0, Q = memory

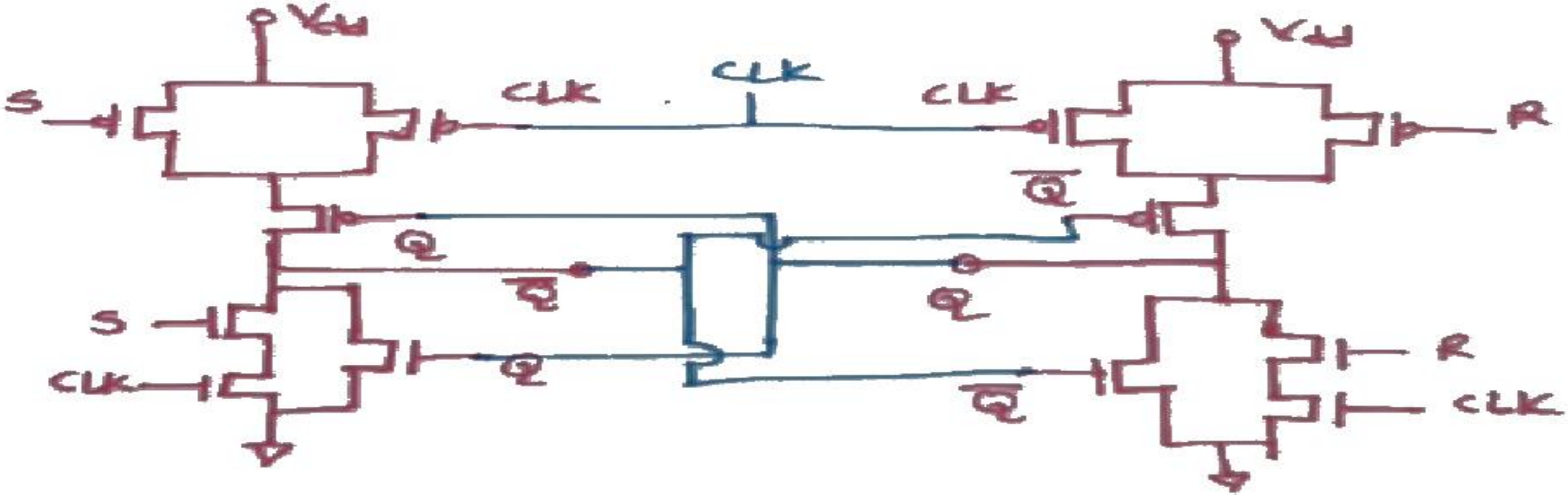




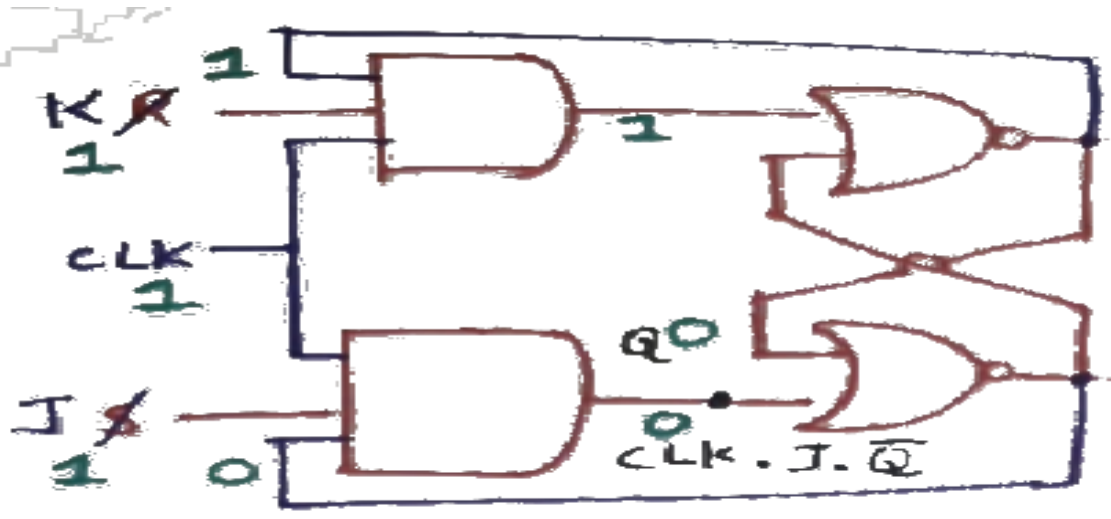
SR FF CMOS



CLK	S	R	Q	$\overline{Q}$	Operation
0	X	X	Qn	$\overline{Q}_n$	Hold
1	0	0	Qn	$\overline{Q}_n$	Hold
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	0	0	Invalid

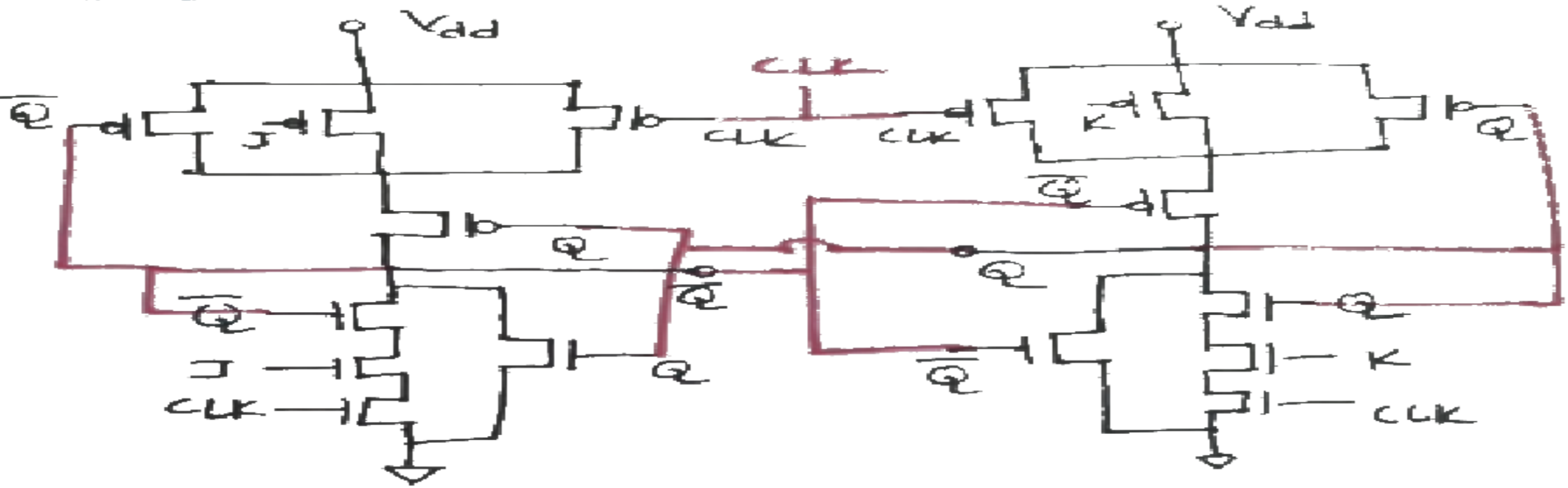


JK FF CMOS



CLK	J	K	Q	$\overline{Q}$
0	X	X	no change	
1	0	0	no change	
1	0	1	0	1
1	1	0	1	0
1	1	1		

$= CLK \cdot J \cdot \overline{Q} + Q$



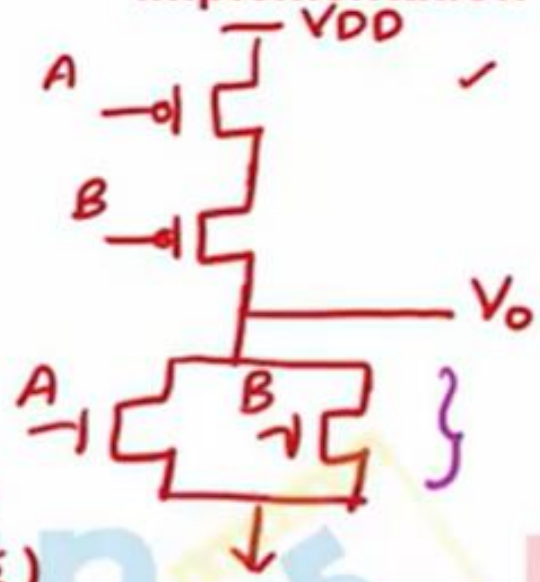
Implementation of 2 input Nor Gate in different Styles

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$\bar{A}B + A\bar{B} + AB + AB$

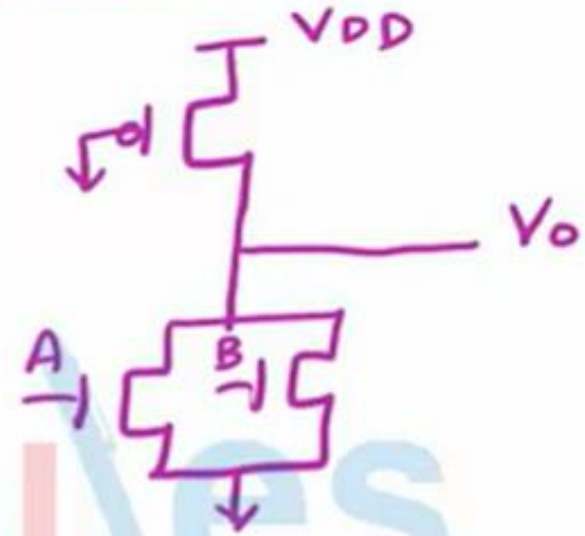
$= B(A+\bar{A}) + A(B+\bar{B})$

$= B + A$ //

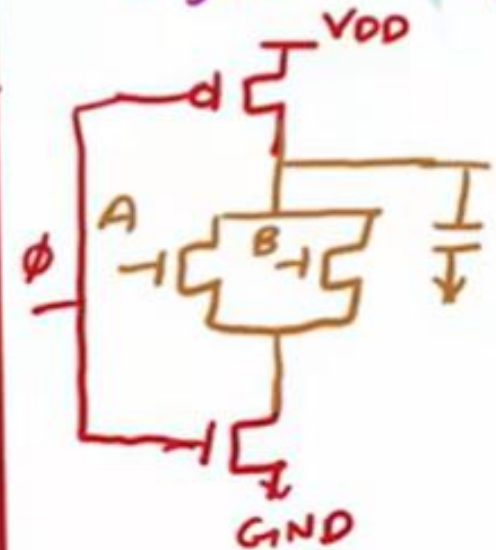


Static

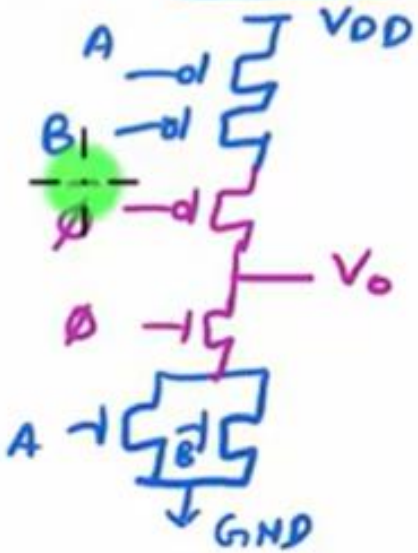
Pseudo NMOS



Dynamic style



C²MOS



$Y = \overline{A+B}$

$A + B$