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# VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

## Continuous Assessment Test I – March 2024

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|---|---|---|---|---|---|
| Programme | : | B. Tech (ECE/ECM) | Semester | : | WS 2023-24 |
| Course | : | VLSI System Design | Code | : | BECE303L |
| | | | Class Nbr. | : | CH2023240501057 |
| Faculty | : | Dr. Manikandan.P | Slot | : | F2+TF2 |
| Time | : | 90 Minutes | Max. Marks | : | 50 |

**Answer ALL the questions (5*10=50)**

**Assume and justify if any data is missing.**

| Q.No. | Sub. Sec. | Questions | Marks |
|---|---|---|---|
| 1. | | Sketch a color-coded stick diagram for the circuit that implements the Boolean function below;<br>$F = \overline{[(XYZ + P(Q+R)]}$<br>Use Euler's methods organize the layout so that the transistors can be implemented on a continuous strip of active. | 10 |
| 2. | | Consider the circuit illustrated in Fig.1. Calculate the propagation delay $\tau_{pd}$ at the output node Y for $R = 0$ and $\infty$. Assume $\left(\frac{W}{L}\right)_1 = \frac{4\,\mu m}{1\,\mu m}, \left(\frac{W}{L}\right)_{2-3} = \frac{1\,\mu m}{1\,\mu m}, C = 10\,pF$, $\mu_n C_{ox} = 100\,\frac{\mu A}{V^2}$, $\mu_p C_{ox} = 50\,\frac{\mu A}{V^2}$, $V_{THN} = 1\,V$, $V_{THP} = -1\,V, \lambda_N = \lambda_P = 0$, $\gamma_N = \gamma_P = 0$, $V_{DD} = 3\,V$. | 10 |

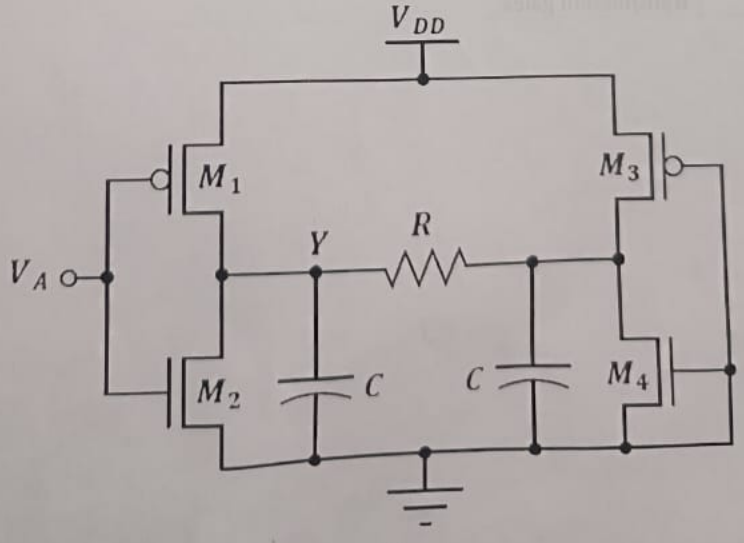


Fig. 1



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(i) Determine the minimum delay of the path from A to B in the circuit depicted in Fig. 2. Size the gates (X, Y) in order to achieve this delay using two different load capacitors: $C_L = 25$ **(5 Marks).**

(ii) Calculate the ratio of NMOS and PMOS in each stage, considering their (W/L) ratios, for the load capacitances mentioned in (i) **(5 Marks).**

**10**

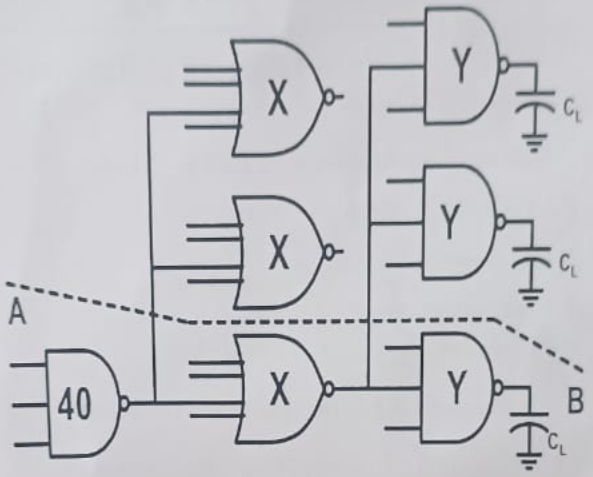


Fig. 2

Implement the Boolean expression using pass transistor logic;

$$Y = \overline{(AB) + (CDE) + F}$$
$$K = \overline{X(M + N) + PQ}$$

**10**

Design a logical circuit featuring three inputs and two outputs that adheres to the following conditions:

- When all inputs are at logic 0, both outputs should also be at logic 0.
- When any single input is at logic 1, at least one of the outputs should be at logic 1.
- When any two inputs are at logic 1, at least one of the outputs should be at logic 1.
- When all inputs are at logic 1, both outputs should be at logic 1.

Identify the type of circuit that meets these requirements and implement it using transmission gates.

**10**