Reg. No.:

Name :

VIT

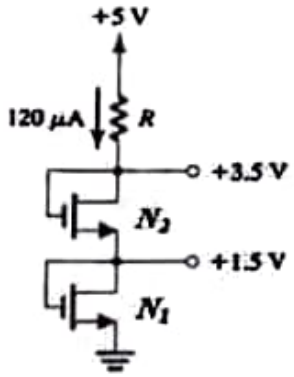
Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test I – January 2023

Programme	:	B. Tech (ECM)	Semester	:	WS 2022-23
Course	:	VLSI System Design	Code	:	BECE303L
			Class Nbr	:	CH2022235001205 CH2022235001207 CH2022235001212 CH2022235001213
Faculty	:	Dr Ananiah Durai S, Dr Lakshmi Priya G, Dr Ravi Sankar A, Dr Sakthivel. S M	Slot	:	B1+TB1
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		A VLSI design engineer develops a graphical processing unit for multimedia applications. For the above application, discuss the impact of different VLSI design styles on the cycle time and the achievable performance metrics. Also, briefly elaborate on the list of steps involved in the VLSI design flow for the above design.	10
2.		The circuit in Figure 1 shows NMOS transistors with a threshold voltage of 1 V, $\mu_n C_{ox}$ = 120μA/V², λ = 0, and lengths of 1 μm each. Find the device width and the respective value of R for both N_1 and N_2 to obtain the voltage and current values indicated.  **Figure 1**	10
3.	(i)	Sketch the MOS capacitance (C_G) variation if the gate voltage (V_G) is ramped slowly, from accumulation condition to depletion and then to inversion. Also, discuss with relevant capacitances expression on the dependency of C_G variation with semiconductor capacitance (C_S) for accumulation, depletion, and inversion conditions. **(5 marks)**	10

4.	(ii) How does the velocity saturation limit I_{DSat}? For a very short channel length, discuss the I_{DSat} dependency parameters. **(5 marks)** (i) With a neat circuit diagram, describe the voltage transfer characteristics (VTC) of a CMOS inverter. Mark the different regions in the VTC and comment on the operating mode (i.e., linear or saturation) of NMOS and PMOS transistors. **(3 marks)** (ii) Write the drain current expressions of transistors in regions 2, 3, and 4 of the VTC in terms of V_{IN}, V_{DD} and V_{OUT}. **(3 marks)** (iii)Derive the expression for V_{IT}, i.e., input transition voltage, also called switching threshold. If the NMOS width is increased four times for the fixed PMOS width, what will happen to the Input Transition Voltage (V_{IT}) of the inverter? Assume the threshold voltage of both transistors is the same. **(4 Marks)**	**10**
5.	Implement the following logic functions using static CMOS logic style; i) $f = \overline{[B.(A+C)] + (D.E)}$ ii) $f = \overline{R + S + (T.U)}$ Size the transistors for the worst-case delay of RC of an inverter with a load capacitance of C. Assume $\mu_N = 3\ \mu_P$ for the first logic function and $\mu_N = 2.5\ \mu_P$ for the second logic function.	**10**

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