Reg. No.:

Name :

VIT

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

Continuous Assessment Test I – May 2023

Programme	:	B.Tech (ECE/ECM)	Semester	:	FIS 2022-23
Course	:	VLSI System Design	Code	:	BECE303L
			Slot	:	A1+TA1
Faculty	:	Dr. BISWAJIT JENA Dr. PRASHANTH KUMAR B Dr. SAKTHIVEL S M Dr. RAVI SANKAR A Dr. VELMATHI G	Class Nbr	:	CH2022232500108 CH2022232500107 CH2022232500106 CH2022232500315 CH2022232500109
Time	:	90 Minutes	Max. Marks	:	50

Answer ALL the questions

Q.No.	Sub. Sec.	Questions	Marks
1.		Discuss the key components and design considerations involved in VLSI design and propose an application scenario where the Y chart methodology can effectively optimize the design process. Justify your selection of the application and explain how the Y chart can contribute to its successful implementation.	[10]
2.		For an NMOS transistor with W/L=16μm/0.8μm, t_{ox} =15 nm, μ_n = 500 cm^2/V-S, V_{TN}=0.7 V, ε_r=3.9, and ε_0=8.854 x 10^{-14} F.cm^{-1},	[10]
	(a)	Find C_{ox} and K_n'.	
	(b)	Calculate the values of V_{GS} and V_{DSMIN} needed to operate the transistor in the saturation region with a DC current, I_{DS} = 100 μA.	
	(c)	For the given parameters of the MOSFET, find the value of V_{GS} required to cause the device to operate as a 1000-ohms resistor for a very small V_{DS}.	
3.		Define channel length modulation in a MOS device. Briefly explain the impact of higher drain bias ($V_{DS} \geq V_{DS\_Sat}$) on the channel of MOSFET.	[5]
4.		For a CMOS inverter, let V_{TN} = 0.4 V = $\|V_{TP}\|$, $K_n = K_p$ = 80 μA/V^2, and V_{DD} = 3.3 V.	[10]
	(a)	Evaluate input and output transition voltages (i.e., V_{IT}, V_{OTN}, and V_{OTP})	
	(b)	Evaluate input voltage V_I when output voltage V_O = 0.4 V.	
	(c)	Evaluate output voltage V_O when input voltage V_I = 1.41 V.	
5.		Consider the following statements: Output X will be equal to A when control inputs B and C are the same. X will remain HIGH when B and C are different.	[10]

i) Construct a truth table and fill out the values for input variables A, B, and C and the output X.

ii) Write the Boolean equation that satisfies the above statements.

iii) Design a static CMOS circuit and size the PMOS and NMOS transistors so that the maximum delay is less than RC. Construct an RC equivalent network for the static CMOS circuit.

Implement a simple NAND-based SR latch using static-CMOS logic style. [5]

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