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Vellore Institute of Technology

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Reg. No. : 22BLC1282

Final Assessment Test (FAT) - May 2024

Programme	B.Tech.	Semester	WINTER SEMESTER 2023 - 24
Course Title	VLSI SYSTEM DESIGN	Course Code	BECE303L
Faculty Name	Prof. Sasipriya P	Slot	F1+TF1
		Class Nbr	CH2023240503205
Time	3 Hours	Max. Marks	100

General Instructions:

- Write only Register Number in the Question Paper where space is provided (right-side at the top) & do not write any other details.

Answer all questions (10 X 10 Marks = 100 Marks)

01. a) A VLSI design engineer has designed a novel ARM processor that is suitable for smartphones. What is the design style he may prefer to fabricate a processor IC? Justify your answer. (5 Marks) [10]

b) Write briefly about the MOS structure capacitance and identify their distribution across the different operating regions of the MOS transistor. (5 Marks)

02. A set of I-V characteristics for an nMOS transistor at room temperature for different biasing conditions is shown in Table 1. Using the data, find: (a) the threshold voltage (V_t and V_{t0}). (b) electron mobility for an n-channel MOS transistor with C_{ox}=7X 10^{-8} F/cm^2 , W= 20 mm L= 2 mm and $2\Phi F = 0.7$ V operated in the saturated region. [10]

Table 1

V_{GS} (V)	V_{DS} (V)	V_{SB} (V)	I_D (μA)
4	4	0.0	256
5	5	0.0	441
4	4	2.6	144
5	5	2.6	256

03. Consider the CMOS circuit depicted in Fig. 1(a). Draw a plot of the current I versus the input voltage V_{in} (I vs Vin) (b) Determine the maximum current (I_{max}). Assume $(W/L)_1 = 4$ μm/1 μm , $(W/L)_2$=1 μm/1 μm, $\mu_n C_{ox}$=100 μA/V^2,$\mu_p C_{ox}$=50 μA/V^2,V_{THN}= 1V, V_{THP}= -1V, $\lambda_N = \lambda_P = 0$. [10]

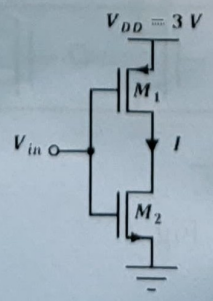


Fig. 1

04. a) Draw the transistor level schematic of a NAND gate-based SR flip flop and explain its operation with the truth table. (6 Marks) [10]

b) Consider the CMOS complex gate illustrated in Fig. 2. (i) Draw the RC equivalent circuit when all n-channel MOSFETs are on. (ii) Determine the fall time for case (i)Take C=100 fF, and ignore all of the MOS and PMOS capacitors. Assume the unit CMOS inverter's NMOS has an aspect ratio of $(W/L)_N = 1/1$ with an equivalent resistance of R=10 kΩ. (4 Marks)

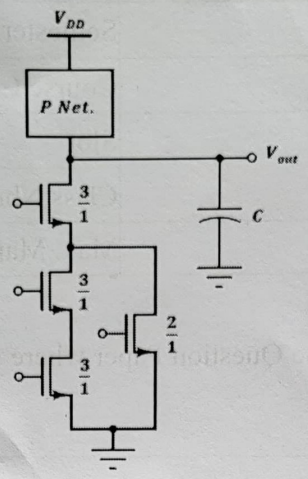


Fig. 2

05. Implement the boolean expressions given below using static CMOS logic and draw the stick diagram. Use Euler's method to organize the layout so that the transistors can be implemented on a continuous strip of active layer. [10]

$$Y = \overline{X(Y+Z)+P.Q}$$

06. Size the circuit in Fig. 3 for minimum delay. Assume that the load is 20 μF and the inverter has 10 μF of gate capacitance. [10]

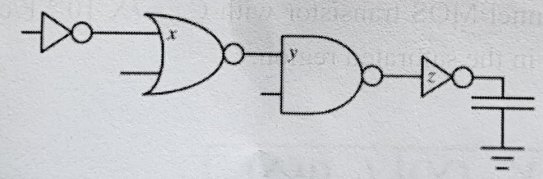


Fig. 3

07. Consider the following Pseudo-NMOS Logic circuit shown in Fig. 4. a) What is the logic value of the output voltage if only one input is high? If all four inputs are high? (5 Marks) [10]

b) What is the average static power consumption if, at any time, each input turns on with an (independent) probability of 0.5 and 0.1? (5 Marks)

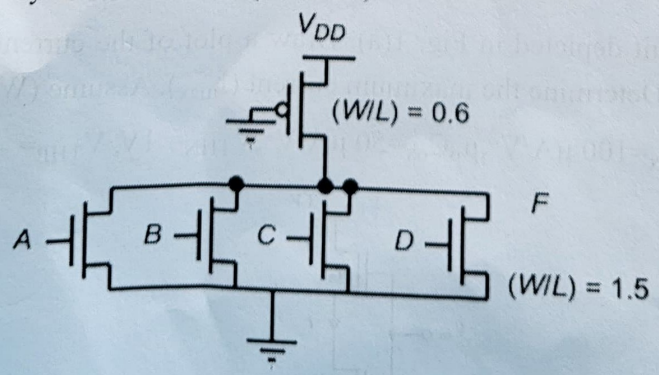


Fig. 4

08. Consider the Pass Transistor Logic and Level Restoration circuit of the following Fig. 5. Assume the inverter switches ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitance. Assume the device parameters are; V_{DD} = 2.5 V, $(W/L)_1$ = 0.5 μm/0.25 μm, $(W/L)_2$ = 1.5 μm/0.25 μm, $(W/L)_{n1\text{-}2}$ = 0.5 μm/0.25 μm, kn' = 115 μA/V², kp' = -30 μA/V², V_{tN} = 0.43 V, V_{tP} = -0.4 V. [10]

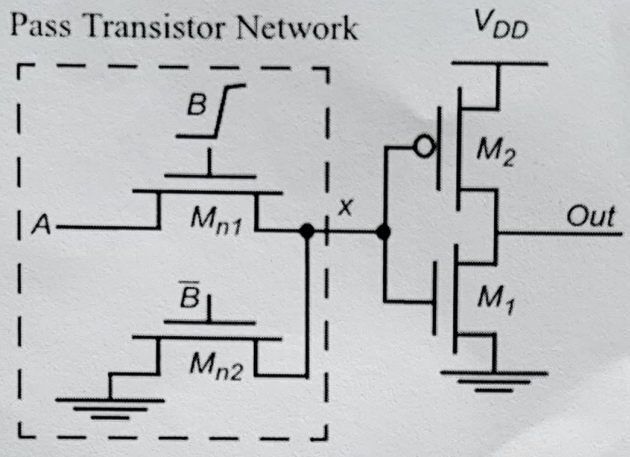


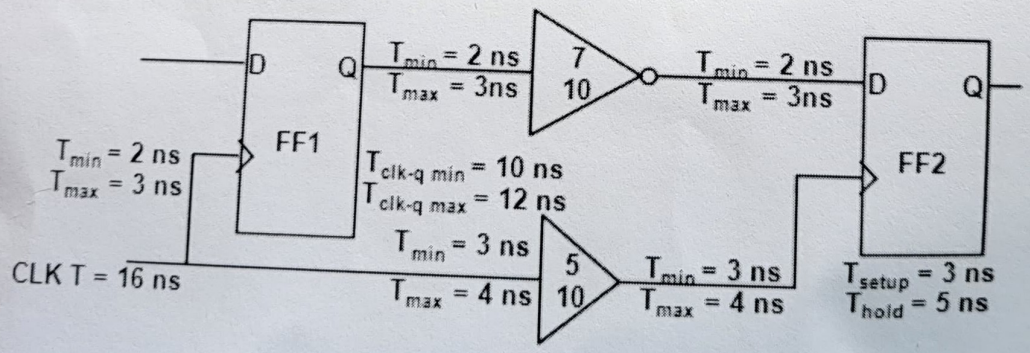
Fig. 5

a)What is the logic function performed by this circuit? Explain why this circuit has non-zero static dissipation. (3 Marks)

b) Using only 1 transistor after the node x, redesign to fix the static power dissipation with proper sizing. Also implement the circuit using transmission gates. (3 Marks)

c) Replace the pass-transistor network in the Fig. 5 with a pass transistor network that computes the following function: x = ABC at the node x. Assume to have the true and complementary versions of the three inputs A, B and C. (4 Marks)

09. a) For the given RTL circuit, check whether any Setup Violation or Hold Violation is there, if so, kindly suggest a measure to rectify it. (5 Marks) [10]



b) With a neat sketch of the waveform, elaborate the Hold Time calculation for an RTL circuit with Launch FF & Latch FF. (5 Marks)

10. Explain how a write operation is conducted in a 6-transistor CMOS SRAM cell with a clear, annotated illustrations. Furthermore, discuss the methodology for sizing the transistors to maintain adequate write stability during the operation. [10]

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