Short Syllabus

BECE303L VLSI System Design (3-0-0-3)

VLSI Design Overview and MOSFET Theory - Concepts of Regularity, Modularity and Locality; CMOS Logic gates - CMOS Sequential Logic Design, Latches and Flip Flops; CMOS Fabrication and Layout - CMOS Process Technology, Layout Design Rule; CMOS Circuits Performance Analysis - Logical Effort and Transistor Sizing; CMOS Logic Families - Transmission Gates based Logic Design; Timing Analysis - Introduction to Static timing analysis; Semiconductor Memory Design- Introduction and types.

Course Code	Course Title	L	T	P	C
BECE303L	VLSI System Design	3	0	0	3
Pre-requisite	BECE204L, BECE204P	Syllabus version			
		1.0			

Course Objectives :

1. To introduce the basic concepts and techniques of modern integrated circuit design.
2. Describe the fundamental principles underlying digital design using CMOS logic and analyze the performance characteristics of these digital circuits.
3. Verify that a design meets its functionality, timing constraints, both manually and through the use of computer-aided design tools.

Course Outcomes :

Students will be able to

1. Analyze the CMOS digital electronics circuits, including logic components and their interconnect using mathematical methods and circuit analysis models
2. Create models of moderately sized CMOS inverters with specified noise margin and propagation delay.
3. Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect.
4. Analyse the various logic families and efficient techniques at circuit level for improving power and speed of combinational and sequential logic.
5. Implement the CMOS digital circuits with the specified timing constraints.
6. Design memories with efficient architectures to improve access times, power consumption

Module:1	VLSI Design Overview and MOSFET Theory	8 hours

VLSI Design Flow, Design Hierarchy, Concepts of Regularity, Modularity and Locality, VLSI Design Styles, Design Quality, MOSFET : Device Structure, Electrical behaviour of MOS transistors, Capacitance- Voltage Characteristics and Non-ideal Effects; Effects of scaling on MOSFETs and Interconnects.

Module:2	CMOS Logic Gates	8 hours

CMOS Inverter: DC Transfer Characteristics, Static and Dynamic Behaviour, CMOS Basic Gates, Compound Gates, CMOS Sequential Logic Design – Latches and Flip Flops

Module:3	CMOS Fabrication and Layout	5 hours

CMOS Process Technology N-well, P-well Process, latch up in CMOS technology, Stick Diagram for Boolean Functions using Euler Theorem, Layout Design Rule

Module:4	CMOS Circuits Performance Analysis	5 hours

Delay Estimation, Logical Effort and Transistor Sizing, Performance Estimation - Static & Dynamic Power Dissipation.

Module:5	CMOS Logic Families	8 hours

Pass Transistor Logic, Transmission Gates based Logic Design, pseudo NMOS, Cascode Voltage Switch Logic Dynamic and domino logic, clocked CMOS (C^2MOS) logic and np – CMOS logic.

Module:6	Timing Analysis	4 hours

Introduction to Static timing analysis, Setup Time, Hold Time, calculation of critical path, slack, setup and hold time violations.

Module:7	Semiconductor Memory Design	5 hours

Introduction, Types - Read-Only Memory (ROM) Circuits, Static Read-Write Memory (SRAM) and Dynamic Read-Write Memory (DRAM) Circuits.		
Module:8	**Contemporary issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)	
1.	Neil H.Weste, Harris, A. Banerjee, CMOS VLSI Design, A circuits and System Perspective, 2015, 4th Edition, Pearson Education, Noida, India.
Reference Book	
1.	Jan M. Rabaey, Anantha Chadrakasan, Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective Paperback, 2016, 2rd Edition, Pearson Education, India.
2.	Sung-Mo Kang, Yusuf Liblebici, Chulwoo Kim, CMOS Digital Integrated Circuits: Analysis and Design, 2019, Revised 4th Edition, Tata Mc Graw Hill, New Delhi, India.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	14-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022