VIT Reg. No. :

Final Assessment Test (FAT) - APRIL/MAY 2023

Programme	**B.Tech**	Semester	**Winter Semester 2022-23**
Course Title	**VLSI SYSTEM DESIGN**	Course Code	**BECE303L**
Faculty Name	**Prof. Ananiah Durai S**	Slot	**B1+TB1**
		Class Nbr	**CH2022235001207**
Time	**3 Hours**	Max. Marks	**100**

Section A (9 X 10 Marks)
Answer All questions

01. a) Derive an expression for the drain current of an N-channel enhancement type MOSFET from the first principles. Draw the transfer and output I-V characteristics of the transistor. **(7 Marks)** [10]
b) From the drain current expression at the saturation region, comment on how to increase the current for a fixed gate-to-source voltage. **(3 Marks)**

02. Consider the NMOS transistor in a 0.65 μm process with W/L = 1.95/0.65. In this process, the gate oxide thickness is 11 nm, and the mobility of electrons is 350 $cm^2/V.s$. The threshold voltage is 0.75 V. Plot I_{ds} vs. V_{ds} for V_{gs} = 0, 1, 2, 3, 4, and 5 V. Assume five different V_{ds} values to get smooth I_{ds}. [10]

03. A positive edge-triggered register on a Master-Slave configuration is shown in Figure 1. Implement the same using transmission gates. Briefly explain how the 'clock load per transistor' can be reduced using a modified diagram **(7+3 Marks)** [10]

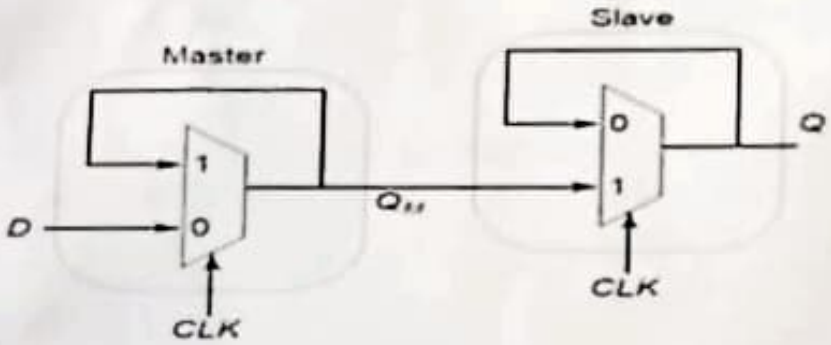

Figure 1

04. An NMOS inverter with a saturated load is shown in Figure 2. Draw the cross-sectional diagram of the same. With neat sketches, explain the fabrication process flow of the device using a self-aligned poly-gate process. We know that a typical fabrication of a CMOS inverter requires 6 photo masks. How many masks will be required to realize this inverter? Assume either positive or negative tone photo-resist. Does the inverter fabrication require a 'p-well,' 'n-well,' or 'twin-well' process? Comment on the same. **Note: You may ignore the bulk diffusion and consider only 3-terminals for FETs.** [10]

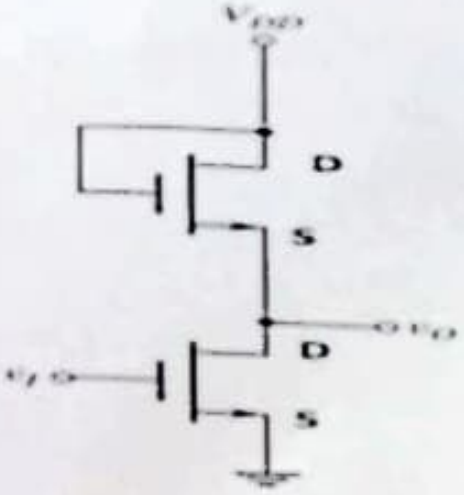

Figure 2

05. Estimate the minimum delay of the path from A to B in Figure 3 and the transistor sizes (X, Y) to achieve this delay. Also, determine the ratio of NMOS and PMOS in each stage with respect to their (W/L) ratios. **[10]**

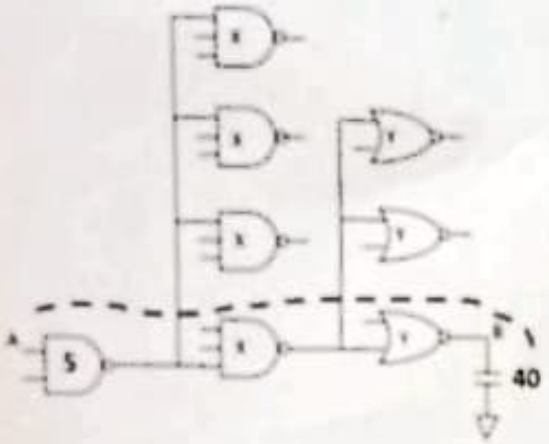

Figure 3

06. Implement the following Boolean logic function using static CMOS logic style, and size the transistors for the worst-case delay of RC of an inverter with a load capacitance of C. Assume $\mu_n = 3\mu_P$ for F_1 & $\mu_n = 4\mu_P$ for F_2 during the sizing. **[10]**

(i) $F_1 = \overline{A(B+C) + D(E+F)}$ **(6 Marks)**

(ii) $F_2 = \overline{XY + Z}$ **(4 Marks)**

07. Compare the implementation of the following functions with Pseudo NMOS and domino logic, and determine the performances of the two in terms of power and delay. Also, comment on the transistor numbers. **[10]**

(i) $F_1 = \overline{(A+C).D(B+E)}$ **(5 Marks)**

(ii) $F_2 = \overline{(ABCD) + E}$ **(5 Marks)**

08. a) For the given circuit in Figure 4, calculate the timing for all the paths and then identify the path which violates the timing requirement based on the required arrival time. **(5 Marks)** **[10]**

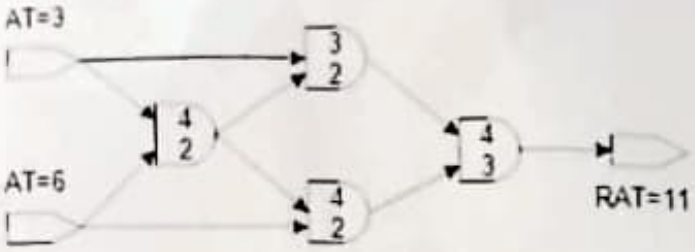

Figure 4

b) With a neat sketch of the waveform, elaborate the Setup Time & Hold time calculation for an RTL circuit with launch & Capture Flops. **(5 Marks)**

09. With neat sketches, explain how "read" and "write" operations are carried out in a CMOS 6T-SRAM cell. Write the conditions on sizing for proper "read" and "write" operations considering the 300 nm technology node. **[10]**

Section B (2 X 5 Marks)
Answer All questions

10. The circuit shown in Figure 5 is realized using Differential Cascode Voltage Switch Logic (DCVSL). Construct a truth table with the input variables A, B, C, and D and identify the function implemented by F and $\bar{F}$. **[5]**

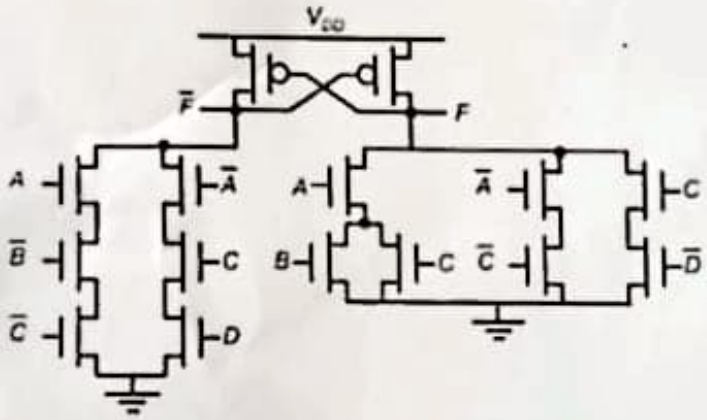

Figure 5

11. Enumerate the various stages that must be traversed throughout the physical design flow of an Integrated Circuit (IC) before the specifications can be taped out. **[5]**

OR

Discuss the various stages and challenges involved in the 'design to realization' of a MEMS microsensor system.