- When the incoming signal frequency is equal to the IF, the responses of H1f and H2f will be equal and so the voltages developed across R1 and R2 will be equal.
- From the way D1 and D2 are connected, terminals A and B will be at the same potential with respect to the ground and so E0, the potential difference between them is zero.
- If the incoming signal has a frequency above the IF, the response of will H2f will be more and that of H1f will be less (when compared to what it was when the incoming signal frequency was IF).
- Hence the voltage drop across R1, will be greater than the voltage drops across R2.
- Hence, terminal A will be at a higher potential than terminal B with respect to ground E0 ≠ 0.
- If the incoming signal has a frequency less than the IF, response H1f will be more than the response H2f, causing B to be at a higher potential than A.
- Thus, the frequency variations of the incoming FM signal are converted into corresponding variations in the amplitude of E0.
- Therefore, E0 will be the modulating signal assuming the overall response to be perfectly linear between f1 and f2.

Foster-Seeley Discriminator/ PHASE DISCRIMINATOR

Circuit::

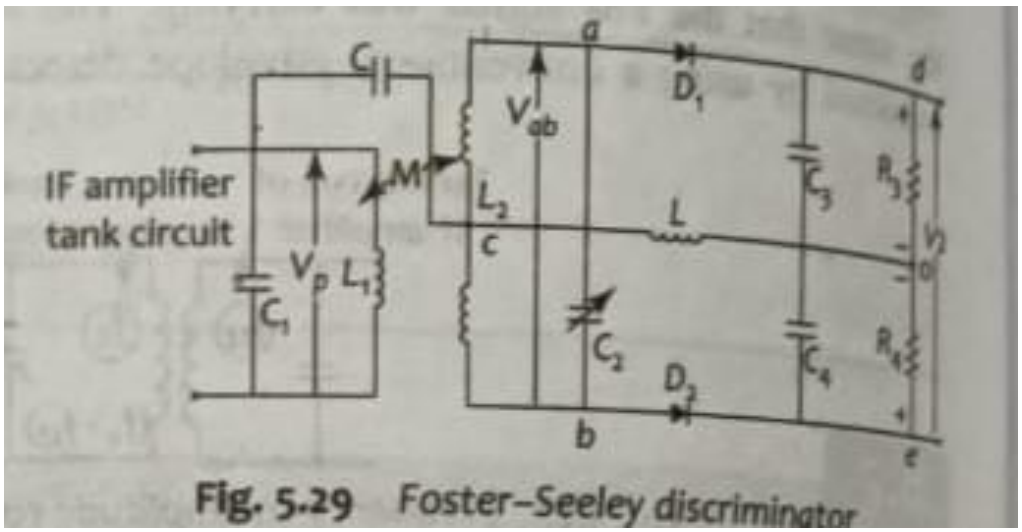

Fig. 5.29 Foster–Seeley discriminator

*Originally developed as a sub-system of an automatic frequency control unit, this FM detector is known as the Foster-Seeley discriminator, phase-shift discriminator, and centre-tuned discriminator.

*A tank circuit consisting of a centre-tapped inductance L_2 and capacitor C_2 is inductively coupled to the inductance L_1, of the tank-circuit of the IF stage.

*The diodes D_1, and D_2, and the elements R_3, C_3, and R_4, C_4, are connected to this secondary side tank circuit. Further, a large RF coupling capacitor C and a large RF choke are connected as shown in the circuit diagram.

*The primary and secondary tank circuits are tuned to the same frequency-the IF, which is the carrier frequency for the FM signal being fed to the discriminator. At the r.f., the circuit comprising C, L and C_4, is effectively coming across L_1.

*Since the reactance of the r.f. choke L far exceeds the reactances of C and C_4, the voltage across the choke L, say V, is practically equal to the voltage across the primary, i.e., Vp.

Therefore $V_L=V_p$

*If M is the mutual inductance between the primary and secondary windings, the voltage induced in the secondary, viz., Vs, is given by

$V=\pm j\omega M Ip$----(1)

*The direction of winding of the secondary determines whether the positive or the negative sign is to be used. Ip in Eq (1) above, denotes the current flowing through the primary winding L_1, and is given by

$Ip=Vp/j\omega L_1$ ----(2)

*While writing Eq. (2), we have assumed that the secondary side load impedance reflected into the primary, as well as the resistance of the primary

coil, are negligible, since the Q-factors of the primary and secondary are large and the mutual inductance M is small.

*Taking the negative sign in RHS of Eq. (1) and substituting in it for I, using Eq. (2), we get

$$V_s = -M * V_p / L_1$$

*This induced voltage V, produces a voltage drop Va, across the capacitor C_2 given by

$$V_{ab} = \frac{V_s(1/j\omega C_2)}{R_2 + j\omega L_2 + (1/j\omega C_2)} = \frac{MV_p}{L_1}\left[\frac{1}{\left\{\left(\frac{\omega}{\omega_c}\right)^2 - 1\right\} - j\omega C_2 R_2}\right]$$ -----(3)

*Hence, when the frequency f of the incoming FM signal is equal to the IF, i.e., f, then

$$V_{ab} = j\left[\frac{M}{L_1 \omega C_2 R_2}\right] V_p$$

ie, V leads V, by 90°.

*The voltage V_{ao} applied to diode D, is given by

$$V_{a0} = V_{ab}/2 + V_L = V_{ab}/2 + V_p$$

*The voltage V_{b0} applied to diode D, is given by

$$V_{bo} = -V_{ab}/2 + V_L = -V_{ab}/2 + V_p$$

*Hence, when f=fc, i.e., when there is no modulation for the incoming signal, the phasor diagram will be as shown in the diagrams.

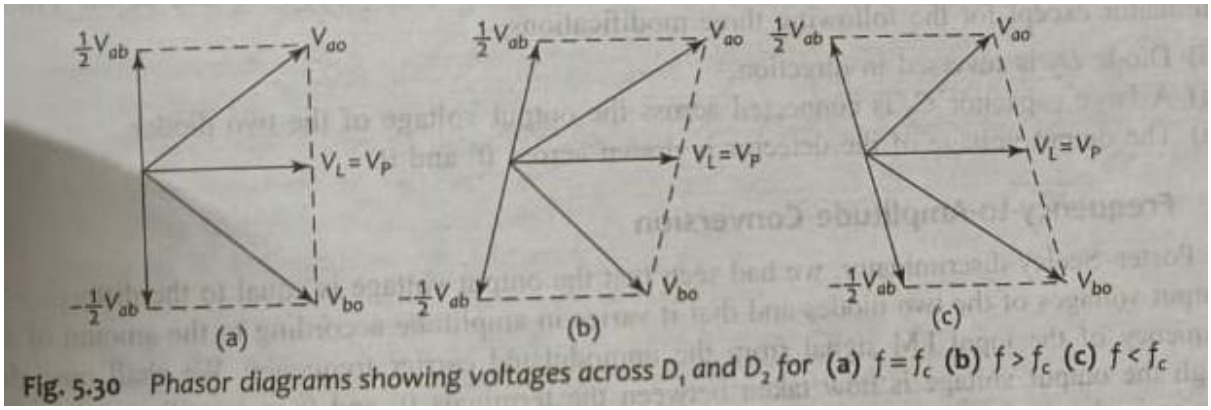

Fig. 5.30 Phasor diagrams showing voltages across D_1 and D_2 for (a) $f = f_c$ (b) $f > f_c$ (c) $f < f_c$

*Thus $V_{ao}=V_{bo}$ The diode D_1, charges capacitor C_3, and diode D_2 charges capacitor C_4. Neglecting the diode drops and assuming R_3C_3, and R_4C_4, to be large compared to (1/fc), we may say that C_3 and C_4 will be charged to the peak values of the voltage V_{a0} and Vb0, respectively. From the diagram, we find that when f=fc, $|V_{a0}|=|V_{b0}|$

*Hence, $V_{d0}=V_{e0}$ and therefore, : $V_2=0$

From Eq. (3), we find that the phasor diagrams for f>fc, and f<fc, will be as shown in Figs and that

(i) For f>fc : $|V_{a0}|>|V_{b0}|$. Therefore V_2 is positive and equal to $|V_{a0}|-|V_{b0}|$

(ii) For f<fc : $|V_{a0}|<|V_{b0}|$. Therefore V_2 is negative and equal in magnitude to $|V_{b0}|-|V_{a0}|$

*For the Foster-Seeley discriminator, if we plot the frequency response around fc, we will get the S-shaped curve and the frequency-to-amplitude conversion is fairly linear if the discriminator is properly designed.

*However, this discriminator responds to amplitude variations also. Hence, if this discriminator is used, it must be preceded by a limiter stage.

RATIO DETECTOR