6.1 T Junction resistive divider

Module:6 Microwave Passive circuits

Course: BECE305L – Antenna and Microwave Engineering

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Assistant Professor - SENSE

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Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
CHENNAI

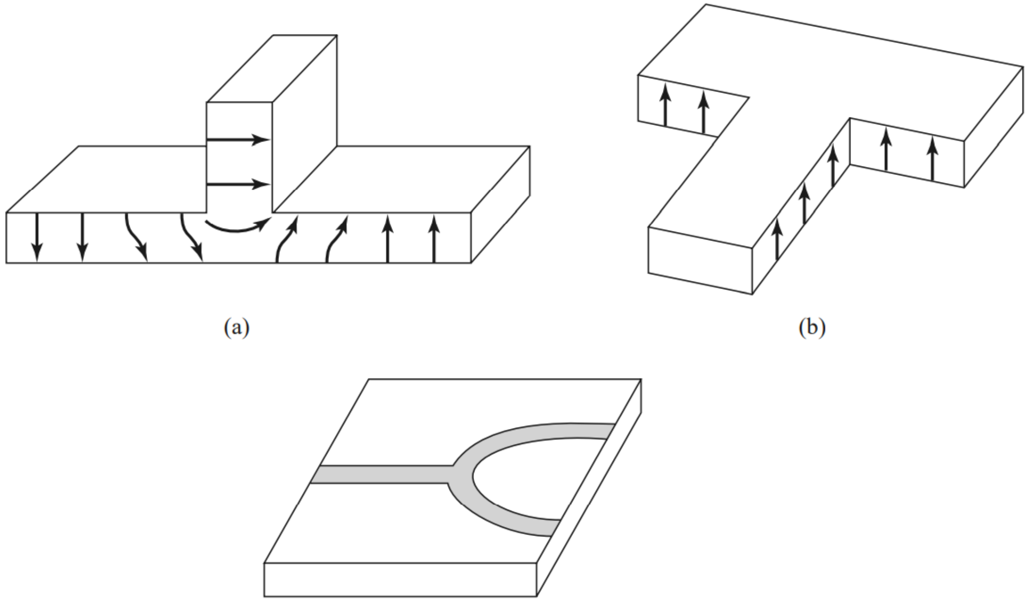
Module:6 Microwave Passive circuits __7 hours

- T junction and resistive power divider, Wilkinson power divider, branch line coupler (equal & unequal), Rat Race Coupler, Filter design: Low pass filter (Butterworth and Chebyshev) - Richards transformation and stepped impedance methods.

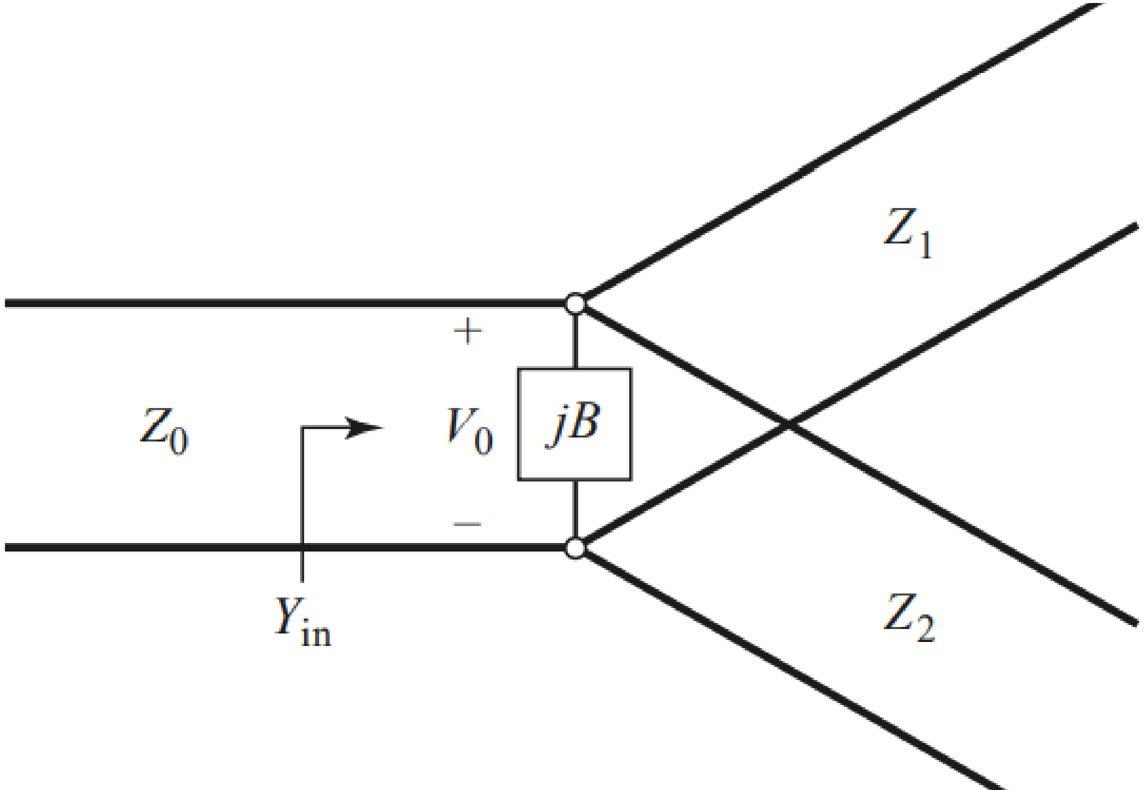
- Source of the contents: Pozar

6.1 Lossless T junctions

- E plane T and H plane T
- Fringing fields and higher order modes with **discontinuity at junctions**



(a) (b) (c)



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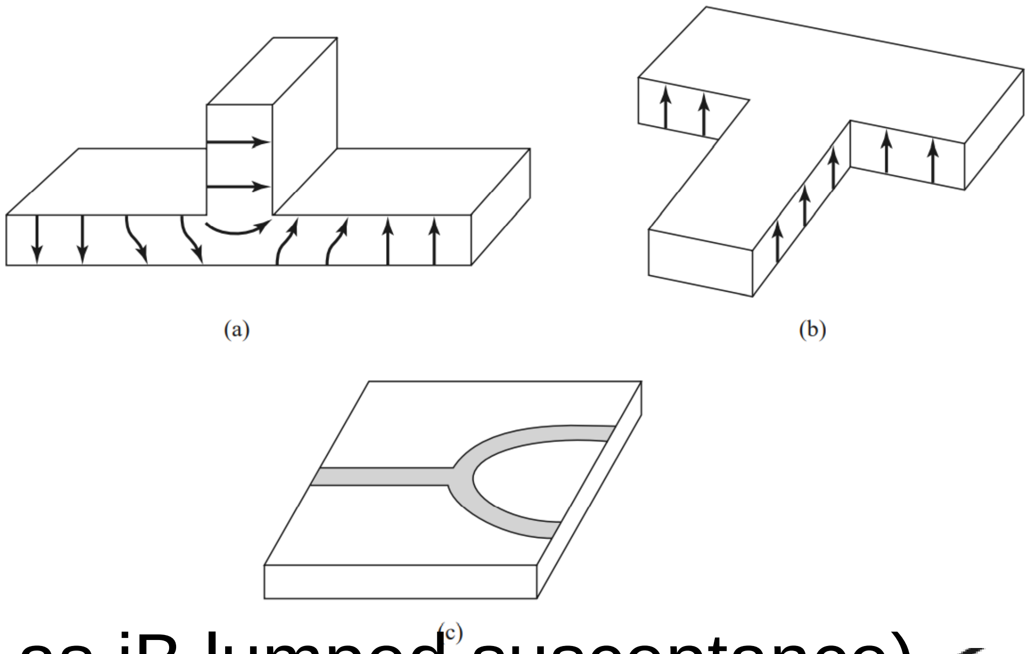
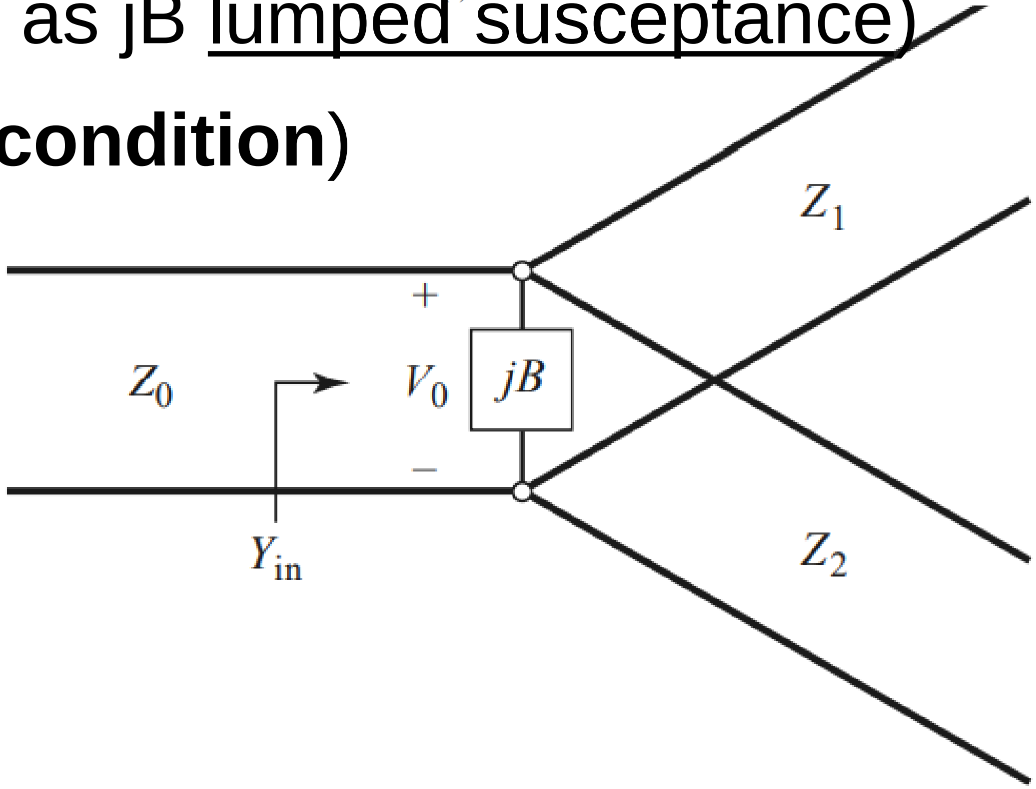


- E plane T and H plane T
- Fringing fields and higher order modes with discontinuity at junctions
- This results in **stored energy** (modelled as jB lumped susceptance)
- $Y_{in} = jB + \frac{1}{Z_1} + \frac{1}{Z_2} \quad = \frac{1}{Z_0}$ **(For matched condition)**



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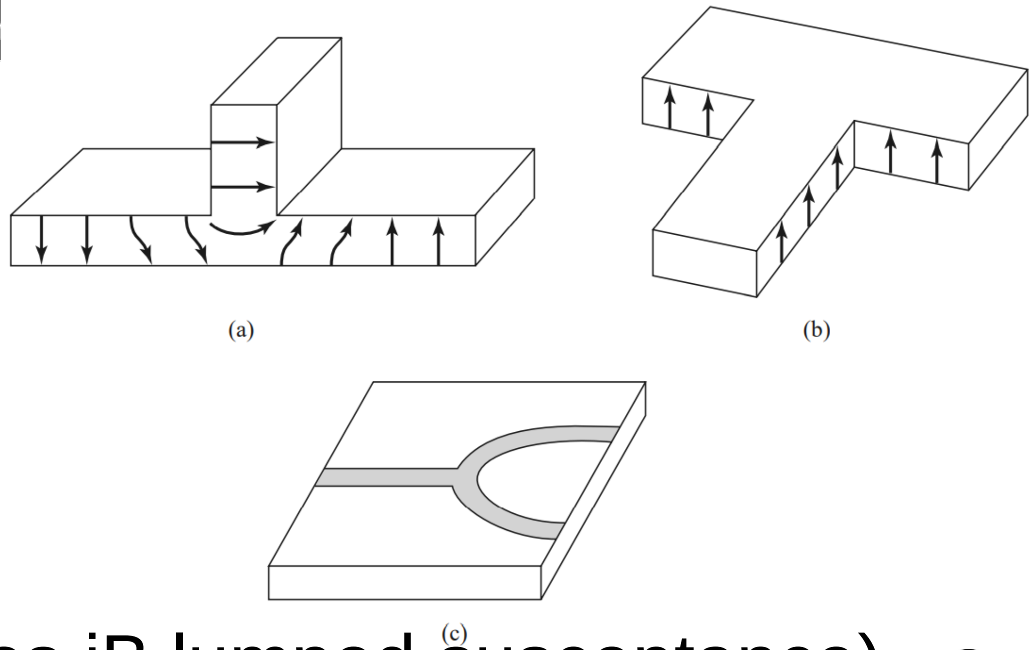

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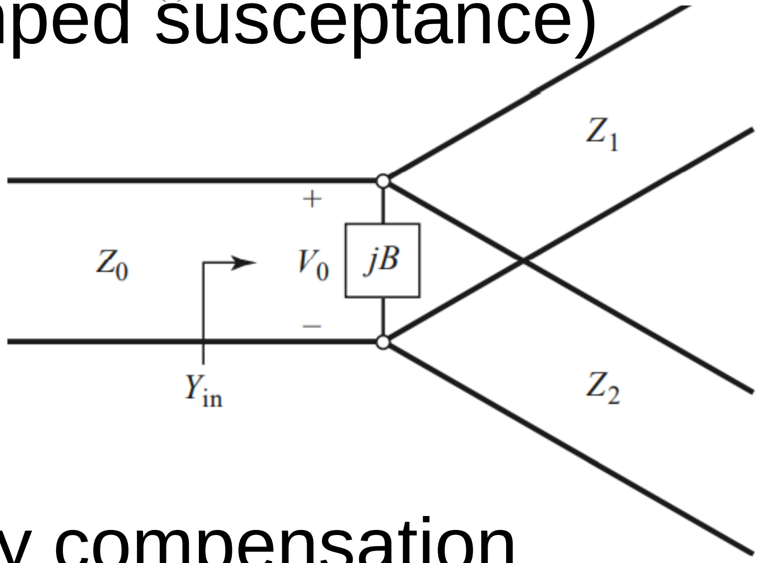
- For **lossless transmission lines**
  Characteristic impedance is real Z_0
- **Practical case**: ***B* is not negligible**,
  <u>Additional reactive tuning element or discontinuity compensation</u>



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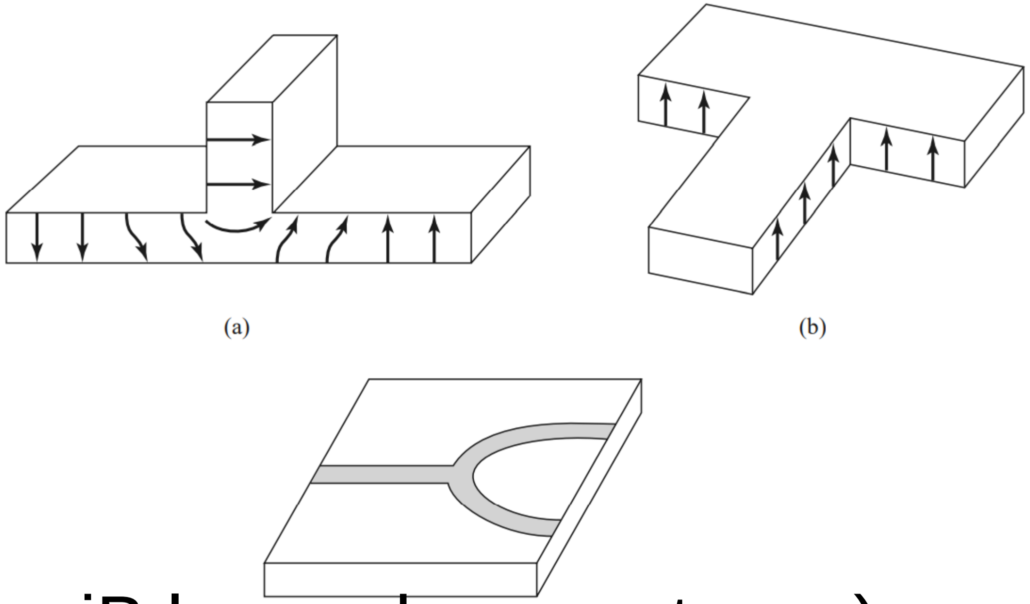

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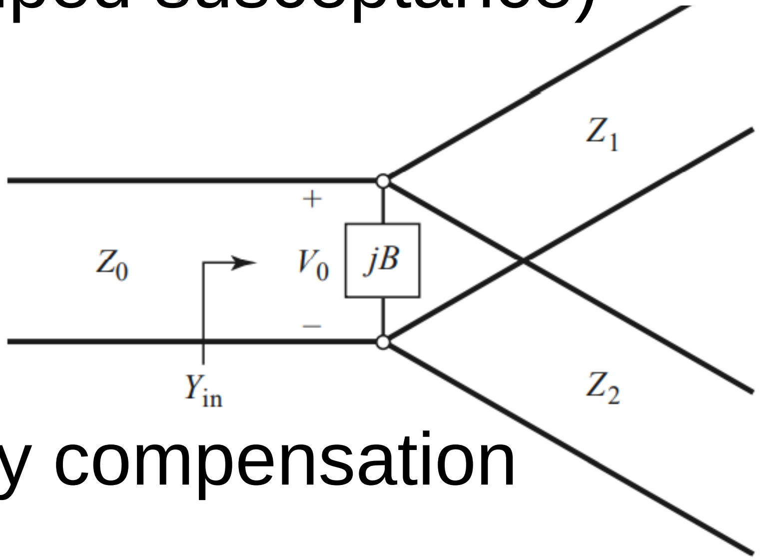
- **Ideal case**: $jB = 0 \quad \frac{1}{Z_1} + \frac{1}{Z_2} = \frac{1}{Z_0}$



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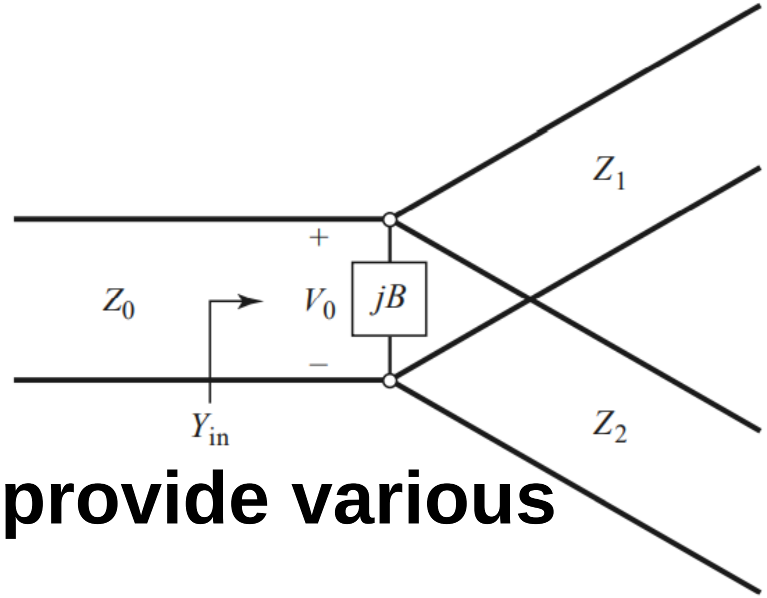

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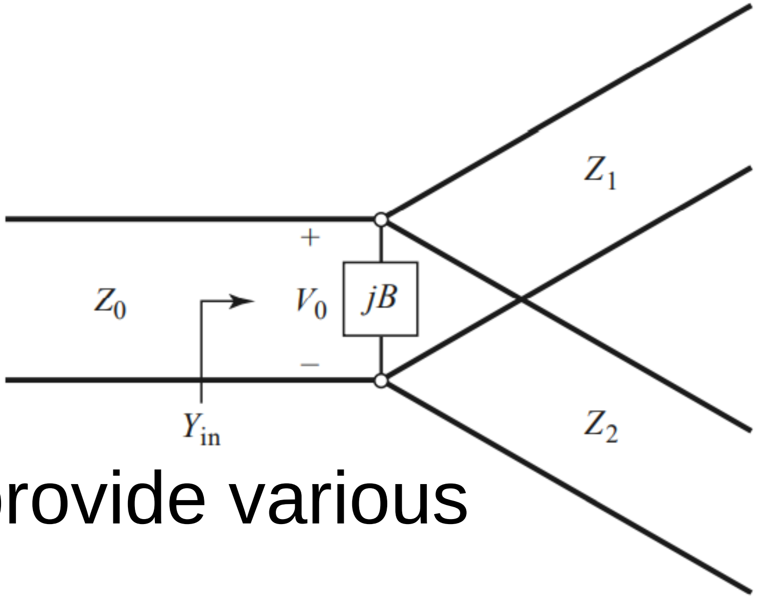

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- **$3dB$(equal split) power divider**:
  For a $Z_0 = 50\Omega$ input line, the **output lines can be made as two 100Ω** lines.

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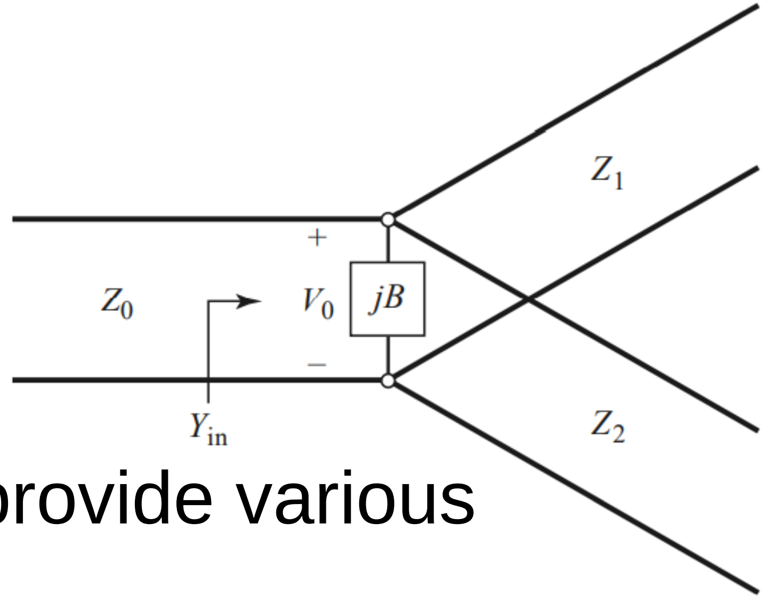

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  Quarter wave transformers can be used **to bring output lines at $\mathbf{50\Omega}$.**

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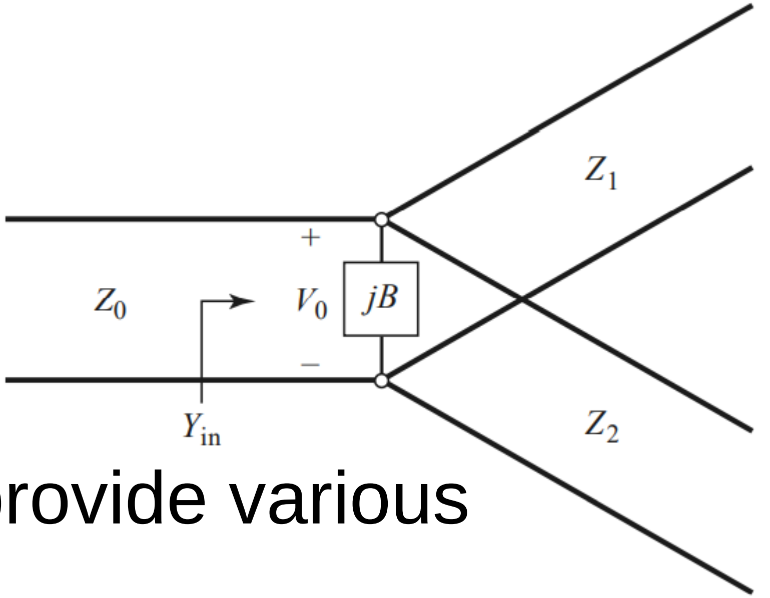

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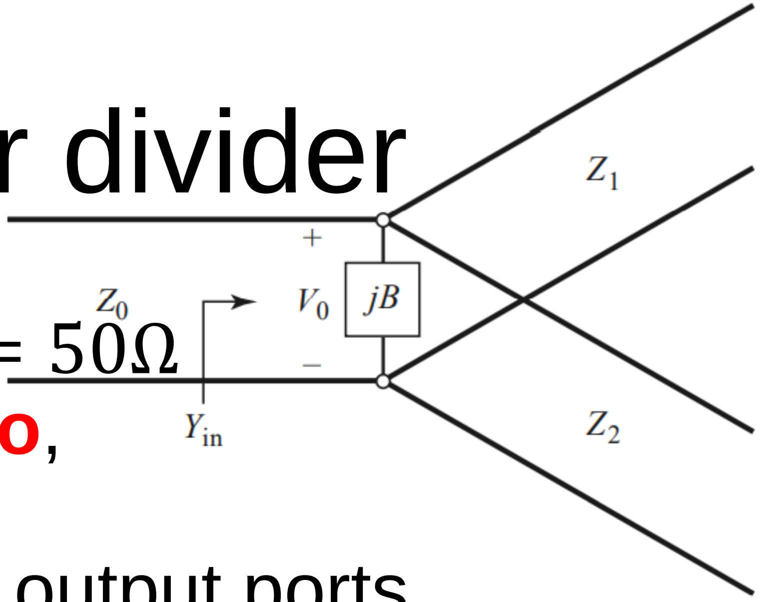
- Output line impedances Z_1 and Z_2 - selected to provide various power divisions.
- $3dB$(equal split) power divider:
  For a $\mathrm{Z}_0 = 50\Omega$ input line, the output lines can be made as two 100Ω lines.
  Quarter wave transformers can be used to bring output lines at 50Ω.
  For matched output lines, **input will also be matched**.
  Disadvantage: **No isolation between two output ports**
  Mismatch looking into output ports

6.2 Problem on T junction power divider



- A lossless T junction power divider – Source $Z_0 = 50\Omega$
  For output powers in **two ports to be in 2: 1 ratio**,
  Find output characteristic impedances.
  Compute reflection coefficients seen looking into output ports.
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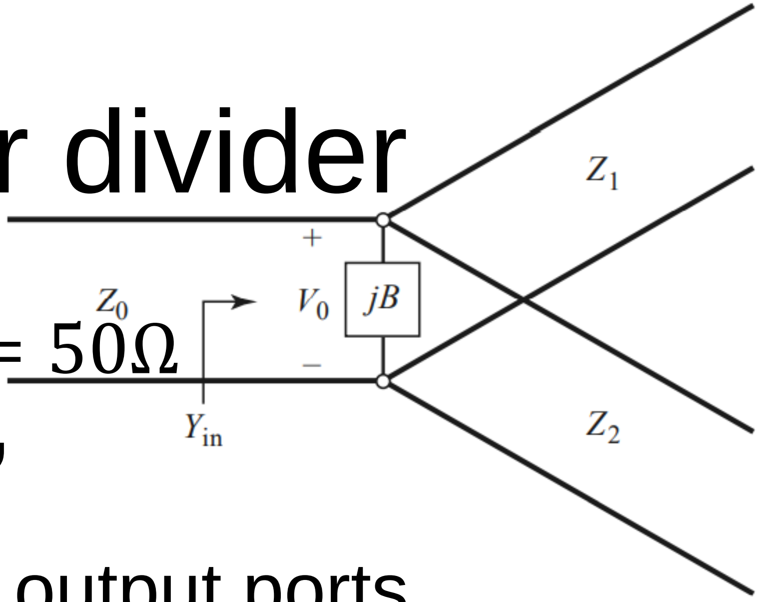

- A lossless T junction power divider – Source $Z_0 = 50\Omega$
  For output powers in two ports to be in **2: 1 ratio**,
  Find output characteristic impedances.
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- **Voltage at junction** is V_0,
  Input power into matched divider: $P_{in} = \frac{1}{2}\frac{V_0^2}{Z_0}$ while
  output powers are $P_1 = \frac{1}{2}\frac{V_0^2}{Z_1} = \frac{1}{3}P_{in}$ and $P_2 = \frac{1}{2}\frac{V_0^2}{Z_2} = \frac{2}{3}P_{in}$

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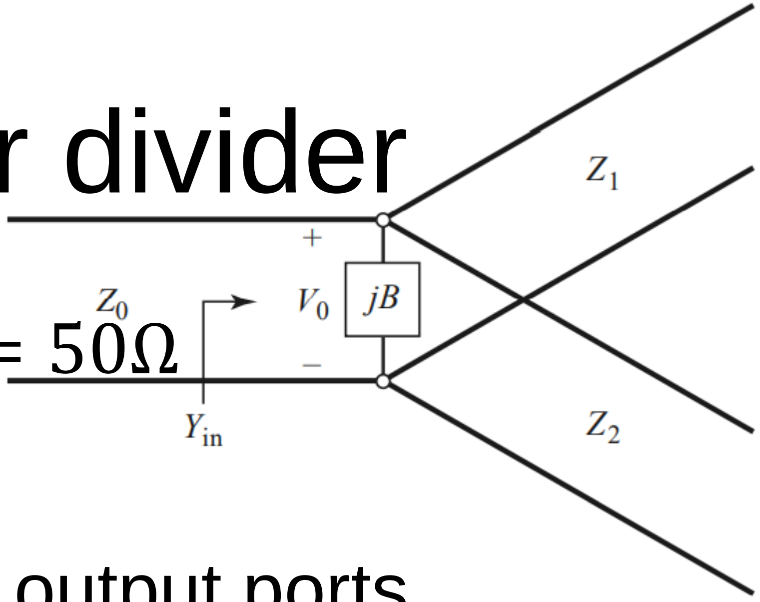

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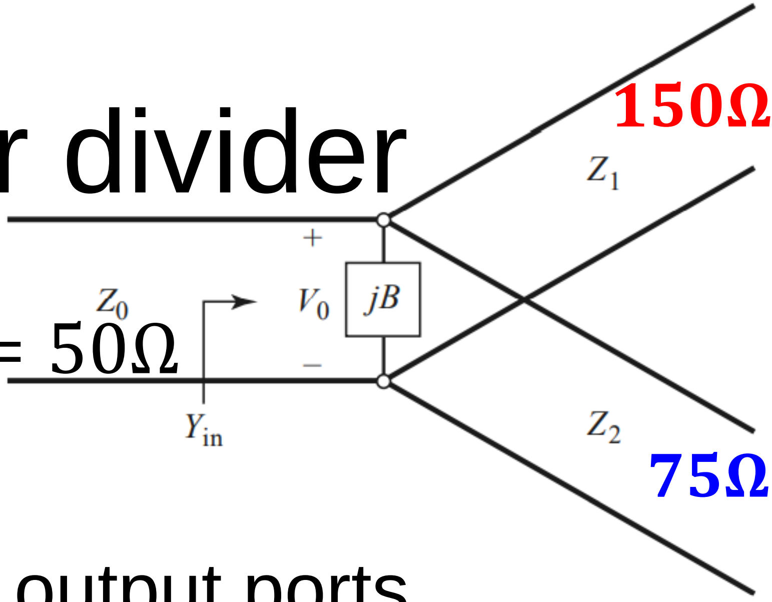

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$$Z_1 = 3Z_0 = 150\Omega \qquad Z_2 = \frac{3Z_0}{2} = 75\Omega$$

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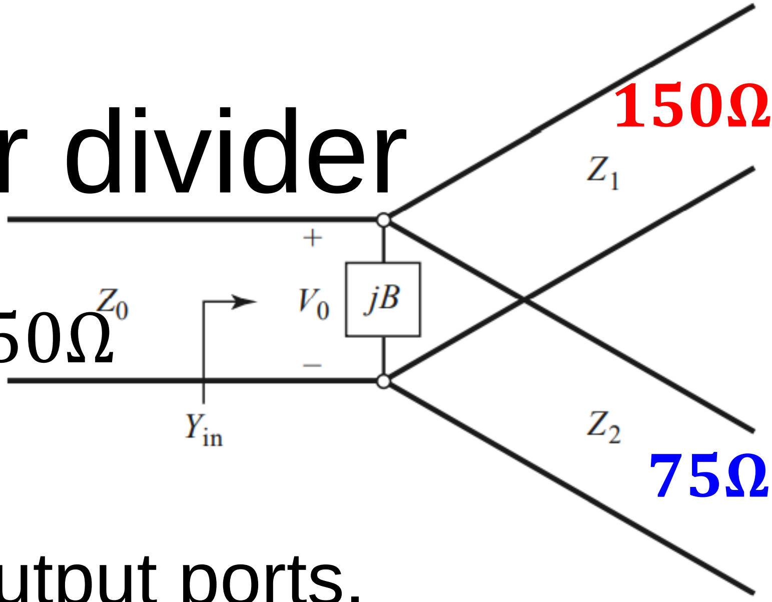

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Input impedance at the transmission lines act as load to that line.

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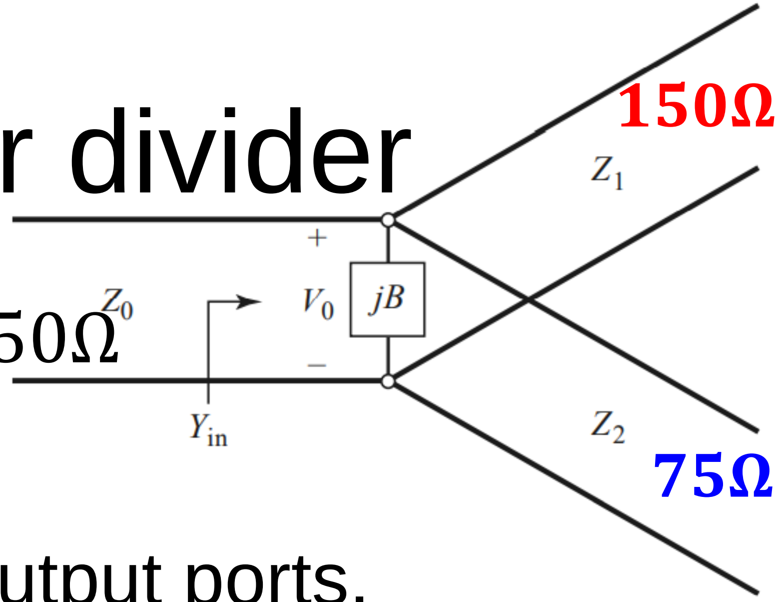

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  Input impedance at the transmission lines act as load to that line.
  When seen from Z_1, input impedance of $50 \parallel 75 = 30\Omega$
  When seen from Z_2, input impedance of $50 \parallel 150 = 37.5\Omega$

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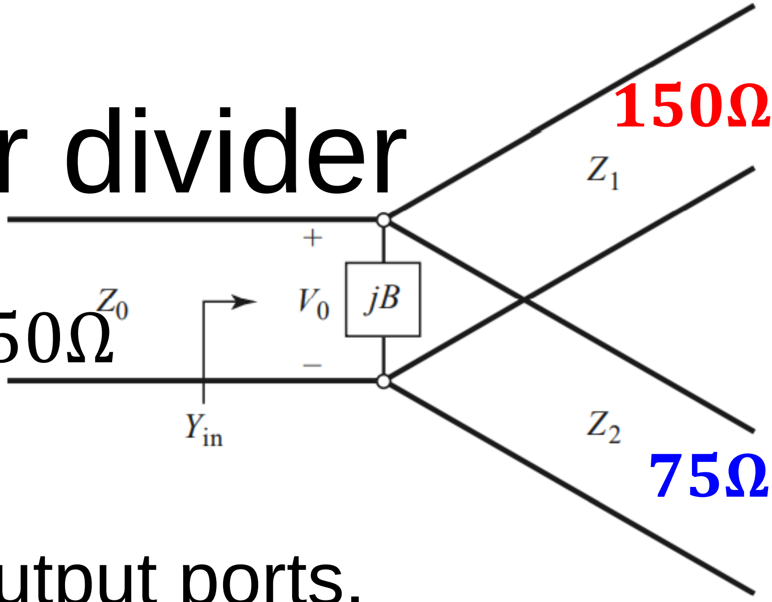

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- The respective reflection coefficients seen looking into these ports are:
  $\Gamma_1 = \frac{Z_{in1} - Z_1}{Z_{in1} + Z_1} = \frac{30-150}{30+150} = -0.667$ and

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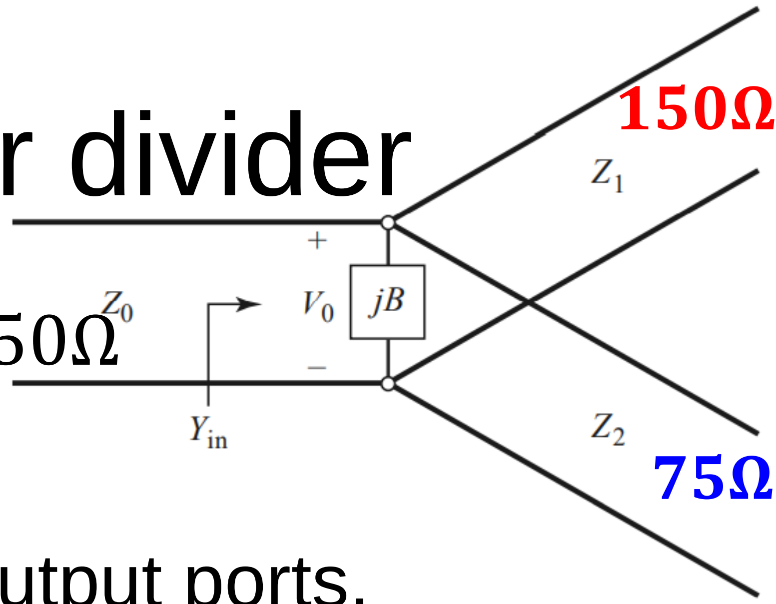

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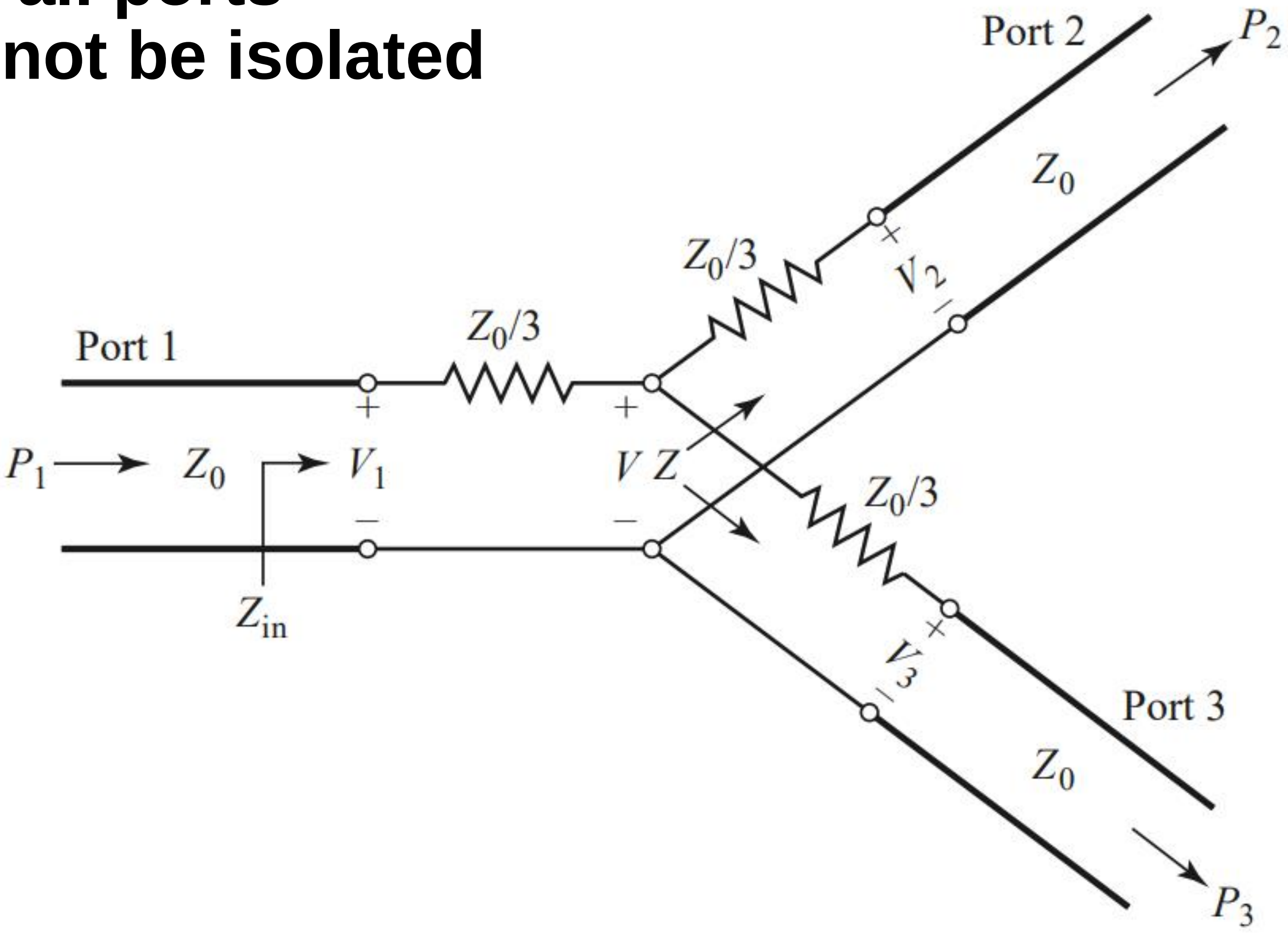
6.3 Resistive divider

- **Three port divider contains lossy components**
  Can be made to be **matched at all ports**
  Though **two output ports may not be isolated**



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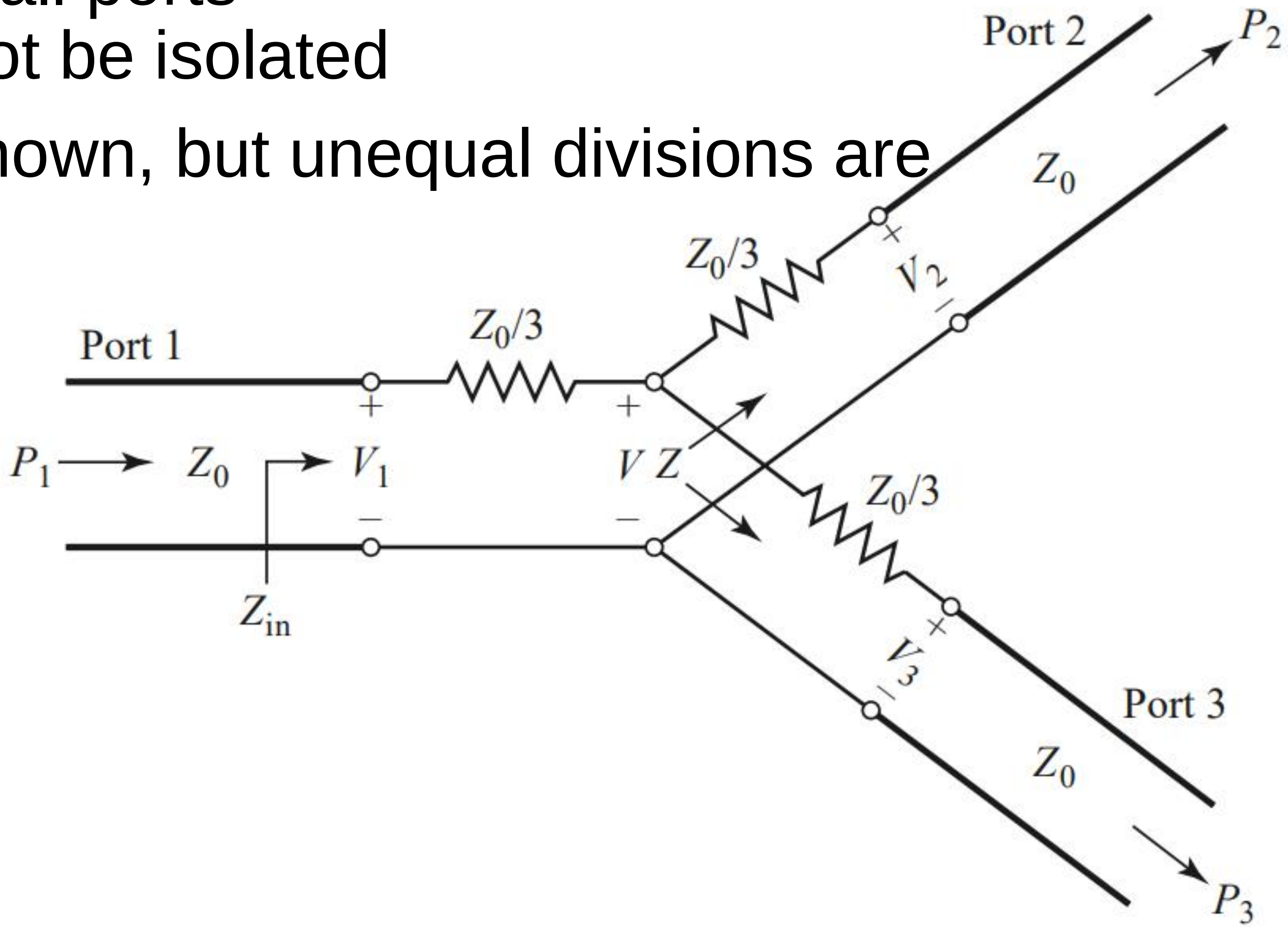

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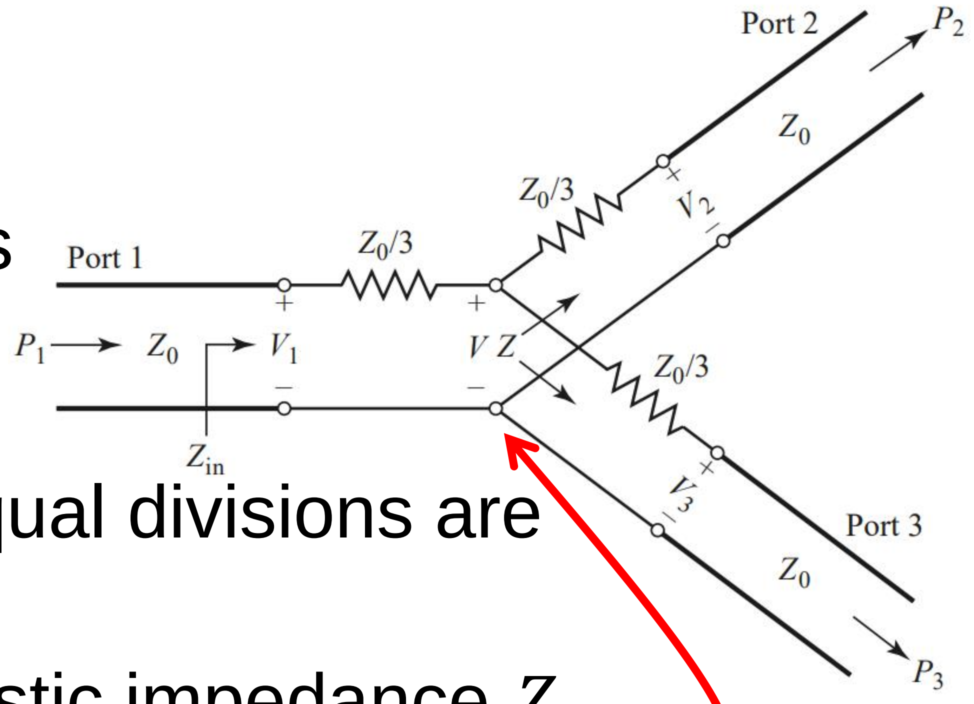

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- Assume all ports are terminated in characteristic impedance Z_0.
  With terminated output line, the impedance Z observed at junction is $Z = \frac{Z_0}{3} + Z_0 = \frac{4Z_0}{3}$

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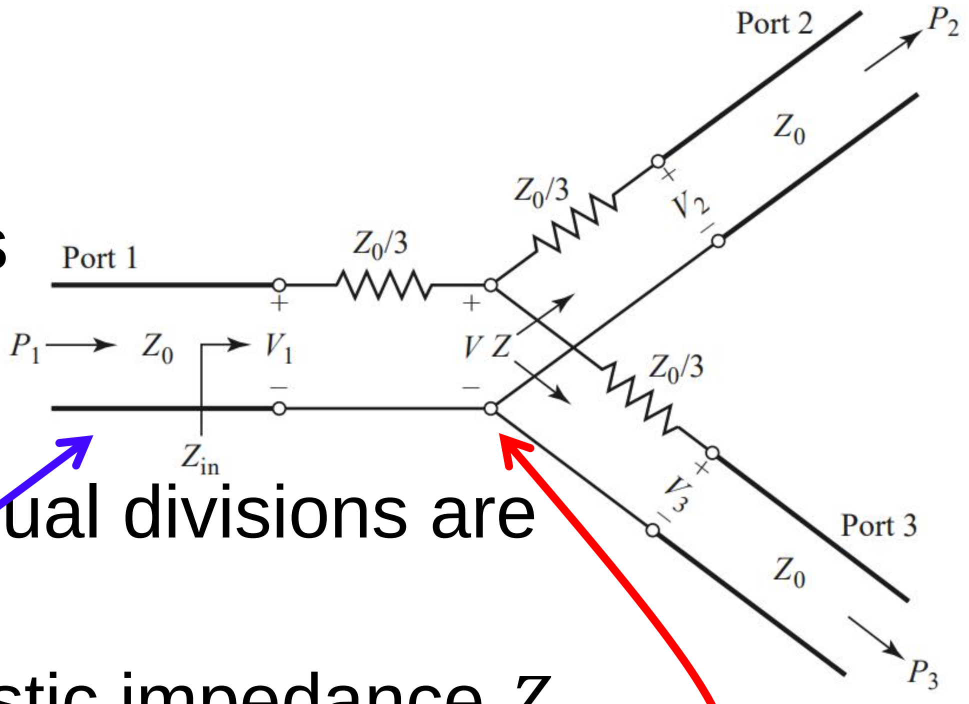

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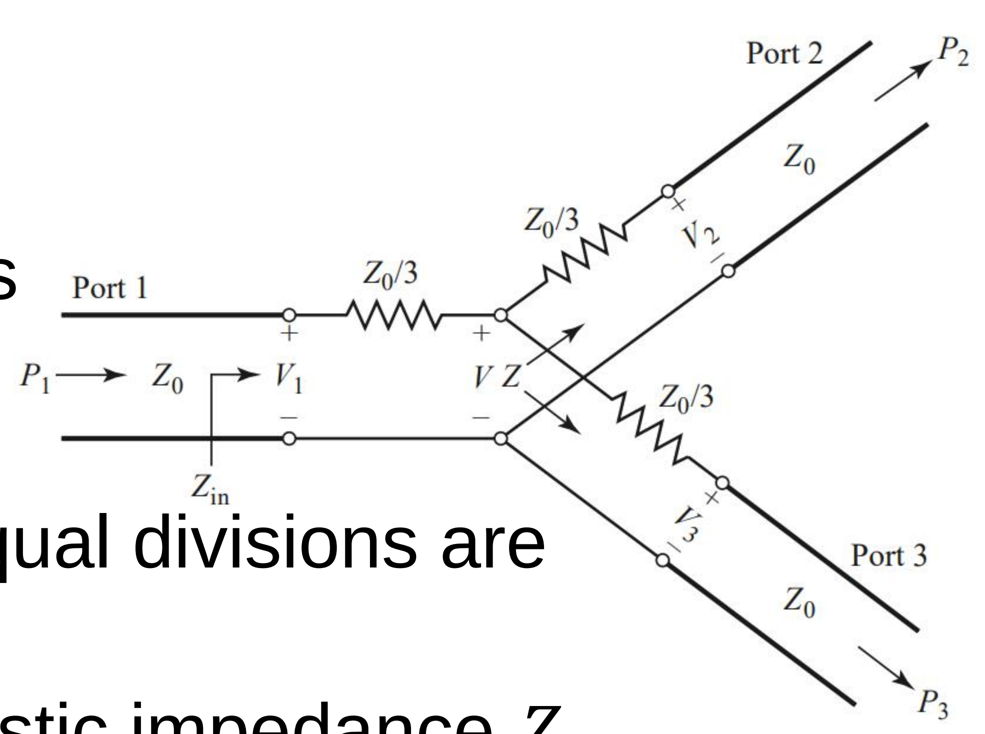

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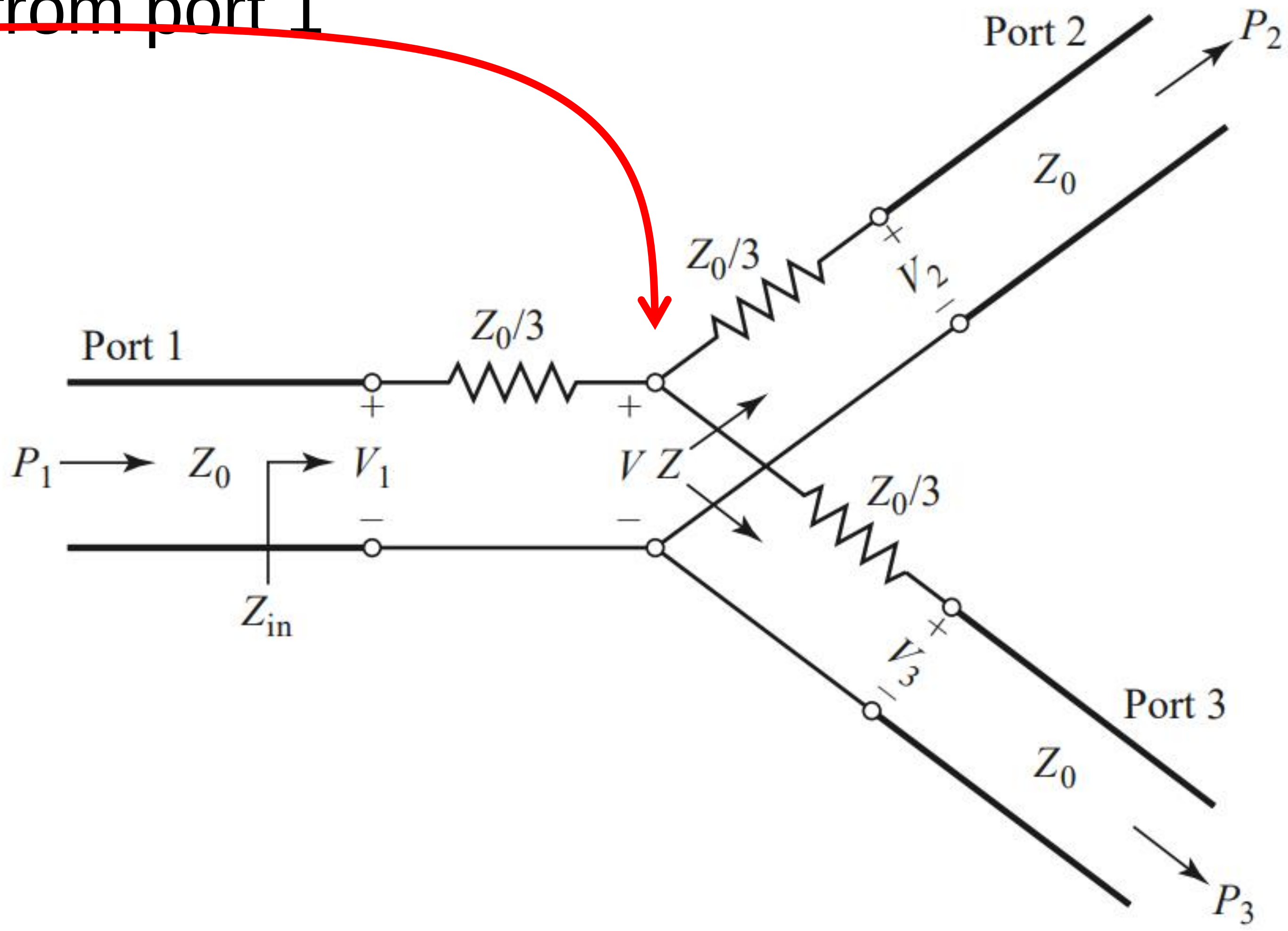
- At input, Input impedance of the divider $Z_{in} = \frac{Z_0}{3} + (Z \parallel Z)$
  $Z_{in} = \frac{Z_0}{3} + \frac{2Z_0}{3} = Z_0$ (Input is matched to feed line).
- Same can be verified from all ports: $S_{11} = S_{22} = S_{33} = 0$

6.3 Resistive divider

- $Z = \frac{Z_0}{3} + Z_0 = \frac{4Z_0}{3}$ $\qquad S_{11} = S_{22} = S_{33} = 0$
- Voltage at junction when looked from port 1

$$V = V_1 \frac{Z \| Z}{Z \| Z + Z_0/3} =$$



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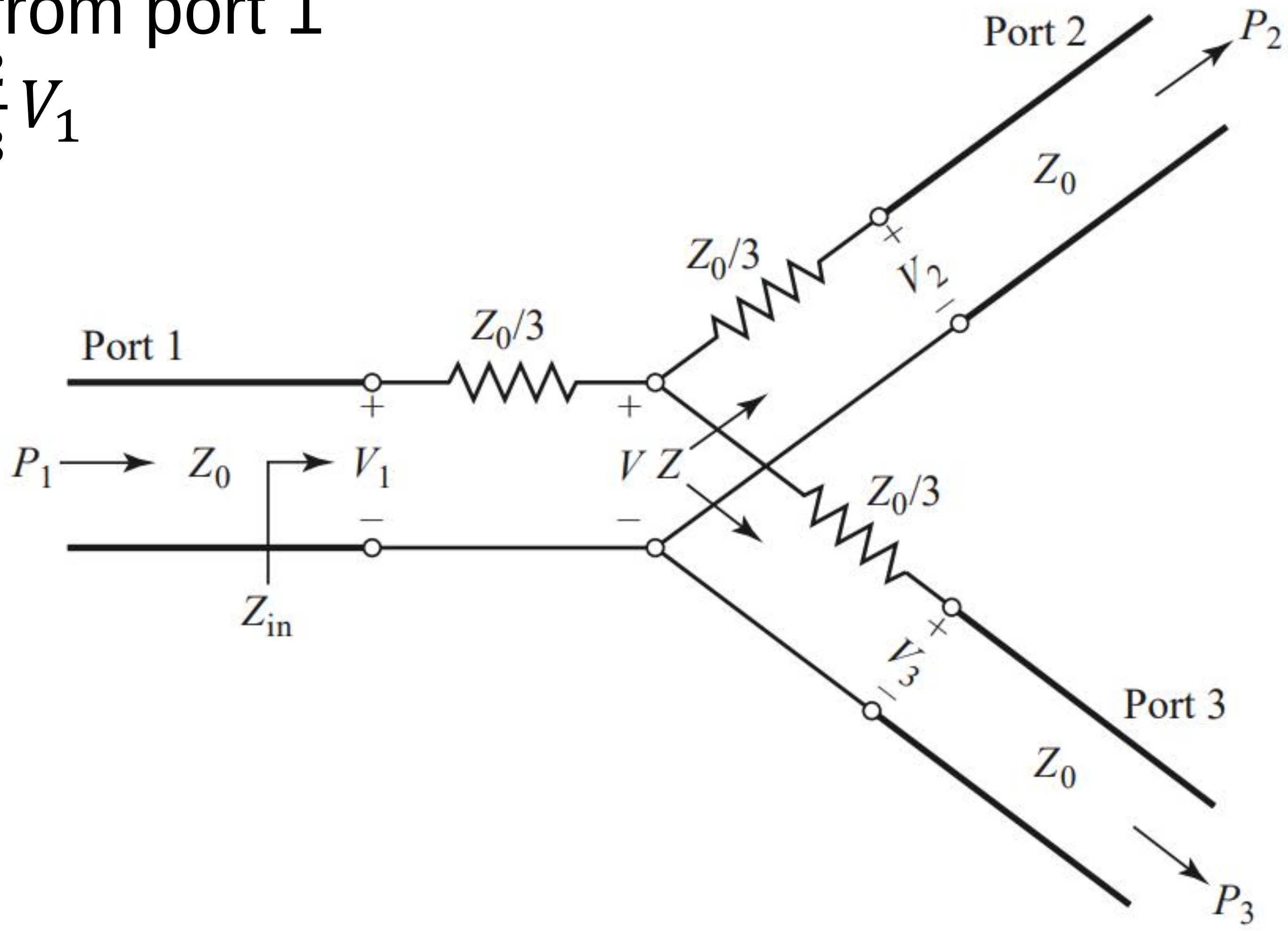
$$V = V_1 \frac{Z \| Z}{Z \| Z + Z_0/3} = V_1 \frac{2Z_0/3}{2Z_0/3 + Z_0/3} = \frac{2}{3} V_1$$



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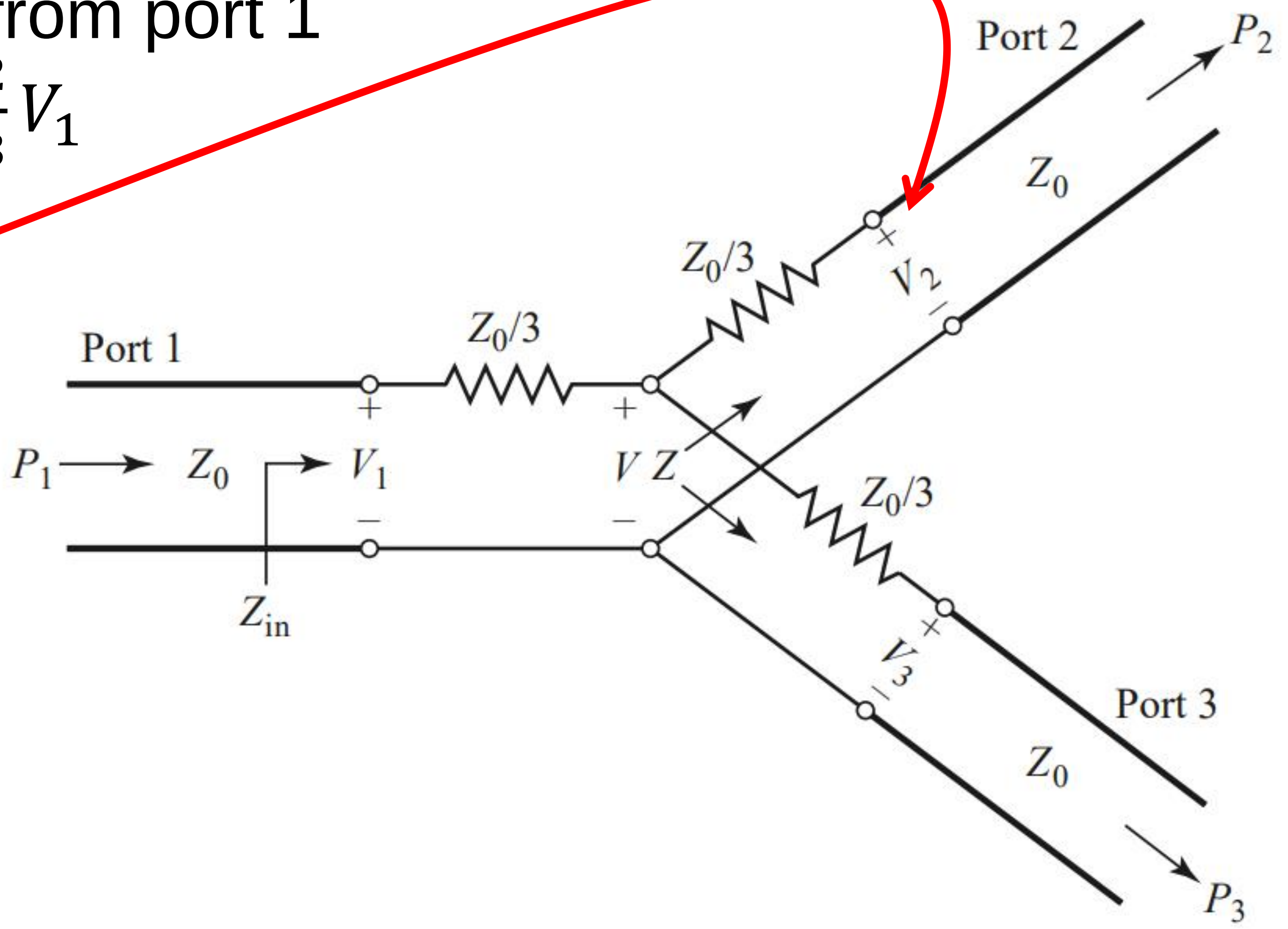
  $V = V_1 \frac{Z\|Z}{Z\|Z + Z_0/3} = V_1 \frac{2Z_0/3}{2Z_0/3 + Z_0/3} = \frac{2}{3} V_1$
- Output voltage at ports 2 and 3
  $V_2 = V_3 = V \frac{Z_0}{Z_0 + Z_0/3} = \frac{3}{4} V =$



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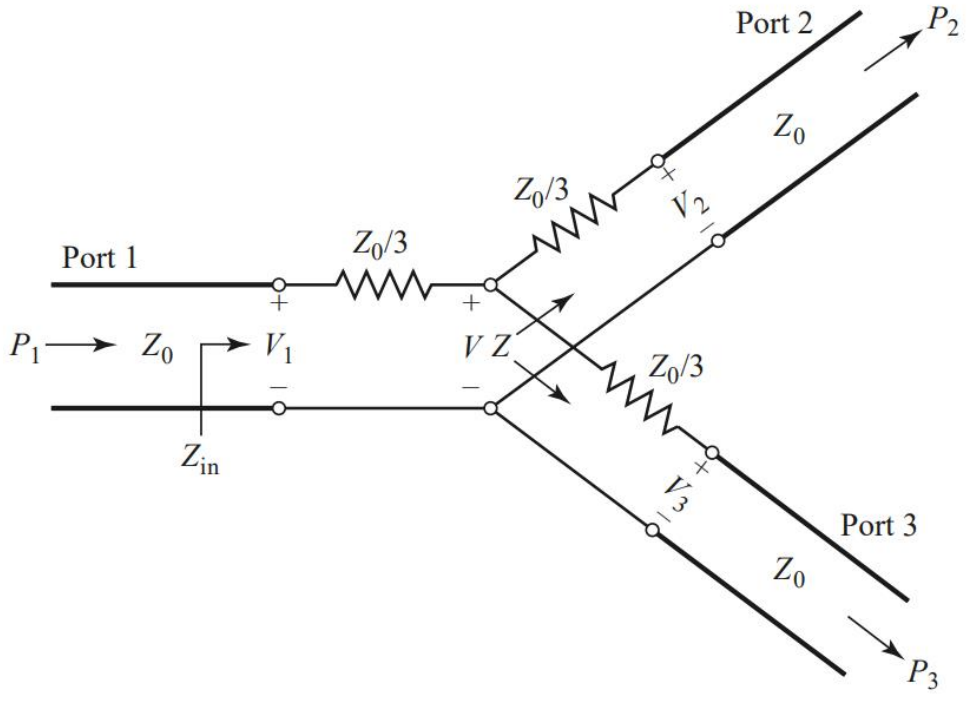
- Output voltage at ports 2 and 3

$$V_2 = V_3 = V \frac{Z_0}{Z_0 + Z_0/3} = \frac{3}{4} V = \frac{3}{4}\left(\frac{2}{3} V_1\right) = \frac{1}{2} V_1$$



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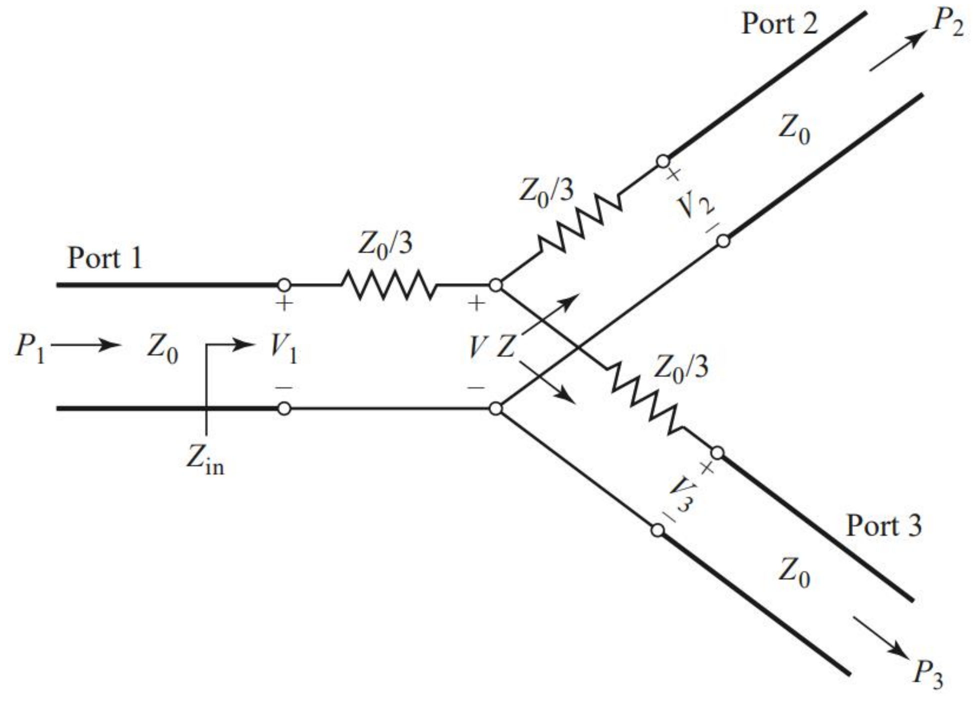

- $Z = \frac{Z_0}{3} + Z_0 = \frac{4Z_0}{3}$ $\quad\quad S_{11} = S_{22} = S_{33} = 0$
- Voltage at junction when looked from port 1

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- *S parameters* $S_{21} = S_{31} = S_{23} = \frac{1}{2}$

6.3 Resistive divider

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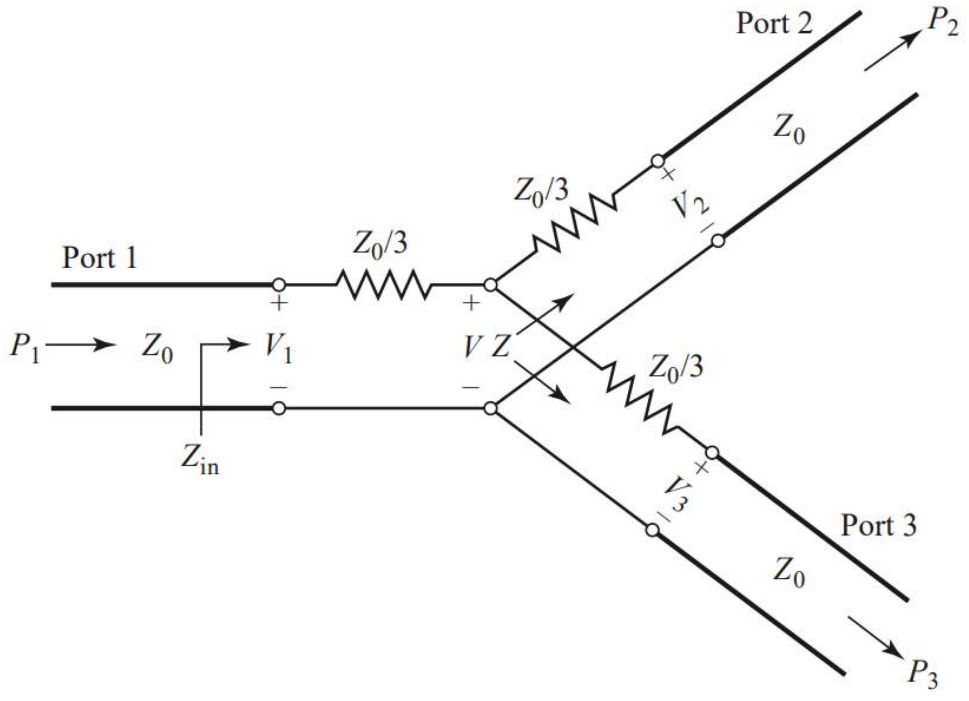
- *S parameters* $S_{21} = S_{31} = S_{23} = \frac{1}{2}$
- *Reciprocal network:* $[S] = \frac{1}{2}\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$



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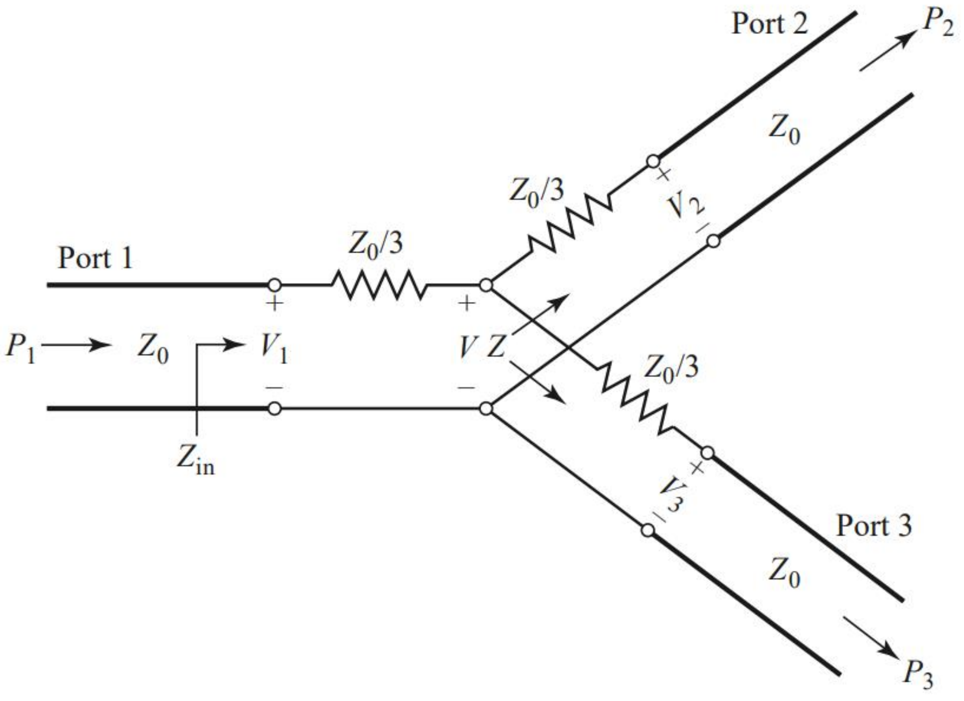
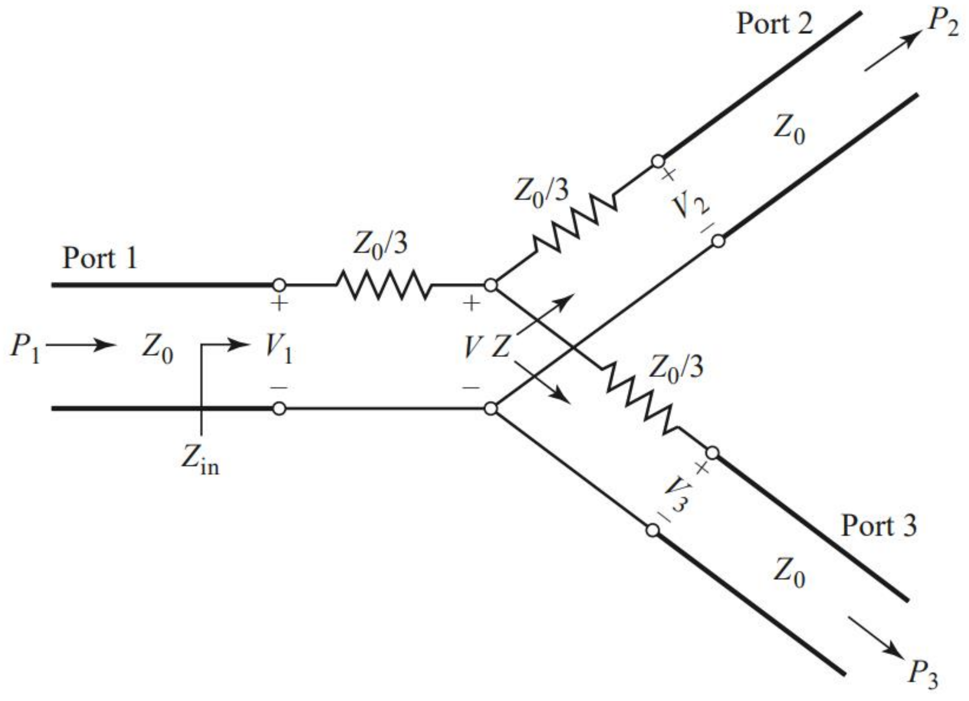


- $Z = \frac{Z_0}{3} + Z_0 = \frac{4Z_0}{3}$ $\quad\quad S_{11} = S_{22} = S_{33} = 0$
- Voltage at junction when looked from port 1
$V = V_1 \frac{Z \| Z}{Z \| Z + Z_0/3} = V_1 \frac{2Z_0/3}{2Z_0/3 + Z_0/3} = \frac{2}{3} V_1$
- Output voltage at ports 2 and 3
$V_2 = V_3 = V \frac{Z_0}{Z_0 + Z_0/3} = \frac{3}{4} V = \frac{3}{4}\left(\frac{2}{3} V_1\right) = \frac{1}{2} V_1$
- *S parameters* $S_{21} = S_{31} = S_{23} = \frac{1}{2}$
- *Reciprocal network:* $[S] = \frac{1}{2}\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$
- With input at port 1, $P_1 = \frac{1}{2}\frac{V_1^2}{Z_0}$ $\quad\quad P_2 = P_3 = \frac{1}{2}\frac{V_2^2}{Z_0} = \frac{1}{4} P_1$ $(6dB$ below input power level)

6.3 Resistive divider



- $Z = \frac{Z_0}{3} + Z_0 = \frac{4Z_0}{3}$ $\qquad S_{11} = S_{22} = S_{33} = 0$
- Voltage at junction when looked from port 1 $V = V_1 \frac{Z \| Z}{Z \| Z + Z_0/3} = V_1 \frac{2Z_0/3}{2Z_0/3 + Z_0/3} = \frac{2}{3} V_1$
- Output voltage at ports 2 and 3 $V_2 = V_3 = V \frac{Z_0}{Z_0 + Z_0/3} = \frac{3}{4} V = \frac{3}{4}\left(\frac{2}{3} V_1\right) = \frac{1}{2} V_1$
- *S parameters* $S_{21} = S_{31} = S_{23} = \frac{1}{2}$
- *Reciprocal network:* $[S] = \frac{1}{2}\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix}$
- With input at port 1, $P_1 = \frac{1}{2}\frac{V_1^2}{Z_0}$ $\qquad P_2 = P_3 = \frac{1}{2}\frac{V_2^2}{Z_0} = \frac{1}{4} P_1$ ($6dB$ below input power level)

Power delivered to ports=$P_2 + P_3 = \frac{1}{2} P_1$

The remaining power $\boldsymbol{\frac{1}{2} P_1}$ is **lost in the resistors**.