SFR

Special Function Registers of 8051

- all internal registers
- why SFRs?
  - to control timer, counters, serial, I/O ports ...
- specific functions
- acts as monitor & control the operation of 8051

Accumulator (A): used for arithmetic & logic operations

B-Register: used for arithmetic & logic especially multiplication & division

Program counter: holds address for next instruction to be executed.

Data pointer (DPTR): Addressing data memory in indirect addressing mode.

Stack pointer (SP): points to the current top of the stack in the stack memory area

PSW (Program status word):- contains various status flags (carry, aux carry, overflow, parity ..)

Timer0 (T0): Control registers (TH0 & TL0)

Timer1 (T1): control registers (TH1 & TL1)

Serial port control Register (SCON):- controls serial comm, baud rate and status flags

Serial Data Register (SBUF) - Holds data to be transmitted or received via serial port

Interrupt Enable Register (IE) - enables or disables interrupts & source.

Interrupt priority Register (IP) - priority level of different interrupt sources.

Timer mode register (TMOD) - mode b/w timer/counter & mode (0, 1, 2, 3)

Timer 2 / counter 2 control register (T2CON) – controls operation & fn of timer 2

Timer / counter 2 Data register (RCAP2H & RCAP2L): Holds the initial value of timer 2

Timer / counter 2 Register (TH2 & TL2) Holds current value of timer 2

Port 0 (P0): bidirectional I/O

Port 1 (P1): "

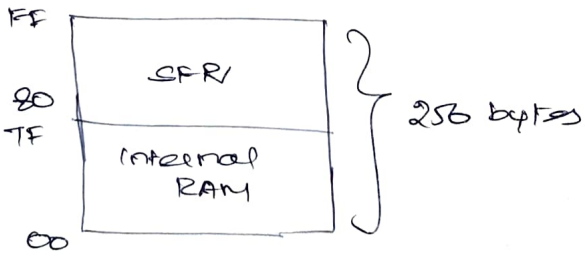
Port 2 (P2): "

Port 3 (P3): " with additional functionality such as interrupt & serial communication

Power control Register (PCON) – control power modes & reset sources.

watchdog timer (WDTC): – Generates system reset if not done by software.

- each SFR has 1 byte of address & unique name for specific functionality.
- 256 bytes of internal RAM accessed by 8 bit address es. (000H to FFFH)
  - → 128 bytes (internal RAM) → 00H to 7FH
  - 128 bytes (SFR) → 80H to FFH



- MOV instruction used to access SFR

different category of SFR,

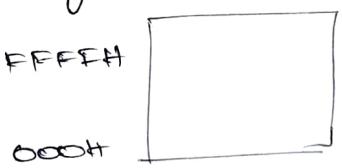
1. Math/CPU registers → A & B registers
2. Pointer registers → DPTR, SP
3. Status register → PSW
4. Input/output port latches → P0, P1, P2, P3
5. Peripheral control register → TCON, SCON, TCON, TMOD, IE, IP
6. Peripheral data registers → TL0, TL1, TH0, TH1, SBUF

A & B Registers: (8 bit)

- used for hold the data for most of the ALU operation
- A/Accumulator - ALU operation results are stored
- B - multiplication & division (16bit), hence A & B register will combine if it goes beyond 8 bit.

DPTR (Data pointer)

- 16 bit — 8bit (Higher order) DPH (D8-D15) → 83H
  — 8bit (Lower order) DPL (D0-D7) → 82H
- external RAM & some instruction involving in program memory.



0 to 65535 (decimal values)

Interrupt Enable (IE)

- Address @ A8H
- Enable/disable interrupts

↓ It has to be enable if you want to enable any interrupt, if it is '0' then if lower bit '1' also won't enable

Interrupt priority Register (IP)

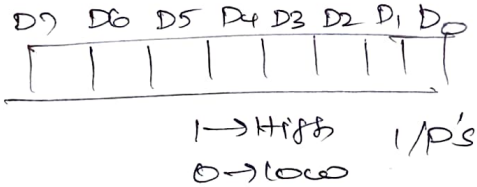
- B8 address
- priority given for the interrupts
- 8 bit register
- high to low priority

5 interrupts
- external hardware interrupt 0 (INT0)
- " " " 1 (INT1)
- Timer 0 overflow interrupt (TF0)
- " 1 " " (TF1)
- Serial comm " (RI/TI)

P0, P1, P2, P3 :-

P0 (Port 0)

- 80H
- 8 bit (P0.0, P0.1, P0.2, P0.3, P0.4, P0.5, P0.6, P0.7)



P1 (Port 1) → 90H address ⇒ P1.0 ... P1.7
P2 (Port 2) → A0H address ⇒ P2.0 ... P2.7
P3 (Port 3) → B0H address ⇒ P3.0 ... P3.7

If you reset, all bits are set (1) — means all are configured as inputs

PCON ⇒ Power Control Register :

- used for power control
- used for baud rate selection
- 8 bit register

PD → Power down mode
when, PD=1 (power supply 5V → 2V)
(internal oscillator is stopped)

IDL → Ideal pin
IDL=1 (Ideal mode)
IDC=0 (NOT)

- In Idle mode, clock signal - stopped
  ↓ (interrupt is activated: timer, serial ports)
  deactivated / terminated by interrupt or RST button

* PD mode can be deactivated / terminated by

- GF1, GF0 ⟹ General purpose flags

Baud Rate → bits transfered per second

- SMOD - serial mode selection
  - speed of the serial communication is fixed / <Baud rate> in serial port by mode 0, 1, 2, 3.

mode 0 → Baud rate fixed
mode 1 & 2 → (2 SMOD/32) × (Timer 1 overflow flag)
mode 2 → SMOD = 0 (Baud rate = $\frac{1}{64}$ oscillator freq)
SMOD = 1 (Baud rate = $\frac{1}{32}$ oscillator freq)

Program Status Word (PSW)

- also called flag register. (8 bit)
- for testing the condition of result & make decision
- 1 bit register (0 | 1) ↓ reset, → set

Carry, Parity

B7	B6	B5	B4	B3	B2	B1	B0
C4	AC	F0	RS1	RS0	OV	-	P

B0 → Parity flag
B2 → overflow flag
B7 → carry flag
B6 → Auxillary carry
B5 → user defined flag

Bank	RS1	RS0
1	0	0
2	0	1
3	1	0
	1	1

SCON → Serial control Register:

- used to control operation modes of serial port, baud rate, transmitting / receiving serial port.

SM0	SM1	SM2	REN	TXD	RXD	TI	RI

- also contains flags that are set when a byte is successfully sent or receive.

SM0, SM1, SM2 } selection of serial modes

REN → Baud rate selection

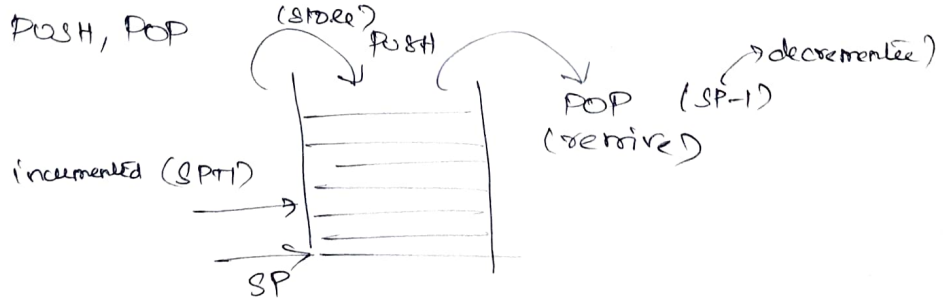
TXD, RXD, TI, RI → Transmission & Receive of the data

Serial buffer (data) (SBUF)

- used to hold the parallel data during transmission & reception
- Serial reception, Serial (RXD) → parallel (SBUF)
- Serial transmission, parallel → Serial (SBUF)
- transmit and receive are assigned same address
- data is written to SBUF it goes to transmit buffer.

Stack pointer (SP)

- 8 bit address
- any portion of RAM can be reserve as stack.
- after Reset / RST → SP is initialized as 07H
- PUSH, POP



Timer/counter (TMOD | TCON) <we have seen>.