Micro commune through processor 1st generation - vaccom tobe, Porch coods 7 2nd Generation - Transismo, Diode 3rd generation - Ic - & Difftal Era> 4th Generation - VLSI microprocessor 5th Generation - ULSI, Super computer. 6th generation - Quantum computing. - Micro processos -> small + bonctional operation 5. Elhereever automation comes to picture, microcontrolly playes important role like whiper in car, acommunic door lock in car, home appliances etc... = - Micro controller => Advancement of microphocessor Micro processor - Manually come mathematical operation like division, we can go upto & to 5 decimal points but if we want to go more and accurate then we opt for machine/comporter calculation. - Hoge data calculation (- Eg: 3x3 matrix but with MP we can do any specification with accuracy. - Mp => combination of different mathematical operation based circuits in one place =) Ic - combination of different circuits like addre, moltifice, divides, differentiator, integrator ... lotical circuits like ADD, OR, NOR... all placed in a single place to do process. IMP => MP => Olp device device Peripheral devices L'external devices) keyboard, mouse, printer, monitor... Hard disk

Compoter compoter is a microprocessor based system (if Mouse => MP => pointer (0/p device) Hard disk, CD, DVD, Floppy (memory device) COMPUTER Buses - How we are connecting if devices to the processor ? - How we are connecting opposerices to the processors? theough wires - Technically => Bases. - Non-Technically, Bos? - Transport Yechicle - transfer of data/person brown one - Technically, Bos? address, controls - Transfer of data, theough wires - Good of wises. - to toanstee the data from 1/p to processor or from processors to ofp. - As MIP is a difital device, to data will be in the torroat of binary 0's, 1's (two level strad) Ex: High state +5 1/-5 1/+3 1/-3 > 12 1000 state OV Positive logic Negative Copic - Representing most Hibri pravid ine +5v-ov/1-0 (imagtration)

The data, when feed as ilp will be in the term of o's, 1s sy when we get the old also in the tororoot Of O's 3, 1's Diffetal tororoot) A B -> 2 woires/buses 1 wire/by Either 0 001 3 wires/buses -> 2/3 -> 8 4 wires/bases 24 -> 16 5 wires/buses 25-32 Data/
Data bus (information tor trapolessor) Buses -> control bus dusires) > Address bus porpase - Group of wises used for data /interrelation $-\frac{Ex!}{(Decimal)} \rightarrow 101 (222) + 4+0+1$ (Decimal) (Binary) For representing 5 (decimal no) inced three wives buses, likewise it I need to represent higher nombers, then I need more no of bases. 1st Micooprocessor => 4 bit (mtel 4004) length of the data bus 4 processors width 2nd Microprocessor => 2 bit (Intel 8008) < 8085,8086,> It we are fiving any intormation, then it will be in the tormat of 8 bit ... so on ... o/p also in very 1st computer comes order 8086 x 8617)

20186-16614 20186-16614 20186-32614 20386 20486 single processor combining a processor Shence the name core 2 dool means in a single processor Ex:- In 8085 processor, (8615) 5 0000 0101 (Decimal) in core 13 processor, (82 bit) (Decimal) > 0000 0000 0000 0000 0000 0000 then think about 64 bit that we are using go why we keep on increasing the data bos from & bit to 64bit?
(easy) (looks messy/bigger) (A-2) Ex: to speak in English we need 26 alphabets to speak in Tamel use need 247 letters Each language has some basic characters, likewise when we commonitate with computer, we need those borstic concepts So we are increasing the data box brown 4 bit -> 8 bit -> 16 bit -> 32 bit -> 64 bit. Here we are not changing the abuta but how many binary terrorats is important In early stage we used only english, but right has we are using many tornats like Ascil, nombers, appraisers, other languages, pictores, riders, many torrats, for this we need terresont in binary toromats so we are Increasing the data bess length/wire/bases.

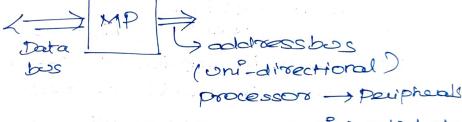
- Bidirectional databas (P/P, OIP) (>>)

Address bus :-

- Every person is called by some name, so that's called address, every home/flat are called by some nombers & street name - address.

- Identification process.

- Every processor is connected by some flp sp olp devices, as a horman use know all those peripherals but microprocessor need to know the location where It is connected, it needs identification, so processor needs to identification, so processor needs to identify the peripherals y address theorth address for the processor.



- Address bus is not only too periphals but

Add Data 3

Memory

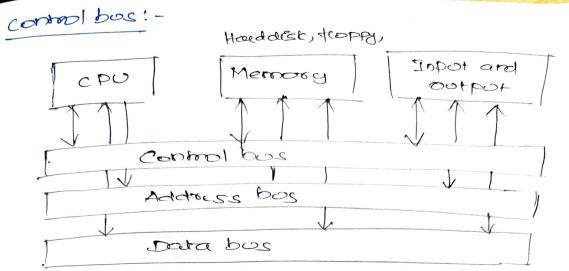
Add Data 3

Memory

Add Data 3

- more data/memory, we need more address

when increasing address bas, we can use many perhiphereals and also memory like 1TB, 512GB memory in our laptop/system.



consider when you are giving print a document, then printer is not connected in your laptop of PC, then we get notifications like printer not ready / printer not connected. Suppose you are cornected printer, but did not town on pause apply, then also we get notification, in another givation we connected printer, twend on power givation we connected printer, twend on power givation we connected printer, twend on power apply of printer, then also we get notification if apply of printer, then also we get notification if we don't don't paper in the tray.

so what producessors do is simply check the address of the peripheral s, it not connected means, it will notify.

Here the processor checks the status of the printer (connected to PC, power exply is on ON condition? Paper status?) - it memory alloted to printer is empty then it sends back next set or to printer is empty then it sends back next set or the printer.

to recity the status, too the peripherals, core use control bus.

Ex: Ack signed -> Acknowledgement

RD signed -> Read signed

WR signed -> write signed

Tolp

Bit-directions

Microprocessor - Diffital signals (High/loco etale 4 0/1) - I/P St OIP y distitud signal - A computer is oldveloped on the basts of microprotessor. - group or wolves & Buses - Data (gp/o/p) Address (memory) - Data Length Y wood Length y box wildth In 8085 processor, Data bus -> 869t Address bus -> 16 (2x8) most of the processor, when compare to the date

bus, double the time we have too address bus we can control a device with the help of smalt phone through simple SMS, but cannot control any devices with the help of compoter. Hence one biggest daceback comb processor is use carnol control any device with computer /processor (micro)

2253, 2251 -> peripretal ICs 8255, too commolling devices Address bos -> memory purpose.

we cannot commol any alevice with the help of prevaisor

Micadrongoolle

- Main perspose is controlling the periphetals. controlling the electrical equipments. - Mc > boilt in controlling circuit with processor.

- Fans (speed = 2 tobelight OFF

- Diffital I C

so control ont differes too each derrices, it want be same too all,

_ In rolcomonsmoller, we wont be having cell the general purpose options, we have specific to the device that we are wring - Klien no one removing realine develop backoose options froom processor, we are adding to mornory I're RAM, ROM. (external) Est: security carriera it caves audiof video _ so we need more memory - it wonth pretosons other operations - External hard disks with more morrowy. processing + controlling + Merrosg.

onit Micro controller = MC -> specific poopose (8051) be due at MP

(Dedicator) 2000 (Dedicated system) Ex: Smart EB meters -MP > General Porrpose - more processing only Ex. Addle, substacted,
multiplier, integer moltiplier, integerter ... - min momory - NO control Circusits address bus >MC - 805) -> 86H -> 16 bit -> Port together 24bits, =) MD -> 8085 -> 86PF -> 166H Jonnethine we can use the reduced vertibe apataconth when use are attilizing address, data has no oce, when we are osing data, address has no ose, 600 here use will be osing libbits address bus for both purspose. > Multiplexing ADO 60 AD7/ABB - ABIS 8000 OF re Ic coll Lower order Higher order

Address / Data Address be reduced. no. of wires are small

Addressing of memory of periphorals BOTH MC and MP are connected by Korne peripherals and andologous morne marries. 100 by default we need to assign forme address too any what if we process like assume 100 address on there, assume 20 address tors peripherals and to remaining address for memory, in this situation it act as limitations, meaning we cannot add more than 20 pheliphers & alloct more than Bo address for memory. unrestricted addressing Memory Peripheray same no? toa pour Peripherals & nomon Address mapped I/O (IO/M HIGH -> PREI Phone 1000 -> Memory Io Mapped memory (no need of using withel like ID/M, but the disadhant here is verage of peripherals or momory is limited. - Rostricted addressing Blocks of Mc and MP: - CPU -> central processing onil I/o > Inpot/outpor. Bos - Address bos/data bus. Memory -> RAM & ROM Times Serial of Payallel commonication Intersolpt.

Bit ? 573 4 3 diff no La chalanter in a decimal no system Deciporal no. of sysce Fos Binary -> 0,1 (0-9) NO. System - 1010 -> 4 5H 101 -> 2616 01-72 516 To character in a biracy no system Bytes? Ly group of & bits - 1 byte (10101011) Stoop of 469ES - 1 nubble (1010) y & bit 1 byte 4 2 nibble 20->1->1 (ten (10)) 21-12-22-)4 23-48 24-916 Loe are fiving poeition too the bies/ 25-132 binary > 26->64 27-7128 we can fenerali (X) 1024 -) Address, we need to address lin 28-> 256 29-1512 218-256K 214-16K 210-3 loau -> 1kb 219-1512 K 25-332k 4lines bil5 220, 1084 K-1005 2" -> 2K 216-364K 212-342 217-128K **は**2¹³ → 8 と Word length/bas length of data Congth no. of binary bits representing the douba. 8085 -> Dora -> 8 bit word congth = 9 8 8086 - Dota - 1668 world length = 16.

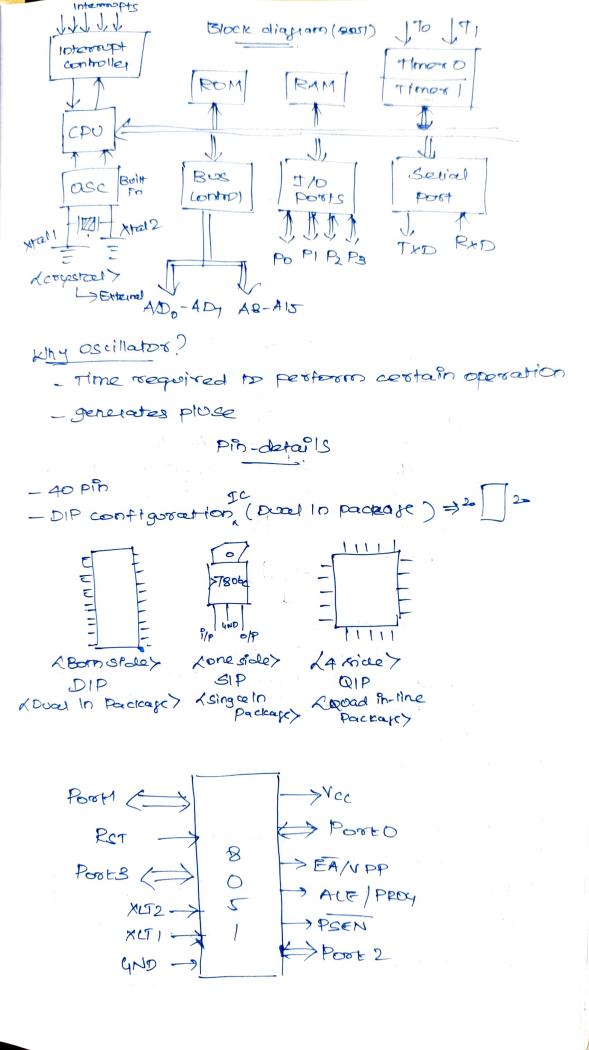
tost:	1400)
- area in which i/P 2, 0/P, are connected	
- data plays irroperations of	
- serial port, USB-type A, K	social, alisplay post, HDM
Etheronet post,	
- Ioport	
social -> bit by bit (internet)	
Parallel -> Stoop o	+ bits (Assignment)
Parts of MP Data bus (Bidirectional) RAM ROM Times CPO Control I/O Seeial Parallel Address bus (one directional) Peripherals (Extranals) Ports of MC:- CPU RAM ROM Times Jing ce chip Parallel	
Difference b/co MC and MP:	
MP	MC
1. CPO-standalone	1. All one in 1 chip
RAM, RON, Times, Sou ial/parallel L) separate	
2 Increase the 1802 of memory	2. Fixed
RAM & ROM	3. Specific
3. General purpose	4. Not
4. Expen sive	5
5. Versatility	

Applications of Mc:-
Home appliances _ Fridge
- Office - carnera, - printer Mechanical - Automatic machines
- Alto bags in cary
8051 Mc family - 8051 - 7/109 80 series - Motorolla 6811 - PIC 8051 Microp controlled - MC51 series Intel, 1981 (MCS-51) - Atmel 8057 - Atmel 8057 - 8051 - 4K - 128bytes - 32 lines - 2 - 1 - 8052 - 8K - 856bytes - 82 lines - 3 - 1 - 8053 - 0K - 128bytes - 32 lines - 2 - 1 - 8053 - 0K - 128bytes - 32 lines - 2 - 1
(*) 805) is a subset of 8052. ROM & RAM: - ROM (Read only Memory) / code memory - ROM (Read only Memory) / code memory - Storing the problem (specific Application) - Storing the problem (specific Application) - RAM (Random Access Memory) / Data memory - Read & write - 128 Bytes - Data essential too the problem (ROM) will be stored.

Ports: - 4 poots - Each point is B bit / 8 ling - 32 lines used too I/o devices Times / counter - Timers O - Timer1 Serial port-- Bit by bit commonication Features - 4k built in ROM/coole/propostar memory. - 128 bytes of built in RAM/doctor marrory - 4 I/o posts, each post & pin (PO, PI, P2, P3) - Full dupler WART (universel asynchronous Receiver and Transmitter) - TV, Radio - House way constrained Duplex -wallie talkie -> Half deplex _cell phore/small -> Full display - 6 sources/5 vectored interestiple - GAIK of External ROM can be connected. - 64k of external RAM can be connected 8651 - Basic Lamponents 4K ROM 图128 byres RAM RAM ROM CPO 4 I/O Ports LPD-P3> Int 6/5 Interroup

serial commonication

single chip



+Vcc (+5V) 40 39 00 0.1 30 POOE 1 1.3 0.2 (I/O) 1.4 36 Address Bus 1.5 0.4 35 1.6 0.5 34 33 9 RST 32 10 EA/VPP 31 ALE / PROY 11 Interret INTO -38.2 12 29 PSEN 13 14 A8-A15 26 (Address 2.4 25 lines) 24 2.3 17 28 2.2 xtal2-2.1 Xtall -21 2.0 4ND - 20 Former supply -> GND (20) +Vcc (+5V) (40) > Mal ((19) =) inoscles coystal osuillators connection (2plns) xtal 2 (18) Reset (RST) =>(9) Post1 -> external memora (External)

PSEN - propriare status enable Pin (29) [1- R

ALE - Address Latch enable [0-data =) Port O

1-Address

EA - External Access [0- External memory

1- Internal memory

-> 21-28

Port 2