Here’s the **format** for each commonly used SFR in the 8051 microcontroller, showing their bit definitions:

**1. Program Status Word (PSW - Address: D0H)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Name | CY | AC | F0 | RS1 | RS0 | OV | - | P |

* **CY**: Carry flag (used in arithmetic operations).
* **AC**: Auxiliary carry (used in BCD operations).
* **F0**: User-defined flag.
* **RS1, RS0**: Register bank select bits (to select one of the four register banks).
* **OV**: Overflow flag.
* **P**: Parity flag (1 if the number of 1s in ACC is odd, otherwise 0).

**2. Timer Mode Register (TMOD - Address: 89H)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Timer** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Timer 1 | GATE1 | C/T1 | M1\_1 | M0\_1 | Timer 0 | GATE0 | C/T0 | M1\_0 |

* **GATE1/GATE0**: Enables or disables the timer via the external pin.
* **C/T1/C/T0**: Selects Counter (1) or Timer (0) mode.
* **M1/M0**: Selects the timer mode (Mode 0, 1, 2, or 3).

**3. Timer Control Register (TCON - Address: 88H)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Name | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 |

* **TF1, TF0**: Timer 1 and Timer 0 overflow flags.
* **TR1, TR0**: Timer 1 and Timer 0 run control bits.
* **IE1, IE0**: External interrupt flags.
* **IT1, IT0**: External interrupt type control (1 = edge-triggered, 0 = level-triggered).

**4. Serial Control Register (SCON - Address: 98H)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Name | SM0 | SM1 | SM2 | REN | TB8 | RB8 | TI | RI |

* **SM0, SM1**: Selects serial communication mode (Mode 0, 1, 2, or 3).
* **SM2**: Enables multiprocessor communication.
* **REN**: Receiver enable.
* **TB8, RB8**: 9th data bit for transmission and reception in Mode 2/3.
* **TI**: Transmit interrupt flag.
* **RI**: Receive interrupt flag.

**5. Interrupt Enable Register (IE - Address: A8H)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Name | EA | - | ET2 | ES | ET1 | EX1 | ET0 | EX0 |

* **EA**: Global interrupt enable (1 = enable all interrupts, 0 = disable all interrupts).
* **ET2**: Enable Timer 2 interrupt.
* **ES**: Enable serial port interrupt.
* **ET1, ET0**: Enable Timer 1 and Timer 0 interrupts.
* **EX1, EX0**: Enable external interrupts 1 and 0.

**6. Port Latches (P0, P1, P2, P3 - Addresses: 80H, 90H, A0H, B0H)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Name | Pn.7 | Pn.6 | Pn.5 | Pn.4 | Pn.3 | Pn.2 | Pn.1 | Pn.0 |

* **Pn.m**: Indicates the m-th bit of port n (Port 0, 1, 2, or 3).

**7. Interrupt Priority Register (IP - Address: B8H)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Name | - | - | PT2 | PS | PT1 | PX1 | PT0 | PX0 |

* **PT2**: Timer 2 priority.
* **PS**: Serial port priority.
* **PT1, PT0**: Timer 1 and Timer 0 priorities.
* **PX1, PX0**: External interrupts 1 and 0 priorities.

These formats provide precise bit-level control over 8051 functionality, making it a versatile microcontroller for embedded applications.