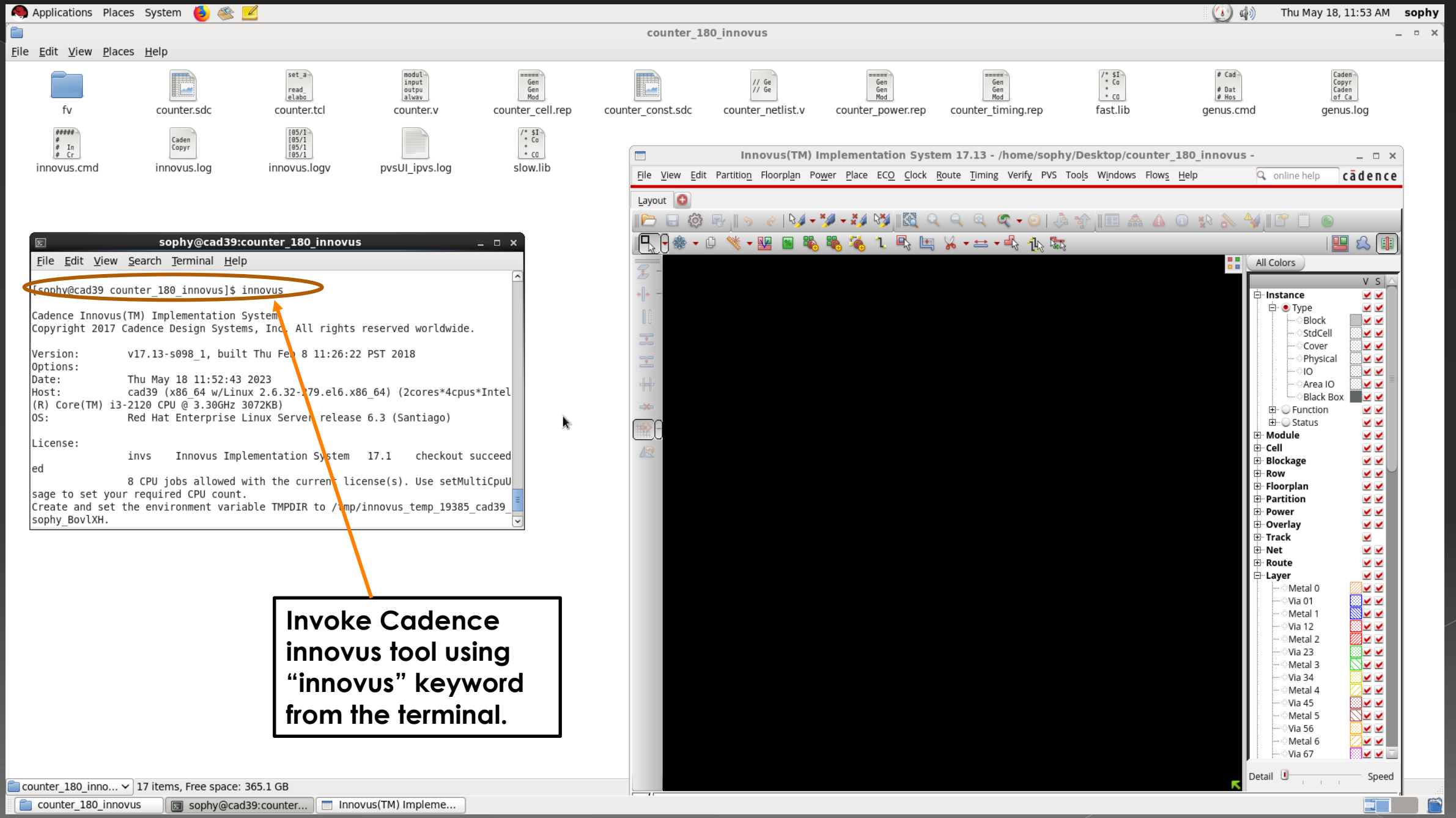
CADENCE INNOVUS

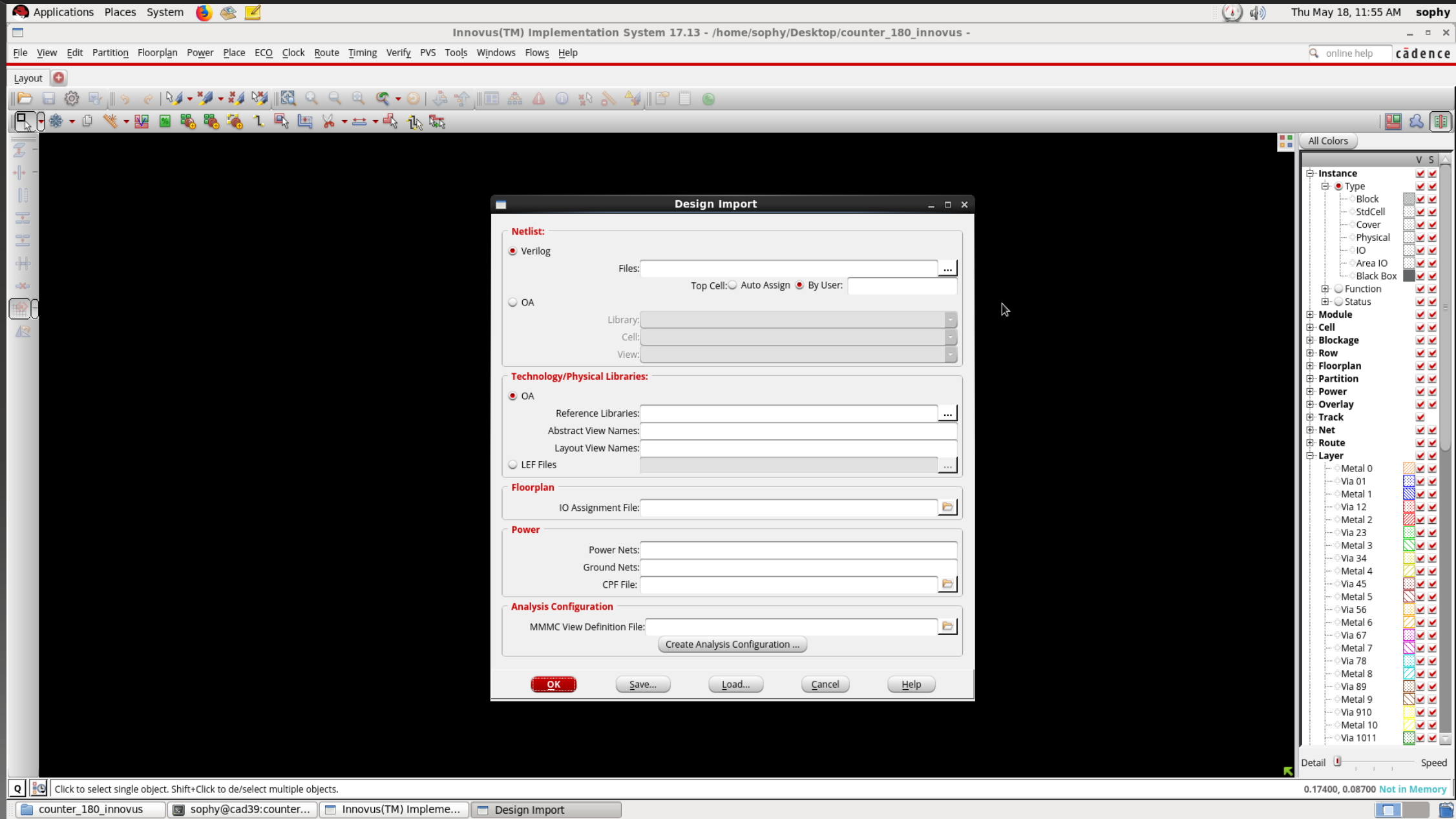
WORK FLOW

PREREQUISITE

- Netlist - post synthesis
- Constraint file - post synthesis
- Library files (slow.lib, fast.lib)
- LEF file

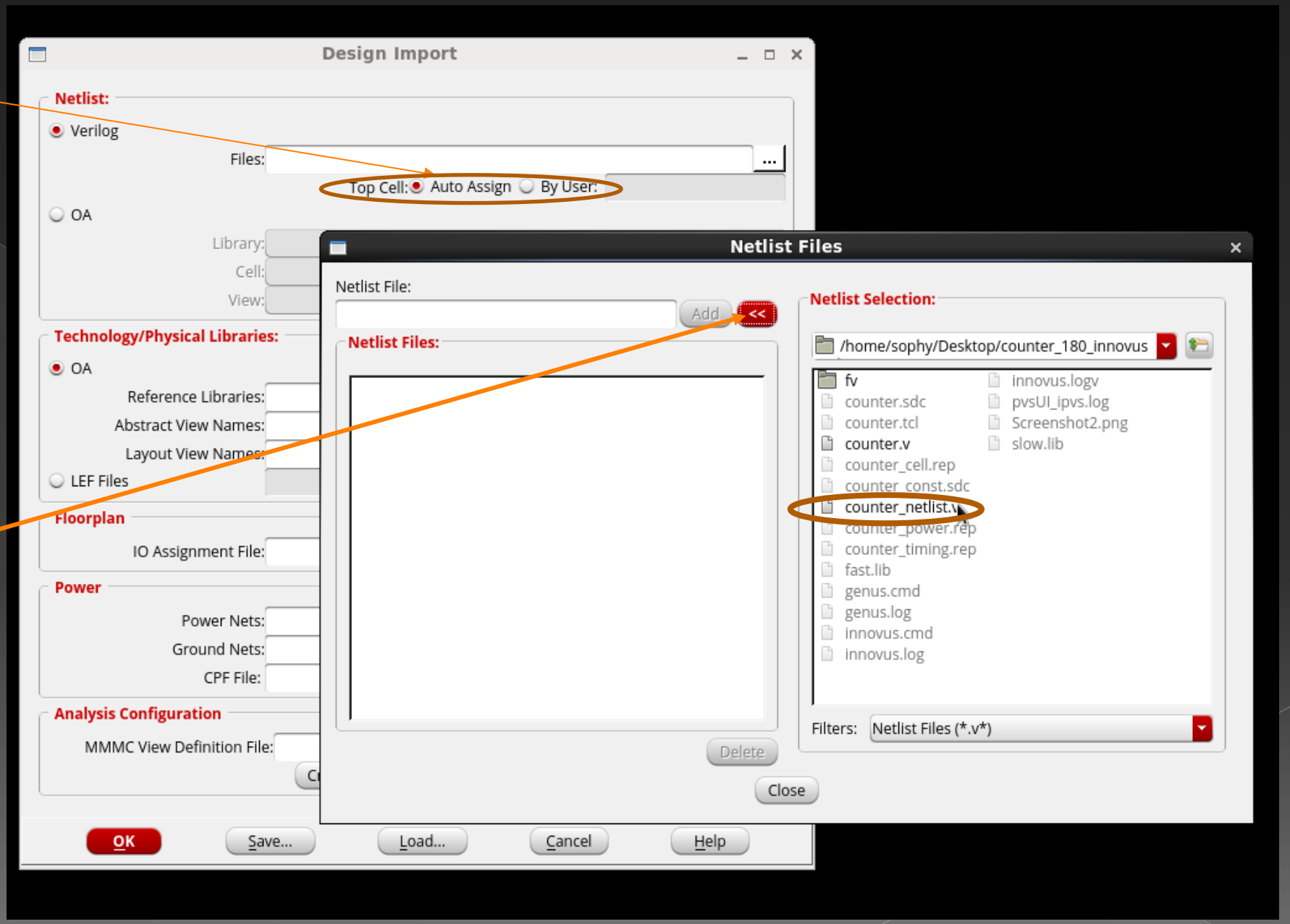

Applications Places System
Thu May 18, 11:53 AM sophy
counter_180_innovus
File Edit View Places Help
fv
counter.sdc
counter.tcl
counter.v
counter_cell.rep
counter_const.sdc
counter_netlist.v
counter_power.rep
counter_timing.rep
fast.lib
genus.cmd
genus.log
innovus.cmd
innovus.log
innovus.logv
pvsUI_ipvs.log
slow.lib
sophy@cad39:counter_180_innovus
File Edit View Search Terminal Help
[sophy@cad39 counter_180_innovus]$ innovus
Cadence Innovus(TM) Implementation System
Copyright 2017 Cadence Design Systems, Inc. All rights reserved worldwide.
Version: v17.13-s098_1, built Thu Fe 8 11:26:22 PST 2018
Options:
Date: Thu May 18 11:52:43 2023
Host: cad39 (x86_64 w/Linux 2.6.32-279.el6.x86_64) (2cores*4cpus*Intel
(R) Core(TM) i3-2120 CPU @ 3.30GHz 3072KB)
OS: Red Hat Enterprise Linux Server release 6.3 (Santiago)
License:
invs Innovus Implementation System 17.1 checkout succeed
ed
8 CPU jobs allowed with the curren license(s). Use setMultiCpuU
sage to set your required CPU count.
Create and set the environment variable TMPDIR to /tmp/innovus_temp_19385_cad39_
sophy_BovlXH.
Invoke Cadence innovus tool using “innovus” keyword from the terminal.
Innovus(TM) Implementation System 17.13 - /home/sophy/Desktop/counter_180_innovus -
File View Edit Partition Floorplan Power Place ECO Clock Route Timing Verify PVS Tools Windows Flows Help
online help
cadence
Layout
All Colors
Instance
Type
Block
StdCell
Cover
Physical
IO
Area IO
Black Box
Function
Status
Module
Cell
Blockage
Row
Floorplan
Partition
Power
Overlay
Track
Net
Route
Layer
Metal 0
Via 01
Metal 1
Via 12
Metal 2
Via 23
Metal 3
Via 34
Metal 4
Via 45
Metal 5
Via 56
Metal 6
Via 67
Detail
Speed
counter_180_inno...
17 items, Free space: 365.1 GB
counter_180_innovus
sophy@cad39:counter...
Innovus(TM) Impleme...

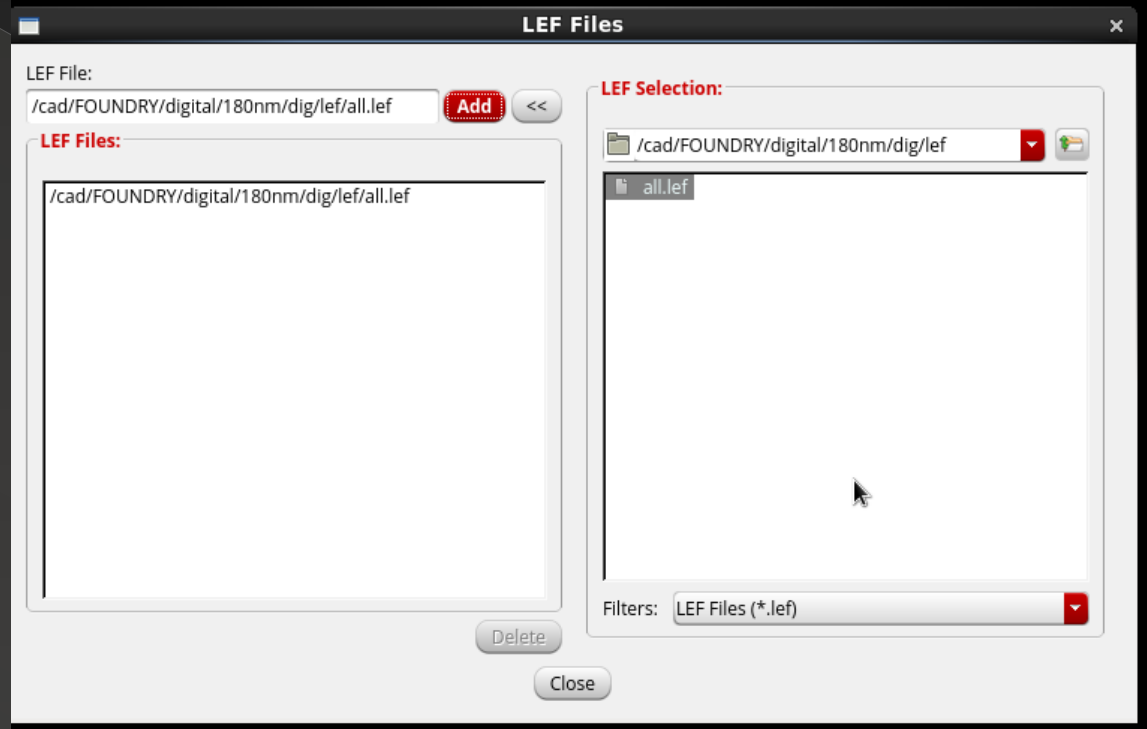
Goto File → Import Design

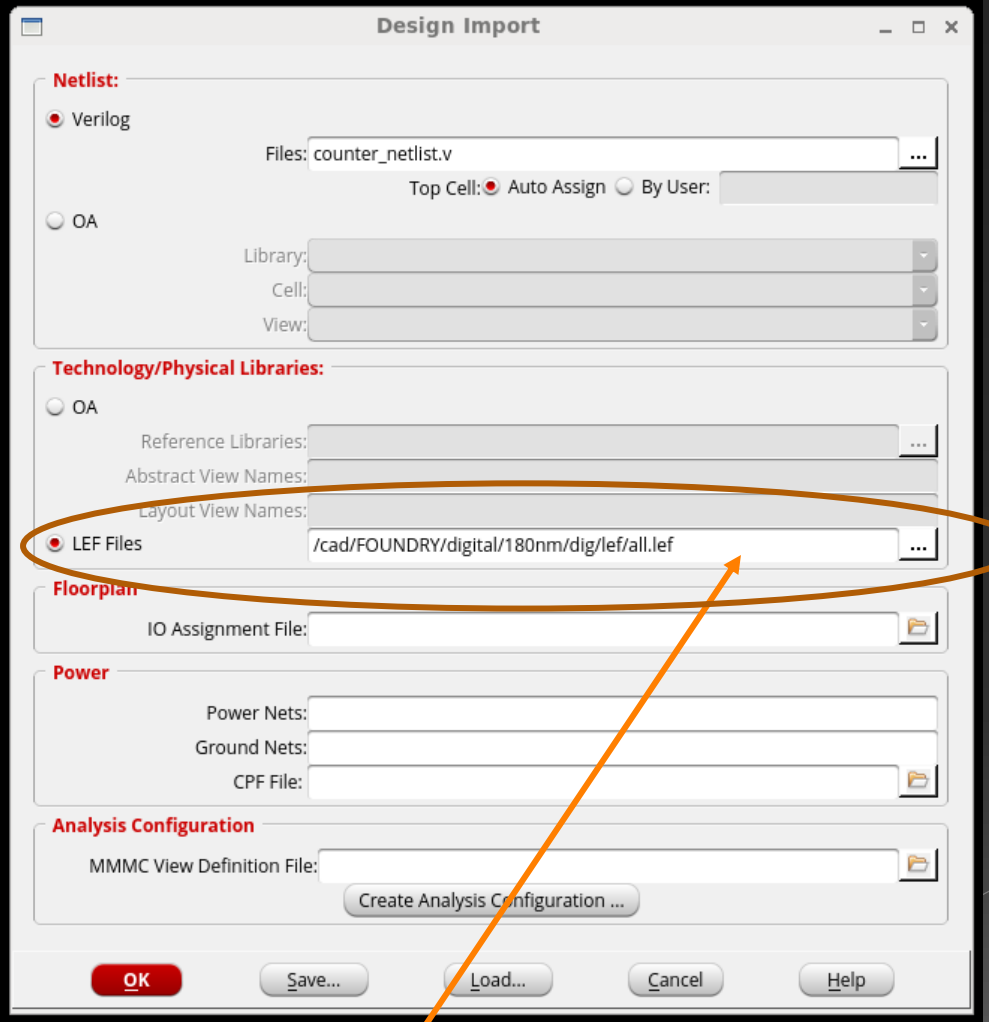


Check on “Auto Assign”

Add the netlist file for the design

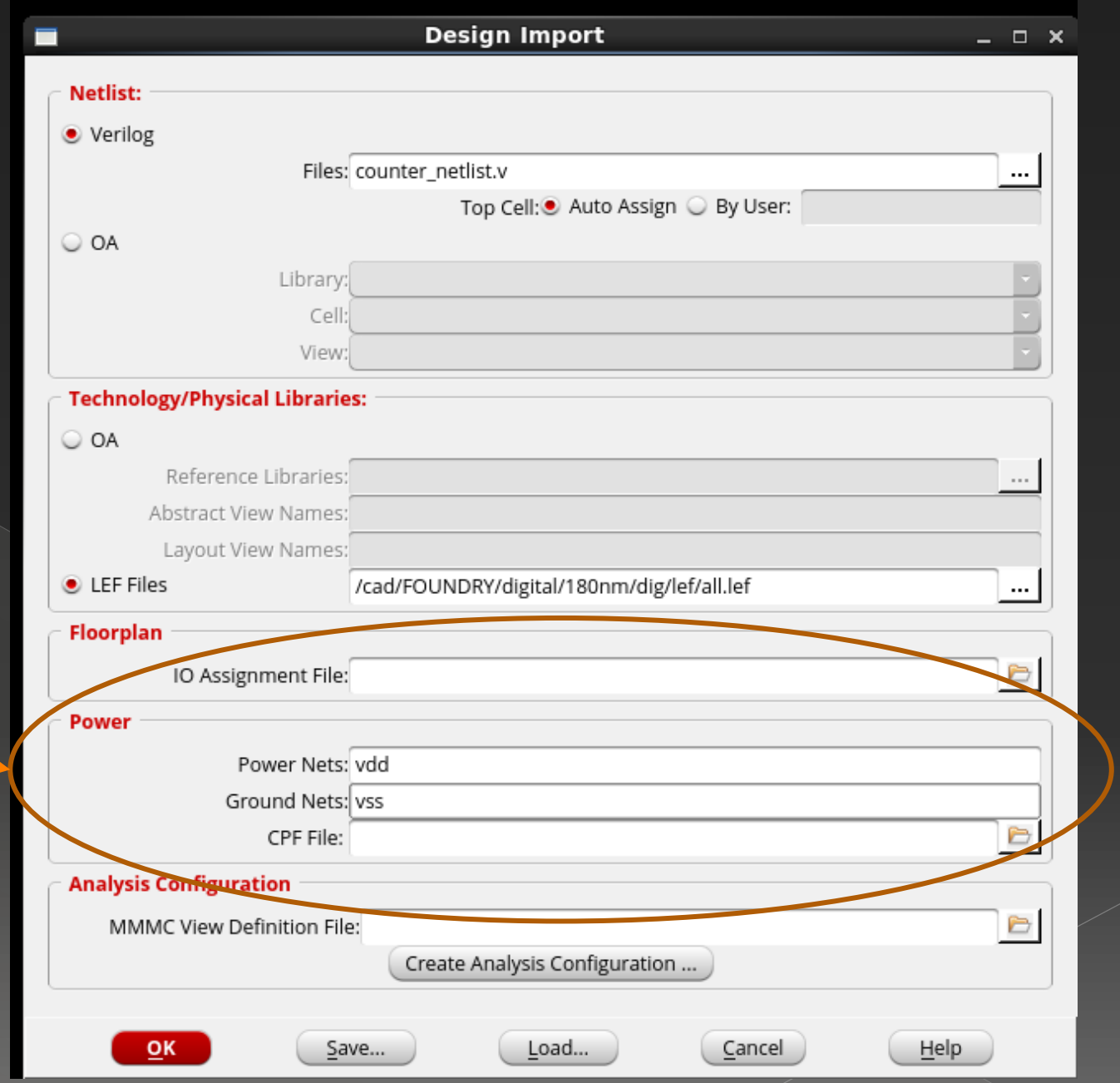






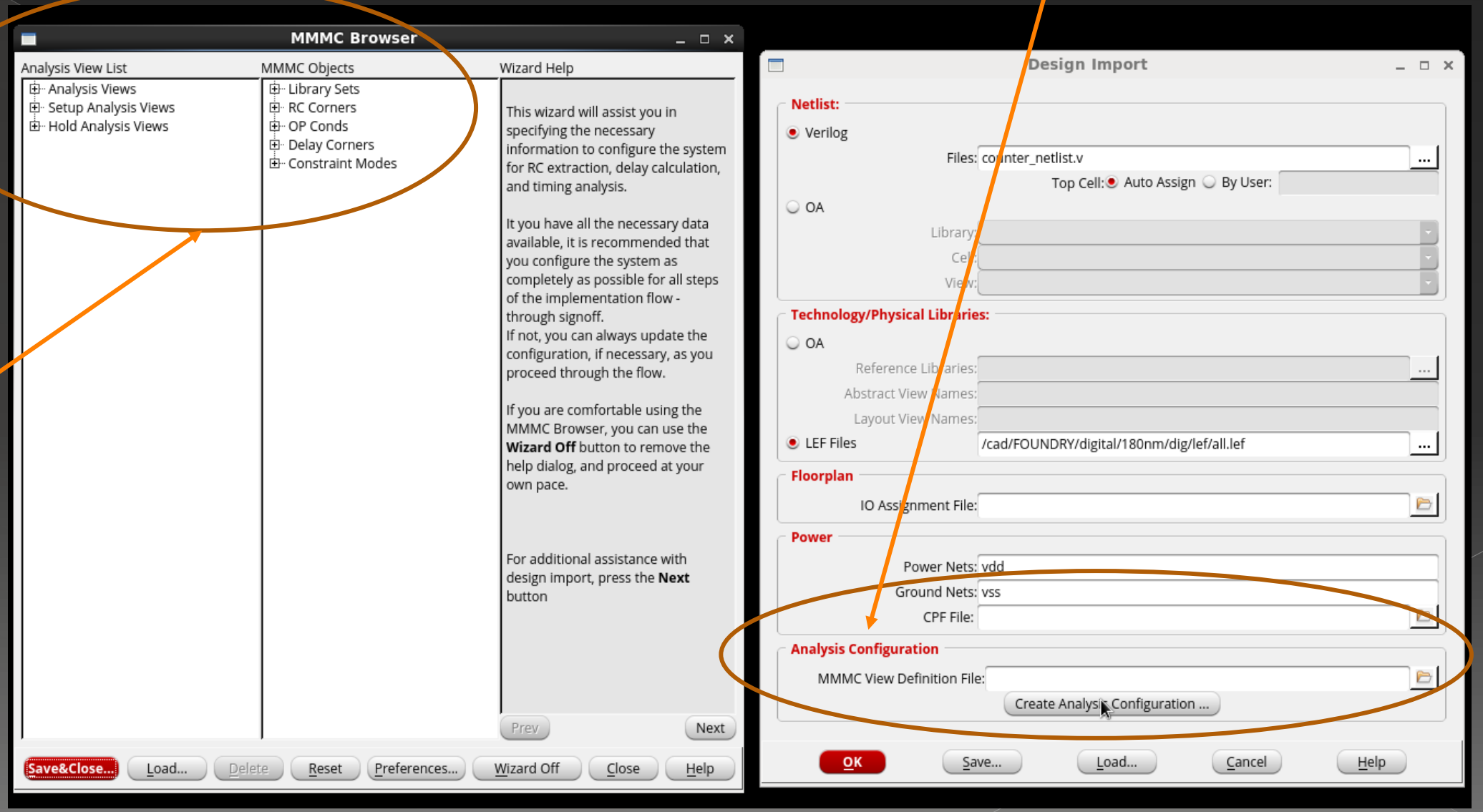
Add LEF file from …./CAD/FOUNDRY/180NM/dig/lef/all.lef

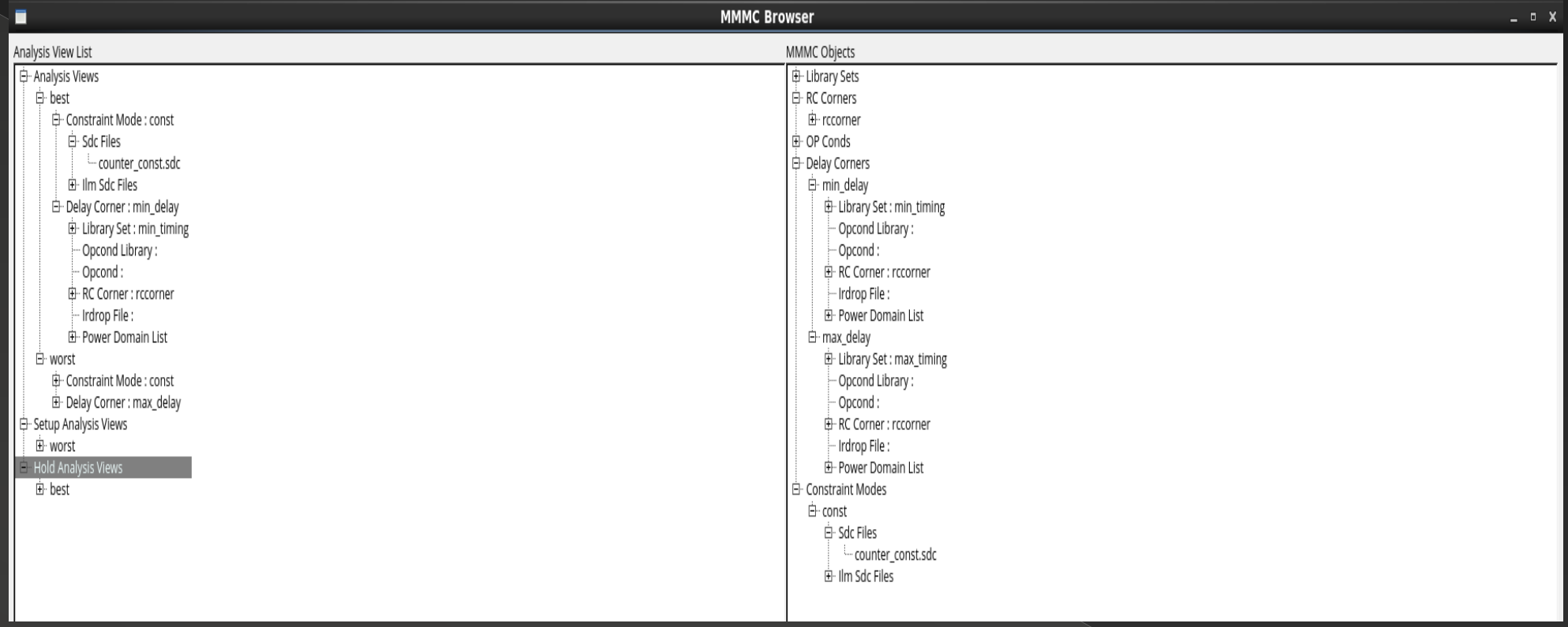
Specify the Power Nets as "vdd" and Ground Nets as "vss"



1. Customize “MMMC objects” and “Analysis views” by clicking on “Create Analysis Configuration”

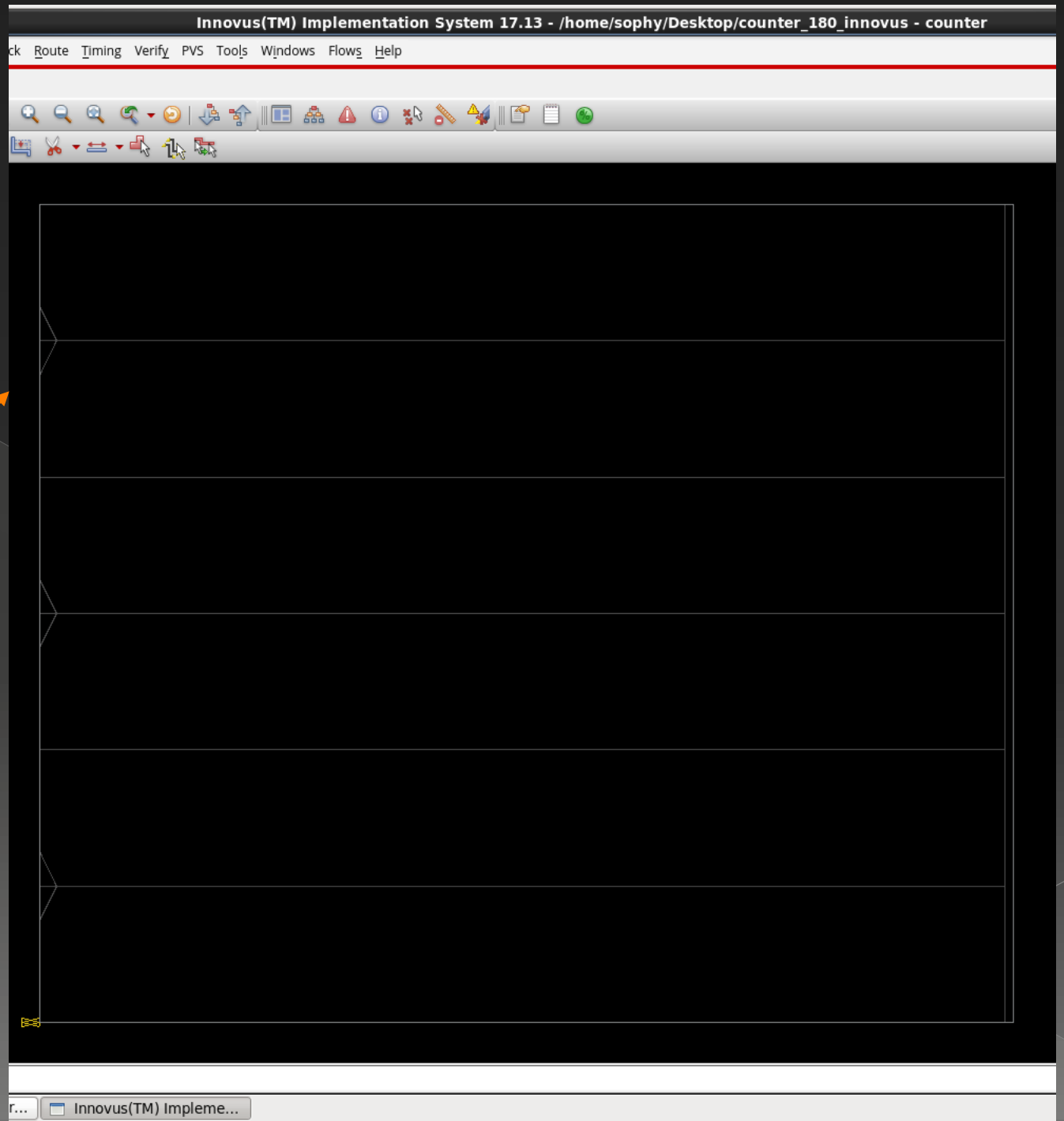
2. Define
- Library Sets
- RC Corners
- Delay Corners
- Constraint Modes
- Analysis Views
- Setup Analysis Views
- Hold Analysis Views

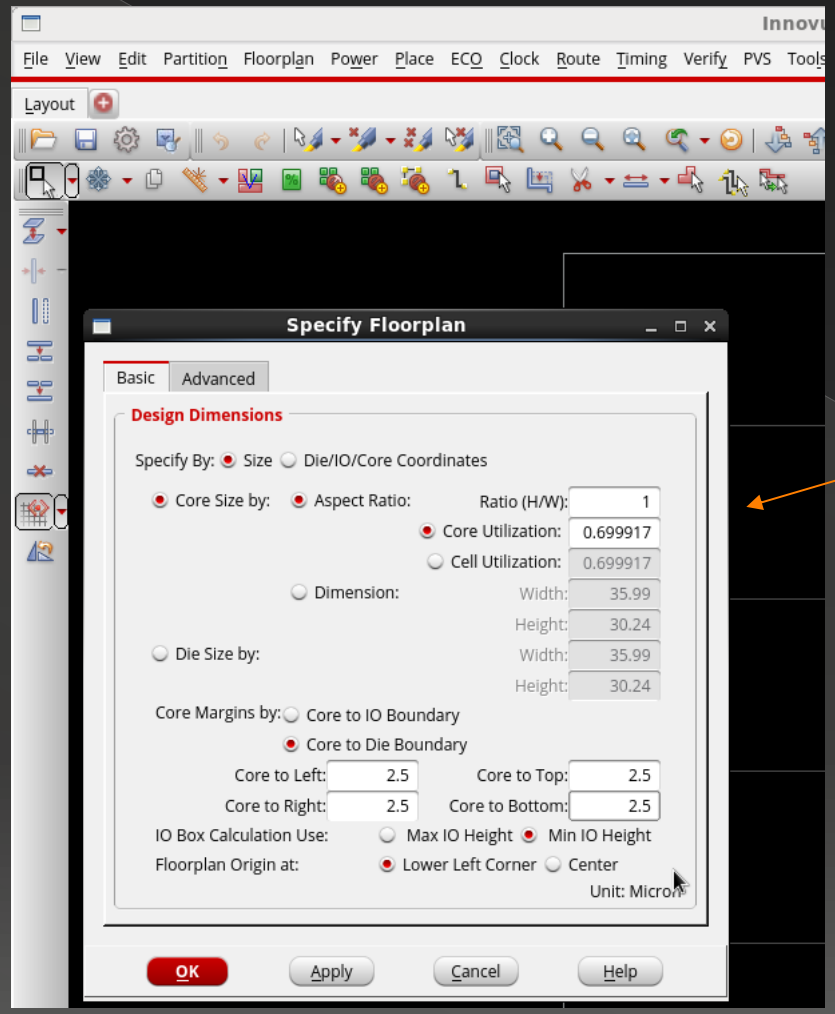




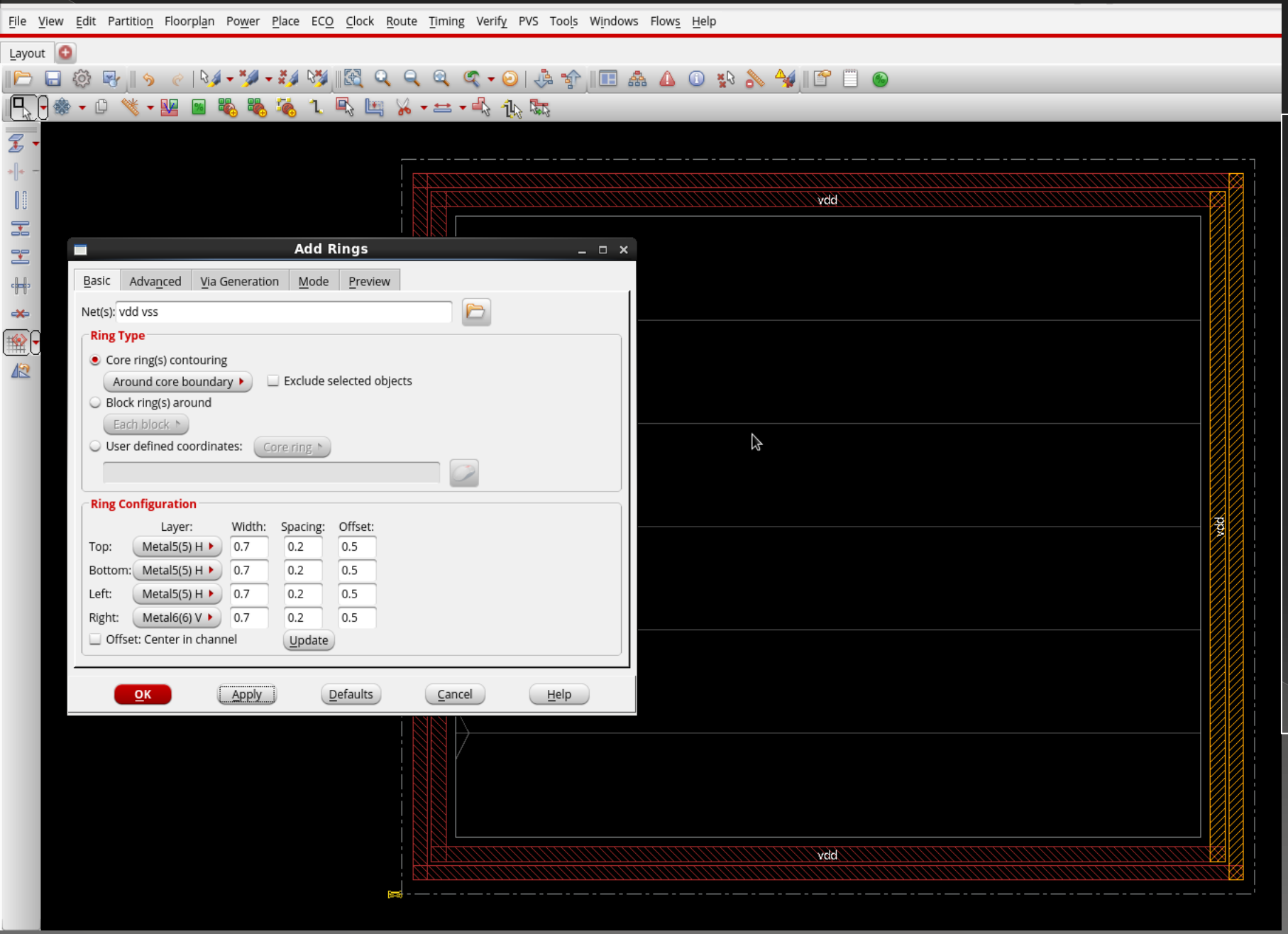
1. In MMMC browser double click on library sets -> Give a name ‘min_timing’ -> Browse and take fast.lib -> Add and press Ok. Similarly do for ‘max_timing’ and choose slow.lib.
2. In RC corner -> Double click. Give some name ‘rccorner’ and choose ‘captable’ from “…./cad/foundry/180nm/dig/captable/*.tbl”
3. In Delay corner -> Double click and choose ‘min_delay’, choose library set ‘min_timing’. Similarly do for ‘max_delay’, choose ‘max_timing’.
4. Double click constraint mode -> Give some name ‘constraints’. Browse and take .sdc file
5. Double click DC Analysis views. Type ‘best_case’ and choose ‘min_delay’ from the drop down list. Similarly type ‘worst_case’ and choose ‘max_delay’
6. In Setup, double click and choose worst case. In Hold, double click and choose best case.

Now the Innovus GUI will look like this

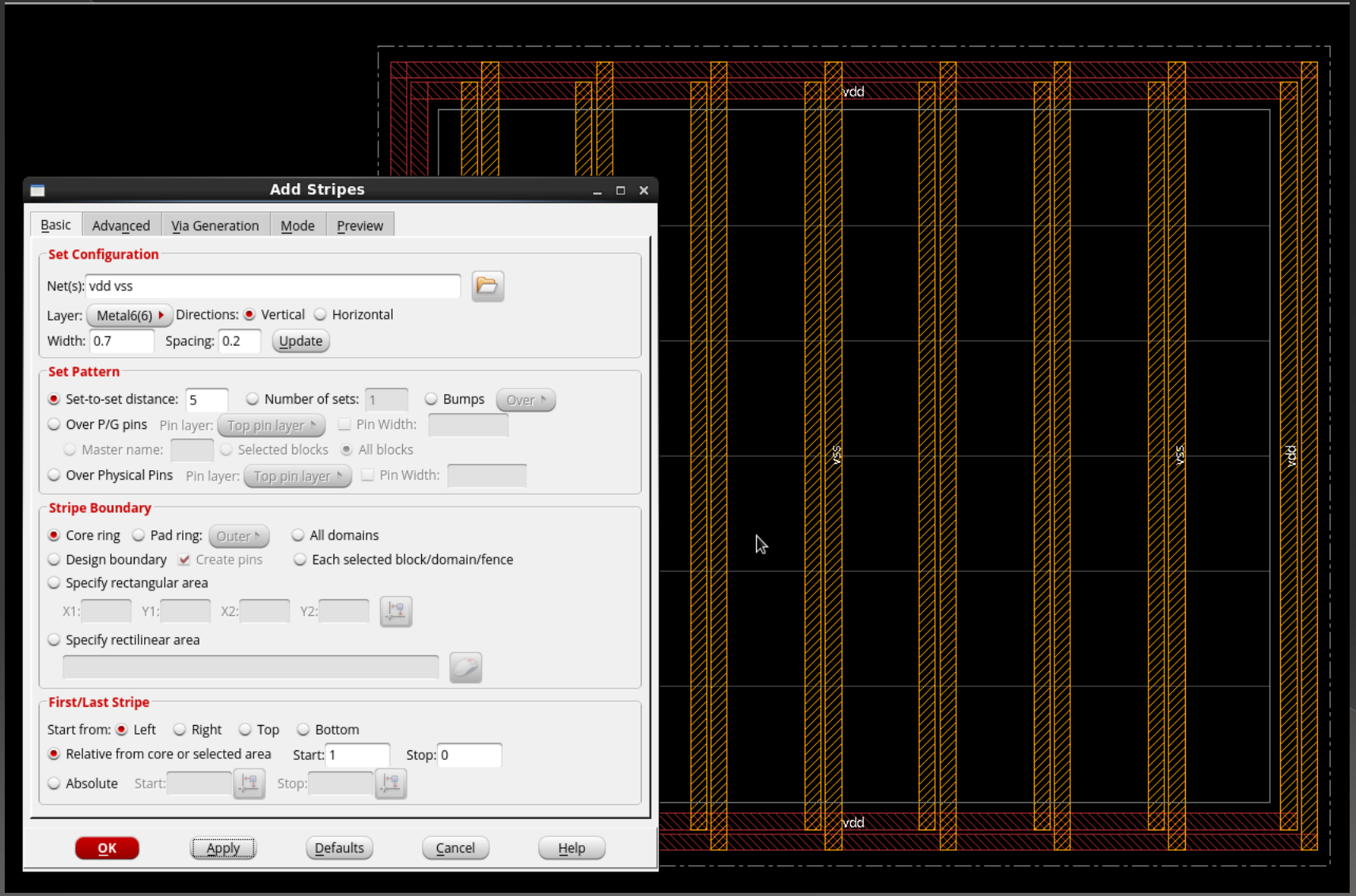




Go to floorplan. Specify Floorplan -> Set Aspect ratio to 1 and put all 'Core to Die Boundary" to 2.5 and click Ok.

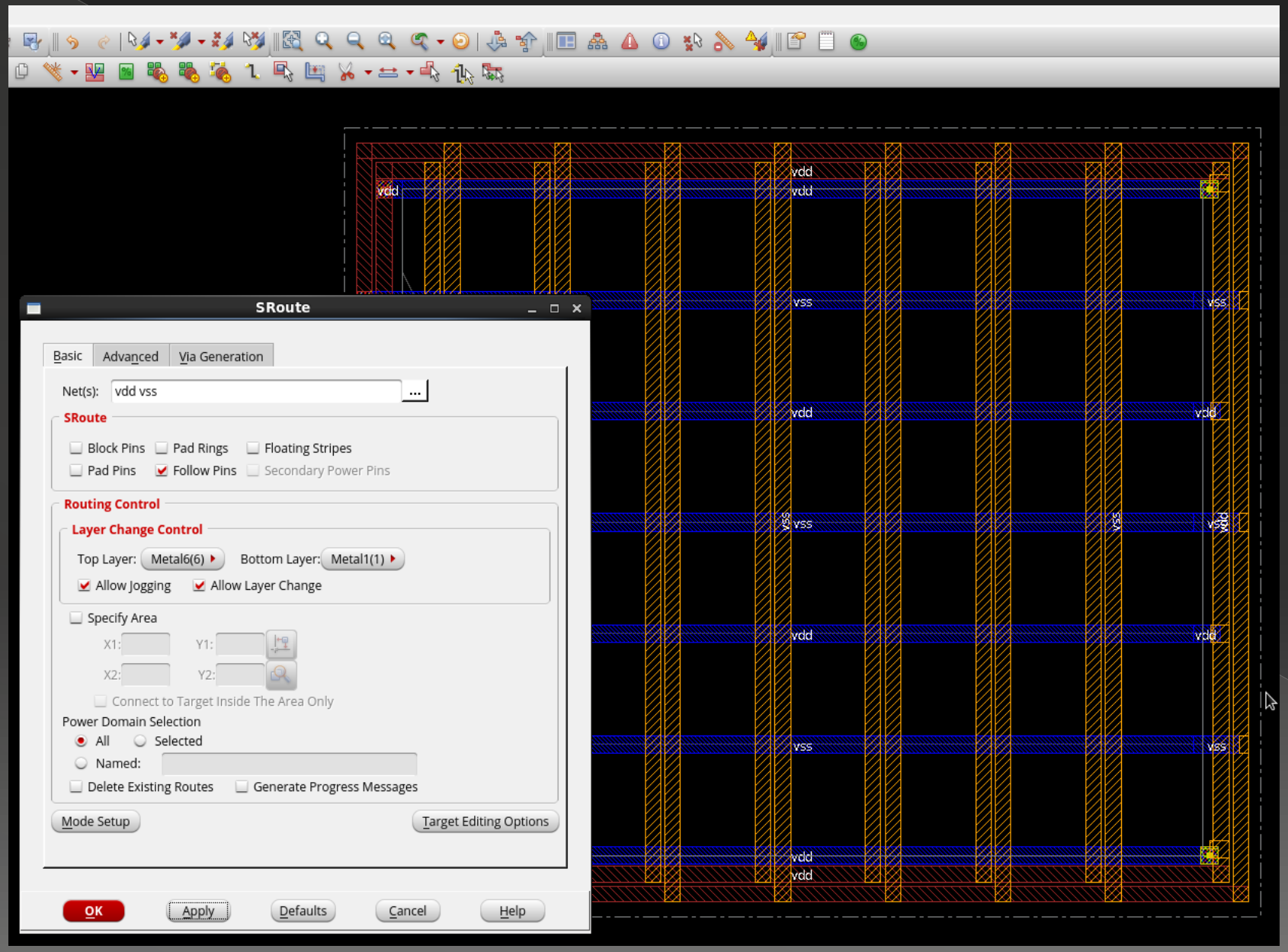


Go to Power -> Power planning -> Add ring -> Nets – VDD VSS (type it). For power we use the top most metal layer (top & bottom choose Metal 5, left & right choose Metal 6). Make all width to 0.7, spacing 0.2 and Offset to 0.5. Click Ok.

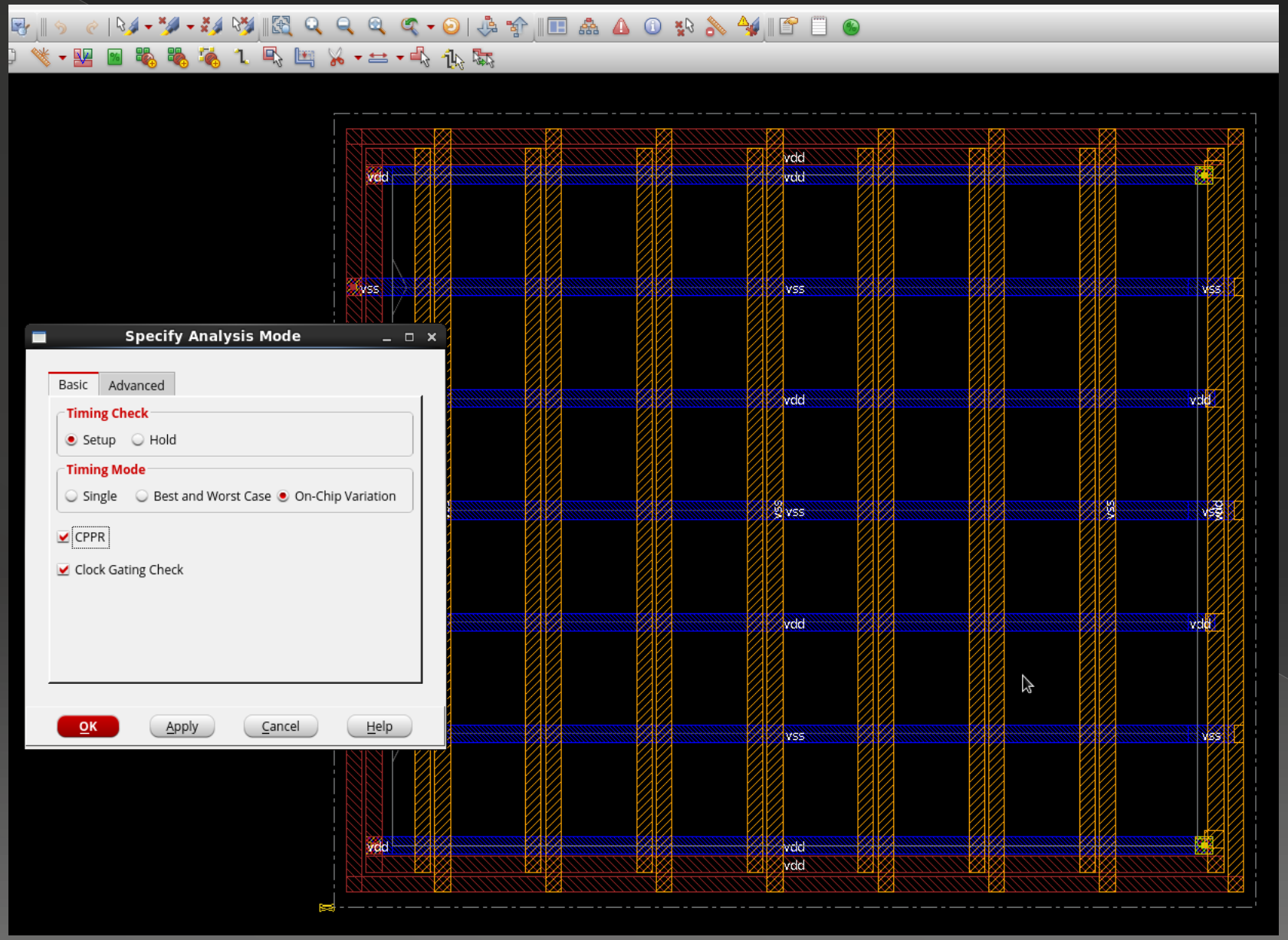


Again go to Power -> Power Planning -> Add Stripes -> Nets – vdd vss(type it) -> Choose Metal 6, Vertical and set width to 0.7 and space to 0.2.

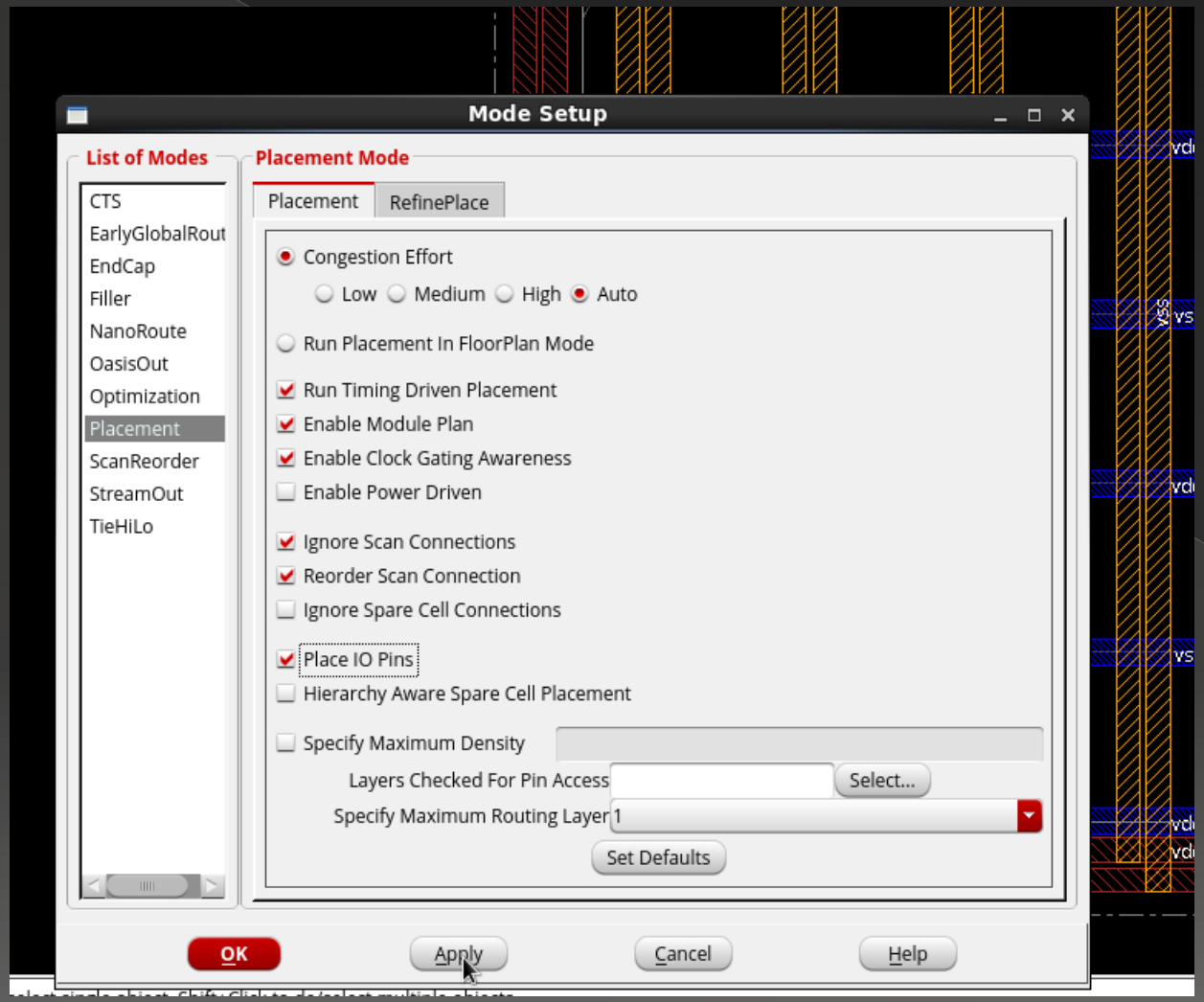
Click ‘Set-to-set to 5. Set Start to 1 and Stop to 0 at the bottom(First and last stripe)



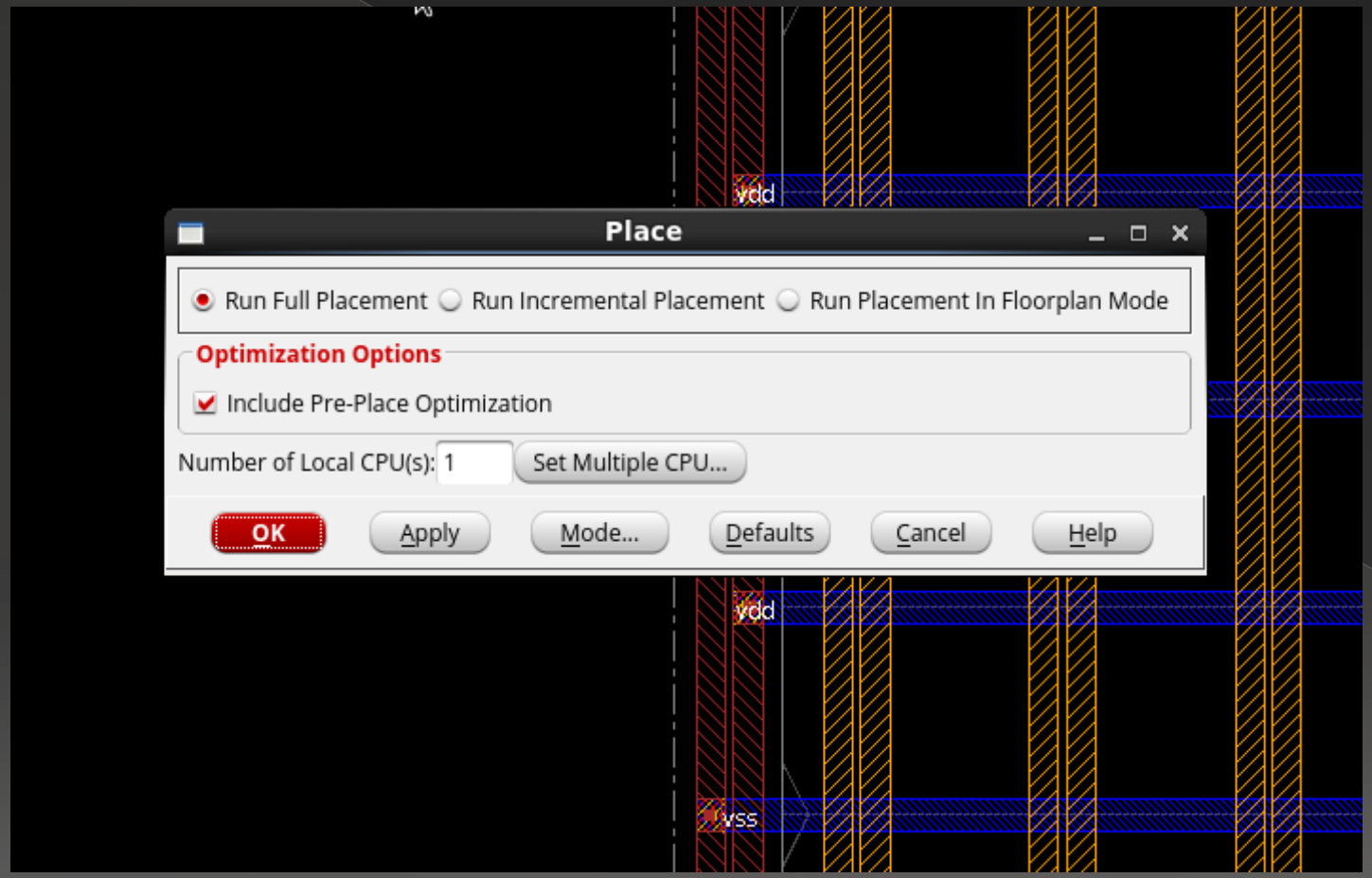
Go to Route -> Special route -> Nets – vdd vss (type it) and press Ok
Uncheck all except ‘Follow Pins’ in SRoute



Go to tools -> Set mode -> Specify analysis mode -> in that enable OCV and CPPR

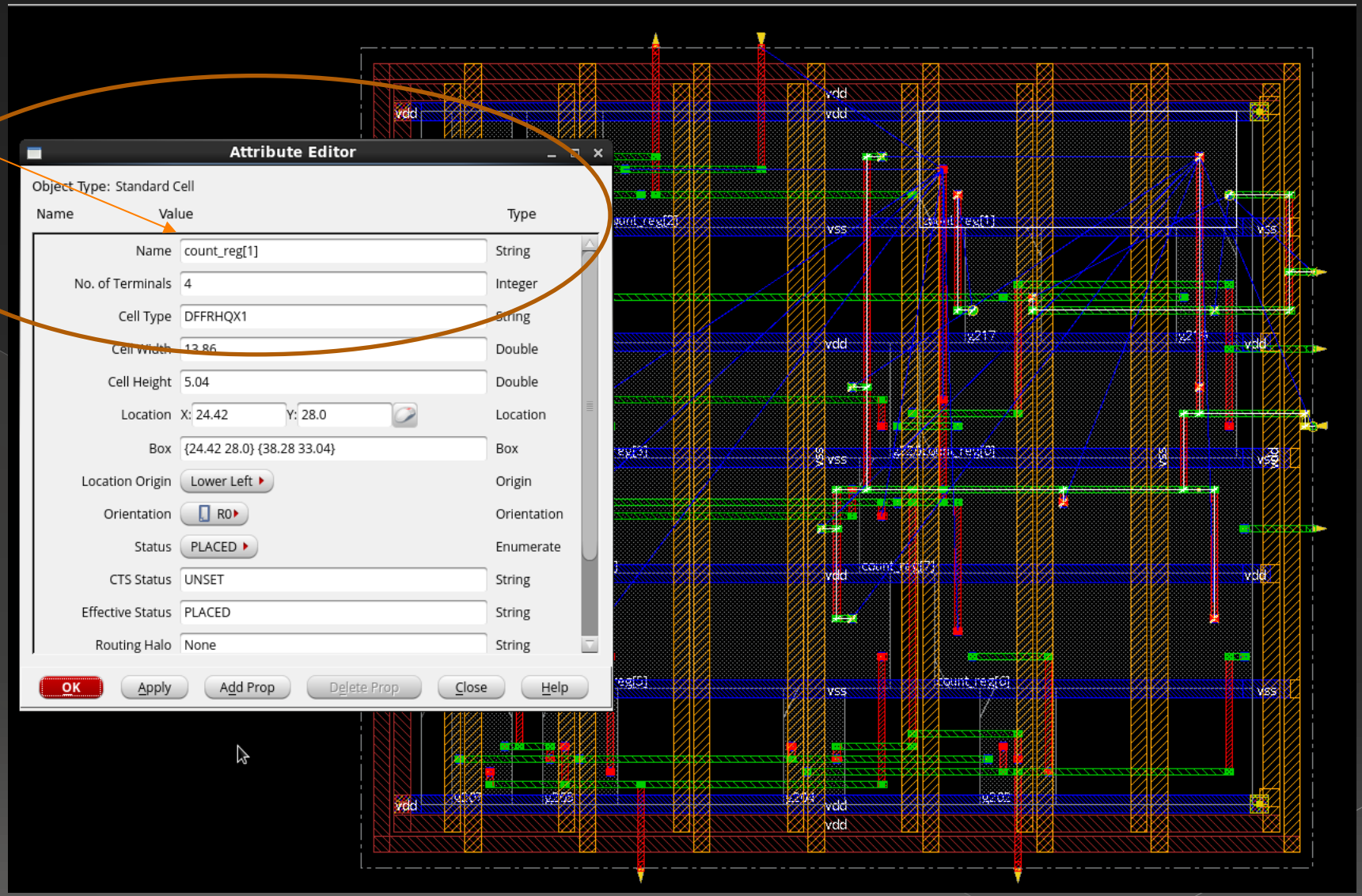


Go to tools -> Set mode -> Mode setup -> Click on Placement and enable I/O pins and press Ok



Now go to Place -> Standard Cell -> Click Ok.

1. View Post Standard Cell Placement.
See that standard cell for ‘count_reg[1]’ is placed.

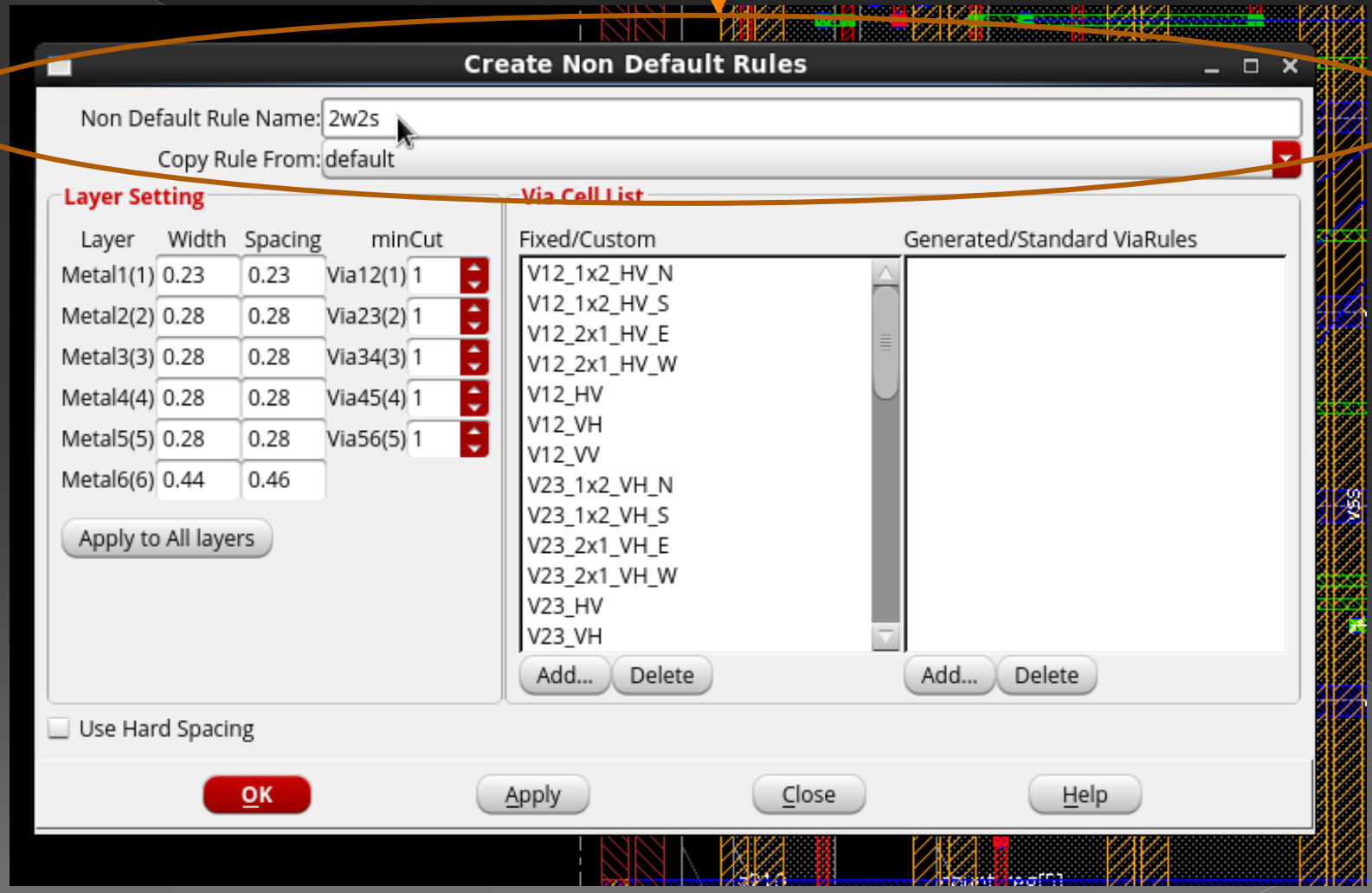


2. Go to timing -> report timing, choose pre CTS and do for both setup and hold one by one.
A timing report named folder gets generated.
Check for values of setup and hold slack whether they are positive or not.

Do Clock Tree Synthesis (CTS)

EDit

1. Goto Edit --> create non default rule --> 2w2s

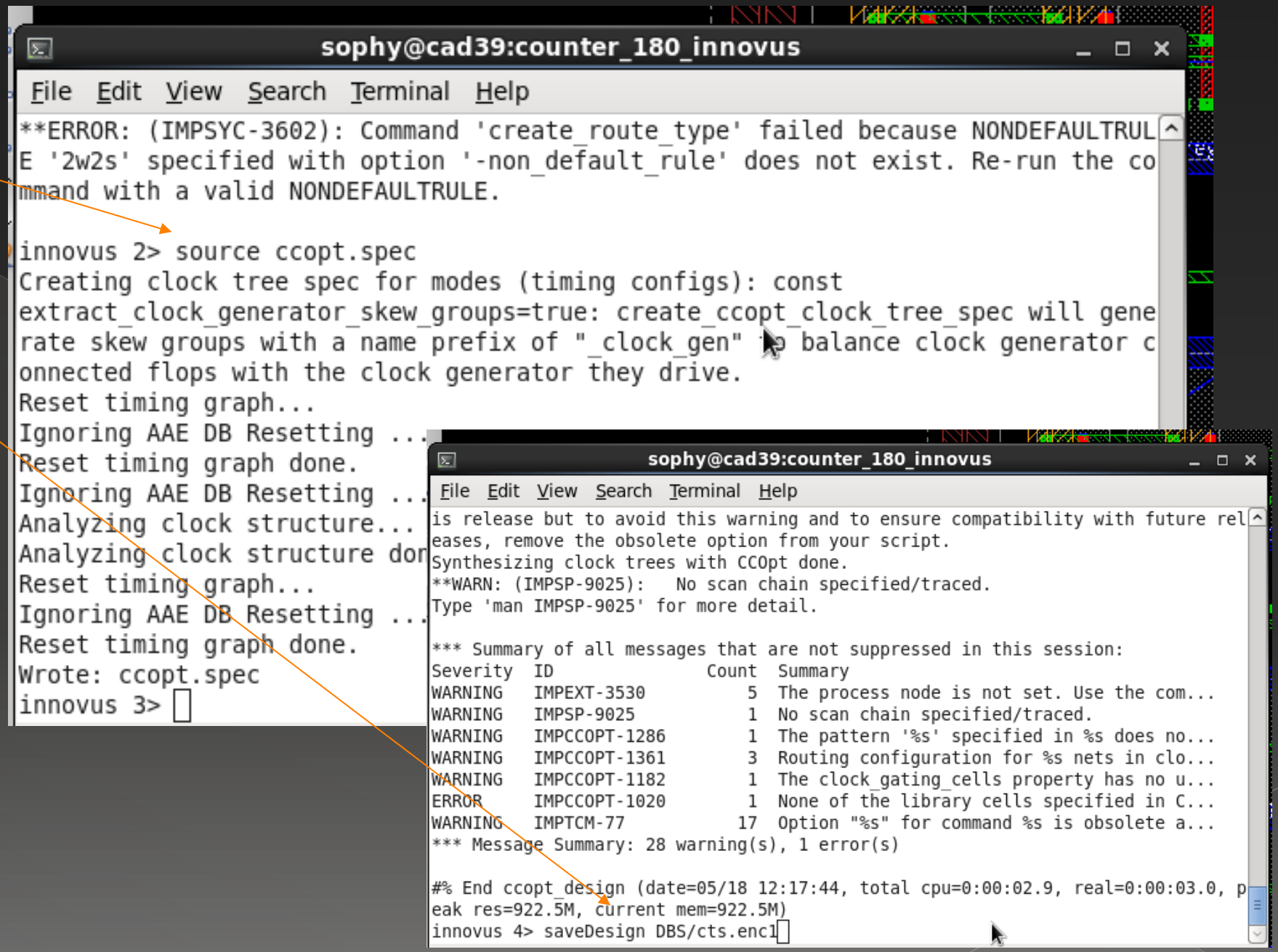


2. Write a CTS script file with following content and save it as ‘ccopt.spec’

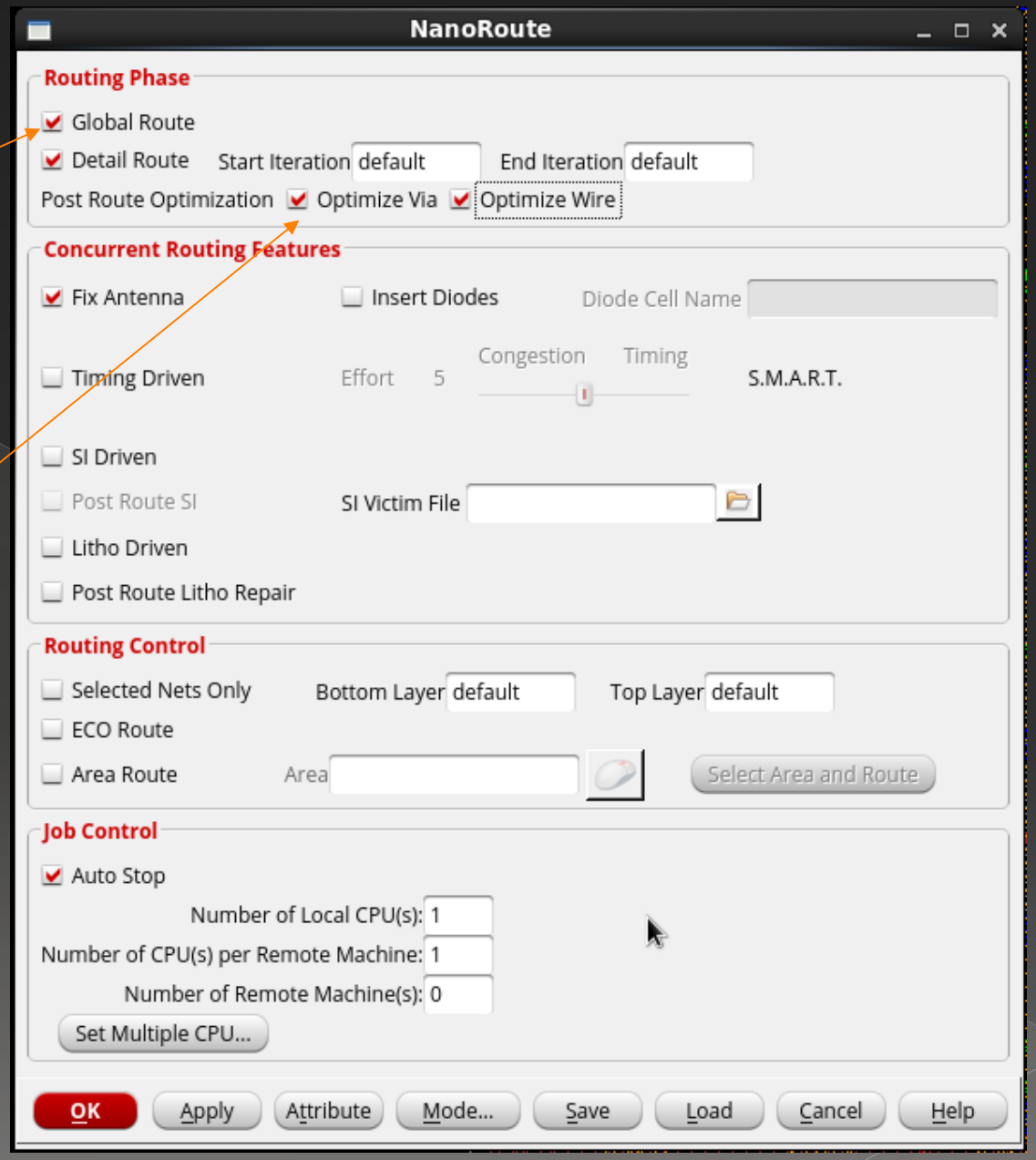
```
create_route_type -name clkroute -non_default_rule 2w2s -bottom_preferred_layer Metal5 -top_preferred_layer Metal6
set_ccopt_property route_type clkroute -net_type trunk
set_ccopt_property route_type clkroute -net_type leaf

##Specify Buffers Inverters and Clock Gating
set_ccopt_property buffer_cells {CLKBUFX2 CLKBUFX4}
set_ccopt_property inverter_cells {CLKINVX2 CLKINVX4}
set_ccopt_property clock_gating_cells TLATNTSCA*

##Generate the ccopt file and source it
create_ccopt_clock_tree_spec -file ccopt.spec
```

In the terminal
>source ccopt.spec
****RUN CTS****
>ccopt_design –cts

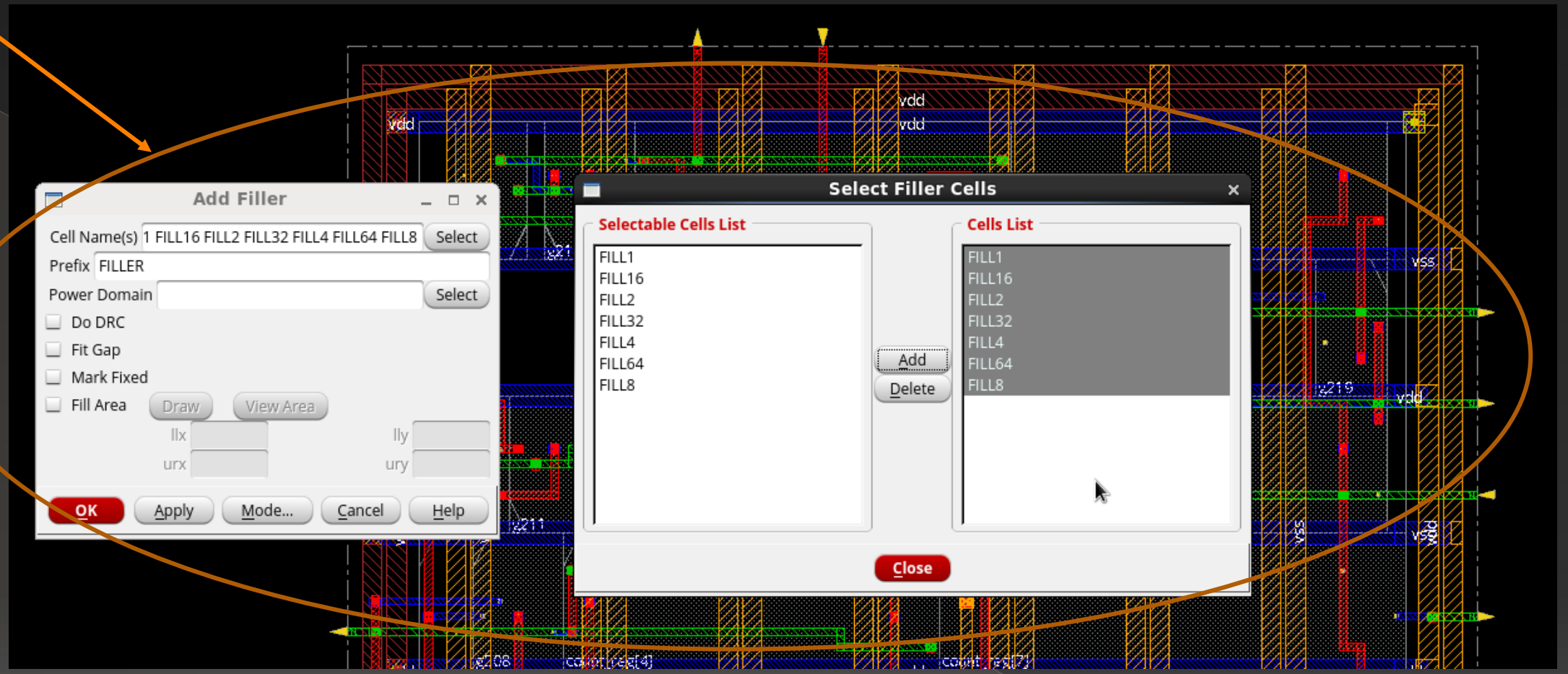
****SAVEDESIGN*****
>saveDesign
DBS/cts.enc1



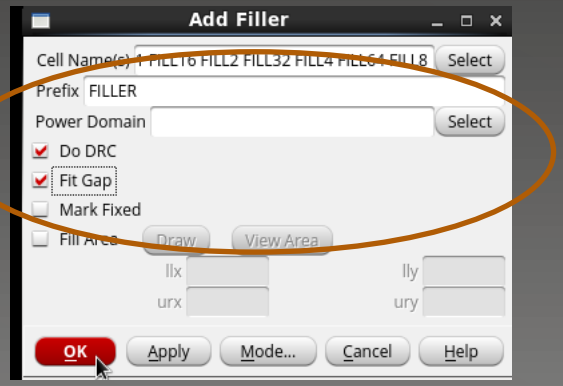
1. Go to Place -> Nano route -> Route (both global and detailed routing done in this step).
2. Enable Optimize via and Optimize wire and Click Ok



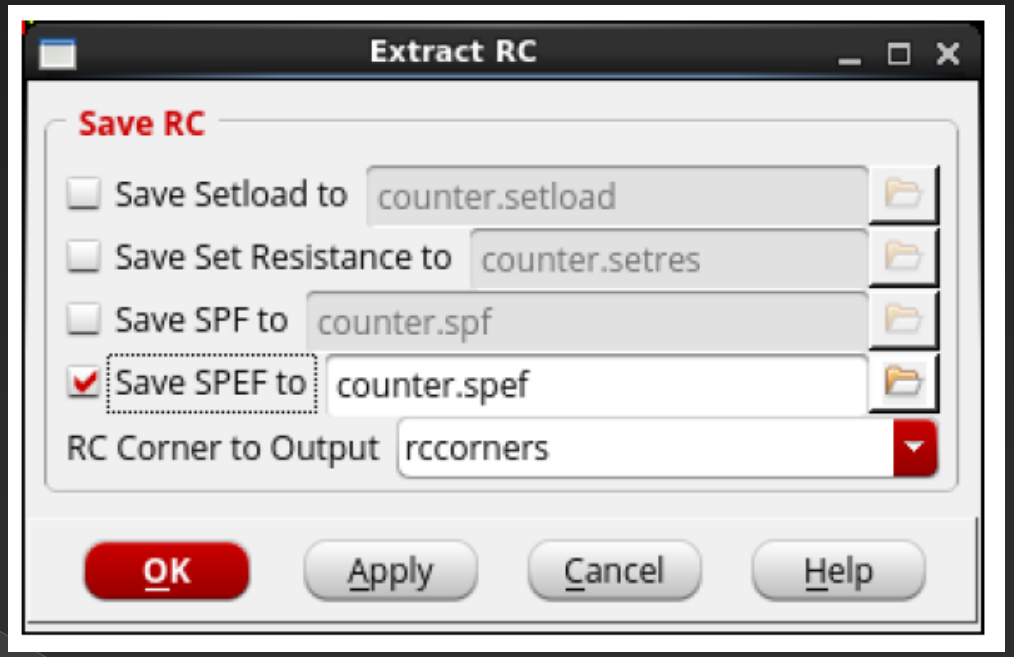
1. Go to Place -> Physical cell -> Add Fillers -> Click on Select -> Add all of the filler cells -> Close -> Ok



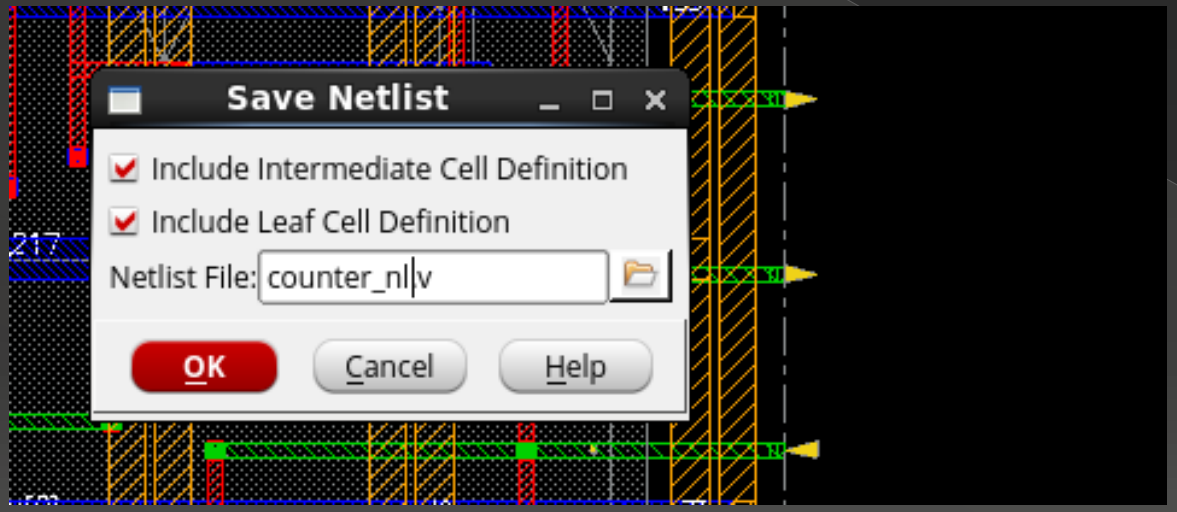
2. Check ‘Do DRC’ and ‘Fit Gap’



1. Go to Timing -> Extract RC -> Check the boxes ‘Save SPF to’ & ‘Save SPEF to’ and press Ok



2. Finally, Go to File -> Save -> Netlist -> Ok.



3. File -> Save Design -> Enable Innovus and type filename.enc and click Ok

Select File-Save-GDS/OASIS.