Vellore Institute of Technology, Chennai

BECE407P - ASIC Design

Lab-1

Design and Simulation of sequential & combinational modules using Cadence® NCLaunch

Name of the Student: _____

Roll Number: _____

Date of the Lab. Class: _____

1. **Aim:**
2. **EDA Tools Used:**
3. **Detailed description of the Designs:**
4. **Proceedure:** (with clear snapshots)
5. **RTL Codes:** (both the *module.v* and *testbench.v*)
6. **Observations:** (with simulation waveforms)
7. **Inference:**