Vellore Institute of Technology, Chennai

BECE407P - ASIC Design

Lab-2

Running the Basic Synthesis Flow using Cadence® Genus

Name of the Student: _____

Roll Number: _____

Date of the Lab. Class: _____

1. **Aim:** To run the basic synthesis flow for our designs.
2. **EDA Tools Used:**
3. **Details of the Synthesis Flow:** (with clear snapshots)
   (a) Method of writing a script file (*.g*) for input *Timing Constraints*:
   (b) Steps to start *Cadence® Genus*:
   (c) Steps to "load the required libraries, designs and synthesizing those designs":
4. **Cadence® Genus Legacy terminal after Synthesis:** (with clear snapshots)
5. **Generate & Read the Reports:** (with clear snapshots)
6. **Writing the Output files:** (with clear snapshots)
7. **Method of writing a script file (*.tcl*) for synthesis:**