Course Code	Course Title	L	T	P	C
BECE406E	FPGA Based System Design	2	0	2	3
Pre-requisite	BECE102L, BECE102P	Syllabus version			
		1.0			

Course Objectives

1. Understand FPGA Architecture and technologies
2. Modeling of complex digital sub-systems
3. Implementation of complex FPGA applications in real world scenario

Course Outcomes

At the end of the course, students will be able to

1. Understand architectures of programmable logic devices
2. Understand various abstraction level in Verilog HDL
3. Construct high speed arithmetic and memory circuits
4. Analyze the synthesis and timing constraints/reports
5. Design the system using soft core processors
6. Develop the FPGA based system for various applications in signal processing
7. Develop and prototype digital systems using FPGA

Module:1	Programmable Logic Devices	4 hours

Types of Programmable Logic Devices: PLA, PAL, CPLD - FPGA Architecture – Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA.

Module:2	HDL Fundamentals	3 hours

Verilog Behavioral, Data Flow and Structural Modeling, Useful Modeling Techniques.

Module:3	Implementation of Arithmetic system	5 hours

Arithmetic Circuits: High Speed Adders, Carry look-ahead adder, Carry save adders, Conditional Sum adders, Sequential and Parallel Multipliers

Module:4	FSM and memory modelling	5 hours

Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM - FSM Verilog modeling of Sequence detector - Serial adder - Vending machine.

Module:5	Synthesis and Timing Analysis	3 hours

Synthesis, Optimization of Speed: Introduction, Strategies for Timing Improvement; Optimization of Area, Optimization of power

Module:6	SoC Design	4 hours

Introduction to hardware – software codesign, Introduction to Qsys and Intel Quartus prime tool, Nios II Software Build Tools for Eclipse, Incorporate custom peripherals & instructions into an embedded system.

Module:7	FPGA Applications	4 hours

Embedded system design using FPGAs, DSP using FPGAs, Dynamic architecture using FPGAs, reconfigurable systems, application case studies. Simulation / implementation exercises of combinational, sequential and DSP kernels on Xilinx / Altera boards.

Module:8	Contemporary Issues	2 hours
	Total Lecture hours:	30 hours

Text Book(s)

1.	Michael D Ciletti, Advanced Digital Design with the Verilog HDL, Prentice Hall, Second Edition, 2017.			
Reference Books				
1.	Charles H Roth Jr, Lizy Kurian John and ByeongKil Lee Digital Systems Design using Verilog, Cengage Learning, First Edition, 2016.			
2.	Wayne Wolf, FPGA Based System Design, Prentices Hall Modern Semiconductor Design Series, 2011.			
3.	Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, Create Space Independent Publishing Platform, Second Edition, 2015.			
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test				
Indicative Experiments				
1.	Design of adders and Multipliers			**6 hours**
2.	Design of FSM			**6 hours**
3.	Design of Memory circuits			**6 hours**
4.	Synthesis and Timing Analysis			**6 hours**
5.	System design using Qsys			**6 hours**
	Total Laboratory Hours			**30 hours**
Mode of assessment: Continuous assessment and FAT				
Recommended by Board of Studies	28-02-2023			
Approved by Academic Council	No. 69	Date	16-03-2023	