

Vellore Institute of Technology, Chennai

BECE407P - ASIC Design

Lab-3

Running the Basic Synthesis Flow using Cadence® Genus

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Date of the Lab. Class: 1/08/24

1. **Aim:** To design , verify and to synthesize 4 bit ALU .

2. **EDA Tools Used:**

Cadence® Genus and Cadence® Naunch

3. **Details of the Synthesis Flow:** (with clear snapshots)

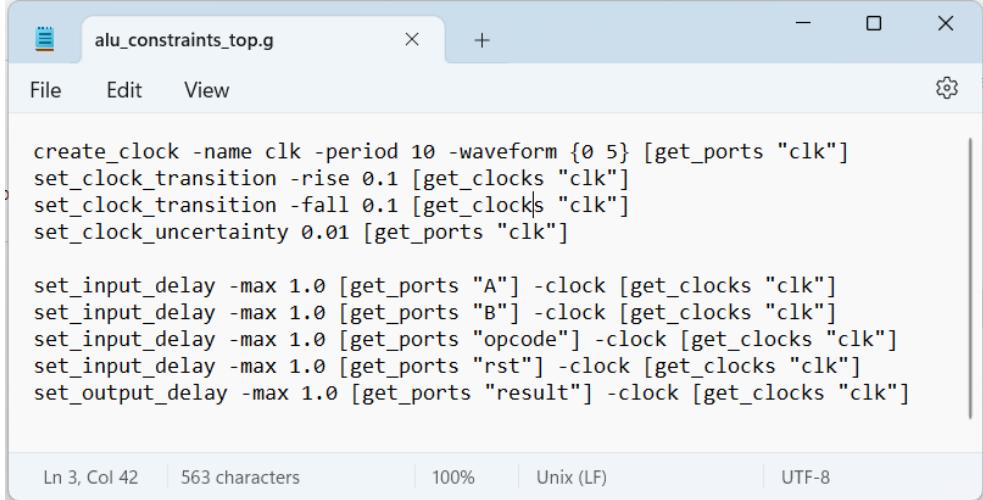
(a) Method of writing a script file (.g) for input *Timing Constraints*:

1.) Create a file with .g extension in the synthesis folder.

2.) Open it and write the following commands and save it:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
```

```
set_input_delay -max 1.0 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "opcode"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "rst"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "result"] -clock [get_clocks "clk"]
```



The screenshot shows a terminal window titled "alu_constraints_top.g". The window contains a script for setting up timing constraints. The script includes commands to create a clock named "clk" with a period of 10 units, set clock transitions for rise and fall times, and specify input and output delays for ports "A", "B", "opcode", "rst", and "result". The window also displays status information at the bottom: "Ln 3, Col 42", "563 characters", "100%", "Unix (LF)", and "UTF-8".

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "A"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "B"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "opcode"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "rst"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "result"] -clock [get_clocks "clk"]
```

(b) Steps to start *Cadence® Genus*:

- 1.) Open the synthesis folder terminal .
- 2.) run the following commands : 'csh' , 'source /home/install/cshrc' , 'genus -legacy -ui' .

(c) Steps to “load the required libraries, designs and synthesizing those designs”:

- 1.) After opening the genus set the library and rtl folder path by using the commands :

```
'set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/'  
'set_attribute init_rtl_search_path /home/student/Desktop/21BEC1033/rtl/'
```

- 2.) Now load the library using the command :

```
'set_attribute library slow_vdd1v0_basicCells.lib'
```

- 3.) Now read the counter.v file by using the command : 'read_hdl alu_4bit.v'
- 4.) Elaborate the design by using the command: 'elaborate'.
- 5.) Now read the timing constraints file by using the command :

```
'read_sdc alu_constraints_top.g'
```

- 6.) To synthesize the design run the command:

```
'set_attribute syn_generic_effort medium'  
'syn_generic'  
'set_attribute syn_map_effort high'  
'set_attribute syn_opt_effort high'
```

```
'syn_map'  
'syn_opt'
```

4. Cadence® Genus Legacy terminal after Synthesis: [Terminal](#)
(click the link for viewing entire terminal)

File Edit View
File Processing Tools Scripts Help

```
#@ Processing -files option
@genus 1> source alu.tcl
Setting attribute of root '/': 'init_lib_search_path' = /home/student/Desktop/21BEC1033/lib/
Setting attribute of root '/': 'init_hdl_search_path' = /home/student/Desktop/21BEC1033/rtl/

Threads Configured:3

Message Summary for Library slow_vddiv0_basiccells.lib:
*****
Missing a function attribute in the output pin definition. [LBR-518]: 1
*****
```

Info : Created nominal operating condition. [LBR-412]
: Operating condition 'nominal' was created for the PVT values (1.000000, 0.900000, 125.000000) in library 'slow_vddiv0_basiccells.lib'.
: The nominal operating condition is represented, either by the nominal PVT values specified in the library source (via nom_process,nom_voltage and nom_temperature respectively), or by the default PVT values (1.0,1.0,1.0).
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'ANTENNA' must have an output pin.
: Add the missing output pin(s), then reload the library. Else the library cell will be marked as timing model i.e. unusable. Timing model means that the cell does not have any defined function. If there is no output pin, Genus will mark library cell as unusable i.e. the attribute 'usable' will be marked to 'false' on the libcell. Therefore, the cell is not used for mapping and it will not be picked up from the library for synthesis. If you query the attribute 'unusable_reason' on the libcell; result will be: 'Library cell has no output pins.' Note: The message LBR-9 is only for the logical pins and not for the power_ground pins. Genus will depend upon the output function defined in the pin group (output pin) of the cell, to use it for mapping. The pg_pin will not have any function defined.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'ANTENNA' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP10' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP10' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP2' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP2' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP3' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP3' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP4' must have an output pin.

```

alu_terminal X +
File Edit View
Setting attribute of root '/': 'library' = slow_vddiv0_basicCells.lib
Library has 324 usable logic and 128 usable sequential lib-cells.
Info : Elaborating Design. [ELAB-1]
: Elaborating top-level block 'alu_4bit' from file '/home/student/Desktop/21BEC1033/rtl/alu_4bit.v'.
Warning : Unreachable statements for case item. [CFG-472]
: Case item 'default' in module 'alu_4bit' in file '/home/student/Desktop/21BEC1033/rtl/alu_4bit.v' on line 14.
Info : Done Elaborating Design. [ELAB-3]
: Done elaborating 'alu_4bit'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_elab
| Trick | Accepts | Rejects | Runtime (ms) |
| _ume_constant_bmux | 0 | 0 | 0.00 |

Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: alu_4bit, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: alu_4bit, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_clip_mux_input | 0 | 0 | 1.00 |
| hlo_clip | 0 | 0 | 0.00 |

Statistics for commands executed by read_sdc:
"create_clock" - successful 1 , failed 0 (runtime 0.00)
"get_clocks" - successful 7 , failed 0 (runtime 0.00)
"get_ports" - successful 7 , failed 0 (runtime 0.00)
"set_clock_transition" - successful 2 , failed 0 (runtime 0.00)
"set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)
"set_input_delay" - successful 4 , failed 0 (runtime 0.00)
Ln 1, Col 1 90.000 characters
100% Unix (LF) UTF-8

```

```

alu_terminal X +
File Edit View
read_sdc completed in 00:00:00 (hh:mm:ss)
Setting attribute of root '/': 'syn_generic_effort' = medium
Setting attribute of root '/': 'syn_map_effort' = medium
Setting attribute of root '/': 'syn_opt_effort' = medium

Stage: pre_early_cg
| Transform | Accepts | Rejects | Runtime (ms) |

## Generic Timing Info for library domain: _default_ typical gate delay: 127.6 ps std_slew: 17.9 ps std_load: 1.0 fF
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: alu_4bit, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_mux_reorder | 0 | 0 | 0.00 |

Info : Synthesizing. [SYNTH-1]
: Synthesizing 'alu_4bit' to generic gates using 'medium' effort.
PBS_Generic_Start - Elapsed Time 0, CPU Time 0.0
stamps 'PBS_Generic_Start' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 11:59:08 (Aug02) | 236.9 MB | PBS_Generic_Start
Number of threads: 8 * 1 (id: pbs.debug, time_info v1.57)
Info: (*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
Ths Restructuring config: no_value at stage generic applied.
Info : Partition Based Synthesis execution skipped. [PHYS-752]
: Design size is less than the partition size '100000' for distributed generic optimization to kick in.
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: alu_4bit, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Ln 1, Col 1 90.000 characters
100% Unix (LF) UTF-8

```

```

alu_terminal X +
File Edit View
CPI-506 [Warning] 1 | Command 'commit_power_intent' cannot proceed as
| there is no power intent loaded.
| PA-7 [Info] 4 | Resetting power analysis results.
| | All computed switching activities are removed.
| SYNTH-5 [Info] 1 | Done mapping.
| SYNTH-7 [Info] 1 | Incrementally optimizing.

Info : Done incrementally optimizing. [SYNTH-8]
: Done incrementally optimizing 'alu_4bit'.
Finished SOC export (command execution time mmiss (real) = 00:00).
Info : Joules engine is used. [PDT-16]
: Joules engine is being used for the command report_power.
Info : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
: alu_4bit
Info : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info : ACTP-0001 Activity propagation ended for stim#0
Info : PWA-0001 [PwrInfo] compute_power effective options
: -mode : vectorless
: -skip_propagation : 1
: -frequency_scaling_factor : 1.0
: -use_clock_freq : stim
: -stim :/stim#0
: -fromGenus : 1
Info : ACTP-0001 Timing initialization started
Info : ACTP-0001 Timing initialization ended
Info : PWA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
: option...
Warning: PWA-0032 [PwrWarn] Frequency scaling is not applicable for vectorless
: flow. Ignoring frequency scaling.
Warning: PWA-0034 [PwrWarn] -stim option is not applicable with vectorless mode
: of power analysis, ignored this option.
Info : PWA-0002 Started 'vectorless' power computation.
Info : PWA-0009 [PwrInfo] Power Computation Progress Report : 100%
Info : PWA-0002 Finished power computation.
Info : PWA-0007 [PwrInfo] Completed successfully.
Info : Info=6, Warn=2, Error=0, Fatal=0
Output file: alu_power.rep
WARNING: This version of the tool is 770 days old.
legacy_genus:/>
Ln 1, Col 1 90.000 characters
100% Unix (LF) UTF-8

```

5. Generate & Read the Reports: (with clear snapshots)

For generating the report run the following commands:

```
report_timing > alu_timing.rep
```

```
report_area > alu_area.rep
```

```
report_power > alu_power.rep
```

The screenshot shows three terminal windows side-by-side:

- alu_area.rep**: Displays synthesis area reports. It includes header information and a table of instance/module counts and areas.
- alu_timing.rep**: Displays synthesis timing reports. It includes header information and a detailed table of timing constraints and delays.
- alu_power.rep**: Displays synthesis power reports. It includes header information and a detailed table of leakage, internal, switching, and total power consumption across various categories like memory, register, latch, logic, bbox, clock, pad, and pin.

A callout box highlights the following summary data from the power report:

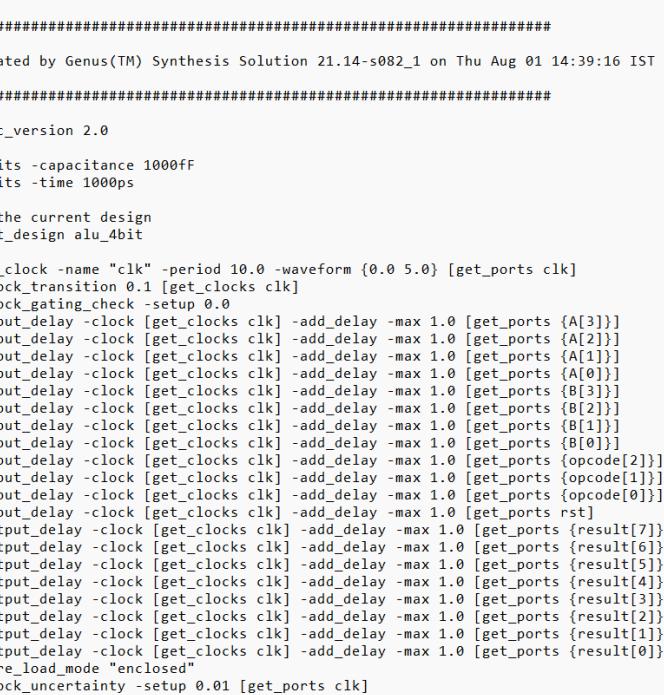
| |
|-----------------------------|
| Cell Count=166 |
| Cell Area=303.696 sq. units |
| Power dissipated=6.9 nW |

6. Writing the Output files: (with clear snapshots)

Run the following commands to write the output files:

```
write_netlist > alu_netlist.v (alu\_netlist--link)
```

```
write_sdc > alu.sdc
```



The screenshot shows a terminal window titled "alu.sdc" with the following content:

```
# #####  
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Aug 01 14:39:16 IST 2024  
# #####  
  
set sdc_version 2.0  
  
set_units -capacitance 1000ff  
set_units -time 1000ps  
  
# Set the current design  
current_design alu_4bit  
  
create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]  
set_clock_transition 0.1 [get_clocks clk]  
set_clock_gating_check -setup 0.0  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {A[3]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {A[2]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {A[1]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {A[0]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {B[3]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {B[2]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {B[1]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {B[0]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {opcode[2]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {opcode[1]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {opcode[0]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {rst}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {result[7]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {result[6]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {result[5]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {result[4]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {result[3]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {result[2]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {result[1]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {result[0]}]  
set_wire_load_mode "enclosed"  
set_clock_uncertainty -setup 0.01 [get_ports clk]  
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082.1
// Generated on: Aug 1 2024 14:39:16 IST (Aug 1 2024 09:09:16 UTC)

// Verification Directory fv/alu_6bit

module alu_6bit(A, B, opcode, clk, rst, result);
input [3:0] A, B;
input [2:0] opcode;
input clk, rst;
output [7:0] result;
wire [3:0] A, B;
wire [2:0] opcode;
wire clk, rst;
wire [7:0] result;
wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
wire n_8, n_9, n_10, n_11, n_12, n_14, n_15, n_16;
wire n_17, n_18, n_21, n_22, n_23, n_24, n_25, n_26;
wire n_27, n_28, n_29, n_30, n_31, n_32, n_33, n_34;
wire n_35, n_36, n_37, n_39, n_40, n_41, n_42, n_43;
wire n_44, n_45, n_46, n_47, n_48, n_49, n_50, n_51;
wire n_52, n_53, n_54, n_55, n_56, n_58, n_59, n_60;
wire n_61, n_62, n_63, n_65, n_66, n_67, n_68, n_69;
wire n_70, n_71, n_72, n_73, n_74, n_75, n_76, n_77;
wire n_78, n_79, n_80, n_81, n_82, n_83, n_84, n_85;
wire n_86, n_87, n_88, n_89, n_90, n_91, n_92, n_93;
wire n_94, n_95, n_96, n_97, n_99, n_101, n_102, n_103;
wire n_104, n_105, n_106, n_107, n_108, n_109, n_110, n_111;
wire n_112, n_113, n_114, n_115, n_116, n_118, n_119, n_120;
wire n_121, n_122, n_123, n_124, n_125, n_126, n_127, n_128;
wire n_129, n_130, n_131, n_132, n_133, n_134, n_135, n_136;
wire n_138, n_139, n_140, n_141, n_142, n_143, n_144, n_145;
wire n_146, n_148, n_149, n_150, n_151, n_152, n_153, n_154;
wire n_155, n_156, n_157, n_158, n_159, n_160, n_161, n_162;
wire n_164, n_165, n_166, n_167, n_168, n_169, n_170, n_184;
wire n_185, n_186, n_187, n_188, n_189;
DFFRQX1 [result_reg[3]] (.RN(n_169), .CK(clk), .D(n_170), .Q(result[3]));
OAI221X1 g35743_2398(.A0_(n_28), .A1_(n_158), .B0_(n_66), .B1_(n_15), .C0_(n_167), .Y_(n_170));
DFFRQX1 [result_reg[4]] (.RN(n_169), .CK(clk), .D(n_168), .Q(result[4]));
OAI221X1 g35722_5107(.A0_(n_165), .A1_(n_132), .B0_(n_138), .B1_(n_157), .C0_(n_161), .Y_(n_168));
NOR2X1 g35728_6260(.A0_(n_70), .B_(n_162), .Y_(n_167));
DFFRQX1 [result_reg[7]] (.RN(n_169), .CK(clk), .D(n_164), .Q(result[7]));
DFFRQX1 [result_reg[6]] (.RN(n_169), .CK(clk), .D(n_166), .Q(result[6]));
DFFRQX1 [result_reg[5]] (.RN(n_169), .CK(clk), .D(n_160), .Q(result[5]));
OAI21X1 g35726_4319(.A0_(n_165), .A1_(n_145), .B0_(n_186), .Y_(n_166));
OAI21X1 g35723_8428(.A0_(n_165), .A1_(n_136), .B0_(n_186), .Y_(n_164));
OAI21X1 g35730_5526(.A0_(A[3]), .A1_(n_161), .B0_(n_126), .C0_(n_153), .Y_(n_162));
DFFRQX1 [result_reg[2]] (.RN(n_169), .CK(clk), .D(n_159), .Q(result[2]));
OAI2B8X1 g35725_6783(.A0N_(n_189), .A1N_(n_155), .B0_(n_186), .Y_(n_160));
DFFRQX1 [result_reg[0]] (.RN(n_169), .CK(clk), .D(n_154), .Q(result[0]));
OAI21X1 g35731_3680(.A0_(n_1), .A1_(n_158), .B0_(n_52), .C0_(n_148), .Y_(n_159));
DFFRQX1 [result_reg[1]] (.RN(n_169), .CK(clk), .D(n_152), .Q(result[1]));
OAI21X1 g35732_2802(.A0_(n_151), .A1_(n_150), .B0_(n_156), .Y_(n_157));
XOR2X1 g35731_1705(.A_(n_124), .B_(n_143), .Y_(n_155));
OAI221X1 g35744_5122(.A0_(n_3), .A1_(n_158), .B0_(A[0]), .B1_(n_161), .C0_(n_149), .Y_(n_154));
OAI221X1 g35733_8246(.A0_(n_141), .A1_(n_146), .B0_(n_51), .B1_(n_188), .Y_(n_153));
OAI21X1 g35749_7098(.A0_(n_5), .A1_(n_158), .B0_(n_48), .C0_(n_142), .Y_(n_152));
NOR2X1 g35737_6131(.A_(n_151), .B_(n_150), .Y_(n_156));
INX1 g35748_0041(.A_(n_144), .Y_(n_149));
OAI221X1 g35739_1881(.A0_(n_189), .A1_(n_182), .B0_(n_140), .B1_(n_53), .C0_(n_139), .Y_(n_148));
ADDFX1 g35741_5115(.A_(A[3]), .B_(n_73), .C1_(n_121), .C0_(n_150), .S_(n_146));
XOR2X1 g35735_7482(.A_(n_94), .B_(n_134), .Y_(n_145));
OAI222X1 g35751_4733(.A0_(n_61), .A1_(n_60), .B0_(n_130), .B1_(n_135), .C0_(n_25), .C1_(n_47), .Y_(n_144));
XOR2X1 g35740_6161(.A_(n_123), .B_(n_184), .Y_(n_143));
OAI221X1 g35753_9315(.A0_(n_141), .A1_(n_106), .B0_(n_140), .B1_(n_101), .C0_(n_131), .Y_(n_142));
DFFRQX1 [result_reg[6]] (.RN(n_169), .CK(clk), .D(n_166), .Q(result[6]));
DFFRQX1 [result_reg[5]] (.RN(n_169), .CK(clk), .D(n_160), .Q(result[5]));
DFFRQX1 [result_reg[4]] (.RN(n_169), .CK(clk), .D(n_154), .Q(result[4]));
DFFRQX1 [result_reg[3]] (.RN(n_169), .CK(clk), .D(n_150), .Q(result[3]));
DFFRQX1 [result_reg[2]] (.RN(n_169), .CK(clk), .D(n_144), .Q(result[2]));
DFFRQX1 [result_reg[1]] (.RN(n_169), .CK(clk), .D(n_138), .Q(result[1]));
DFFRQX1 [result_reg[0]] (.RN(n_169), .CK(clk), .D(n_132), .Q(result[0]));
OAI222X1 g35745_9945(.A0_(n_69), .A1_(n_81), .B0_(n_138), .B1_(n_127), .C0_(A[2]), .C1_(n_161), .Y_(n_139));
OAI2B8X1L g35738_3426(.A0N_(n_92), .A1N_(n_133), .B0_(n_93), .Y_(n_136));
OAI221X1 g35761_1666(.A0_(A[0]), .A1_(n_87), .B0_(n_21), .B1_(n_77), .C0_(n_120), .Y_(n_135));
NAND2X1 g35743_7410(.A_(n_125), .B_(n_133), .Y_(n_134));
XOR2X1 g35750_6417(.A_(n_128), .B_(n_115), .Y_(n_131));
OAI222X1 g35758_5477(.A0_(n_165), .A1_(n_46), .B0_(n_130), .B1_(n_118), .C1_(A[1]), .CI_(n_161), .Y_(n_131));
OAI22XL g35752_2398(.A0_(n_114), .A1_(n_113), .B0_(n_128), .Y_(n_129));
INW1 g35754_5(A_(n_122), .Y_(n_127));
NAND2X1 g35759_5187(.A_(n_189), .B_(n_119), .Y_(n_126));
OAI221X1 g35760_6260(.A0_(n_124), .A1_(n_123), .B0_(n_128), .Y_(n_125));
ADDFX1 g35756_4319(.A_(A[2]), .B_(n_74), .CI_(n_105), .C0_(n_121), .S_(n_122));
OAI221X1 g35747_8428(.A0_(n_123), .A1_(n_116), .B0_(n_124), .Y_(n_133));
OAI221X1 g35763_5526(.A0_(B[1]), .A1_(n_112), .B0_(n_103), .C0_(n_111), .Y_(n_120));
ADDFX1 g35762_6783(.A_(n_33), .B_(n_83), .CI_(n_104), .C0_(n_128), .S_(n_119));
AOI221X1 g35765_3680(.A0_(n_110), .A1_(n_68), .B0_(n_107), .B1_(n_109), .C0_(n_59), .Y_(n_118));
ADDHX1 g35757_1617(.A_(n_114), .B_(n_113), .C0_(n_116), .S_(n_115));
NOR2X1 g35768_2802(.A_(n_99), .B_(n_108), .Y_(n_112));
AOI22XL g35769_1705(.A0_(n_110), .A1_(n_185), .B0_(B[1]), .B1_(n_89), .Y_(n_111));
AOI32X1 g35769_5122(.A_(n_2), .A1_(n_187), .A2_(n_96), .B0_(B[1]), .B1_(n_97), .Y_(n_189));
OAI21X1 g35770_8246(.A0_(n_107), .A1_(n_90), .B0_(n_86), .C0_(n_95), .Y_(n_108));
ADDFX1 g35767_7998(.A_(A[1]), .B_(n_62), .CI_(n_63), .C0_(n_105), .S_(n_106));
ADDFX1 g35764_6131(.A_(n_37), .B_(n_31), .CI_(n_55), .C0_(n_123), .S_(n_113));
ADDFX1 g35775_1881(.A_(n_10), .B_(n_11), .CI_(n_58), .C0_(n_114), .S_(n_104));
AOI32X1 g35777_5115(.A0_(B[3]), .A1_(n_85), .A2_(n_84), .B0_(A[0]), .B1_(n_91), .Y_(n_103));
XOR2X1 g35772_7482(.A_(n_101), .B_(n_80), .Y_(n_102));
NAND2X1 g35773_6161(.A_(n_96), .B_(n_88), .Y_(n_97));
OAI2B8X1L g35780_9315(.A0N_(n_45), .A1N_(n_75), .B0_(A[0]), .Y_(n_95));
NOR2X1 g35771_9945(.A_(n_93), .B_(n_92), .Y_(n_94));
OAI221X1 g35784_2883(.A0_(A[2]), .A1_(n_187), .B0_(n_90), .C0_(n_56), .Y_(n_91));

Three screenshots of a terminal window showing Verilog code for an ALU. The code defines various logic functions and their implementations using different logic gates (AND, OR, NOT, etc.). The code is highly repetitive, showing multiple instances of similar logic blocks with different variable names.

```

alu_netlist.v
File Edit View
File Edit View
alu_netlist.v
File Edit View
NAND2X1 g35836_4319(.A (A[3]), .A1 (A[1]), .A2 (n_43), .B0 (n_88),
.B1 (n_110), .B2 (n_67), .Y (n_89));
INVX1 g35789_(A (n_86), .Y (n_87));
OAI22X1 g35787_1666(.A0 (B[2]), .A1 (n_71), .B0 (n_85), .B1 (n_84),
.Y (n_96));
OAI21X1 g35779_7410(.A (n_17), .A1 (n_78), .B0 (n_79), .Y (n_83));
OAI22BX1 g35785_6417(.A0 (B[1]), .A1N (n_90), .B0 (n_50), .Y (n_82));
OAI21X1 g35790_5477(.A0 (A[3]), .A1 (n_22), .B0 (n_76), .C0 (n_42),
.Y (n_71));
XNOR2X1 g35781_2398(.A (n_79), .B (n_78), .Y (n_80));
XNOR2X1 g35774_5107(.A (n_65), .B (n_44), .Y (n_124));
OAI22X1 g35793_6260(.A0 (n_76), .A1 (n_39), .B0 (n_0), .B1 (n_27),
.Y (n_77));
OAI22X1 g35792_8428(.B[2]), .A1 (n_151), .B0 (n_85), .B1 (n_72),
.Y (n_74));
OAI22X1 g35799_5526(.B[3]), .A1 (n_151), .B0 (n_107), .B1 (n_27),
.Y (n_73));
NAND2X1 g35793_6783(.A (B[2]), .B (n_71), .D (n_86));
NOR4X1 g35783_3680(.A (B[1]), .B (n_56), .C (n_69), .D (n_130), .Y (n_70));
OAI22X1 g35796_1617(.A0 (B[1]), .A1 (n_67), .B0 (n_26), .B1 (n_65),
.C0 (B[3]), .C1 (n_49), .Y (n_68));
NOR2BX1 g35801_2882(.A (n_60), .B (n_55), .Y (n_92));
XNOR2X1 g35790_1705(.A (n_61), .B (n_15), .Y (n_65));
OAI21X1 g35800_5122(.A0 (B[1]), .A1 (n_151), .B0 (n_61), .Y (n_62));
NOR2X1 g35805_8246(.A (n_48), .B (n_54), .C (n_76), .Y (n_59));
NOR3X1 g35806_7098(.A (n_54), .B (n_69), .C (n_8), .Y (n_58));
XNOR2X1 g35811_6131(.A (n_4), .B (n_19), .C (n_76), .Y (n_59));
INVX1 g35827_(A (n_56), .Y (n_99));
INVX1 g35815_(A (n_189), .Y (n_165));
XNOR2X1 g35798_7482(.A (n_51), .B (n_34), .Y (n_55));
NAND2X1 g35790_4733(.A (n_51), .B (n_34), .Y (n_52));
NAND4X1 g35791_6161(.A (n_49), .B (n_69), .C (n_9), .D (n_35), .Y (n_50));
NAND2X1 g35792_9315(.A (n_51), .B (n_23), .Y (n_48));
NOR2X1 g35807_9945(.A (n_141), .B (n_51), .Y (n_47));
NAND2BX1 g35782_2883(.AN (n_14), .B (n_79), .Y (n_46));
NAND2X1 g35888_2346(.A (n_36), .B (n_45), .Y (n_71));
XNOR2X1 g35810_1666(.A (n_29), .B (n_38), .Y (n_44));
OAI22X1 g35812_7098(.A (n_41), .B (n_69), .Y (n_43));
INVX1 g35813_7098(.A (n_38), .Y (n_42));
INVX1 g35816_(A (n_151), .Y (n_72));
XNOR2X1 g35812_6417(.A (n_32), .B (n_41), .Y (n_78));
NOR2X1 g35831_2398(.A (B[2]), .B (n_18), .Y (n_40));
OAI21X1 g35834_5107(.A0 (A[1]), .A1 (n_24), .B0 (n_88), .Y (n_39));
NOR2BX1 g35794_6260(.AN (n_53), .B (n_54), .Y (n_65));

```

Ln 186, Col 58 12,949 characters Ln 235, Col 57 12,949 characters Ln 235, Col 57 12,949 characters

80% Unix (LF) 80% Unix (LF) 80% Unix (LF)

Unix (LF) Unix (LF) Unix (LF)

UTF-8 UTF-8 UTF-8

09:51 04-08-2024 ENG IN 28°C Mostly cloudy

7. Method of writing a script file (.tcl) for synthesis:

1.) Create a file with .tcl extension in synthesis folder and type the following commands and save it:

```

set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {alu_4bit.v}

elaborate
read_sdc alu_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort medium
set_attribute syn_opt_effort medium

syn_generic
syn_map
syn_opt

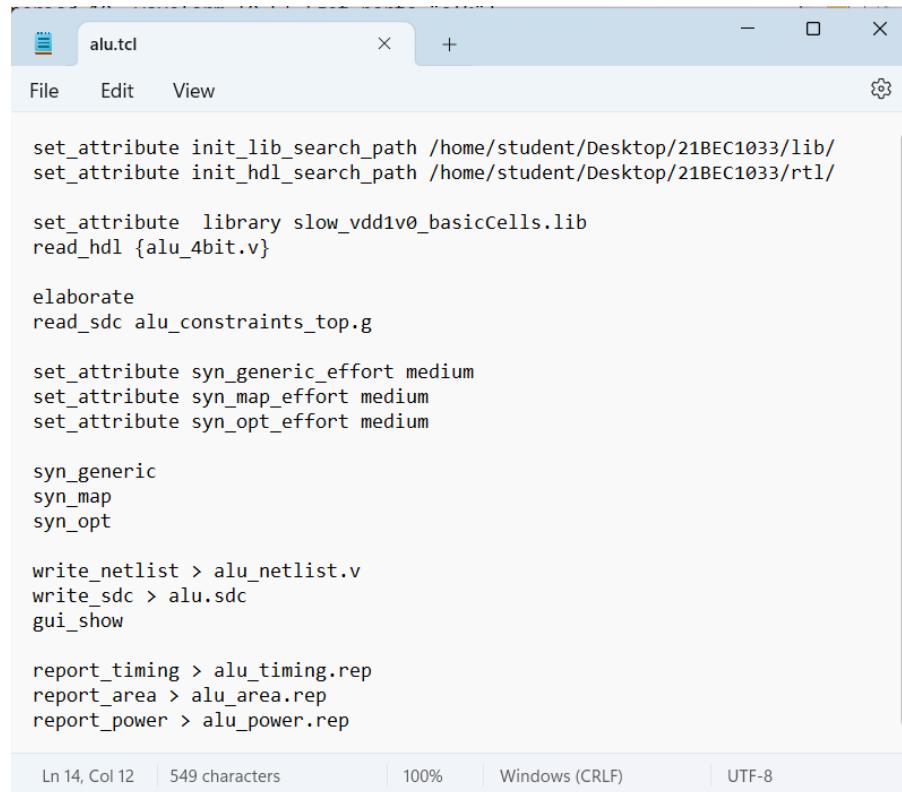
write_netlist > alu_netlist.v
write_sdc > alu.sdc
gui_show

report_timing > alu_timing.rep
report_area > alu_area.rep
report_power > alu_power.rep

```

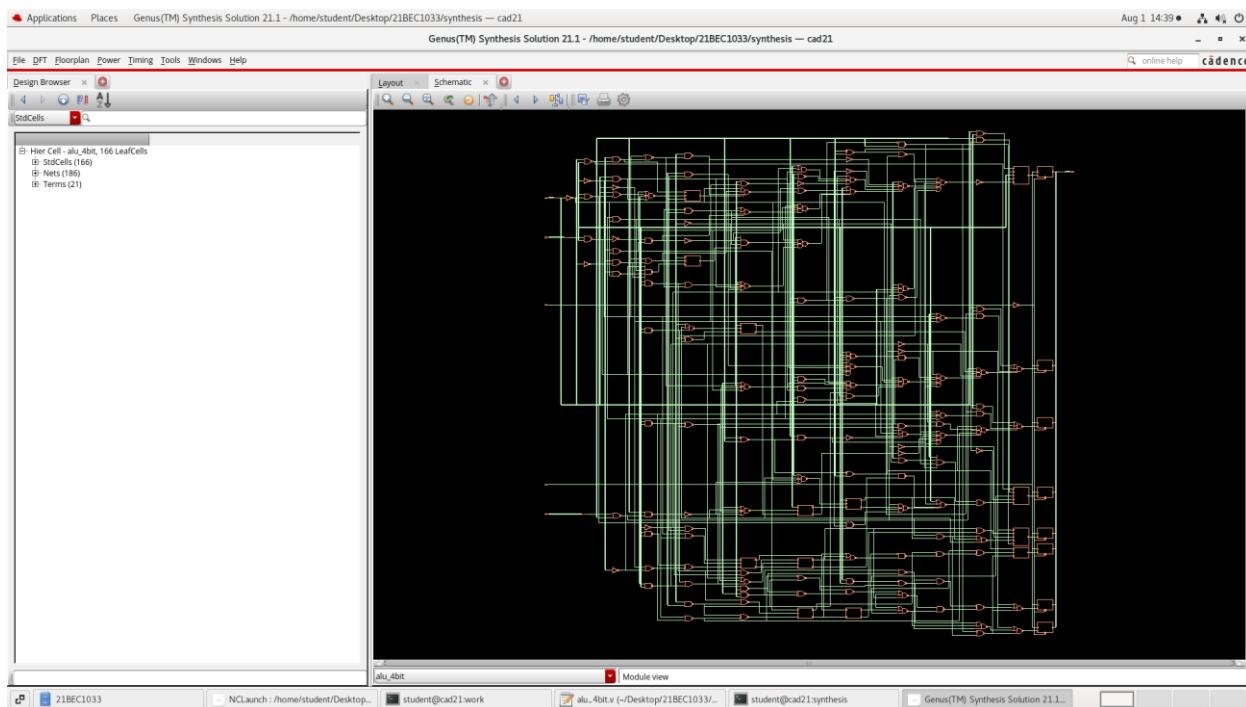
2.) After creating the .g and .tcl file open the terminal of synthesis folder and run the following commands:

```
'csh'  
'source /home/install/cshrc'  
'genus -legacy -ui -f alu.tcl'
```

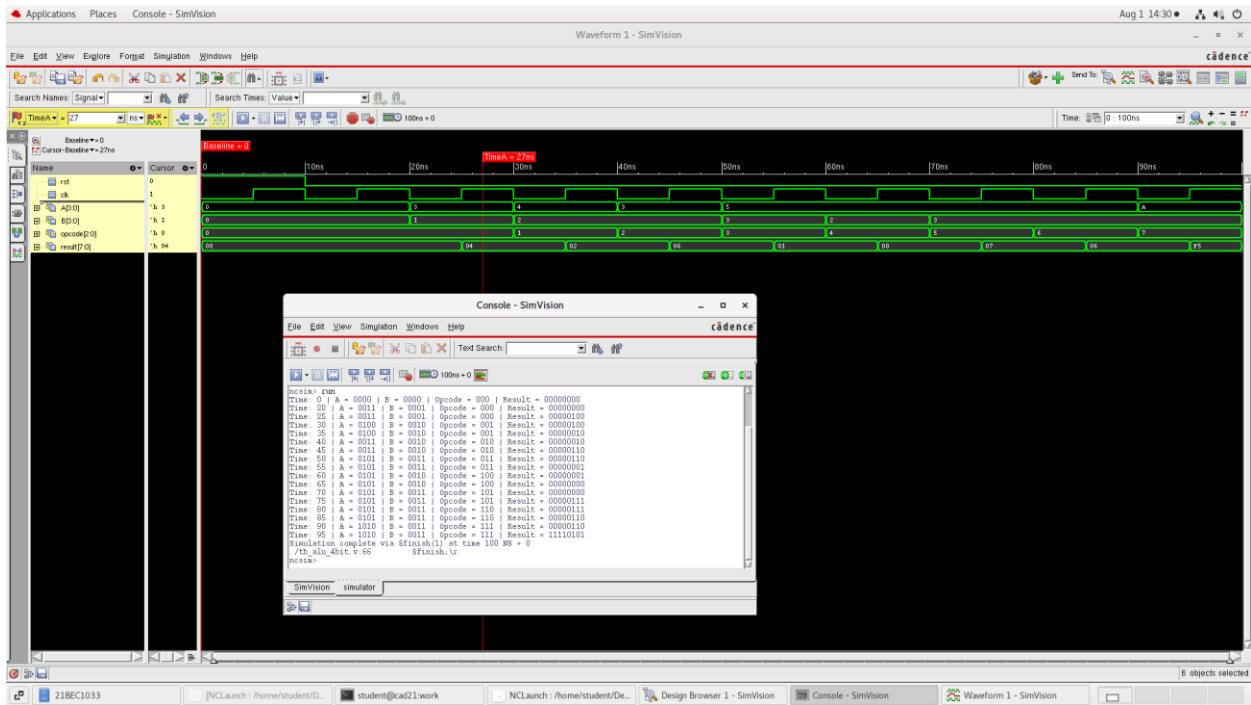


```
File Edit View  
  
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/  
  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl {alu_4bit.v}  
  
elaborate  
read_sdc alu_constraints_top.sdc  
  
set_attribute syn_generic_effort medium  
set_attribute syn_map_effort medium  
set_attribute syn_opt_effort medium  
  
syn_generic  
syn_map  
syn_opt  
  
write_netlist > alu_netlist.v  
write_sdc > alu.sdc  
gui_show  
  
report_timing > alu_timing.rep  
report_area > alu_area.rep  
report_power > alu_power.rep  
  
Ln 14, Col 12 549 characters 100% Windows (CRLF) UTF-8
```

8. Genus Schematic:



9. Functional verification:



Vellore Institute of Technology, Chennai

BECE407P - ASIC Design

Lab-3

Running the Basic Synthesis Flow using Cadence® Genus

Name of the Student: PRANAV.G

Roll Number: 21BEC1033

Date of the Lab. Class: 1/08/24

1. **Aim:** To design , verify and to synthesize 4 bit ripple carry adder .

2. **EDA Tools Used:**

Cadence® Genus and Cadence® Naunch

3. **Details of the Synthesis Flow:** (with clear snapshots)

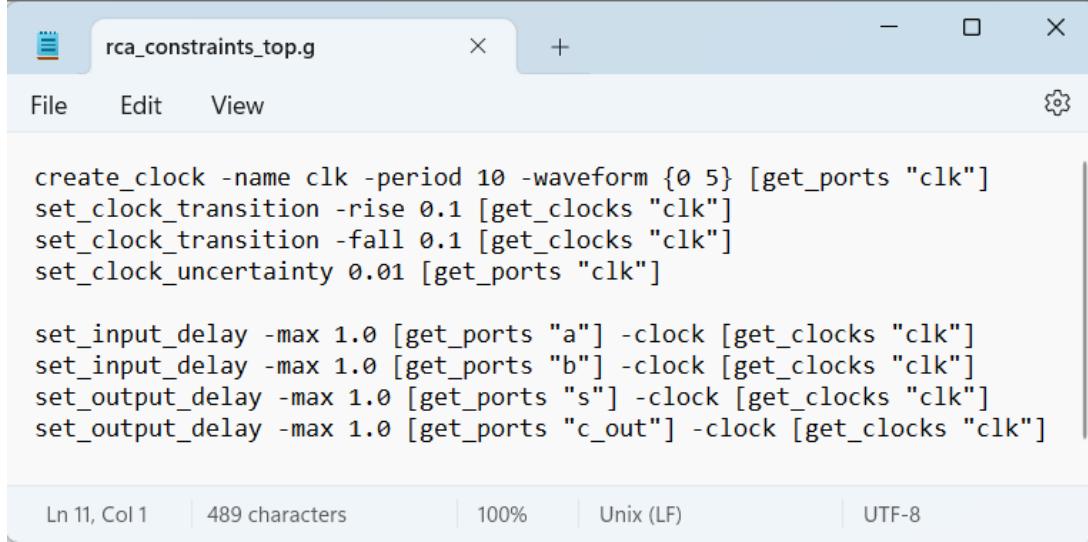
(a) Method of writing a script file (.g) for input *Timing Constraints*:

1.) Create a file with .g extension in the synthesis folder.

2.) Open it and write the following commands and save it:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "s"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "c_out"] -clock [get_clocks "clk"]
```



The screenshot shows a terminal window titled "rca_constraints_top.g". The window contains a script for setting up timing constraints. The script includes commands to create a clock named "clk" with a period of 10 units, set clock transition times for rise and fall, and specify input and output delays for ports "a", "b", "s", and "c_out". The bottom status bar indicates the file is at line 11, column 1, with 489 characters, at 100% zoom, in Unix (LF) mode, and using UTF-8 encoding.

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "s"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "c_out"] -clock [get_clocks "clk"]
```

Ln 11, Col 1 | 489 characters | 100% | Unix (LF) | UTF-8

(b) Steps to start *Cadence® Genus*:

- 1.) Open the synthesis folder terminal .
- 2.) run the following commands : 'csh' , 'source /home/install/cshrc' , 'genus -legacy -ui' .

(c) Steps to “load the required libraries, designs and synthesizing those designs”:

- 1.) After opening the genus set the library and rtl folder path by using the commands :

```
'set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/ '
'set_attribute init_rtl_search_path /home/student/Desktop/21BEC1033/rtl/ '
```

- 2.) Now load the library using the command :

```
'set_attribute library slow_vdd1v0_basicCells.lib '
```

- 3.) Now read the counter.v file by using the command :'

```
read_hdl ripple_carry_adder_4bit.v'
```

- 4.) Elaborate the design by using the command: 'elaborate'.

- 5.) Now read the timing constraints file by using the command :

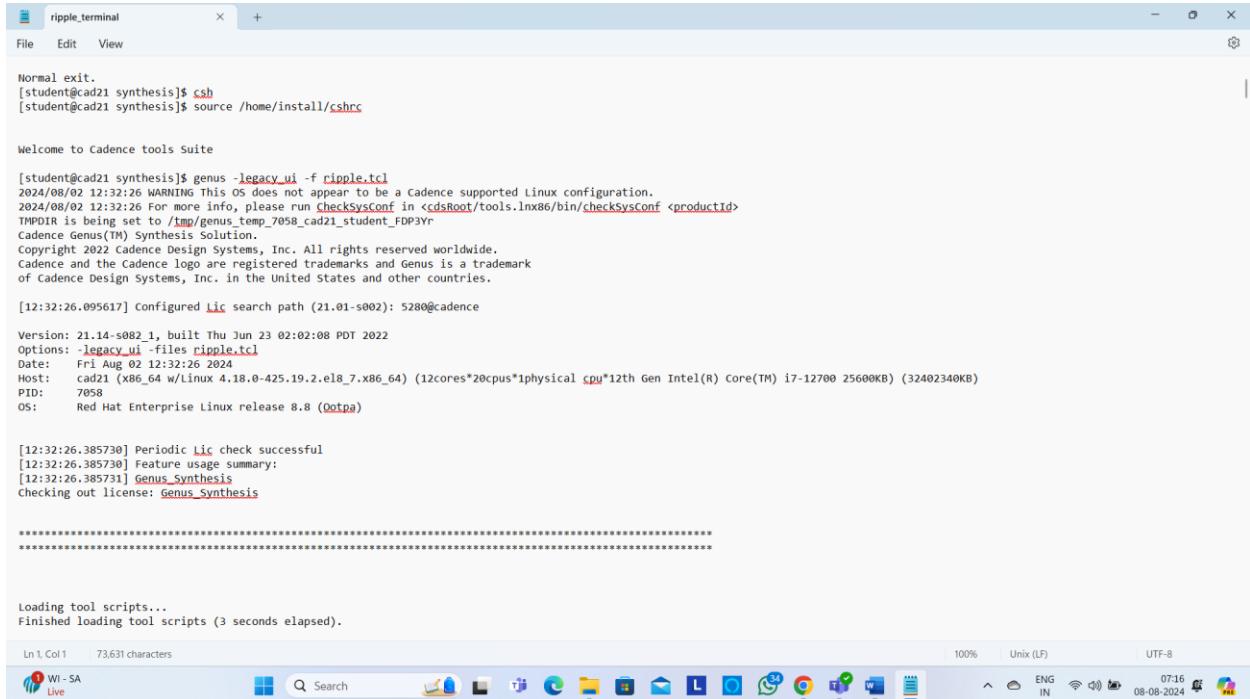
```
'read_sdc rca_constraints_top.g'
```

- 6.) To synthesize the design run the command:

```
'set_attribute syn_generic_effort medium'
'syn_generic'
iset_attribute syn_map_effort high'
iset_attribute syn_opt_effort high'
```

```
'syn_map'
'syn_opt'
```

4. Cadence® Genus Legacy terminal after Synthesis: [Terminal](#) (click the link for viewing entire terminal)



```

Normal exit.
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -legacy_ui -f ripple.tcl
2024/08/02 12:32:26 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/08/02 12:32:26 For more info, please run checkSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productId>
TMPDIR is being set to /tmp/genus_temp_7058_cad21_student_FDP3Yr
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[12:32:26.095617] Configured lic search path (21.01-s002): 5280@cadence

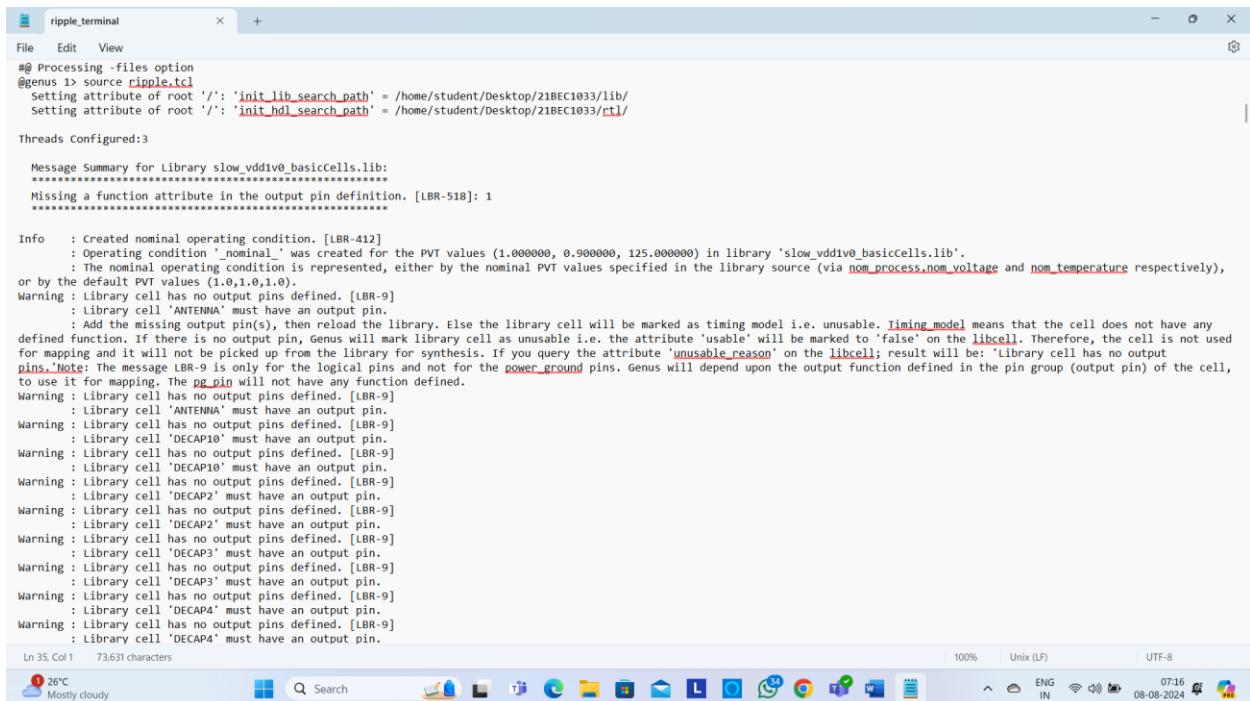
Version: 21.14-s002_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files ripple.tcl
Date: Fri Aug 02 12:32:26 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64) (12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700 25600KB) (32402340KB)
PID: 7058
OS: Red Hat Enterprise Linux release 8.8 (osptpa)

[12:32:26.385730] Periodic lic check successful
[12:32:26.385730] Feature usage summary:
[12:32:26.385731] Genus_Synthesis
Checking out license: Genus_Synthesis

*****
***** Loading tool scripts...
Finished loading tool scripts (3 seconds elapsed).

Ln 1, Col 1 73.631 characters
100% Unix (LF) UTF-8
Wi - SA Live
Search
L W
ENG IN 07:16 08-08-2024

```



```

# Processing -files option
@genus 1> source ripple.tcl
Setting attribute of root '/': 'init_lib_search_path' = /home/student/Desktop/21BEC1033/lib/
Setting attribute of root '/': 'init_hdl_search_path' = /home/student/Desktop/21BEC1033/rtl/
Threads Configured:

Message Summary for Library slow_vddiv0_basicCells.lib:
*****
Missing a function attribute in the output pin definition. [LBR-518]: 1
*****
Info : Created nominal operating condition. [LBR-412]
: Operating condition 'nominal' was created for the PVT values (1.000000, 0.900000, 125.000000) in library 'slow_vddiv0_basiccells.lib'.
: The nominal operating condition is represented, either by the nominal PVT values specified in the library source (via nom_process.nom_voltage and nom_temperature respectively), or by the default PVT values (1.0,1.0,1.0).
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'ANTENNA' must have an output pin.
: Add the missing output pin(s), then reload the library. Else the library cell will be marked as timing model i.e. unusable. Timing model means that the cell does not have any defined function. If there is no output pin, Genus will mark library cell as unusable i.e. the attribute 'usable' will be marked to 'false' on the libcell. Therefore, the cell is not used for mapping and will not be picked up from the library for synthesis. If you query the attribute 'unusable_reason' on the libcell; result will be: 'Library cell has no output pins.' Note: The message LBR-9 is only for the logical pins and not for the power_ground pins. Genus will depend upon the output function defined in the pin group (output pin) of the cell, to use it for mapping. The pg_pin will not have any function defined.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'ANTENNA' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP10' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP10' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP2' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP2' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP3' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP3' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP4' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAP4' must have an output pin.

Ln 35, Col 1 73.631 characters
100% Unix (LF) UTF-8
26°C Mostly cloudy
Search
L W
ENG IN 07:16 08-08-2024

```

```

ripple_terminal x +
File Edit View
Info : Done Elaborating Design. [ELAB-3]
      : Done elaborating 'ripple_carry_adder_4bit'.
Warning : Black-boxes are represented as unresolved references in the design. [TUI-273]
      : Cannot resolve reference to 'full_adder'.
      : Run check_design to get all unresolved instance. To resolve the reference, either load a technology library containing the cell by appending to the 'library' attribute, or read in the hdl file containing the module before performing elaboration. As the design is incomplete, synthesis results may not correspond to the entire design.
Checking for analog nets...
Check completed for analog nets...
Checking for source RTL...
Check completed for source RTL...
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks...

Stage: post_elab
| Trick | Accepts | Rejects | Runtime (ms) |
| ume_constant_mux | 0 | 0 | 0.00 |

Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: ripple_carry_adder_4bit, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: ripple_carry_adder_4bit, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_clip_mux_input | 0 | 0 | 0.00 |
| hlo_clip | 0 | 0 | 0.00 |

Statistics for commands executed by read_sdc:
"create_clock" - successful 1 , failed 0 (runtime 0.00)
"get_clocks" - successful 6 , failed 0 (runtime 0.00)
"get_ports" - successful 6 , failed 0 (runtime 0.00)
"set_clock_transition" - successful 2 , failed 0 (runtime 0.00)
"set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)
"set_input_delay" - successful 2 , failed 0 (runtime 0.00)
"set_output_delay" - successful 2 , failed 0 (runtime 0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
Setting attribute of root '/' : 'svn_generic_effort' = medium
Ln 151, Col 59 73.631 characters

```

```

26°C Desktop - OneDrive
ripple_terminal x +
File Edit View
| PA-7 | Info | 4 | there is no power intent loaded. |
| PA-7 | Info | 4 | All computed switching activities are removed. |
| SYNTH-5 | Info | 1 | Done mapping. |
| SYNTH-7 | Info | 1 | Incrementally optimizing. |

Info : Done incrementally optimizing. [SYNTH-8]
      : Done incrementally optimizing 'ripple_carry_adder_4bit'.
Finished SDC export (command execution time rmmiss (real) = 0:00:00).
Warning : The details given in report might be incorrect or incomplete. [RPT-80]
      : The design ./designs/ripple_carry_adder_4bit should be mapped to get accurate area details.
      : Map the design using syn_map before using the '-detail' option of the 'report_area' command.
Info : Joules engine is used. [RPT-16]
      : Joules engine is being used for the command report_power.
Info : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
      : ripple_carry_adder_4bit
Info : ACTP-0001 Activity propagation ended for stim#0
Info : PWRA-0001 [PwriInfo] compute_power effective options
      : mode : vectorless
      : -skip_propagation : 1
      : -frequency_scaling_factor : 1.0
      : -use_clock_freq : stim
      : stim : /stim#0
      : -fromGates : 1
Info : ACTP-0001 Timing initialization started
Info : ACTP-0001 Timing initialization ended
Info : PWRA-0002 [PwriInfo] Skipping activity propagation due to _skip_ap
      : option...
Warning : PWRA-0302 [PwriWarn] Frequency scaling is not applicable for vectorless
      : flow. Ignoring frequency scaling.
Warning : PWRA-0304 [PwriWarn] -stim option is not applicable with vectorless mode
      : of power analysis, ignored this option.
Info : PWRA-0002 Started 'vectorless' power computation.
Info : PWRA-0002 Finished power computation.
Info : PWRA-0007 [PwriInfo] completed successfully.
      : Info=6, Warn=2, Error=0, Fatal=0
Output file: rca_power.rep
WARNING: This version of the tool is 770 days old.
legacy_genus:/>

Ln 319, Col 53 73.631 characters

```

```

Humid Now
ripple_terminal x +
File Edit View
| ume_runtime | 0 | 0 | 0.00 |

Number of big b'muxes before = 0
Info : Pre-processed datapath logic. [DPOPT-6]
      : No pre-processing optimizations applied to datapath logic in 'ripple_carry_adder_4bit'.
Info : Skipping datapath optimization. [DPOPT-5]
      : There is no datapath logic in 'ripple_carry_adder_4bit'.
Number of big b'muxes after = 0
Starting logic reduction [v1.0] (stage: post_rlopt, startdef: ripple_carry_adder_4bit, recur: true)
Completed logic reduction (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux data reorder optimization [v1.0] (stage: post_rlopt, startdef: ripple_carry_adder_4bit, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_rlopt
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_logic_reduction | 0 | 0 | 0.00 |
| hlo_mux_reorder | 0 | 0 | 0.00 |

Starting mux speculation [v1.0] (stage: post_muxopt, startdef: ripple_carry_adder_4bit, recur: true)
Starting speculation optimization
Completed speculation optimization (accepts:0)
Completed mux speculation (accepts: 0, rejects: 0, runtime: 0.001s)

Stage: post_muxopt
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_speculation | 0 | 0 | 1.00 |

=====
Stage : to_generic
=====
Message Summary
=====

| Id | Sev | Count | Message Text |
| --- | --- | --- | --- |
| 1 | INFO | 1 | Warning! In legacy mode, Genius creates a blank hw.acf file.

Ln 164, Col 36 73.631 characters

```

5. Generate & Read the Reports: (with clear snapshots)

For generating the report run the following commands:

```
report_timing > rca_timing.rep
```

```
report_area > rca_area.rep
```

```
report_power > rca_power.rep
```

The screenshot shows three terminal windows side-by-side, each displaying a synthesis report for a ripple carry adder.

- rca_power.rep:** Displays power consumption details. It includes a table for leakage power by category (memory, register, latch, logic, bbox, clock, pad, pm) and a summary table for total power consumption.
- rca_timing.rep:** Displays timing constraints. It shows generated by information (Genus(TM) Synthesis Solution 21.14-s082_1, Aug 02 2024 12:32:31 pm), module (ripple_carry_adder_4bit), technology library (slow_vddlv0 1.0), operating conditions (PVT_0P9V_125C (balanced_tree)), wireload mode (enclosed), and area mode (timing library). It also lists pins, types, fanout, load, slew, delay, and arrival times.
- rca_area.rep:** Displays area usage. It includes a table for total area by instance and a note that wireload is default in the technology library.

6. Writing the Output files: (with clear snapshots)

Run the following commands to write the output files:

```
write_netlist > rca_netlist.v (alu\_netlist--link)
```

```
write_sdc > rca.sdc
```

rca.sdc

File Edit View

```
# #####  
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Fri Aug 02 12:32:31 IST 2024  
# #####  
  
set sdc_version 2.0  
  
set_units -capacitance 1000fF  
set_units -time 1000ps  
  
# Set the current design  
current_design ripple_carry_adder_4bit  
  
create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]  
set_clock_transition 0.1 [get_clocks clk]  
set_clock_gating_check -setup 0.0  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {a[3]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {a[2]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {a[1]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {a[0]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {b[3]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {b[2]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {b[1]}]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {b[0]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {s[3]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {s[2]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {s[1]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {s[0]}]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports c_out]  
set_wire_load_mode "enclosed"  
set_clock_uncertainty -setup 0.01 [get_ports clk]  
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

rca_netlist.v

File Edit View

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1  
// Generated on: Aug 2 2024 12:32:31 IST (Aug 2 2024 07:02:31 UTC)  
  
// Verification Directory fv/ripple_carry_adder_4bit  
  
module ripple_carry_adder_4bit(a, b, clk, s, c_out);  
    input [3:0] a, b;  
    input clk;  
    output [3:0] s;  
    output c_out;  
    wire [3:0] a, b;  
    wire clk;  
    wire [3:0] s;  
    wire c_out;  
    wire [3:0] carry;  
    full_adder fa0(.a (a[0]), .b (b[0]), .c (1'b0), .clk (clk), .s  
        (s[0]), .c_out (carry[0]));  
    full_adder fa1(.a (a[1]), .b (b[1]), .c (carry[0]), .clk (clk), .s  
        (s[1]), .c_out (carry[1]));  
    full_adder fa2(.a (a[2]), .b (b[2]), .c (carry[1]), .clk (clk), .s  
        (s[2]), .c_out (carry[2]));  
    full_adder fa3(.a (a[3]), .b (b[3]), .c (carry[2]), .clk (clk), .s  
        (s[3]), .c_out (c_out));  
endmodule
```

Ln 1, Col 1 | 813 characters | 100% | Unix (LF) | UTF-8

7. Method of writing a script file (.tcl) for synthesis:

1.)Create a file with .tcl extension in synthesis folder and type the following commands and save it:

```
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/  
  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl {ripple_carry_adder_4bit.v}  
  
elaborate  
read_sdc rca_constraints_top.g  
  
set_attribute syn_generic_effort medium  
set_attribute syn_map_effort medium  
set_attribute syn_opt_effort medium  
  
syn_generic  
syn_map  
syn_opt  
  
write_netlist > rca_netlist.v  
write_sdc > rca.sdc  
gui_show  
  
report_timing > rca_timing.rep  
report_area > rca_area.rep  
report_power > rca_power.rep
```

2.)After creating the .g and .tcl file open the terminal of synthesis folder and the run the following commands:

```
'csh'  
'source /home/install/cshrc'  
'genus -legacy -ui -f ripple.tcl'
```

ripple.tcl

```

File Edit View

set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {ripple_carry_adder_4bit.v}

elaborate
read_sdc rca_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort medium
set_attribute syn_opt_effort medium

syn_generic
syn_map
syn_opt

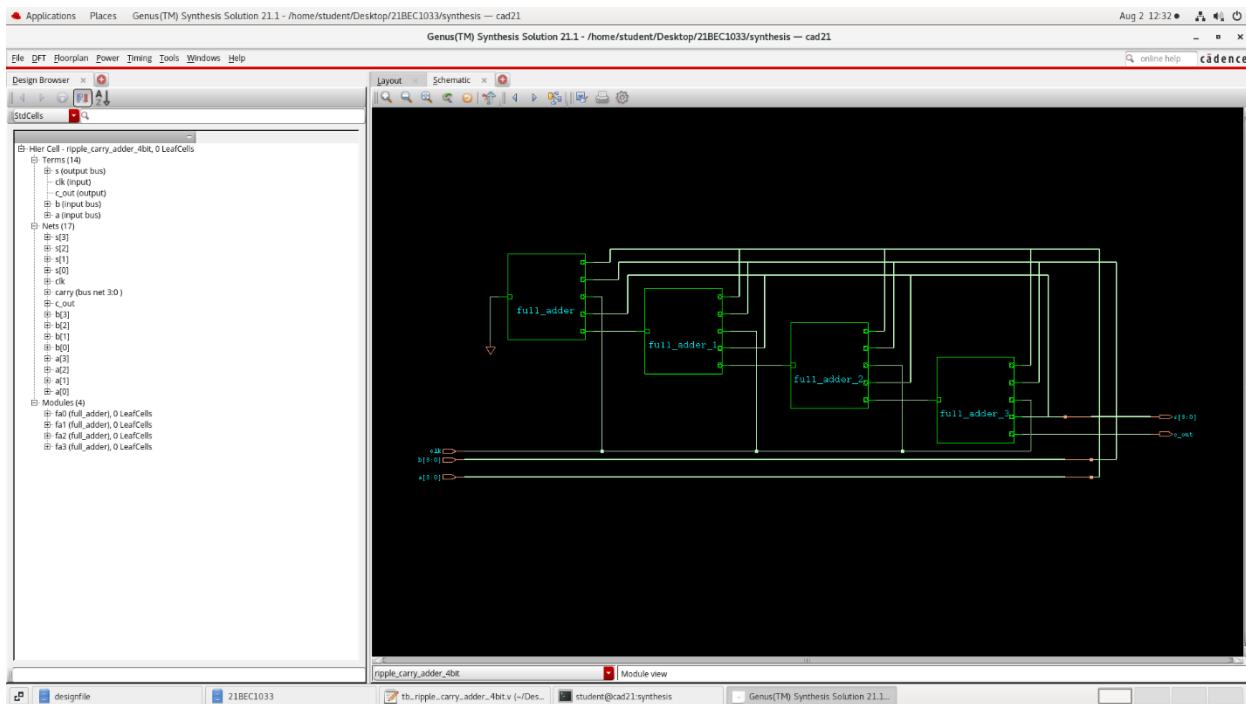
write_netlist > rca_netlist.v
write_sdc > rca.sdc
gui_show

report_timing > rca_timing.rep
report_area > rca_area.rep
report_power > rca_power.rep

```

Ln 5, Col 37 | 564 characters | 100% | Windows (CRLF) | UTF-8

8. Genus Schematic:



9. Functional verification:

