

Lab-5: Logic synthesis and Physical Desgin of an adding CPU

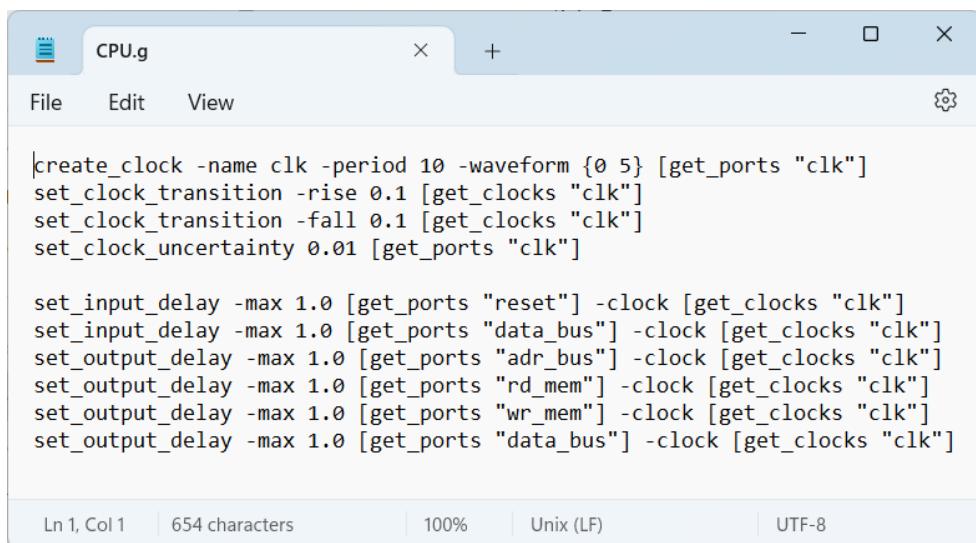
Aim: To synthesize an adding CPU and to get the gate level netlist with timing, area, and power reports.

EDA Tools Used: Cadence Genus (Logic synthesis tool) and Innovus

Description: An Adding CPU reads Load, Add, Store, and Jump instructions from its memory, and depending on the instruction it reads, loads data, performs addition, stores data into memory, or jumps to another memory location. The Adding CPU has a main register called AC (accumulator). The Load instruction directs the machine to load the addressed data from the memory into AC. The Store instruction causes contents of AC to be written into the addressed location in the memory. The operand of the Add instruction is immd (immediate). This instruction adds immd to the present contents of AC and puts the result back into AC. The Jump instruction loads the 6-bit address into the program counter of our machine, causing the next instruction to be fetched from this address.

Procedure:

1. Copy the fast.lib and slow.lib files into the folder where (.v) files are located.
2. Create a Synopsys design constraint file (.SDC file) by entering the design constraints required for the synthesis.



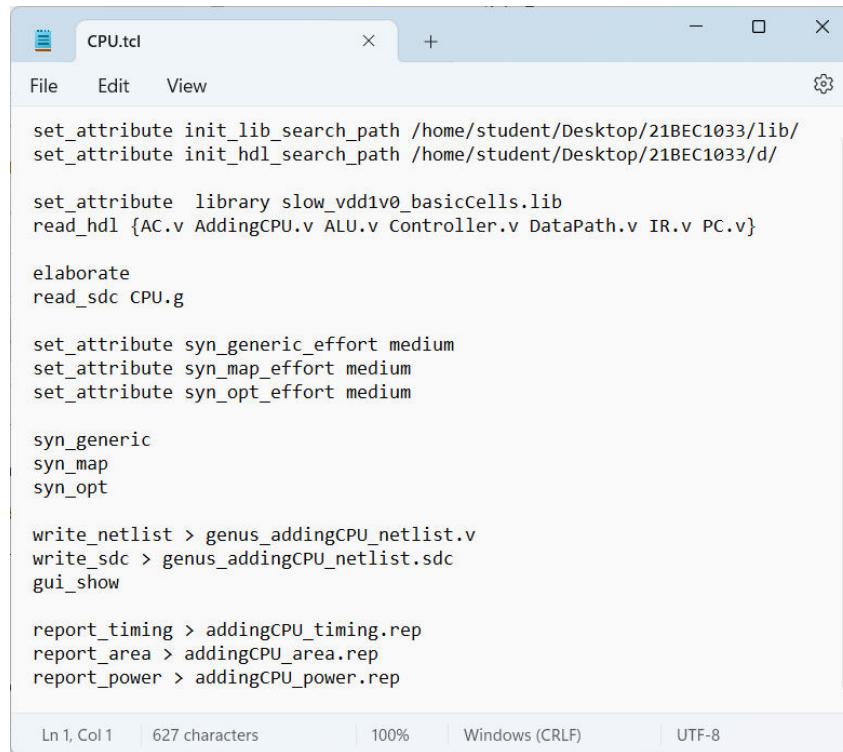
```
|create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "data_bus"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "adr_bus"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "rd_mem"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "wr_mem"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "data_bus"] -clock [get_clocks "clk"]
```

Ln 1, Col 1 654 characters 100% Unix (LF) UTF-8

Lab-5: Logic synthesis of an adding CPU

3. Create a (.tcl) file containing all the commands for performing the logic synthesis.
Synthesis effort can be medium or high.



```
File Edit View
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/d/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {AC.v AddingCPU.v ALU.v Controller.v DataPath.v IR.v PC.v}

elaborate
read_sdc CPU.sdc

set_attribute syn_generic_effort medium
set_attribute syn_map_effort medium
set_attribute syn_opt_effort medium

syn_generic
syn_map
syn_opt

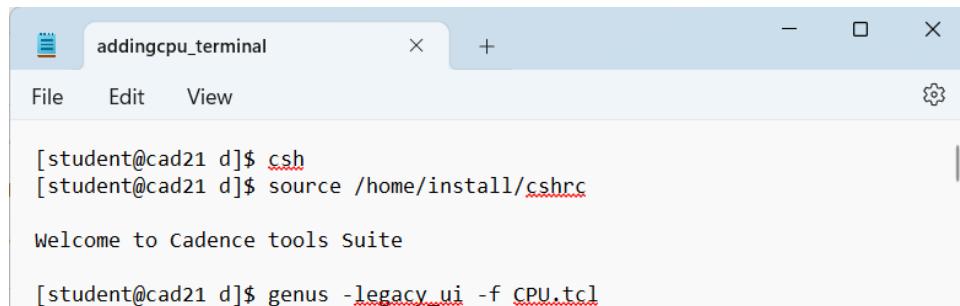
write_netlist > genus_addingCPU_netlist.v
write_sdc > genus_addingCPU_netlist.sdc
gui_show

report_timing > addingCPU_timing.rep
report_area > addingCPU_area.rep
report_power > addingCPU_power.rep

Ln 1, Col 1 627 characters 100% Windows (CRLF) UTF-8
```

4. Invoke the C shell and launch the Genus tool by entering the below commands.

Lab-5: Logic synthesis & Physical design of an adding CPU

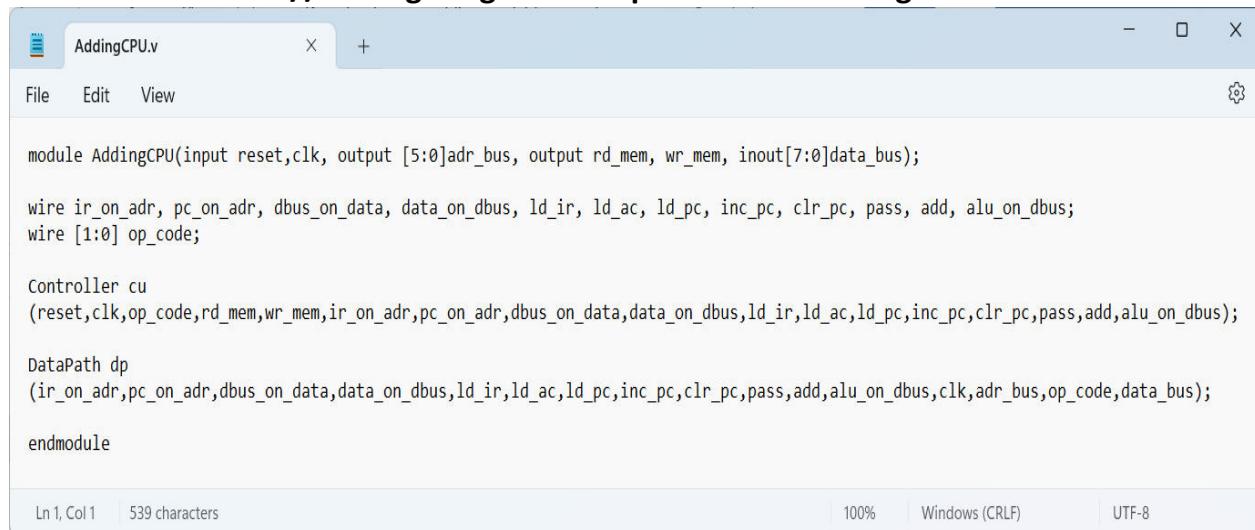


```
[student@cad21 d]$ csh
[student@cad21 d]$ source /home/install/cshrc
Welcome to Cadence tools Suite
[student@cad21 d]$ genus -legacy_ui -f CPU.tcl
```

5. Execute the commands in the (.tcl file) by entering **source CPU.tcl** command in the command line window.
6. Check for the area, timing and power reports generated in the respective adding CPU folder. Also check the gate level netlist generated in the Genus synthesis solution window.

Verilog Programs:

//Verilog Program of top module of adding CPU



```
module AddingCPU(input reset,clk, output [5:0]adr_bus, output rd_mem, wr_mem, inout[7:0]data_bus);

wire ir_on_adr, pc_on_adr, dbus_on_data, data_on_dbus, ld_ir, ld_ac, ld_pc, inc_pc, clr_pc, pass, add, alu_on_dbus;
wire [1:0] op_code;

Controller cu
(reset,clk,op_code,rd_mem,wr_mem,ir_on_adr,pc_on_adr,dbus_on_data,data_on_dbus,ld_ir,ld_ac,ld_pc,inc_pc,clr_pc,pass,add,alu_on_dbus);

DataPath dp
(ir_on_adr,pc_on_adr,dbus_on_data,data_on_dbus,ld_ir,ld_ac,ld_pc,inc_pc,clr_pc,pass,add,alu_on_dbus,clk,adr_bus,op_code,data_bus);

endmodule
```

Ln 1, Col 1 539 characters 100% Windows (CRLF) UTF-8

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//Verilog Program of the Controller

```
Controller.v
```

```
File Edit View
`define Reset 2'b00
`define Fetch 2'b01
`define Decode 2'b10
`define Execute 2'b11
module Controller (input reset,clk, input [1:0] op_code,output reg
rd_mem,wr_mem,ir_on_adr,pc_on_adr,dbus_on_data,data_on_dbus,ld_ir,ld_ac,ld_pc,inc_pc,clr_pc,pass,add,alu_on_dbus);
reg [1:0] present_state,next_state;
always@(posedge clk)
if (reset)present_state <= `Reset;
else present_state <= next_state;
always @(*present_state or reset)
begin: Combinational
rd_mem=1'b0;wr_mem=1'b0;ir_on_adr=1'b0;pc_on_adr=1'b0;dbus_on_data=1'b0;data_on_dbus=1'b0; ld_ir=1'b0;
ld_ac=1'b0;ld_pc=1'b0;inc_pc=1'b0;clr_pc=1'b0;pass=1'b0;add=1'b0;alu_on_dbus=1'b0;
case (present_state)`Reset: begin next_state = reset ? `Reset : `Fetch; clr_pc = 1'b1; end
`Fetch: begin next_state = `Decode;pc_on_adr = 1'b1;rd_mem = 1'b1;data_on_dbus = 1'b1;ld_ir = 1'b1;inc_pc = 1'b1;end
`Decode: next_state = `Execute; //End `Decode
`Execute: begin next_state = `Fetch; case (op_code) 2'b00: begin ir_on_adr = 1'b1;rd_mem = 1'b1;data_on_dbus =
1'b1;ld_ac = 1'b1;end
2'b01: begin pass = 1'b1;ir_on_adr = 1'b1;alu_on_dbus =
2'b10: ld_pc = 1'b1;
2'b11: begin add = 1'b1;alu_on_dbus = 1'b1;ld_ac = 1'b1;end
endcase
default: next_state = `Reset;
endcase
end
endmodule
Ln 8, Col 35 1,372 characters
140% Windows (CRLF) UTF-8
```

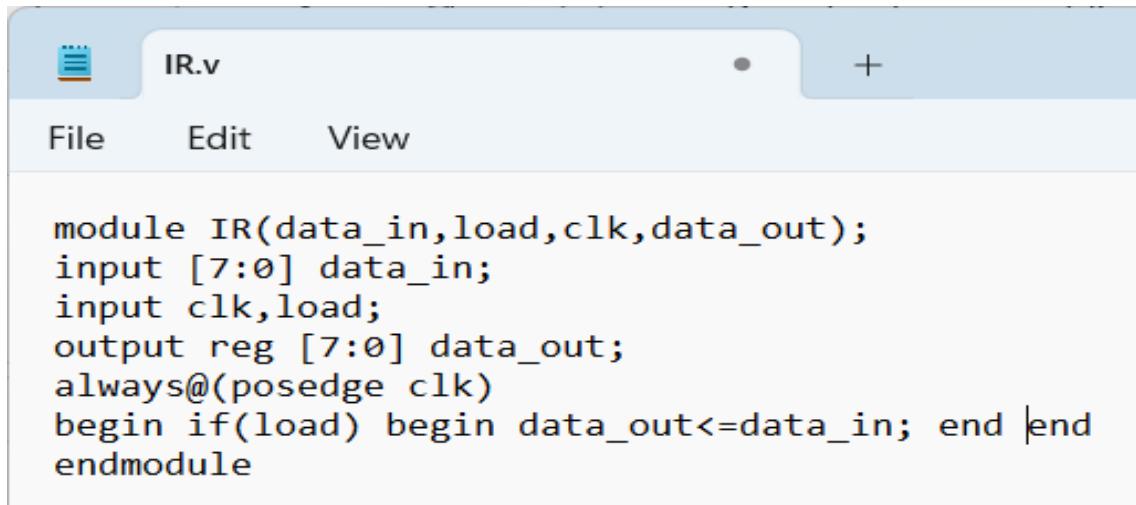
//Verilog Program of DataPath

```
DataPath.v
```

```
File Edit View
module DataPath ( input ir_on_adr,pc_on_adr,dbus_on_data,data_on_dbus,ld_ir,ld_ac,ld_pc,inc_pc,clr_pc,pass,add,alu_on_dbus,clk,
                  output [5:0] adr_bus,
                  output [1:0] op_code,
                  inout [7:0] data_bus);
wire [7:0] dbus,ir_out,a_side,alu_out;
wire [5:0] pc_out;
IR ir (dbus,ld_ir,clk,ir_out);
PC pc (ir_out[5:0],ld_pc,inc_pc,clr_pc,clk,pc_out);
AC ac (dbus,ld_ac,clk,a_side);
ALU alu (a_side,{2'b00,ir_out[5:0]},pass,add,alu_out);
assign adr_bus = ir_on_adr ? ir_out[5:0] : 6'bzz_zzzz;
assign adr_bus = pc_on_adr ? pc_out : 6'bzz_zzzz;
assign dbus = alu_on_dbus ? alu_out : 8'bzzzz_zzzz;
assign data_bus = dbus_on_data ? dbus : 8'bzzzz_zzzz;
assign dbus = data_on_dbus ? data_bus : 8'bzzzz_zzzz;
assign op_code = ir_out[7:6];
endmodule
Ln 11, Col 1 739 characters
```

Lab-5: Logic synthesis & Physical design of an adding CPU

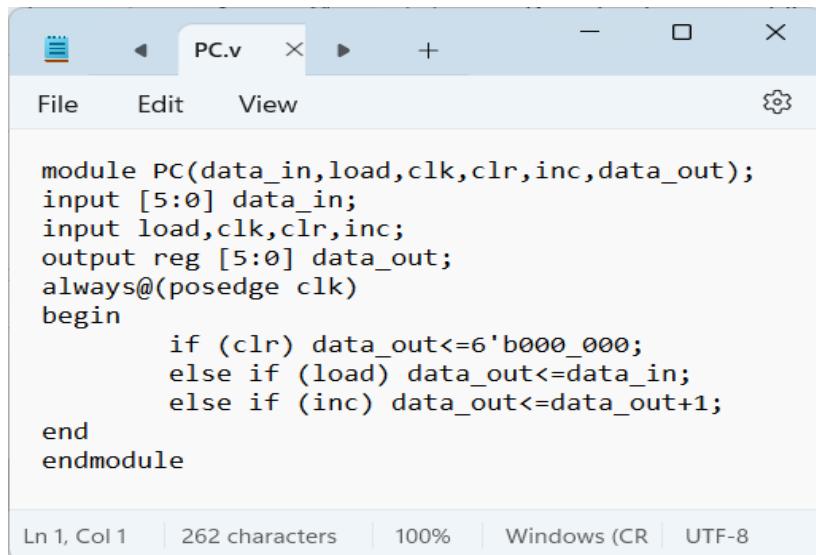
//Verilog Program of IR



```
IR.v
File Edit View

module IR(data_in,load,clk,data_out);
input [7:0] data_in;
input clk,load;
output reg [7:0] data_out;
always@(posedge clk)
begin if(load) begin data_out<=data_in; end end
endmodule
```

//Verilog Program of PC

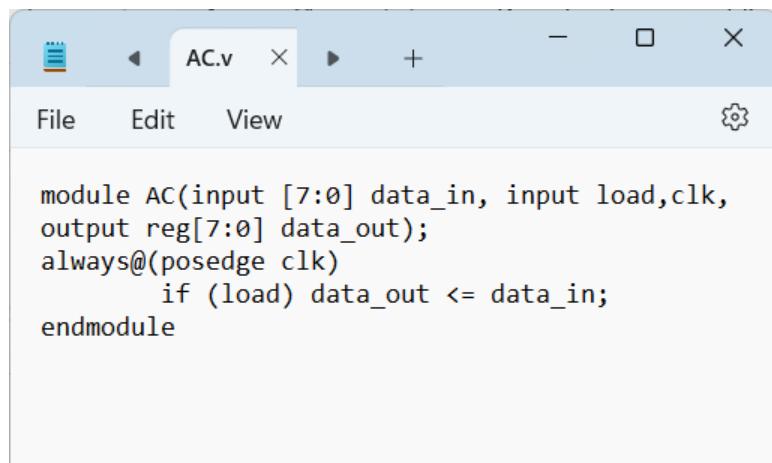


```
PC.v
File Edit View

module PC(data_in,load,clk,clr,inc,data_out);
input [5:0] data_in;
input load,clk,clr,inc;
output reg [5:0] data_out;
always@(posedge clk)
begin
    if (clr) data_out<=6'b000_000;
    else if (load) data_out<=data_in;
    else if (inc) data_out<=data_out+1;
end
endmodule

Ln 1, Col 1 | 262 characters | 100% | Windows (CR) | UTF-8
```

//Verilog Program of AC



```
AC.v
File Edit View

module AC(input [7:0] data_in, input load,clk,
output reg[7:0] data_out);
always@(posedge clk)
    if (load) data_out <= data_in;
endmodule
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

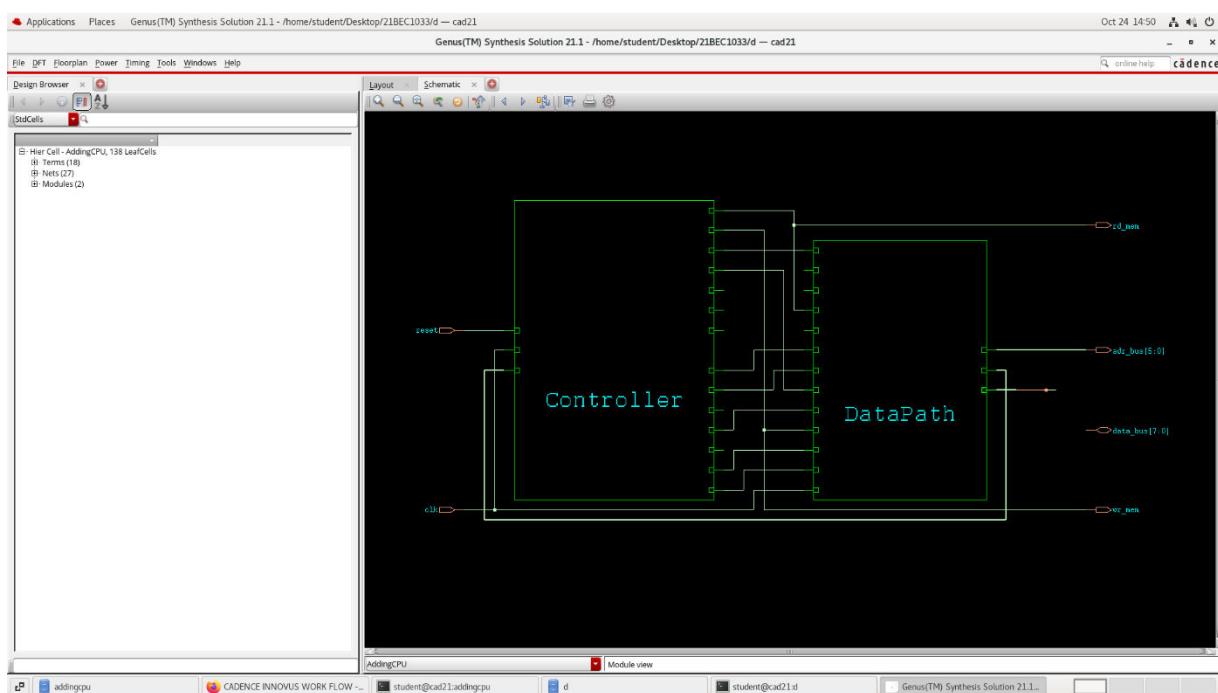
/Verilog Program of the ALU

```
ALU.v
```

```
module ALU (input [7:0]a,b,input pass,add, output reg [7:0]alu_out);
always@(a or b or pass or add)
    if (pass) alu_out = a;
    else if (add) alu_out = a+b;
    else alu_out = 0;
endmodule
```

Ln 1, Col 1 | 183 characters | 100% | Windows (CRLF) | UTF-8

Gate level Netlist:



Lab-5: Logic synthesis & Physical Design of an adding CPU

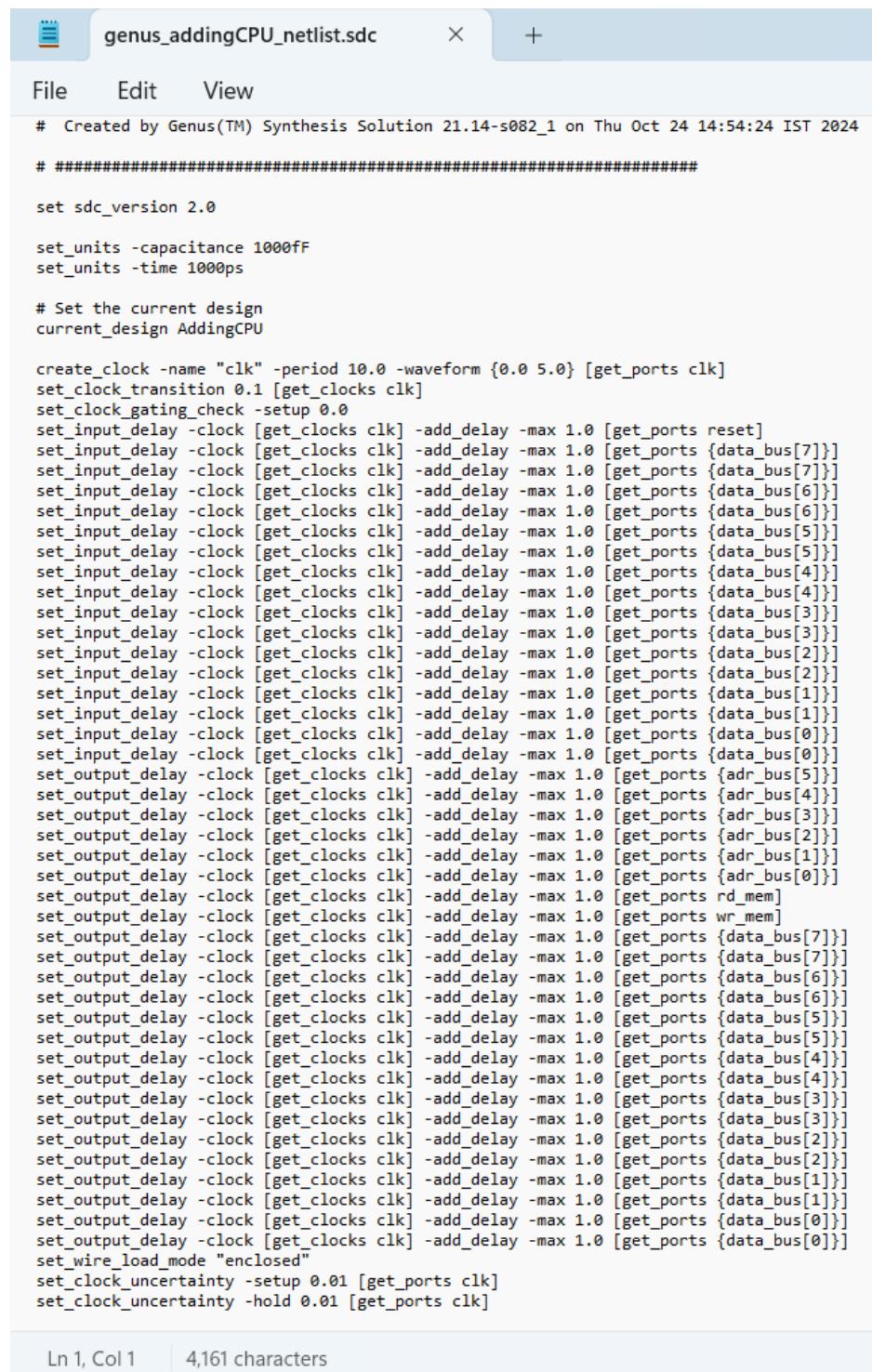
Observations:

Synthesis effort: Medium

a) addingCPU_netlist_created file

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b) addingCPU _Constraint_created file



The screenshot shows a software window titled "genus_addingCPU_netlist.sdc". The window has a menu bar with "File", "Edit", and "View". The main area contains the following SDC (Setup/Constraints) code:

```
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Oct 24 14:54:24 IST 2024
# #####
set sdc_version 2.0

set_units -capacitance 1000ff
set_units -time 1000ps

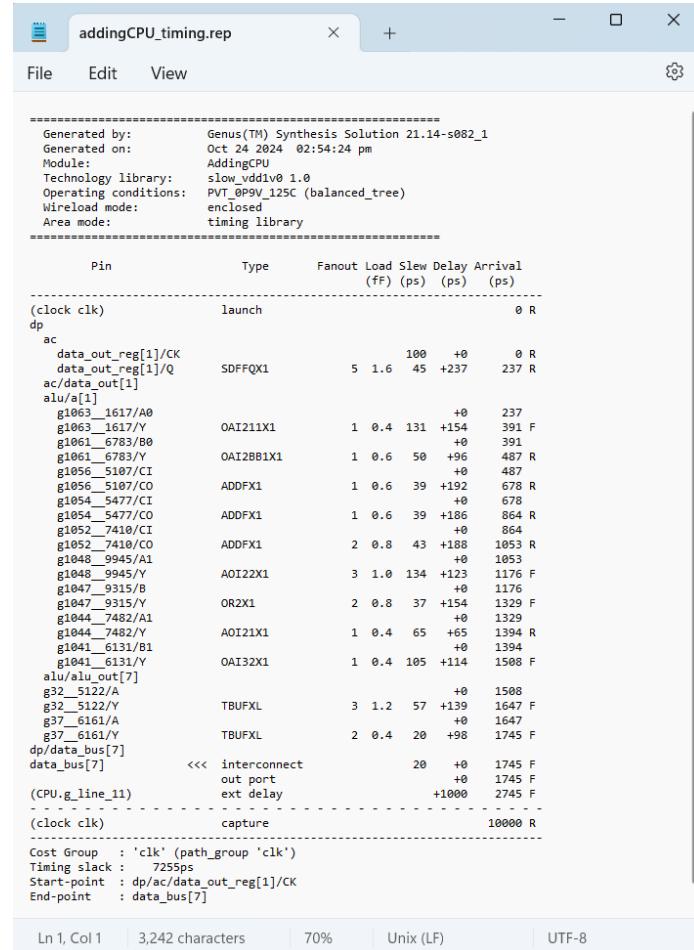
# Set the current design
current_design AddingCPU

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports reset]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[7]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[6]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[6]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[5]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[5]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[4]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[4]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[3]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[3]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[2]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[2]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[1]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[1]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[0]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[0]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {adr_bus[5]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {adr_bus[4]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {adr_bus[3]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {adr_bus[2]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {adr_bus[1]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {adr_bus[0]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports rd_mem]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports wr_mem]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[7]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[7]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[6]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[6]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[5]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[5]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[4]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[4]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[3]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[3]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[2]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[2]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[1]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[1]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[0]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {data_bus[0]}]
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.01 [get_ports clk]
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

At the bottom of the window, it says "Ln 1, Col 1" and "4,161 characters".

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c) addingCPU_timing_created file



```

=====
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Oct 24 2024 02:54:24 pm
Module: AddingCPU
Technology library: slow_vdd1v0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====

Pin          Type      Fanout Load Slew Delay Arrival
             (ff) (ps)   (ps) (ps)

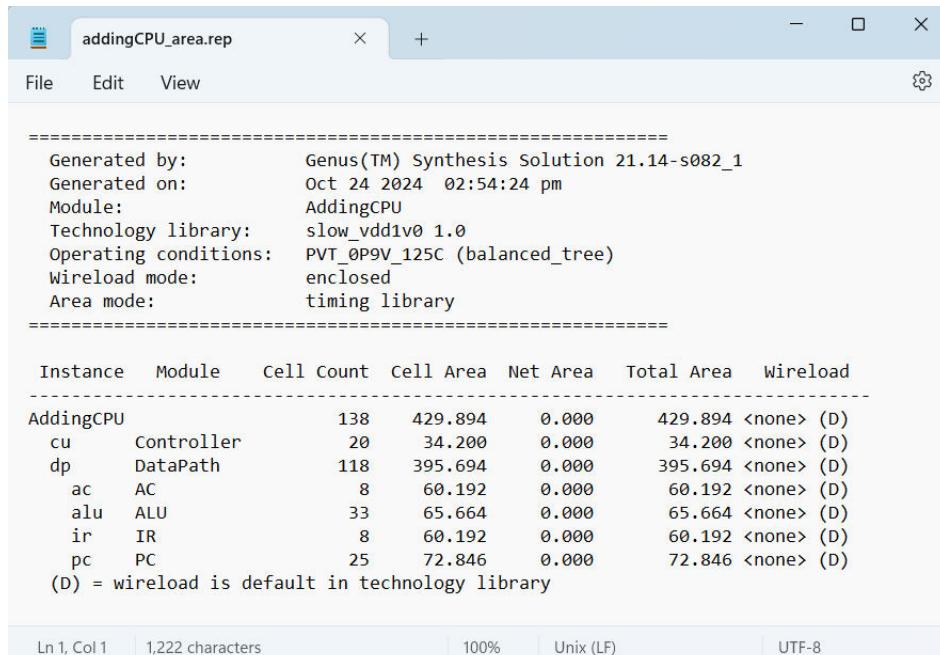
(clock clk)    launch           0 R
dp
  ac
    data_out_reg[1]/CK
    data_out_reg[1]/Q  SDFFQX1      5 1.6 45 +237  237 R
  ac/data_out[1]
  alu/a[1]
  g1063_1617/A0
  g1063_1617/Y
  g1061_6783/B0
  g1061_6783/Y
  g1056_5107/CI
  g1056_5107/CO
  g1054_5477/CI
  g1054_5477/CO
  g1052_7418/CI
  g1052_7418/CO
  g1048_9945/A1
  g1048_9945/Y
  g1047_9315/B
  g1047_9315/Y
  g1044_7482/A1
  g1044_7482/Y
  g1041_6131/B1
  g1041_6131/Y
  alu/alu_out[7]
  g32_5122/A
  g32_5122/Y
  TBUFLX
  g37_6161/A
  g37_6161/Y
  TBUFLX
  dp/data_bus[7]
  data_bus[7]    <<< interconnect
                 out port
                 ext delay
(CPU.g_line_11)
  (clock clk)    capture           10000 R

Cost Group : 'clk' (path_group 'clk')
Timing slack : 7255ps
Start-point : dp/ac/data_out_reg[1]/CK
End-point : data_bus[7]

Ln 1, Col 1 | 3,242 characters | 70% | Unix (LF) | UTF-8

```

d) addingCPU_area_created file



```

=====
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Oct 24 2024 02:54:24 pm
Module: AddingCPU
Technology library: slow_vdd1v0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====

Instance  Module      Cell Count  Cell Area  Net Area  Total Area  Wireload
-----+
AddingCPU
  cu     Controller    20        34.200   0.000    34.200 <none> (D)
  dp     DataPath     118       395.694   0.000    395.694 <none> (D)
  ac     AC            8         60.192   0.000    60.192 <none> (D)
  alu    ALU           33        65.664   0.000    65.664 <none> (D)
  ir     IR            8         60.192   0.000    60.192 <none> (D)
  pc     PC            25        72.846   0.000    72.846 <none> (D)
(D) = wireload is default in technology library

Ln 1, Col 1 | 1,222 characters | 100% | Unix (LF) | UTF-8

```

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e) addingCPU _power_created file

addingCPU_power.rep

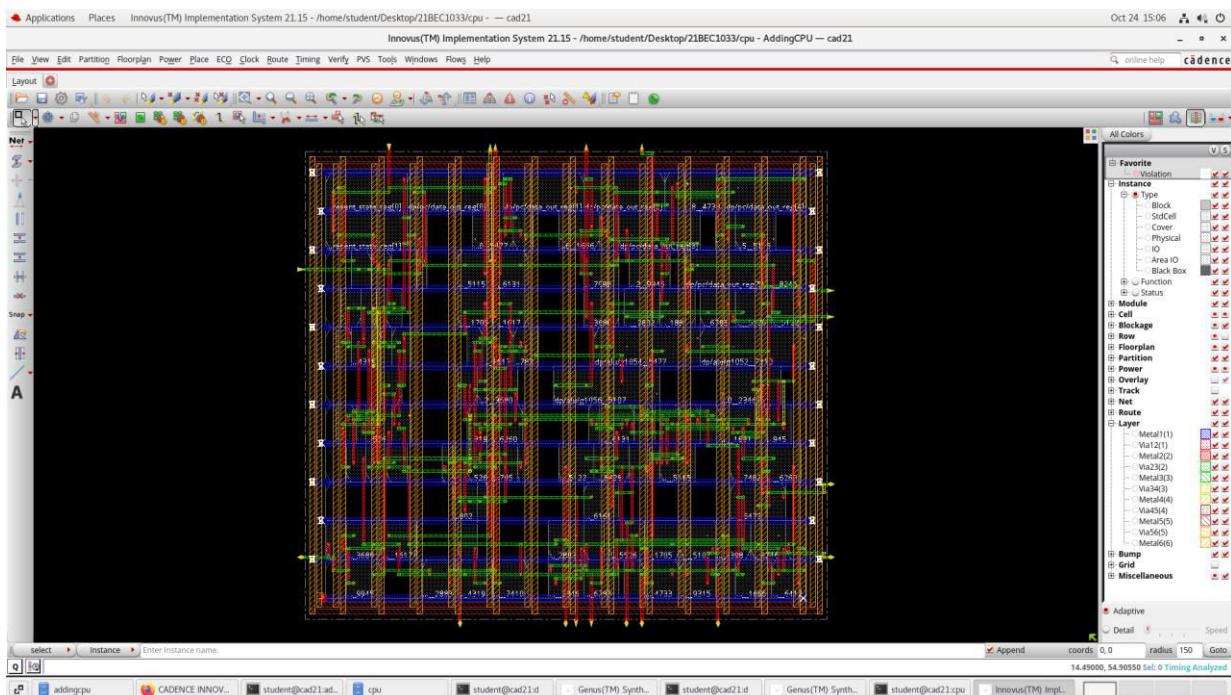
File Edit View

```
Instance: /AddingCPU
Power Unit: W
PDB Frames: /stim#0/frame#0
```

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	2.86784e-09	4.22850e-06	2.38743e-07	4.47011e-06	67.66%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	3.74852e-09	8.42245e-07	3.54288e-07	1.20028e-06	18.17%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	6.95167e-10	5.47958e-07	3.87878e-07	9.36531e-07	14.18%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	7.31153e-09	5.61870e-06	9.80909e-07	6.60692e-06	100.01%
Percentage	0.11%	85.04%	14.85%	100.00%	100.00%

Ln 1, Col 1 | 1,203 characters | 100% | Unix (LF) | UTF-8

f) Physical design of the CPU:



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g) Innovus Terminal:

```
[student@cad21 cpu]$ csh
[student@cad21 cpu]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 cpu]$ innovus

Cadence Innovus(TM) Implementation System.
Copyright 2021 Cadence Design Systems, Inc. All rights reserved
worldwide.

Version: v21.15-s110_1, built Fri Sep 23 13:08:12 PDT 2022
Options:
Date: Thu Oct 24 14:56:16 2024
Host: cad21 (x86_64 w/Linux 4.18.0-477.10.1.el8_8.x86_64)
(12cores*20cpus*12th Gen Intel(R) Core(TM) i7-12700 25600KB)
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

License:
[14:56:16.095673] Configured Lic search path (21.01-s002):
5280@cadence

      invs  Innovus Implementation System      21.1  checkout
succeeded
      8 CPU jobs allowed with the current license(s). Use
setMultiCpuUsage to set your required CPU count.
Create and set the environment variable TMPDIR to
/tmp/innovus_temp_33654_cad21_student_fiH8FJ.

Change the soft stacksize limit to 0.2%RAM (63 mbytes). Set global
soft_stack_size_limit to change the value.

**INFO: MMMC transition support version v31-84

[INFO] Loading PVS 22.20 fill procedures
innovus 1> **ERROR: (IMPSYT-16085): Specify the name of Analysis
View.
#% Begin Load MMMC data ... (date=10/24 15:01:15, mem=1035.2M)
#% End Load MMMC data ... (date=10/24 15:01:15, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1035.9M, current mem=1035.9M)

Loading LEF file
../../../../install/FOUNDRY/digital/180nm/dig/lef/all.lef ...
Set DBUPerIGU to M2 pitch 1320.
**WARN: (IMPLF-200): Pin 'A' in macro 'ANTENNA' has no ANTENNAGATEAREA
value defined. The library data is incomplete and some process antenna
rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-201): Pin 'Q[0]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
```

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```
**WARN: (IMPLF-201): Pin 'Q[10]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[11]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[12]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[13]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[14]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[15]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[1]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[2]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[3]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[4]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[5]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[6]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[7]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
```

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```
**WARN: (TECHLIB-302): No function defined for cell 'HOLDX1'. The cell
will only be used for analysis. (File
/home/install/FOUNDRY/digital/180nm/dig/lib/fast.lib)
Read 470 cells in library 'tsmc18'
*** End library_loading (cpu=0.01min, real=0.02min, mem=32.9M,
fe_cpu=0.54min, fe_real=5.00min, fe_mem=1068.7M) ***
#% Begin Load netlist data ... (date=10/24 15:01:16, mem=1058.4M)
*** Begin netlist parsing (mem=1068.7M) ***
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR3X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR3X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR3X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
```

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```
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (EMS-27):Message (IMPVL-159) has exceeded the current message
display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
Created 470 new cells from 2 timing libraries.
Reading netlist ...
Backslashed names will retain backslash and a trailing blank character.
Reading verilog netlist 'genus_addingCPU_netlist.v'
**WARN: (IMPVL-346): Module 'SDFFQX1' is instantiated in the netlist,
but is not defined in the LEF files. Since there is no real cell
definition for such a cell, it will be treated as an empty module.
Type 'man IMPVL-346' for more detail.
**WARN: (IMPVL-346): Module 'AO22XL' is instantiated in the netlist,
but is not defined in the LEF files. Since there is no real cell
definition for such a cell, it will be treated as an empty module.
Type 'man IMPVL-346' for more detail.
**WARN: (IMPVL-346): Module 'AO22X1' is instantiated in the netlist,
but is not defined in the LEF files. Since there is no real cell
definition for such a cell, it will be treated as an empty module.
Type 'man IMPVL-346' for more detail.
**WARN: (IMPVL-346): Module 'CLKXOR2X1' is instantiated in the netlist,
but is not defined in the LEF files. Since there is no real cell
definition for such a cell, it will be treated as an empty module.
Type 'man IMPVL-346' for more detail.

*** Memory Usage v#1 (Current mem = 1068.680M, initial mem = 483.863M)
***
*** End netlist parsing (cpu=0:00:00.0, real=0:00:00.0, mem=1068.7M) ***
#% End Load netlist data ... (date=10/24 15:01:16, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1073.1M, current mem=1073.1M)
Top level cell is AddingCPU.
Hooked 932 DB cells to tlib cells.
** Removed 8 unused lib cells.
**WARN: (IMPDB-2504): Unable to find netlist cell in the design data of
the library or LEF. The 'SDFFQX1' cell is instantiated in the Verilog
netlist, but not defined in the library or design data. Its pin
directions might be derived incorrectly. Include the cell definition or
its pin information in the library or design data and reload the design
to avoid potential issues.
```

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```
**WARN: (IMPLF-201): Pin 'Q[8]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[9]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[0]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[10]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[11]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[12]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (EMS-27):Message (IMPLF-201) has exceeded the current message
display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
**WARN: (IMPLF-200): Pin 'PAD' in macro 'PDB04DGZ' has no
ANTENNAGATEAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-200): Pin 'OEN' in macro 'PDB04DGZ' has no
ANTENNAGATEAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-200): Pin 'I' in macro 'PDB04DGZ' has no ANTENNAGATEAREA
value defined. The library data is incomplete and some process antenna
rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.

## Check design process and node:
## Both design process and tech node are not set.

Loading view definition file from Default.view
Reading max_timing timing library
'/home/install/FOUNDRY/digital/180nm/dig/lib/slow.lib' ...
**WARN: (TECHLIB-302): No function defined for cell 'HOLDX1'. The cell
will only be used for analysis. (File
'/home/install/FOUNDRY/digital/180nm/dig/lib/slow.lib')
Read 462 cells in library 'tsmc18'
Reading min_timing timing library
'/home/install/FOUNDRY/digital/180nm/dig/lib/fast.lib' ...
```

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```
Type 'man IMPDB-2504' for more detail.  
**WARN: (IMPDB-2504): Unable to find netlist cell in the design data of  
the library or LEF. The 'CLKXOR2X1' cell is instantiated in the Verilog  
netlist, but not defined in the library or design data. Its pin  
directions might be derived incorrectly. Include the cell definition or  
its pin information in the library or design data and reload the design  
to avoid potential issues.  
Type 'man IMPDB-2504' for more detail.  
**WARN: (IMPDB-2504): Unable to find netlist cell in the design data of  
the library or LEF. The 'AO22XI' cell is instantiated in the Verilog  
netlist, but not defined in the library or design data. Its pin  
directions might be derived incorrectly. Include the cell definition or  
its pin information in the library or design data and reload the design  
to avoid potential issues.  
Type 'man IMPDB-2504' for more detail.  
**WARN: (IMPDB-2504): Unable to find netlist cell in the design data of  
the library or LEF. The 'AO22XL' cell is instantiated in the Verilog  
netlist, but not defined in the library or design data. Its pin  
directions might be derived incorrectly. Include the cell definition or  
its pin information in the library or design data and reload the design  
to avoid potential issues.  
Type 'man IMPDB-2504' for more detail.  
4 empty module found.  
Starting recursive module instantiation check.  
No recursion found.  
Term dir updated for 0 vinsts of 4 cells.  
Building hierarchical netlist for Cell AddingCPU ...  
*** Netlist is unique.  
** info: there are 961 modules.  
** info: there are 112 stdCell insts.  
  
*** Memory Usage v#1 (Current mem = 1126.094M, initial mem = 483.863M)  
***  
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard  
cells in the LEF/OA library. The calculations for this site type cannot  
be made unless standard cell models of this type exist in the LEF/OA  
library. Ignore this warning if the SITE is not used by the library.  
Alternatively, remove the SITE definition for the LEF/OA library to avoid  
this message.  
Type 'man IMPFP-3961' for more detail.  
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells  
in the LEF/OA library. The calculations for this site type cannot be made  
unless standard cell models of this type exist in the LEF/OA library.  
Ignore this warning if the SITE is not used by the library.  
Alternatively, remove the SITE definition for the LEF/OA library to avoid  
this message.  
Type 'man IMPFP-3961' for more detail.  
Horizontal Layer M1 offset = 560 (derived)  
Vertical Layer M2 offset = 660 (derived)  
Start create_tracks  
Generated pitch 0.99 in Metal6 is different from 1.32 defined in  
technology file in preferred direction.  
Generated pitch 0.56 in Metal5 is different from 1.12 defined in  
technology file in preferred direction.
```

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```
Extraction setup Started
Initializing multi-corner RC extraction with 1 active RC Corners ...
**WARN: (IMPEXT-2773): The via resistance between layers POLY and M1
could not be determined from the LEF technology file because the via
resistance specification is missing. A default of 4 Ohms will be used as
via resistance between these layers.
Type 'man IMPEXT-2773' for more detail.
**WARN: (IMPEXT-2776): The via resistance between layers M1 and M2 is not
defined in the capacitance table file. The via resistance of 6.4 Ohms
defined in the LEF technology file will be used as via resistance between
these layers.
Type 'man IMPEXT-2776' for more detail.
**WARN: (IMPEXT-2776): The via resistance between layers M2 and M3 is not
defined in the capacitance table file. The via resistance of 6.4 Ohms
defined in the LEF technology file will be used as via resistance between
these layers.
Type 'man IMPEXT-2776' for more detail.
**WARN: (IMPEXT-2776): The via resistance between layers M3 and M4 is not
defined in the capacitance table file. The via resistance of 6.4 Ohms
defined in the LEF technology file will be used as via resistance between
these layers.
Type 'man IMPEXT-2776' for more detail.
**WARN: (IMPEXT-2776): The via resistance between layers M4 and M5 is not
defined in the capacitance table file. The via resistance of 6.4 Ohms
defined in the LEF technology file will be used as via resistance between
these layers.
Type 'man IMPEXT-2776' for more detail.
**WARN: (IMPEXT-2776): The via resistance between layers M5 and M6 is not
defined in the capacitance table file. The via resistance of 2.54 Ohms
defined in the LEF technology file will be used as via resistance between
these layers.
Type 'man IMPEXT-2776' for more detail.
**WARN: (IMPEXT-2766): The sheet resistance for layer M1 is not defined
in the cap table. Therefore, the LEF value 0.101 will be used instead. To
avoid this message, update the relevant cap table to include the sheet
resistance for the specified layer and read it back in.
**WARN: (IMPEXT-2766): The sheet resistance for layer M2 is not defined
in the cap table. Therefore, the LEF value 0.101 will be used instead. To
avoid this message, update the relevant cap table to include the sheet
resistance for the specified layer and read it back in.
**WARN: (IMPEXT-2766): The sheet resistance for layer M3 is not defined
in the cap table. Therefore, the LEF value 0.101 will be used instead. To
avoid this message, update the relevant cap table to include the sheet
resistance for the specified layer and read it back in.
**WARN: (IMPEXT-2766): The sheet resistance for layer M4 is not defined
in the cap table. Therefore, the LEF value 0.101 will be used instead. To
avoid this message, update the relevant cap table to include the sheet
resistance for the specified layer and read it back in.
**WARN: (IMPEXT-2766): The sheet resistance for layer M5 is not defined
in the cap table. Therefore, the LEF value 0.101 will be used instead. To
avoid this message, update the relevant cap table to include the sheet
resistance for the specified layer and read it back in.
**WARN: (IMPEXT-2766): The sheet resistance for layer M6 is not defined
in the cap table. Therefore, the LEF value 0.045 will be used instead. To
```

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avoid this message, update the relevant cap table to include the sheet resistance for the specified layer and read it back in.

Summary of Active RC-Corners :

```
Analysis View: worst_case
RC-Corner Name      : default_rc_corner
RC-Corner Index     : 0
RC-Corner Temperature : 25 Celsius
RC-Corner Cap Table  : ''
RC-Corner PreRoute Res Factor      : 1
RC-Corner PreRoute Cap Factor     : 1
RC-Corner PostRoute Res Factor    : 1 {1 1 1}
RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
RC-Corner PreRoute Clock Res Factor : 1 [Derived from Cap Table]
RC-Corner PreRoute Clock Cap Factor : 1 [Derived from Cap Table]
RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}      [Derived from
postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}      [Derived from
postRoute_res (effortLevel low)]
RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}

Analysis View: best_Case
RC-Corner Name      : default_rc_corner
RC-Corner Index     : 0
RC-Corner Temperature : 25 Celsius
RC-Corner Cap Table  : ''
RC-Corner PreRoute Res Factor      : 1
RC-Corner PreRoute Cap Factor     : 1
RC-Corner PostRoute Res Factor    : 1 {1 1 1}
RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
RC-Corner PreRoute Clock Res Factor : 1 [Derived from Cap Table]
RC-Corner PreRoute Clock Cap Factor : 1 [Derived from Cap Table]
RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}      [Derived from
postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}      [Derived from
postRoute_res (effortLevel low)]
RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}

Updating RC grid for preRoute extraction ...
Initializing multi-corner resistance tables ...
*Info: initialize multi-corner CTS.
Reading timing constraints file 'genus_addingCPU_netlist.sdc' ...
Current (total cpu=0:00:32.8, real=0:05:00, peak res=1378.4M, current
mem=1378.4M)
**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
genus_addingCPU_netlist.sdc, Line 9).

**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
genus_addingCPU_netlist.sdc, Line 10).

AddingCPU
INFO (CTE): Reading of timing constraints file
genus_addingCPU_netlist.sdc completed, with 2 WARNING
```

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```
Ending "Constraint file reading stats" (total cpu=0:00:00.0,
real=0:00:00.0, peak res=1392.4M, current mem=1392.4M)
Current (total cpu=0:00:32.8, real=0:05:00, peak res=1392.4M, current
mem=1392.4M)
Total number of combinational cells: 266
Total number of sequential cells: 178
Total number of tristate cells: 18
Total number of level shifter cells: 0
Total number of power gating cells: 0
Total number of isolation cells: 0
Total number of power switch cells: 0
Total number of pulse generator cells: 0
Total number of always on buffers: 0
Total number of retention cells: 0
List of usable buffers: BUFX2 BUFX1 BUFX12 BUFX16 BUFX20 BUFX3 BUFX4
BUFX8 BUFXL CLKBUFX2 CLKBUFX1 CLKBUFX12 CLKBUFX16 CLKBUFX20 CLKBUFX3
CLKBUFX4 CLKBUFX8 CLKBUFXL
Total number of usable buffers: 18
List of unusable buffers:
Total number of unusable buffers: 0
List of usable inverters: CLKINVX2 CLKINVX1 CLKINVX12 CLKINVX16 CLKINVX20
CLKINVX3 CLKINVX4 CLKINVX8 CLKINVXL INVX1 INVX2 INVX12 INVX16 INVX20
INVX3 INVXL INVX4 INVX8
Total number of usable inverters: 18
List of unusable inverters: RFRDX2 RFRDX1 RFRDX4
Total number of unusable inverters: 3
List of identified usable delay cells: DLY2X1 DLY1X1 DLY4X1 DLY3X1
Total number of identified usable delay cells: 4
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPLF-200      4  Pin '%s' in macro '%s' has no
ANTENNAGAT...
WARNING IMPLF-201      50 Pin '%s' in macro '%s' has no
ANTENNADIF...
WARNING IMPFP-3961     2  The techSite '%s' has no related
standar...
WARNING IMPEXT-2766     6  The sheet resistance for layer %s is
not...
WARNING IMPEXT-2773     1  The via resistance between layers %s
and...
WARNING IMPEXT-2776     5  The via resistance between layers %s
and...
WARNING IMPVL-346       4  Module '%s' is instantiated in the
netli...
WARNING IMPVL-159      924 Pin '%s' of cell '%s' is defined in LEF
...
WARNING IMPDB-2504      4  Unable to find netlist cell in the
desig...
WARNING TCLCMD-1461      2  Skipped unsupported command: %s
WARNING TECHLIB-302      2  No function defined for cell '%s'. The
c...
```

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```
*** Message Summary: 1004 warning(s), 0 error(s)

innovus 1> Adjusting coreMargin left      to finFet grid (PlacementGrid) :
after adjusting :2.64
Adjusting coreMargin bottom   to finFet grid (PlacementGrid) : after
adjusting :2.8
Adjusting coreMargin right    to finFet grid (PlacementGrid) : after
adjusting :2.64
Adjusting coreMargin top     to finFet grid (PlacementGrid) : after
adjusting :2.8
Adjusting core size to PlacementGrid : width :62.7 height : 55.44
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
unless standard cell models of this type exist in the LEF/OA library.
Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 560 (derived)
Vertical Layer M2 offset = 660 (derived)
Start create_tracks
Generated pitch 0.99 in Metal6 is different from 1.32 defined in
technology file in preferred direction.
Generated pitch 0.56 in Metal5 is different from 1.12 defined in
technology file in preferred direction.
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

viaInitial starts at Thu Oct 24 15:02:47 2024
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM1 GENERATE.
Type 'man IMPPP-557' for more detail.
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM2 GENERATE.
Type 'man IMPPP-557' for more detail.
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM3 GENERATE.
Type 'man IMPPP-557' for more detail.
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM4 GENERATE.
```

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```
Type 'man IMPPP-557' for more detail.  
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is  
obsolete and is being ignored. Remove this statement from the technology  
file: VIARULE TURNM5 GENERATE.  
Type 'man IMPPP-557' for more detail.  
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is  
obsolete and is being ignored. Remove this statement from the technology  
file: VIARULE TURNM6 GENERATE.  
Type 'man IMPPP-557' for more detail.  
viaInitial ends at Thu Oct 24 15:02:47 2024  
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:  
1709.7M)  
**WARN: (IMPPP-136): The currently specified top spacing 0.200000 is  
less than the required spacing 0.280000 for widths specified as 0.700000  
and 0.700000.  
**WARN: (IMPPP-136): The currently specified bottom spacing 0.200000  
is less than the required spacing 0.280000 for widths specified as  
0.700000 and 0.700000.  
**WARN: (IMPPP-136): The currently specified left spacing 0.200000 is  
less than the required spacing 0.460000 for widths specified as 0.700000  
and 0.700000.  
**WARN: (IMPPP-136): The currently specified right spacing 0.200000 is  
less than the required spacing 0.460000 for widths specified as 0.700000  
and 0.700000.  
Ring generation is complete.  
vias are now being generated.  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (1.70, 1.68) (2.14, 2.30).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (1.70, 58.74) (2.14,  
59.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 1.68) (66.28,  
2.30).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 58.74) (66.28,  
59.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (1.70, 1.68) (2.14,  
2.30).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (1.70, 58.74) (2.14,  
59.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 1.68) (66.28,  
2.30).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 58.74) (66.28,  
59.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (0.54, 0.70) (0.98, 1.40).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (0.54, 59.90) (1.24,  
60.34).
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (67.00, 0.70) (67.44,
1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (67.00, 59.64) (67.44,
60.34).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 0.70) (0.98, 1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (67.00, 0.70) (67.44,
1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 59.90) (1.24,
60.34).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (67.00, 59.64) (67.44,
60.34).
addRing created 8 wires.
ViaGen created 0 via, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+-----+
| Metal5 |        4       |      NA      |
| Metal6 |        4       |      NA      |
+-----+-----+-----+
innovus 1> addStripe will allow jog to connect padcore ring and block
ring.

Stripes will stop at the boundary of the specified area.
When breaking rings, the power planner will consider the existence of
blocks.
Stripes will not extend to closest target.
The power planner will set stripe antenna targets to none (no trimming
allowed).
Stripes will not be created over regions without power planning wires.
The entire stripe set will break at the domain if one of the nets is not
in the domain.
addStripe will break automatically at non-default domains when generating
global stripes over the core area or default domain.
Offset for stripe breaking is set to 0.

Initialize fgc environment(mem: 1714.8M) ... fail and won't use fgc to
check drc(cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1714.8M)
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1714.8M)
Loading wires (cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1714.8M)
Loading via instances (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1714.8M)
**WARN: (IMPPP-136): The currently specified spacing 0.200000 in -
spacing option is less than the required spacing 0.460000 for widths
specified as 0.700000 and 0.700000.
Starting stripe generation ...
Non-Default Mode Option Settings :
    NONE
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
Completing 10% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 20% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 30% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 40% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 50% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 60% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 70% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 80% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 90% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Completing 100% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1714.8M)
Stripe generation is complete.
vias are now being generated.
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (3.64, 1.68) (4.08, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (3.64, 58.74) (4.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (8.64, 1.68) (9.08, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (8.64, 58.74) (9.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (13.64, 1.68) (14.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (13.64, 58.74) (14.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (18.64, 1.68) (19.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (18.64, 58.74) (19.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (23.64, 1.68) (24.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (23.64, 58.74) (24.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (28.64, 1.68) (29.08,
2.30).
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (28.64, 58.74) (29.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (33.64, 1.68) (34.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (33.64, 58.74) (34.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (38.64, 1.68) (39.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (38.64, 58.74) (39.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (43.64, 1.68) (44.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (43.64, 58.74) (44.08,
59.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (48.64, 1.68) (49.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (48.64, 58.74) (49.08,
59.36).
**WARN: (EMS-27):Message (IMPPP-531) has exceeded the current message
display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
addStripe created 26 wires.
ViaGen created 0 via, deleted 0 via to avoid violation.
+-----+-----+
| Layer | Created | Deleted |
+-----+-----+
| Metal6 |    26   |      NA   |
+-----+-----+
innovus 1> **WARN: (IMPSR-4058): Sroute option: blockPinTarget should be
used in conjunction with option: -connect blockPin.
*** Begin SPECIAL ROUTE on Thu Oct 24 15:03:43 2024 ***
SPECIAL ROUTE ran on directory: /home/student/Desktop/21BEC1033/cpu
SPECIAL ROUTE ran on machine: cad21 (Linux 4.18.0-477.10.1.el8_8.x86_64
x86_64 2.10Ghz)

Begin option processing ...
srouteConnectPowerBump set to false
routeSelectNet set to "VDD VSS"
routeSpecial set to true
srouteBottomLayerLimit set to 1
srouteBottomTargetLayerLimit set to 1
srouteConnectBlockPin set to false
srouteConnectConverterPin set to false
srouteConnectPadPin set to false
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
srouteConnectStripe set to false
srouteCrossoverViaBottomLayer set to 1
srouteCrossoverViaTopLayer set to 6
srouteFollowCorePinEnd set to 3
srouteFollowPadPin set to false
srouteJogControl set to "preferWithChanges differentLayer"
srouteNoViaOnWireShape set to "padring ring stripe blockring blockpin
coverpin blockwire corewire followpin iowire"
sroutePadPinAllPorts set to true
sroutePreserveExistingRoutes set to true
srouteRoutePowerBarPortOnBothDir set to true
srouteStopBlockPin set to "nearestTarget"
srouteTopLayerLimit set to 6
srouteTopTargetLayerLimit set to 6
End option processing: cpu: 0:00:00, real: 0:00:00, peak: 3217.00 megs.

Reading DB technology information...
Finished reading DB technology information.
Reading floorplan and netlist information...
Finished reading floorplan and netlist information.
Read in 12 layers, 6 routing layers, 1 overlap layer
Read in 471 macros, 34 used
Read in 32 components
    32 core components: 32 unplaced, 0 placed, 0 fixed
Read in 18 logical pins
Read in 18 nets
Read in 2 special nets, 2 routed
2 nets selected.

Begin power routing ...
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the VDD net.
    Run the globalNetConnect command or change the CPF file to ensure that
    the netlist reflects the correct power ground connections. The standard
    cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
    connection.
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the VSS net.
    Run the globalNetConnect command or change the CPF file to ensure that
    the netlist reflects the correct power ground connections. The standard
    cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
    connection.
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VDD.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VDD.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 52.80) (66.28,  
53.60).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.87, 52.80) (66.28,  
53.60).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (66.14, 52.80) (66.28,  
53.60).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 42.72) (66.28,  
43.52).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 42.72) (66.28,  
43.52).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.87, 42.72) (66.28,  
43.52).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (66.14, 42.72) (66.28,  
43.52).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 32.64) (66.28,  
33.44).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 32.64) (66.28,  
33.44).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.87, 32.64) (66.28,  
33.44).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (66.14, 32.64) (66.28,  
33.44).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 22.56) (66.28,  
23.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.84, 22.56) (66.28,  
23.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (65.87, 22.56) (66.28,  
23.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,  
viaGen fail to generate via on layer Via56 at (66.14, 22.56) (66.28,  
23.36).
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VSS.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VSS.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VDD.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VSS.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VDD.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
CPU time for VDD FollowPin 0 seconds
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VSS.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
CPU time for VSS FollowPin 0 seconds
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (65.84, 52.80) (66.28,
53.60).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (65.84, 52.80) (66.28,
53.60).
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
**WARN: (EMS-27):Message (IMPPP-531) has exceeded the current message
display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
    Number of Core ports routed: 23  open: 1
    Number of Followpin connections: 12
End power routing: cpu: 0:00:00, real: 0:00:00, peak: 3228.00 megs.

Begin updating DB with routing results ...
Updating DB with 5 via definition ...Extracting standard cell pins and
blockage .....
Pin and blockage extraction finished

sroute post-processing starts at Thu Oct 24 15:03:43 2024
The viaGen is rebuilding shadow vias for net VDD.
sroute post-processing ends at Thu Oct 24 15:03:43 2024
sroute created 59 wires.
ViaGen created 1 via, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created   |     Deleted   |
+-----+-----+-----+
| Metal1 |      35       |      NA        |
| Vial2  |      1        |      0         |
| Metal2 |      1        |      NA        |
| Metal6 |     23        |      NA        |
+-----+-----+-----+
*** placeDesign #1 [begin] : totSession cpu/real = 0:00:46.1/0:09:00.4
(0.1), mem = 1722.6M
Extracting standard cell pins and blockage .....
Pin and blockage extraction finished
*** Starting placeDesign default flow ***
*** Start deleteBufferTree ***
Info: Detect buffers to remove automatically.
Analyzing netlist ...
Updating netlist

*summary: 0 instances (buffers/inverters) removed
*** Finish deleteBufferTree (0:00:00.1) ***
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
Set Default Input Pin Transition as 1 ps.
**INFO: Analyzing IO path groups for slack adjustment
Effort level <high> specified for reg2reg_tmp.33654 path_group
AAE_INFO: opIsDesignInPostRouteState() is 0
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
AAE DB initialization (MEM=1857.64 CPU=0:00:00.0 REAL=0:00:00.0)
#####
# Design Stage: PreRoute
# Design Name: AddingCPU
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=1860.65)
*** Calculating scaling factor for max_timing libraries using the default
operating condition of each library.
Total number of fetched objects 127
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=2025.47 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2025.47 CPU=0:00:00.0
REAL=0:00:00.0)
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Input Pin Transition as 0.1 ps.
Set Default Net Load as 0.5 pF.
**INFO: Pre-place timing setting for timing analysis already disabled
Deleted 0 physical inst (cell - / prefix -).
INFO: #ExclusiveGroups=0
INFO: There are no Exclusive Groups.
*** Starting "NanoPlace(TM) placement v#6 (mem=1999.7M)" ...
*** Build Buffered Sizing Timing Model
(cpu=0:00:00.9 mem=2007.7M) ***
*** Build Virtual Sizing Timing Model
(cpu=0:00:01.0 mem=2007.7M) ***
No user-set net weight.
Net fanout histogram:
2          : 40 (38.1%) nets
3          : 40 (38.1%) nets
4      -    14      : 24 (22.9%) nets
15     -    39      : 1 (1.0%) nets
40     -    79      : 0 (0.0%) nets
80     -   159      : 0 (0.0%) nets
160    -   319      : 0 (0.0%) nets
320    -   639      : 0 (0.0%) nets
640    -  1279      : 0 (0.0%) nets
1280   -  2559      : 0 (0.0%) nets
2560   -  5119      : 0 (0.0%) nets
5120+   : 0 (0.0%) nets
Options: timingDriven clkGateAware ignoreScan pinGuide congEffort=auto
gpeffort=medium
**WARN: (IMPSP-9042): Scan chains were not defined, -
place_global_ignore_scan option will be ignored.
Define the scan chains before using this option.
Type 'man IMPSP-9042' for more detail.
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#std cell=112 (0 fixed + 112 movable) #buf cell=8 #inv cell=10 #block=0
(0 floating + 0 preplaced)
#ioInst=0 #net=105 #term=348 #term/net=3.31, #fixedIo=0, #floatIo=0,
#fixedPin=0, #floatPin=18
stdCell: 112 single + 0 double + 0 multi
Total standard cell length = 0.4798 (mm), area = 0.0024 (mm^2)
Average module density = 0.696.
Density for the design = 0.696.
    = stdcell_area 727 sites (2418 um^2) / alloc_area 1045 sites (3476
um^2).
Pin Density = 0.3330.
    = total # of pins 348 / total area 1045.
== lastAutoLevel = 5
Clock gating cells determined by native netlist tracing.
Iteration 1: Total net bbox = 2.692e-13 (0.00e+00 2.69e-13)
    Est. stn bbox = 2.918e-13 (0.00e+00 2.92e-13)
    cpu = 0:00:00.0 real = 0:00:00.0 mem = 2051.8M
Iteration 2: Total net bbox = 2.692e-13 (0.00e+00 2.69e-13)
    Est. stn bbox = 2.918e-13 (0.00e+00 2.92e-13)
    cpu = 0:00:00.0 real = 0:00:00.0 mem = 2051.8M
Iteration 3: Total net bbox = 2.014e+02 (1.01e+02 1.01e+02)
    Est. stn bbox = 2.244e+02 (1.12e+02 1.12e+02)
    cpu = 0:00:00.0 real = 0:00:00.0 mem = 2053.2M
Active setup views:
worst_case
Iteration 4: Total net bbox = 8.252e+02 (4.10e+02 4.15e+02)
    Est. stn bbox = 9.614e+02 (4.97e+02 4.64e+02)
    cpu = 0:00:00.0 real = 0:00:00.0 mem = 2053.2M
Iteration 5: Total net bbox = 1.010e+03 (5.26e+02 4.84e+02)
    Est. stn bbox = 1.184e+03 (6.46e+02 5.38e+02)
    cpu = 0:00:00.0 real = 0:00:00.0 mem = 2053.2M
Iteration 6: Total net bbox = 1.366e+03 (7.25e+02 6.41e+02)
    Est. stn bbox = 1.555e+03 (8.51e+02 7.05e+02)
    cpu = 0:00:00.1 real = 0:00:01.0 mem = 2053.2M
*** cost = 1.366e+03 (7.25e+02 6.41e+02) (cpu for global=0:00:00.1)
real=0:00:01.0 ***
Info: 0 clock gating cells identified, 0 (on average) moved 0/1
Solver runtime cpu: 0:00:00.1 real: 0:00:00.1
Core Placement runtime cpu: 0:00:00.1 real: 0:00:01.0
**WARN: (IMPSP-9025): No scan chain specified/traced.
Type 'man IMPSP-9025' for more detail.
*** Starting refinePlace (0:00:48.2 mem=2045.2M) ***
Total net bbox length = 1.394e+03 (7.403e+02 6.534e+02) (ext = 2.204e+02)
Move report: Detail placement moves 112 insts, mean move: 3.93 um, max
move: 12.93 um
    Max move on inst (dp/pc/g494_4319): (14.36, 49.67) --> (23.76,
53.20)
    Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 2069.2MB
Summary Report:
Instances move: 112 (out of 112 movable)
Instances flipped: 0
Mean displacement: 3.93 um
Max displacement: 12.93 um (Instance: dp/pc/g494_4319) (14.3625,
49.6685) -> (23.76, 53.2)
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
Length: 3 sites, height: 1 rows, site name: tsm3site, cell type:  
NAND2XL  
Total net bbox length = 1.561e+03 (7.533e+02 8.079e+02) (ext = 1.857e+02)  
Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 2069.2MB  
*** Finished refinePlace (0:00:48.2 mem=2069.2M) ***  
*** End of Placement (cpu=0:00:01.3, real=0:00:02.0, mem=2069.2M) ***  
default core: bins with density > 0.750 = 0.00 % ( 0 / 4 )  
Density distribution unevenness ratio = 0.000%  
*** Free Virtual Timing Model ... (mem=2069.2M)  
Starting IO pin assignment...  
The design is not routed. Using placement based method for pin  
assignment.  
Completed IO pin assignment.  
**INFO: Enable pre-place timing setting for timing analysis  
Set Using Default Delay Limit as 101.  
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is  
less than the default of 1000 and may result in inaccurate delay  
calculation for nets with a fanout higher than the setting. If needed,  
the default delay limit may be adjusted by running the command 'set  
delaycal_use_default_delay_limit'.  
Set Default Net Delay as 0 ps.  
Set Default Net Load as 0 pF.  
**INFO: Analyzing IO path groups for slack adjustment  
Effort level <high> specified for reg2reg_tmp.33654 path_group  
AAE_INFO: opIsDesignInPostRouteState() is 0  
#####  
# Design Stage: PreRoute  
# Design Name: AddingCPU  
# Design Mode: 90nm  
# Analysis Mode: MMMC OCV  
# Parasitics Mode: No SPEF/RCDB  
# Signoff Settings: SI Off  
#####  
Start delay calculation (fullDC) (1 T). (MEM=2051.27)  
Total number of fetched objects 127  
AAE_INFO: Total number of nets for which stage creation was skipped for  
all views 0  
End delay calculation. (MEM=2102.7 CPU=0:00:00.0 REAL=0:00:00.0)  
End delay calculation (fullDC). (MEM=2102.7 CPU=0:00:00.0 REAL=0:00:00.0)  
**INFO: Disable pre-place timing setting for timing analysis  
Set Using Default Delay Limit as 1000.  
Set Default Net Delay as 1000 ps.  
Set Default Net Load as 0.5 pF.  
Info: Disable timing driven in postCTS congRepair.  
  
Starting congRepair ...  
[NR-eGR] Num Prerouted Nets = 0 Num Prerouted Wires = 0  
[NR-eGR] Read 105 nets ( ignored 0 )  
[NR-eGR] There are 1 clock nets ( 0 with NDR ).  
[NR-eGR] Layer group 1: route 105 net(s) in layer range [2, 6]  
[NR-eGR] Early Global Route overflow of layer group 1: 0.00% H + 0.00% V.  
EstWL: 1.617840e+03um
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
End to check current routing status for nets (mem=1999.7M)
Extraction called for design 'AddingCPU' of instances=112 and nets=143
using extraction engine 'preRoute'.
**WARN: (IMPEXT-3530): The process node is not set. Use the command
setDesignMode -process <process node> prior to extraction for maximum
accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design AddingCPU.
RC Extraction called in multi-corner(1) mode.
**WARN: (IMPEXT-6197): The Cap table file is not specified. This will
result in lower parasitic accuracy when using preRoute extraction or
postRoute extraction with effort level 'low'. It is recommended to
generate the Cap table file using the 'generateCapTbl' command and
specify it before extraction using 'create_rc_corner/update_rc_corner -
cap_table'.
Type 'man IMPEXT-6197' for more detail.
RCMode: PreRoute
    RC Corner Indexes          0
    Capacitance Scaling Factor : 1.00000
    Resistance Scaling Factor : 1.00000
    Clock Cap. Scaling Factor : 1.00000
    Clock Res. Scaling Factor : 1.00000
    Shrink Factor             : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Updating RC grid for preRoute extraction ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0
MEM: 1999.656M)
Starting delay calculation for Setup views
AAE_INFO: opIsDesignInPostRouteState() is 0
#####
# Design Stage: PreRoute
# Design Name: AddingCPU
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=2013.21)
Total number of fetched objects 127
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=2113.77 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2113.77 CPU=0:00:00.0
REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0
totSessionCpu=0:00:52.4 mem=2113.8M)

-----
                timeDesign Summary
-----
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
[NR-eGR] Overflow after Early Global Route 0.00% H + 0.00% V
Early Global Route congestion estimation runtime: 0.01 seconds, mem =
2093.0M
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00,
normalized total congestion hotspot area = 0.00 (area is in unit of 4
std-cell row bins)
Skipped repairing congestion.
[NR-eGR]          Length (um)   Vias
[NR-eGR] -----
[NR-eGR] Metal1 (1H)           0    330
[NR-eGR] Metal2 (2V)          919   418
[NR-eGR] Metal3 (3H)          794    16
[NR-eGR] Metal4 (4V)          55     0
[NR-eGR] Metal5 (5H)           0     0
[NR-eGR] Metal6 (6V)           0     0
[NR-eGR] -----
[NR-eGR]          Total        1768   764
[NR-eGR] -----
-----[NR-eGR] Total half perimeter of net bounding box: 1536um
[NR-eGR] Total length: 1768um, number of vias: 764
[NR-eGR] -----
-----[NR-eGR] Total eGR-routed clock nets wire length: 31um, number of vias: 7
[NR-eGR] -----
-----Early Global Route wiring runtime: 0.00 seconds, mem = 2093.0M
Tdgp not successfully initied but do clear! skip clearing
End of congRepair (cpu=0:00:00.0, real=0:00:00.0)
*** Finishing placeDesign default flow ***
***** Total cpu 0:0:2
***** Total real time 0:0:3
**placeDesign ... cpu = 0: 0: 2, real = 0: 0: 3, mem = 2028.0M **
Tdgp not successfully initied but do clear! skip clearing

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPDC-1629      2  The default delay limit was set to %d.
T...
WARNING IMPSP-9025      1  No scan chain specified/traced.
WARNING IMPSP-9042      1  Scan chains were not defined, -
place_glo...
*** Message Summary: 4 warning(s), 0 error(s)

*** placeDesign #1 [finish] : cpu/real = 0:00:02.4/0:00:03.5 (0.7),
totSession cpu/real = 0:00:48.4/0:09:03.8 (0.1), mem = 2028.0M
innovus 1> AAE DB initialization (MEM=2009.66 CPU=0:00:00.0
REAL=0:00:00.0)
*** timeDesign #1 [begin] : totSession cpu/real = 0:00:52.2/0:10:15.3
(0.1), mem = 2009.7M
Setting timing_disable_library_data_to_data_checks to 'true'.
Setting timing_disable_user_data_to_data_checks to 'true'.
Start to check current routing status for nets...
All nets are already routed correctly.
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
Setup views included:  
worst_case  


| Setup mode       | all   | reg2reg | default |
|------------------|-------|---------|---------|
| WNS (ns):        | 5.723 | 8.772   | 5.723   |
| TNS (ns):        | 0.000 | 0.000   | 0.000   |
| Violating Paths: | 0     | 0       | 0       |
| All Paths:       | 18    | 2       | 18      |


| DRVs       | Real           |           | Total          |
|------------|----------------|-----------|----------------|
|            | Nr nets(terms) | Worst Vio | Nr nets(terms) |
| max_cap    | 0 (0)          | 0.000     | 0 (0)          |
| max_tran   | 0 (0)          | 0.000     | 0 (0)          |
| max_fanout | 0 (0)          | 0         | 0 (0)          |
| max_length | 0 (0)          | 0         | 0 (0)          |

  
Density: 69.56%  
Routing Overflow: 0.00% H and 0.00% V  
-----  
Reported timing to dir timingReports  
Total CPU time: 0.24 sec  
Total Real time: 1.0 sec  
Total Memory Usage: 2080.191406 Mbytes  
*** timeDesign #1 [finish] : cpu/real = 0:00:00.2/0:00:01.1 (0.2),  
totSession cpu/real = 0:00:52.5/0:10:16.4 (0.1), mem = 2080.2M  
innovus 1> *** timeDesign #2 [begin] : totSession cpu/real =  
0:00:52.9/0:10:23.2 (0.1), mem = 2090.4M  
Start to check current routing status for nets...  
All nets are already routed correctly.  
End to check current routing status for nets (mem=2044.7M)  
Starting delay calculation for Hold views  
AAE_INFO: opIsDesignInPostRouteState() is 0  
#####  
# Design Stage: PreRoute  
# Design Name: AddingCPU  
# Design Mode: 90nm  
# Analysis Mode: MMMC OCV  
# Parasitics Mode: No SPEF/RCDB  
# Signoff Settings: SI Off  
#####  
Start delay calculation (fullDC) (1 T). (MEM=2055.96)  
*** Calculating scaling factor for min_timing libraries using the default  
operating condition of each library.  
Total number of fetched objects 127
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
**ERROR: (IMPTCM-6): Missing object value for option "-bottom_preferred_layer".  
  
innovus 2> source ccopt.spec  
Creating clock tree spec for modes (timing configs): constraints  
extract_clock_generator_skew_groups=true: create_ccopt_clock_tree_spec  
will generate skew groups with a name prefix of "_clock_gen" to balance  
clock generator connected flops with the clock generator they drive.  
Reset timing graph...  
Ignoring AAE DB Resetting ...  
Reset timing graph done.  
Ignoring AAE DB Resetting ...  
Analyzing clock structure...  
Analyzing clock structure done.  
Reset timing graph...  
Ignoring AAE DB Resetting ...  
Reset timing graph done.  
Wrote: ccopt.spec  
innovus 3> saveDesignDBS/cts.enc1  
invalid command name "saveDesignDBS/cts.enc1"  
innovus 4> saveDesign DBS/cts.enc1  
% Begin save design ... (date=10/24 15:12:01, mem=1811.4M)  
% Begin Save ccopt configuration ... (date=10/24 15:12:01, mem=1811.4M)  
% End Save ccopt configuration ... (date=10/24 15:12:01, total  
cpu=0:00:00.0, real=0:00:00.0, peak res=1812.1M, current mem=1812.1M)  
% Begin Save netlist data ... (date=10/24 15:12:01, mem=1812.1M)  
Writing Binary DB to DBS/cts.enc1.dat/AddingCPU.v.bin in single-threaded  
mode...  
% End Save netlist data ... (date=10/24 15:12:01, total cpu=0:00:00.0,  
real=0:00:00.0, peak res=1812.9M, current mem=1812.9M)  
Saving symbol-table file ...  
Saving congestion map file DBS/cts.enc1.dat/AddingCPU.route.congmap.gz  
...  
% Begin Save AAE data ... (date=10/24 15:12:01, mem=1812.9M)  
Saving AAE Data ...  
% End Save AAE data ... (date=10/24 15:12:01, total cpu=0:00:00.0,  
real=0:00:00.0, peak res=1812.9M, current mem=1812.9M)  
Saving preference file DBS/cts.enc1.dat/gui.pref.tcl ...  
Saving mode setting ...  
Saving global file ...  
% Begin Save floorplan data ... (date=10/24 15:12:01, mem=1814.8M)  
Saving floorplan file ...  
% End Save floorplan data ... (date=10/24 15:12:01, total cpu=0:00:00.0,  
real=0:00:00.0, peak res=1814.9M, current mem=1814.9M)  
Saving Drc markers ...  
... 23 markers are saved ...  
... 0 geometry drc markers are saved ...  
... 0 antenna drc markers are saved ...  
% Begin Save placement data ... (date=10/24 15:12:01, mem=1814.9M)  
** Saving stdCellPlacement_binary (version# 2) ...  
Save Adaptive View Pruning View Names to Binary file  
% End Save placement data ... (date=10/24 15:12:01, total cpu=0:00:00.0,  
real=0:00:00.0, peak res=1815.2M, current mem=1815.2M)  
% Begin Save routing data ... (date=10/24 15:12:01, mem=1815.2M)
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=2112.64 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC) . (MEM=2112.64 CPU=0:00:00.0
REAL=0:00:00.0)
Turning on fast DC mode.
*** Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0
totSessionCpu=0:00:53.0 mem=2120.6M)

-----
          timeDesign Summary
-----

Hold views included:
best_Case

+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+-----+
|           WNS (ns):| 0.312 | 0.312 | 0.000 |
|           TNS (ns):| 0.000 | 0.000 | 0.000 |
| Violating Paths:| 0 | 0 | 0 |
| All Paths:| 2 | 2 | 0 |
+-----+-----+-----+-----+

Density: 69.569%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.21 sec
Total Real time: 0.0 sec
Total Memory Usage: 2032.914062 Mbytes
*** timeDesign #2 [finish] : cpu/real = 0:00:00.2/0:00:00.2 (1.0),
totSession cpu/real = 0:00:53.1/0:10:23.4 (0.1), mem = 2032.9M
innovus 1>
innovus 1> source ccopt.spec

Usage: create_route_type [-help] [-em_ndr_dist <float>]
                         [-em_ndr_rule <rule_name>] [-min_stack_layer
<layer>]
                         -name <string>
                         [-one_side_spacing_range
<bottomLayerNum:>topLayerNum]
                         [-prefer_multi_cut_via]
                         [-shield_side {one_side both_side}]
                         [-shield_tap_instance_insertion_effort {none
standard high}]
                         [-stack_distance <float>] [[[-non_default_rule
<ndr_name>] [-shield_net <net_name>] [-top_preferred_layer <layer>] [-
bottom_preferred_layer <layer>] [-preferred_routing_layer_effort {low
medium high}]]] [-mask <mask_number> [-layer_mask_range
<bottomLayerNum:>topLayerNum]]]
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:01.0 mem=2039.3M) ***
% End Save routing data ... (date=10/24 15:12:02, total cpu=0:00:00.0,
real=0:00:01.0, peak res=1815.5M, current mem=1815.5M)
Saving property file DBS/cts.encl.dat/AddingCPU.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=2042.3M) ***
% Begin Save power constraints data ... (date=10/24 15:12:02,
mem=1816.5M)
% End Save power constraints data ... (date=10/24 15:12:02, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1816.5M, current mem=1816.5M)
Generated self-contained design cts.encl.dat
#% End save design ... (date=10/24 15:12:02, total cpu=0:00:00.2,
real=0:00:01.0, peak res=1818.9M, current mem=1818.9M)
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 5> #WARNING (NRIF-91) Option setNanoRouteMode -
routeTopRoutingLayer is obsolete. It will continue to work for the
current release. To ensure compatibility with future releases, use option
setDesignMode -topRoutingLayer instead.
#WARNING (NRIF-90) Option setNanoRouteMode -routeBottomRoutingLayer is
obsolete. It will continue to work for the current release. To ensure
compatibility with future releases, use option setDesignMode -
bottomRoutingLayer instead.
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory =
1820.51 (MB), peak = 1855.08 (MB)
AAE_INFO: Pre Route call back at the beginning of routeDesign
#**INFO: setDesignMode -flowEffort standard
#**INFO: setDesignMode -powerEffort none
#WARNING (NRIG-96) Selected single pass global detail route "--"
globalDetail". Clock eco and post optimizations will not be run. See "man
NRIG-96" for more details.
#WARNING (NRIG-144) Cannot combine -viaOpt with -globalDetail option. The
-viaOpt will be ignored.
**INFO: User settings:
setNanoRouteMode -drouteEndIteration          1
setNanoRouteMode -droutePostRouteSpreadWire    1
setNanoRouteMode -extractThirdPartyCompatible  false
setNanoRouteMode -routeBottomRoutingLayer       1
setNanoRouteMode -routeTopRoutingLayer          6
setNanoRouteMode -routeWithSiDriven           false
setNanoRouteMode -routeWithTimingDriven        false
setNanoRouteMode -timingEngine                 {}
setExtractRCMode -engine                      preRoute
setDelayCalMode -enable_high_fanout           true
setDelayCalMode -engine                      aae
setDelayCalMode -ignoreNetLoad                false
setDelayCalMode -socv_accuracy_mode          low
setSIMode -separate_delta_delay_on_data      true

#**INFO: multi-cut via swapping will not be performed after routing.
#**INFO: All auto set options tuned by routeDesign will be restored to
their original settings on command completion.
Begin checking placement ... (start mem=2071.9M, init mem=2071.9M)
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.56000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1831.00 (MB),
peak = 1861.62 (MB)
#
#Finished routing data preparation on Thu Oct 24 15:13:01 2024
#
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 8.73 (MB)
#Total memory = 1831.00 (MB)
#Peak memory = 1861.62 (MB)
#
#
#Start global routing on Thu Oct 24 15:13:01 2024
#
#
#Start global routing initialization on Thu Oct 24 15:13:01 2024
#
#Number of eco nets is 0
#
#Start global routing data preparation on Thu Oct 24 15:13:01 2024
#
#Start routing resource analysis on Thu Oct 24 15:13:01 2024
#
#Routing resource analysis is done on Thu Oct 24 15:13:01 2024
#
# Resource Analysis:
#
#          Routing  #Avail      #Track      #Total      %Gcell
# Layer     Direction Track Blocked   Gcell    Blocked
# -----
#  Metal1       H        12        97        56      53.57%
#  Metal2       V       101         2        56      0.00%
#  Metal3       H       108         1        56      0.00%
#  Metal4       V       102         1        56      0.00%
#  Metal5       H       101         8        56      0.00%
#  Metal6       V        25        43        56      0.00%
# -----
#  Total           450      27.08%      336      8.93%
#
#
#
#
#Global routing data preparation is done on Thu Oct 24 15:13:01 2024
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1831.00 (MB),
peak = 1861.62 (MB)
#
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
*info: Placed = 112
*info: Unplaced = 0
Placement Density:69.57%(2418/3476)
Placement Density (including fixed std cells):69.57%(2418/3476)
Finished checkPlace (total: cpu=0:00:00.0, real=0:00:00.0; vio checks:
cpu=0:00:00.0, real=0:00:00.0; mem=2071.9M)
Turning off fast DC mode.

changeUseClockNetStatus Option : -noFixedNetWires
*** Changed status on (0) nets in Clock.
*** End changeUseClockNetStatus (cpu=0:00:00.0, real=0:00:00.0,
mem=2071.9M) ***

globalDetailRoute

#Start globalDetailRoute on Thu Oct 24 15:13:01 2024
#
#WARNING (NRIG-1303) The congestion map does not match the GCELL grid.
Clearing the map.
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
#num needed restored net=0
#need_extraction net=0 (total=143)
#WARNING (NRDB-2005) SPECIAL_NET VDD has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#WARNING (NRDB-2005) SPECIAL_NET VSS has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Total number of trivial nets (e.g. < 2 pins) = 38 (skipped).
#Total number of routable nets = 105.
#Total number of nets in the design = 143.
#105 routable nets do not have any wires.
#105 nets will be global routed.
#Start routing data preparation on Thu Oct 24 15:13:01 2024
#
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.980.
#Voltage range [0.000 - 1.980] has 141 nets.
#Voltage range [1.620 - 1.980] has 1 net.
#Voltage range [0.000 - 0.000] has 1 net.
#Build and mark too close pins for the same net.
#Rebuild pin access data for design.
#Initial pin access analysis.
#Detail pin access analysis.
# Metall      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.48500
# Metal2     V  Track-Pitch = 0.66000   Line-2-Via Pitch = 0.56000
# Metal3      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.56000
# Metal4      V  Track-Pitch = 0.66000   Line-2-Via Pitch = 0.56000
# Metal5      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.56000
# Metal6      V  Track-Pitch = 0.99000   Line-2-Via Pitch = 0.95000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1828.20 (MB),
peak = 1861.62 (MB)
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#  
#Global routing initialization is done on Thu Oct 24 15:13:01 2024  
#  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1831.00 (MB),  
peak = 1861.62 (MB)  
#  
#start global routing iteration 1...  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1832.68 (MB),  
peak = 1861.62 (MB)  
#  
#start global routing iteration 2...  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1832.68 (MB),  
peak = 1861.62 (MB)  
#  
#  
#Total number of trivial nets (e.g. < 2 pins) = 38 (skipped).  
#Total number of routable nets = 105.  
#Total number of nets in the design = 143.  
#  
#105 routable nets have routed wires.  
#  
#Routed nets constraints summary:  
#-----  
#      Rules   Unconstrained  
#-----  
#      Default       105  
#-----  
#      Total        105  
#-----  
#  
#Routing constraints summary of the whole design:  
#-----  
#      Rules   Unconstrained  
#-----  
#      Default       105  
#-----  
#      Total        105  
#-----  
#  
#  
# Congestion Analysis: (blocked Gcells are excluded)  
#  
#      OverCon  
#          #Gcell    %Gcell  
#      Layer      (1)  OverCon  
#-----  
#      Metal1     0(0.00%) (0.00%)  
#      Metal2     0(0.00%) (0.00%)  
#      Metal3     0(0.00%) (0.00%)  
#      Metal4     0(0.00%) (0.00%)  
#      Metal5     0(0.00%) (0.00%)  
#      Metal6     0(0.00%) (0.00%)  
#-----  
#      Total      0(0.00%) (0.00%)
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#          440
#
#Max overcon = 0 track.
#Total overcon = 0.00%.
#Worst layer Gcell overcon rate = 0.00%.
#
#Global routing statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.89 (MB)
#Total memory = 1832.89 (MB)
#Peak memory = 1861.62 (MB)
#
#Finished global routing on Thu Oct 24 15:13:01 2024
#
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1832.89 (MB),
peak = 1861.62 (MB)
#Start Track Assignment.
#Done with 85 horizontal wires in 1 hboxes and 98 vertical wires in 1
hboxes.
#Done with 14 horizontal wires in 1 hboxes and 28 vertical wires in 1
hboxes.
#Done with 1 horizontal wires in 1 hboxes and 1 vertical wires in 1
hboxes.
#
#Track assignment summary:
# layer      (wire length)      (overlap)      (long ovlp) (with obs/pg/clk)
#-----
# Metal1      0.00    0.00%    0.00%    0.00%
# Metal2     846.83   0.07%    0.00%    0.00%
# Metal3     662.68   0.08%    0.00%    0.00%
# Metal4      0.00    0.00%    0.00%    0.00%
# Metal5      0.00    0.00%    0.00%    0.00%
# Metal6      0.00    0.00%    0.00%    0.00%
#-----
# All       1509.51   0.07%    0.00%    0.00%
#Complete Track Assignment.
#Total wire length = 1479 um.
#Total half perimeter of net bounding box = 1745 um.
#Total wire length on LAYER Metal1 = 0 um.
#Total wire length on LAYER Metal2 = 825 um.
#Total wire length on LAYER Metal3 = 654 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 440
#Up-Via Summary (total 440):
#
#-----
# Metal1      305
# Metal2     134
# Metal3      1
#-----
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#  
# The worst congested Gcell overcon (routing demand over resource in  
number of tracks) = 1  
# Overflow after GR: 0.00% H + 0.00% V  
#  
#Hotspot report including placement blocked areas  
[hotspot] +-----+-----+-----+-----+  
-----+  
[hotspot] | layer | max hotspot | total hotspot |  
hotspot bbox |  
[hotspot] +-----+-----+-----+-----+  
-----+  
[hotspot] | Metal1(H) | 0.00 | 0.00 |  
(none) |  
[hotspot] | Metal2(V) | 0.00 | 0.00 |  
(none) |  
[hotspot] | Metal3(H) | 0.00 | 0.00 |  
(none) |  
[hotspot] | Metal4(V) | 0.00 | 0.00 |  
(none) |  
[hotspot] | Metal5(H) | 0.00 | 0.00 |  
(none) |  
[hotspot] | Metal6(V) | 0.00 | 0.00 |  
(none) |  
[hotspot] +-----+-----+-----+-----+  
-----+  
[hotspot] | worst | 0.00 | 0.00 |  
|  
[hotspot] +-----+-----+-----+-----+  
-----+  
[hotspot] | all layers | 0.00 | 0.00 |  
|  
[hotspot] +-----+-----+-----+-----+  
-----+  
Local HotSpot Analysis (blockage included) (3d): normalized congestion  
max/total hotspot area = 0.00/0.00 (area is in unit of 4 std-cell row  
bins)  
#Complete Global Routing.  
#Total wire length = 1569 um.  
#Total half perimeter of net bounding box = 1745 um.  
#Total wire length on LAYER Metal1 = 0 um.  
#Total wire length on LAYER Metal2 = 858 um.  
#Total wire length on LAYER Metal3 = 711 um.  
#Total wire length on LAYER Metal4 = 0 um.  
#Total wire length on LAYER Metal5 = 0 um.  
#Total wire length on LAYER Metal6 = 0 um.  
#Total number of vias = 440  
#Up-Via Summary (total 440):  
#  
#-----  
# Metal1 305  
# Metal2 134  
# Metal3 1  
#-----
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#          440
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1833.02 (MB),
peak = 1861.62 (MB)
#
#Routing data preparation, pin analysis, global routing and track
assignment statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 10.75 (MB)
#Total memory = 1833.02 (MB)
#Peak memory = 1861.62 (MB)
#
#Start Detail Routing..
#start initial detail routing ...
#   number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1833.44 (MB),
peak = 1861.62 (MB)
#Complete Detail Routing.
#Total wire length = 1806 um.
#Total half perimeter of net bounding box = 1745 um.
#Total wire length on LAYER Metal1 = 108 um.
#Total wire length on LAYER Metal2 = 1020 um.
#Total wire length on LAYER Metal3 = 619 um.
#Total wire length on LAYER Metal4 = 60 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 473
#Up-Via Summary (total 473):
#
#-----
# Metal1      318
# Metal2      146
# Metal3       9
#-----
#           473
#
#Total number of DRC violations = 0
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 0.42 (MB)
#Total memory = 1833.44 (MB)
#Peak memory = 1861.62 (MB)
#
#Start Post Route wire spreading..
#
#Start DRC checking..
#   number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1834.32 (MB),
peak = 1861.62 (MB)
#CELL_VIEW AddingCPU,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#Total number of vias = 473
#Up-Via Summary (total 473):
#
#-----
# Metall1      318
# Metall2      146
# Metall3       9
#-----
#                      473
#
#detailRoute Statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.11 (MB)
#Total memory = 1834.13 (MB)
#Peak memory = 1861.62 (MB)
#      no debugging net set
#
#globalDetailRoute statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 21.24 (MB)
#Total memory = 1842.48 (MB)
#Peak memory = 1861.62 (MB)
#Number of warnings = 3
#Total number of warnings = 7
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Thu Oct 24 15:13:01 2024
#
#Default setup view is reset to worst_case.

detailRoute

#Start detailRoute on Thu Oct 24 15:13:01 2024
#
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
#num needed restored net=0
#need_extraction net=0 (total=143)
#WARNING (NRDB-2005) SPECIAL_NET VDD has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#WARNING (NRDB-2005) SPECIAL_NET VSS has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Start routing data preparation on Thu Oct 24 15:13:01 2024
#
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.980.
#Voltage range [0.000 - 1.980] has 141 nets.
#Voltage range [1.620 - 1.980] has 1 net.
#Voltage range [0.000 - 0.000] has 1 net.
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#  
#Start data preparation for wire spreading...  
#  
#Data preparation is done on Thu Oct 24 15:13:01 2024  
#  
#  
#Start Post Route Wire Spread.  
#Done with 8 horizontal wires in 1 hboxes and 5 vertical wires in 1  
hboxes.  
#Complete Post Route Wire Spread.  
#  
#Total wire length = 1824 um.  
#Total half perimeter of net bounding box = 1745 um.  
#Total wire length on LAYER Metal1 = 110 um.  
#Total wire length on LAYER Metal2 = 1025 um.  
#Total wire length on LAYER Metal3 = 628 um.  
#Total wire length on LAYER Metal4 = 61 um.  
#Total wire length on LAYER Metal5 = 0 um.  
#Total wire length on LAYER Metal6 = 0 um.  
#Total number of vias = 473  
#Up-Via Summary (total 473):  
#  
#-----  
# Metal1      318  
# Metal2      146  
# Metal3       9  
#-----  
#           473  
#  
#  
#Start DRC checking..  
#   number of violations = 0  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1834.13 (MB),  
peak = 1861.62 (MB)  
#CELL_VIEW AddingCPU,init has no DRC violation.  
#Total number of DRC violations = 0  
#Total number of process antenna violations = 0  
#Total number of net violated process antenna rule = 0  
#   number of violations = 0  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1834.13 (MB),  
peak = 1861.62 (MB)  
#CELL_VIEW AddingCPU,init has no DRC violation.  
#Total number of DRC violations = 0  
#Total number of process antenna violations = 0  
#Total number of net violated process antenna rule = 0  
#Post Route wire spread is done.  
#Total wire length = 1824 um.  
#Total half perimeter of net bounding box = 1745 um.  
#Total wire length on LAYER Metal1 = 110 um.  
#Total wire length on LAYER Metal2 = 1025 um.  
#Total wire length on LAYER Metal3 = 628 um.  
#Total wire length on LAYER Metal4 = 61 um.  
#Total wire length on LAYER Metal5 = 0 um.  
#Total wire length on LAYER Metal6 = 0 um.
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#Build and mark too close pins for the same net.
#Initial pin access analysis.
#Detail pin access analysis.
# Metal1      H   Track-Pitch = 0.56000      Line-2-Via Pitch = 0.48500
# Metal2      V   Track-Pitch = 0.66000      Line-2-Via Pitch = 0.56000
# Metal3      H   Track-Pitch = 0.56000      Line-2-Via Pitch = 0.56000
# Metal4      V   Track-Pitch = 0.66000      Line-2-Via Pitch = 0.56000
# Metal5      H   Track-Pitch = 0.56000      Line-2-Via Pitch = 0.56000
# Metal6      V   Track-Pitch = 0.99000      Line-2-Via Pitch = 0.95000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1839.55 (MB),
peak = 1861.62 (MB)
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.56000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1842.12 (MB),
peak = 1861.62 (MB)
#
#Start Post Route wire spreading..
#
#Start data preparation for wire spreading...
#
#Data preparation is done on Thu Oct 24 15:13:01 2024
#
#
#Start Post Route Wire Spread.
#Done with 1 horizontal wires in 1 hboxes and 1 vertical wires in 1
hboxes.
#Complete Post Route Wire Spread.
#
#Total wire length = 1825 um.
#Total half perimeter of net bounding box = 1745 um.
#Total wire length on LAYER Metal1 = 110 um.
#Total wire length on LAYER Metal2 = 1026 um.
#Total wire length on LAYER Metal3 = 628 um.
#Total wire length on LAYER Metal4 = 61 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 473
#Up-Via Summary (total 473):
#
-----#
# Metal1      318
# Metal2      146
# Metal3       9
#-----#
#          473
#
#    number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1842.22 (MB),
peak = 1861.62 (MB)
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
*INFO: Added 30 filler insts (cell FILL1 / prefix FILLER).
*INFO: Total 90 filler insts added - prefix FILLER (CPU: 0:00:00.0).
For 90 new insts, innovus 5> **WARN: (IMPSP-5217): addFiller command is
running on a postRoute database. It is recommended to be followed by
ecoRoute -target command to make the DRC clean.
Type 'man IMPSP-5217' for more detail.
*INFO: Adding fillers to top-module.
*INFO: Added 0 filler inst of any cell-type.
innovus 5> Performing RC Extraction ...
Extraction called for design 'AddingCPU' of instances=202 and nets=143
using extraction engine 'preRoute' .
**WARN: (IMPEXT-3530): The process node is not set. Use the command
setDesignMode -process <process node> prior to extraction for maximum
accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design AddingCPU.
RC Extraction called in multi-corner(1) mode.
**WARN: (IMPEXT-6197): The Cap table file is not specified. This will
result in lower parasitic accuracy when using preRoute extraction or
postRoute extraction with effort level 'low'. It is recommended to
generate the Cap table file using the 'generateCapTbl' command and
specify it before extraction using 'create_rc_corner/update_rc_corner -
cap_table'.
Type 'man IMPEXT-6197' for more detail.
RCMode: PreRoute
    RC Corner Indexes          0
    Capacitance Scaling Factor : 1.00000
    Resistance Scaling Factor : 1.00000
    Clock Cap. Scaling Factor : 1.00000
    Clock Res. Scaling Factor : 1.00000
    Shrink Factor             : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Updating RC grid for preRoute extraction ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0
MEM: 2103.852M)
innovus 5> Writing Netlist "AddingCPU_innovus.v" ...
innovus 5> #% Begin save design ... (date=10/24 15:15:37, mem=1842.8M)
% Begin Save ccopt configuration ... (date=10/24 15:15:37, mem=1842.8M)
% End Save ccopt configuration ... (date=10/24 15:15:37, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1843.1M, current mem=1843.1M)
% Begin Save netlist data ... (date=10/24 15:15:37, mem=1843.1M)
Writing Binary DB to AddingCPU.enc.dat/AddingCPU.v.bin in single-threaded
mode...
% End Save netlist data ... (date=10/24 15:15:37, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1843.2M, current mem=1843.2M)
Saving symbol-table file ...
Saving congestion map file AddingCPU.enc.dat/AddingCPU.route.congmap.gz
...
% Begin Save AAE data ... (date=10/24 15:15:37, mem=1843.2M)
Saving AAE Data ...
AAE DB initialization (MEM=2103.49 CPU=0:00:00.0 REAL=0:00:00.0)
% End Save AAE data ... (date=10/24 15:15:37, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1843.8M, current mem=1843.8M)
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
#CELL_VIEW AddingCPU,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#Post Route wire spread is done.
#Total wire length = 1825 um.
#Total half perimeter of net bounding box = 1745 um.
#Total wire length on LAYER Metal1 = 110 um.
#Total wire length on LAYER Metal2 = 1026 um.
#Total wire length on LAYER Metal3 = 628 um.
#Total wire length on LAYER Metal4 = 61 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 473
#Up-Via Summary (total 473):
#
#-----
# Metal1      318
# Metal2      146
# Metal3       9
#-----
#          473
#
#      no debugging net set
#
#detailRoute statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.17 (MB)
#Total memory = 1839.06 (MB)
#Peak memory = 1861.62 (MB)
#Number of warnings = 2
#Total number of warnings = 9
#Number of fails = 0
#Total number of fails = 0
#Complete detailRoute on Thu Oct 24 15:13:01 2024
#
#Default setup view is reset to worst_case.
AAE_INFO: Post Route call back at the end of routeDesign
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:01, memory =
1839.07 (MB), peak = 1861.62 (MB)
*** Message Summary: 0 warning(s), 0 error(s)

innovus 5> **WARN: (IMPSP-5217): addFiller command is running on a
postRoute database. It is recommended to be followed by ecoRoute -target
command to make the DRC clean.
Type 'man IMPSP-5217' for more detail.
*INFO: Adding fillers to top-module.
*INFO: Added 0 filler inst (cell FILL64 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILL32 / prefix FILLER).
*INFO: Added 3 filler insts (cell FILL16 / prefix FILLER).
*INFO: Added 15 filler insts (cell FILL8 / prefix FILLER).
*INFO: Added 18 filler insts (cell FILL4 / prefix FILLER).
*INFO: Added 24 filler insts (cell FILL2 / prefix FILLER).
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

```
Saving preference file AddingCPU.enc.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=10/24 15:15:37, mem=1844.4M)
Saving floorplan file ...
% End Save floorplan data ... (date=10/24 15:15:37, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1844.4M, current mem=1844.4M)
Saving Drc markers ...
... 23 markers are saved ...
... 0 geometry drc markers are saved ...
... 0 antenna drc markers are saved ...
% Begin Save placement data ... (date=10/24 15:15:37, mem=1844.4M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=10/24 15:15:37, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1844.4M, current mem=1844.4M)
% Begin Save routing data ... (date=10/24 15:15:37, mem=1844.4M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=2104.0M) ***
% End Save routing data ... (date=10/24 15:15:37, total cpu=0:00:00.0,
real=0:00:01.0, peak res=1844.6M, current mem=1844.6M)
Saving property file AddingCPU.enc.dat/AddingCPU.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=2107.0M) ***
#Saving pin access data to file AddingCPU.enc.dat/AddingCPU.apa ...
#
% Begin Save power constraints data ... (date=10/24 15:15:38,
mem=1844.6M)
% End Save power constraints data ... (date=10/24 15:15:38, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1844.6M, current mem=1844.6M)
Generated self-contained design AddingCPU.enc.dat
#% End save design ... (date=10/24 15:15:38, total cpu=0:00:00.2,
real=0:00:01.0, peak res=1875.0M, current mem=1845.3M)
*** Message Summary: 0 warning(s), 0 error(s)

Parse flat map file...
Writing GDSII file ...
***** db unit per micron = 2000 *****
***** output gds2 file unit per micron = 2000 *****
***** unit scaling factor = 1 *****
Output for instance
Output for bump
Output for physical terminals
Output for logical terminals
Output for regular nets
Output for special nets and metal fills
Output for via structure generation total number 7
Statistics for GDS generated (version 3)
-----
Stream Out Layer Mapping Information:
GDS Layer Number      GDS Layer Name
-----
121                  COMP
122                  DIEAREA
58                   Via34
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

49	Metal3
18	Via12
47	Metal3
24	Metal2
100	Via56
48	Metal3
106	Metal6
25	Metal2
3	Metal1
79	Via45
26	Metal2
102	Via56
4	Metal1
27	Metal2
85	Metal5
104	Via56
60	Via34
61	Via34
68	Metal4
69	Metal4
70	Metal4
71	Metal4
72	Metal4
73	Metal4
80	Via45
82	Via45
90	Metal5
91	Metal5
92	Metal5
93	Metal5
94	Metal5
101	Via56
103	Via56
111	Metal6
112	Metal6
113	Metal6
114	Metal6
115	Metal6
110	Metal6
89	Metal5
117	Metal6
56	Metal3
55	Metal3
54	Metal3
53	Metal3
32	Metal2
98	Metal5
96	Metal5
76	Metal4
33	Metal2
75	Metal4
97	Metal5
74	Metal4
119	Metal6

Lab-5: Logic synthesis & Physical Design of an adding CPU

57	Via34
50	Metal3
107	Metal6
46	Metal3
45	Metal3
44	Metal3
63	Via34
43	Metal3
62	Via34
41	Via23
22	Metal2
40	Via23
37	Via23
59	Via34
36	Via23
31	Metal2
88	Metal5
29	Metal2
86	Metal5
105	Via56
9	Metal1
66	Metal4
42	Via23
23	Metal2
99	Via56
19	Via12
8	Metal1
65	Metal4
84	Via45
30	Metal2
87	Metal5
7	Metal1
6	Metal1
64	Metal4
83	Via45
39	Via23
16	Via12
52	Metal3
109	Metal6
2	Metal1
21	Via12
78	Via45
10	Metal1
67	Metal4
51	Metal3
108	Metal6
28	Metal2
1	Metal1
20	Via12
38	Via23
15	Via12
5	Metal1
81	Via45
17	Via12

Lab-5: Logic synthesis & Physical Design of an adding CPU

12	Metal1
77	Metal4
118	Metal6
11	Metal1
34	Metal2
116	Metal6
35	Metal2
13	Metal1
14	Metal1
95	Metal5

Stream Out Information Processed for GDS version 3:
Units: 2000 DBU

Object	Count
<hr/>	
Instances	202
Ports/Pins	18
metal layer Metal2	11
metal layer Metal3	6
metal layer Metal4	1
Nets	603
metal layer Metal1	64
metal layer Metal2	373
metal layer Metal3	156
metal layer Metal4	10
Via Instances	473
Special Nets	93
metal layer Metal1	35
metal layer Metal2	1
metal layer Metal5	4
metal layer Metal6	53
Via Instances	1
Metal Fills	0
Via Instances	0
Metal FillOPCs	0
Via Instances	0
Metal FillDRCs	0
Via Instances	0
Text	125
metal layer Metal1	12

Lab-5: Logic synthesis & Physical Design of an adding CPU

metal layer Metal2	92
metal layer Metal3	17
metal layer Metal4	2
metal layer Metal6	2
Blockages	0
Custom Text	0
Custom Box	0
Trim Metal	0
#####Streamout is finished!	
innovus 5>	

Inference: A total of 138 leaf instance count is present in the gate level netlist with total area of 1,118.682, total power of 6606.92nW.

Result: Hence an addingCPU is synthesized and the gate level netlist with timing, area and power report has been generated.

Lab-5: Logic synthesis & Physical Design of an Full Adder

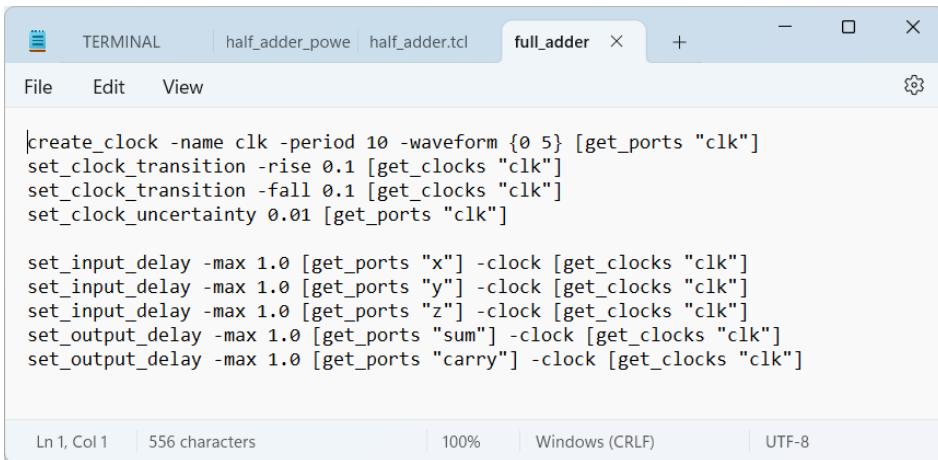
Aim: To synthesize an full adder and to get the gate level netlist with timing, area, and power reports.

EDA Tools Used: Cadence Genus (Logic synthesis tool) and Innovus

Description: A full adder is a fundamental digital circuit used in computing and digital electronics to perform the addition of three binary bits. It consists of three inputs: two significant bits, A and B, and a carry-in bit, Cin, which represents the carry from a previous addition operation. The full adder generates two outputs: the sum bit (S) and the carry-out bit (Cout). The sum output represents the least significant bit of the result, while the carry-out bit indicates whether a carry is generated to the next higher bit position, essential for multi-bit binary addition. The full adder's ability to handle carry input makes it suitable for constructing arithmetic units in CPUs and other digital systems, enabling complex calculations by linking multiple full adders in series to add binary numbers of arbitrary length.

Procedure:

1. Copy the fast.lib and slow.lib files into the folder where (.v) files are located.
2. Create a Synopsys design constraint file (.SDC file) by entering the design constraints required for the synthesis.



The screenshot shows a terminal window with the following content:

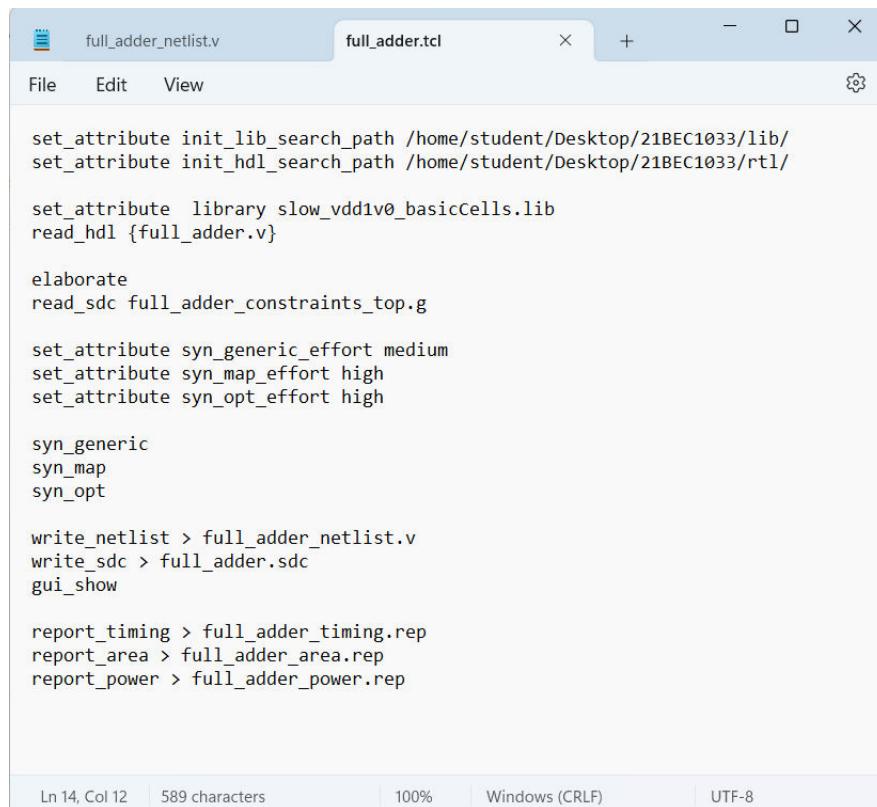
```
TERMINAL | half_adder_powr | half_adder.tcl | full_adder × + - □ ×
File Edit View
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "x"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "y"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "z"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "sum"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "carry"] -clock [get_clocks "clk"]
```

Ln 1, Col 1 | 556 characters | 100% | Windows (CRLF) | UTF-8

Lab-5: Logic synthesis & Physical Design of Full Adder

3. Create a (.tcl) file containing all the commands for performing the logic synthesis.
Synthesis effort can be medium or high.



The screenshot shows a text editor window titled "full_adder.tcl". The code in the editor is a Tcl script used for logic synthesis. It includes commands to set library search paths, read HDL files, elaborate designs, and generate reports for timing, area, and power. The script ends with a command to write the netlist to a file named "full_adder_netlist.v".

```
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {full_adder.v}

elaborate
read_sdc full_adder_constraints_top.g

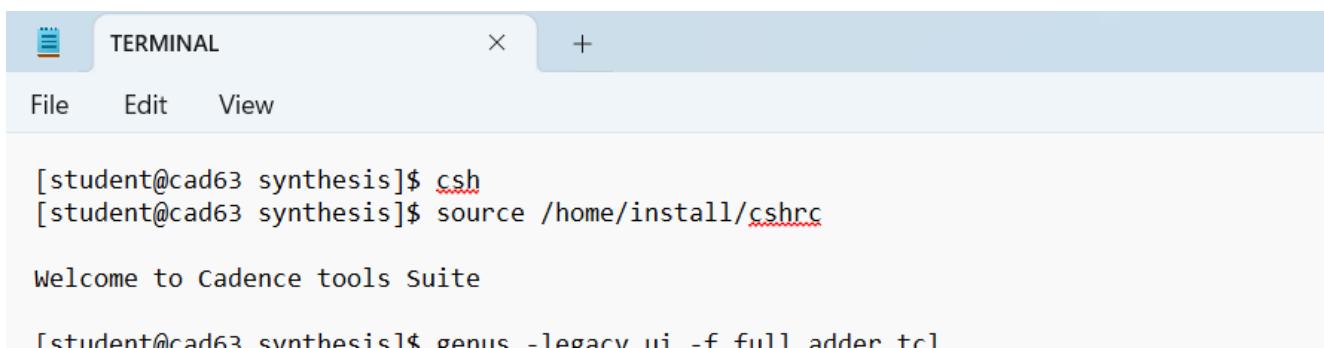
set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > full_adder_netlist.v
write_sdc > full_adder.sdc
gui_show

report_timing > full_adder_timing.rep
report_area > full_adder_area.rep
report_power > full_adder_power.rep
```

4. Invoke the C shell and launch the Genus tool by entering the below commands.



The screenshot shows a terminal window titled "TERMINAL". The user has entered the following commands in the terminal:

```
[student@cad63 synthesis]$ csh
[student@cad63 synthesis]$ source /home/install/cshrc
```

After running these commands, the terminal displays a welcome message from the Cadence tools suite:

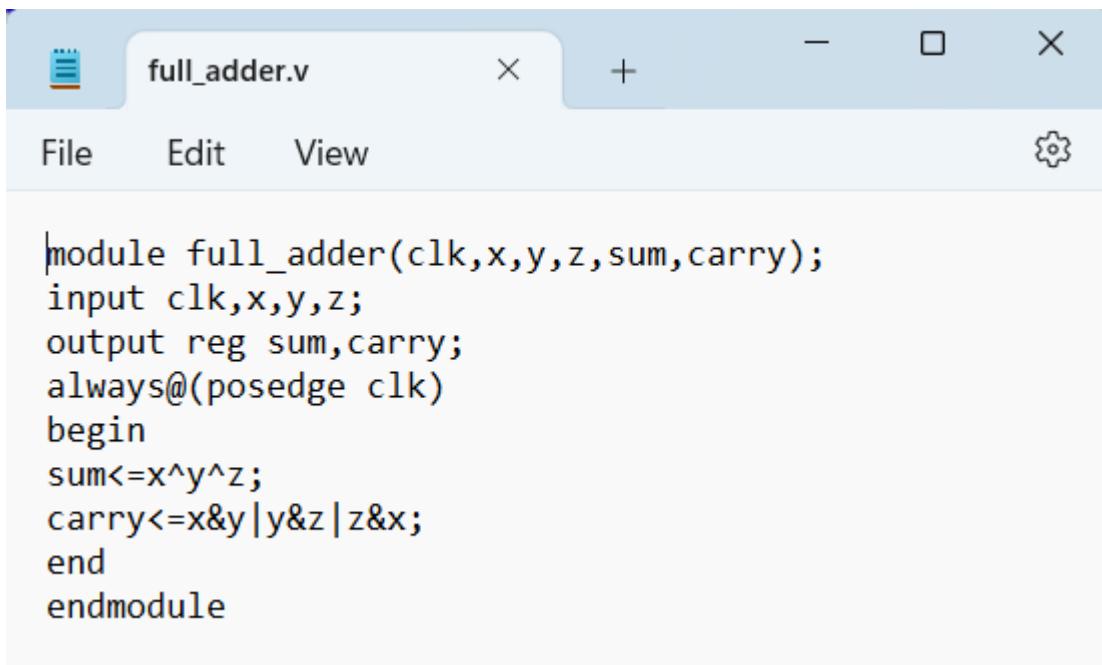
```
Welcome to Cadence tools Suite
```

Finally, the user runs the "genus -legacy ui -f full_adder.tcl" command to launch the tool.

5. Execute the commands in the (.tcl file) by entering **source full_adder.tcl** command in the command line window.
6. Check for the area, timing and power reports generated in the respective adding CPU folder. Also check the gate level netlist generated in the Genus synthesis solution window.

Verilog Programs:

//Verilog Program of full adder

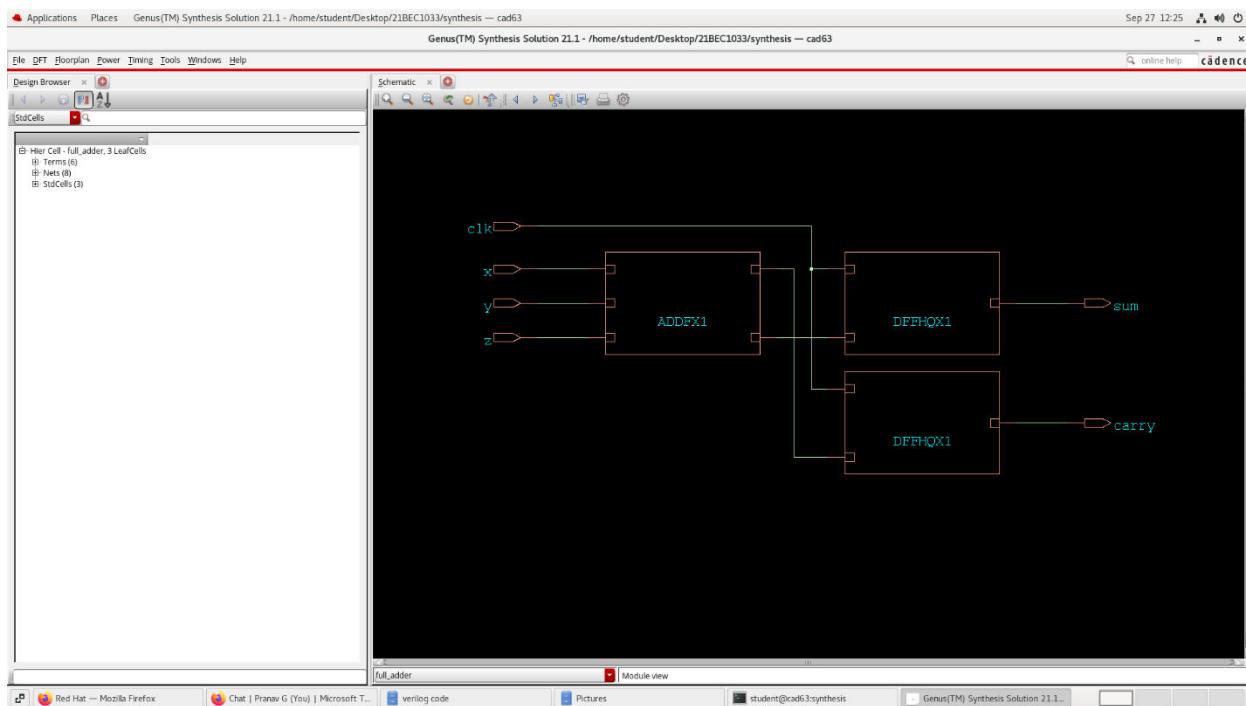


The screenshot shows a Verilog code editor window titled "full_adder.v". The window has a standard OS X style title bar with icons for minimize, maximize, and close. Below the title bar is a menu bar with "File", "Edit", "View", and a gear icon for settings. The main area contains the Verilog code for a full adder module:

```
module full_adder(clk,x,y,z,sum,carry);
  input clk,x,y,z;
  output reg sum,carry;
  always@(posedge clk)
  begin
    sum<=x^y^z;
    carry<=x&y | y&z | z&x;
  end
endmodule
```

Lab-5: Logic synthesis & Physical Design of Full Adder

Gate level Netlist:

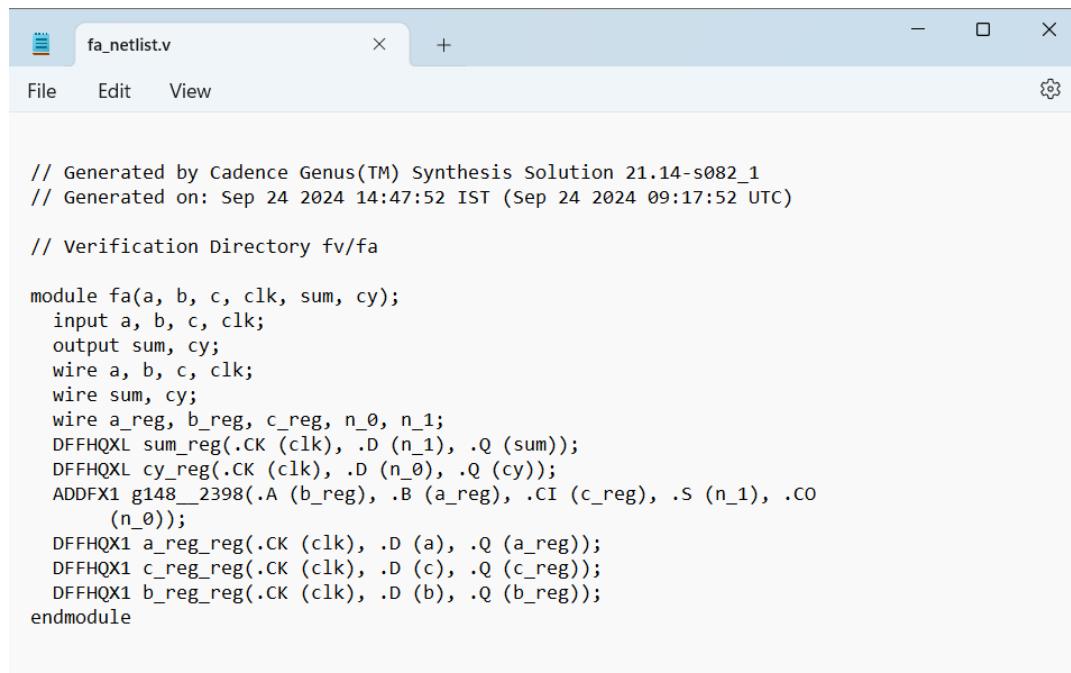


Lab-5: Logic synthesis & Physical Design of Full Adder

Observations:

Synthesis effort: Medium

a) Full Adder_netlist_created file

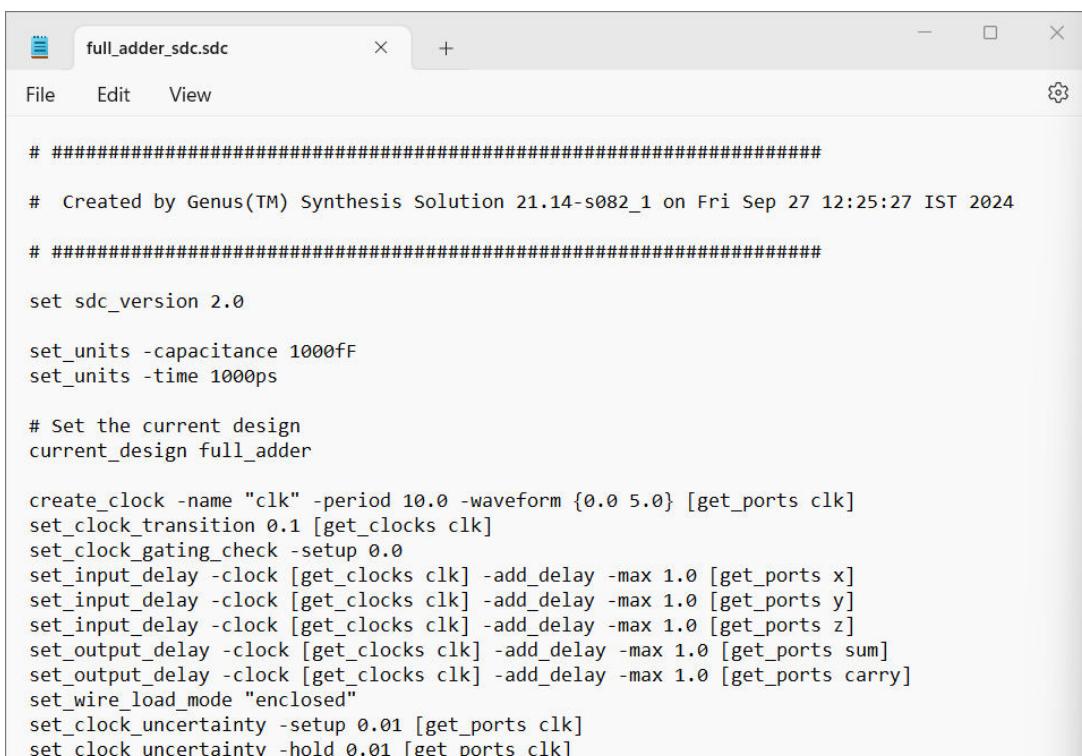


```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Sep 24 2024 14:47:52 IST (Sep 24 2024 09:17:52 UTC)

// Verification Directory fv/fa

module fa(a, b, c, clk, sum, cy);
    input a, b, c, clk;
    output sum, cy;
    wire a, b, c, clk;
    wire sum, cy;
    wire a_reg, b_reg, c_reg, n_0, n_1;
    DFFHQXL sum_reg(.CK (clk), .D (n_1), .Q (sum));
    DFFHQXL cy_reg(.CK (clk), .D (n_0), .Q (cy));
    ADDFX1 g148_2398(.A (b_reg), .B (a_reg), .CI (c_reg), .S (n_1), .CO
        (n_0));
    DFFHQX1 a_reg_reg(.CK (clk), .D (a), .Q (a_reg));
    DFFHQX1 c_reg_reg(.CK (clk), .D (c), .Q (c_reg));
    DFFHQX1 b_reg_reg(.CK (clk), .D (b), .Q (b_reg));
endmodule
```

b) Full Adder_Constraint_created file



```
# #####
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Fri Sep 27 12:25:27 IST 2024
# #####
set sdc_version 2.0

set_units -capacitance 1000ff
set_units -time 1000ps

# Set the current design
current_design full_adder

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports x]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports y]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports z]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports sum]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports carry]
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.01 [get_ports clk]
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

Lab-5: Logic synthesis & Physical Design of Full Adder

c) Full Adder_timing_created file

```
full_adder_timing.rep x +  
File Edit View  
=====  
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1  
Generated on: Sep 27 2024 12:25:27 pm  
Module: full_adder  
Technology library: slow_vdd1v0 1.0  
Operating conditions: PVT_0P9V_125C (balanced_tree)  
Wireload mode: enclosed  
Area mode: timing library  
=====  
Pin Type Fanout Load Slew Delay Arrival  
(fF) (ps) (ps) (ps)  
-----  
(clock clk) launch 0 R  
(full_adder.g_line_7) ext delay +1000 1000 F  
y in port 1 0.7 0 +0 1000 F  
g155_2398/B +0 1000  
g155_2398/S ADDFX1 1 0.3 35 +272 1272 R  
sum_reg/D <<< DFFHQX1 +0 1272  
sum_reg/CK setup 100 +94 1366 R  
-----  
(clock clk) capture 10000 R  
uncertainty -10 9990 R  
-----  
Cost Group : 'clk' (path_group 'clk')  
Timing slack : 8624ps  
Start-point : y  
End-point : sum_reg/D
```

d) FullAdder_area_created file

```
full_adder_area.rep x +  
File Edit View  
=====  
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1  
Generated on: Sep 27 2024 12:25:27 pm  
Module: full_adder  
Technology library: slow_vdd1v0 1.0  
Operating conditions: PVT_0P9V_125C (balanced_tree)  
Wireload mode: enclosed  
Area mode: timing library  
=====  
Instance Module Cell Count Cell Area Net Area Total Area Wireload  
-----  
full_adder 3 16.074 0.000 16.074 <none> (D)  
(D) = wireload is default in technology library  
  
Ln 1, Col 1 | 734 characters | 100% | Unix (LF) | UTF-8
```

Lab-5: Logic synthesis & Physical Design of Full Adder

e) FullAdder _power_created file

full_adders_power.rep

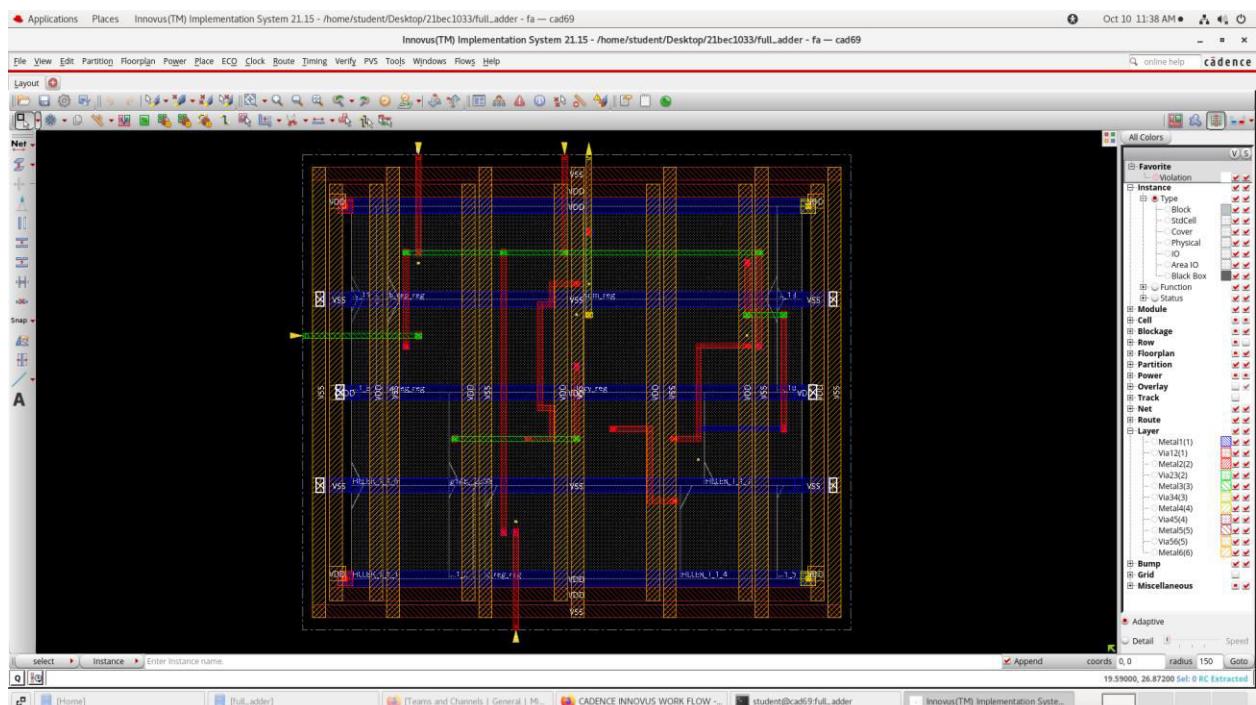
File Edit View

Instance: /full_adder
Power Unit: W
PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	2.40680e-10	4.61914e-07	0.00000e+00	4.62154e-07	81.85%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	1.01043e-10	4.60597e-08	2.38950e-08	7.00557e-08	12.41%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	3.24000e-08	3.24000e-08	5.74%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	3.41723e-10	5.07973e-07	5.62950e-08	5.64610e-07	100.00%
Percentage	0.06%	89.97%	9.97%	100.00%	100.00%

Ln 1, Col 1 | 1,204 characters | 100% | Unix (LF) | UTF-8

f) Physical design of the FullAdder:



Lab-5: Logic synthesis & Physical Design of Full Adder

g) Innovus Terminal:

```
[student@cad69 full_adder]$ csh
[student@cad69 full_adder]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad69 full_adder]$ innovus

Cadence Innovus(TM) Implementation System.
Copyright 2021 Cadence Design Systems, Inc. All rights reserved
worldwide.

Version: v21.15-s110_1, built Fri Sep 23 13:08:12 PDT 2022
Options:
Date: Thu Oct 10 11:17:18 2024
Host: cad69 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64)
(12cores*20cpus*12th Gen Intel(R) Core(TM) i7-12700 25600KB)
OS: Red Hat Enterprise Linux release 8.10 (Ootpa)

License:
[11:17:18.095641] Configured Lic search path (21.01-s002):
5280@cadence

      invs Innovus Implementation System      21.1 checkout
succeeded
      8 CPU jobs allowed with the current license(s). Use
setMultiCpuUsage to set your required CPU count.
Create and set the environment variable TMPDIR to
/tmp/innovus_temp_53898_cad69_student_1NVSy9.

Change the soft stacksize limit to 0.2%RAM (63 mbytes). Set global
soft_stack_size_limit to change the value.

**INFO: MMMC transition support version v31-84

[INFO] Loading PVS 22.20 fill procedures
innovus 1> #% Begin Load MMMC data ... (date=10/10 11:21:18, mem=1027.4M)
#% End Load MMMC data ... (date=10/10 11:21:18, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1028.1M, current mem=1028.1M)

Loading LEF file
../../../../install/FOUNDRY/digital/180nm/dig/lef/all.lef ...
Set DBUPerIGU to M2 pitch 1320.
**WARN: (IMPLF-200): Pin 'A' in macro 'ANTENNA' has no ANTENNAGATEAREA
value defined. The library data is incomplete and some process antenna
rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-201): Pin 'Q[0]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[10]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
**WARN: (IMPLF-201): Pin 'Q[11]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[12]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[13]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[14]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[15]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[1]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[2]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[3]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[4]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[5]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[6]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[7]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[8]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
**WARN: (IMPLF-201): Pin 'Q[9]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[0]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[10]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[11]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[12]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (EMS-27):Message (IMPLF-201) has exceeded the current message
display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
**WARN: (IMPLF-200): Pin 'PAD' in macro 'PDB04DGZ' has no
ANTENNAGATEAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-200): Pin 'OEN' in macro 'PDB04DGZ' has no
ANTENNAGATEAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-200): Pin 'I' in macro 'PDB04DGZ' has no ANTENNAGATEAREA
value defined. The library data is incomplete and some process antenna
rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.

## Check design process and node:
## Both design process and tech node are not set.

Loading view definition file from Default.view
Reading max_timing timing library
'/home/student/Desktop/21bec1033/full_adder/slow.lib' ...
Read 477 cells in library 'slow'
Reading min_timing timing library
'/home/student/Desktop/21bec1033/full_adder/fast.lib' ...
Read 477 cells in library 'fast'
*** End library_loading (cpu=0.01min, real=0.00min, mem=30.0M,
fe_cpu=0.49min, fe_real=4.00min, fe_mem=1116.7M) ***
#% Begin Load netlist data ... (date=10/10 11:21:18, mem=1050.2M)
*** Begin netlist parsing (mem=1116.7M) ***
**WARN: (IMPVL-159): Pin 'VSS' of cell 'OAI211XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
**WARN: (IMPVL-159): Pin 'VDD' of cell 'OAI211XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'SEDFFHQX1' is defined in LEF
but not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'SEDFFHQX1' is defined in LEF
but not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'EDFFTRX2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'EDFFTRX2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'NOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'NOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'DFFHQX4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'DFFHQX4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'OAI222XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'OAI222XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'NOR4X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'NOR4X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'NOR4BXL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'NOR4BXL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'NAND4BBX1' is defined in LEF
but not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'NAND4BBX1' is defined in LEF
but not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'MXI2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
**WARN: (IMPVL-159): Pin 'VDD' of cell 'MXI2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (EMS-27):Message (IMPVL-159) has exceeded the current message
display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
Created 477 new cells from 2 timing libraries.
Reading netlist ...
Backslashed names will retain backslash and a trailing blank character.
Reading verilog netlist 'fa_netlist.v'

*** Memory Usage v#1 (Current mem = 1116.691M, initial mem = 483.867M)
***
*** End netlist parsing (cpu=0:00:00.0, real=0:00:00.0, mem=1116.7M) ***
#% End Load netlist data ... (date=10/10 11:21:18, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1063.9M, current mem=1063.9M)
Top level cell is fa.
Hooked 954 DB cells to tlib cells.
** Removed 129 unused lib cells.
Starting recursive module instantiation check.
No recursion found.
Building hierarchical netlist for Cell fa ...
*** Netlist is unique.
** info: there are 837 modules.
** info: there are 6 stdCell insts.

*** Memory Usage v#1 (Current mem = 1175.105M, initial mem = 483.867M)
***
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
unless standard cell models of this type exist in the LEF/OA library.
Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 560 (derived)
Vertical Layer M2 offset = 660 (derived)
Start create_tracks
Generated pitch 0.99 in Metal6 is different from 1.32 defined in
technology file in preferred direction.
Generated pitch 0.56 in Metal5 is different from 1.12 defined in
technology file in preferred direction.
Extraction setup Started
Initializing multi-corner RC extraction with 1 active RC Corners ...
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
Reading Capacitance Table File
../../../../install/FOUNDRY/digital/180nm/dig/captable/t018s6mlv.capTbl
...
Cap table was created using Encounter 10.10-s002_1.
Process name: t018s6mm.
Importing multi-corner RC tables ...
Summary of Active RC-Corners :

Analysis View: worst_case
RC-Corner Name      : rc
RC-Corner Index     : 0
RC-Corner Temperature : 25 Celsius
RC-Corner Cap Table  :
'../../../../install/FOUNDRY/digital/180nm/dig/captable/t018s6mlv.capTbl'
RC-Corner PreRoute Res Factor      : 1
RC-Corner PreRoute Cap Factor     : 1
RC-Corner PostRoute Res Factor    : 1 {1 1 1}
RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
RC-Corner PreRoute Clock Res Factor : 1 [Derived from postRoute_res
(effortLevel low)]
RC-Corner PreRoute Clock Cap Factor : 1 [Derived from postRoute_cap
(effortLevel low)]
RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}      [Derived from
postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}      [Derived from
postRoute_res (effortLevel low)]
RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}

Analysis View: best_case
RC-Corner Name      : rc
RC-Corner Index     : 0
RC-Corner Temperature : 25 Celsius
RC-Corner Cap Table  :
'../../../../install/FOUNDRY/digital/180nm/dig/captable/t018s6mlv.capTbl'
RC-Corner PreRoute Res Factor      : 1
RC-Corner PreRoute Cap Factor     : 1
RC-Corner PostRoute Res Factor    : 1 {1 1 1}
RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
RC-Corner PreRoute Clock Res Factor : 1 [Derived from postRoute_res
(effortLevel low)]
RC-Corner PreRoute Clock Cap Factor : 1 [Derived from postRoute_cap
(effortLevel low)]
RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}      [Derived from
postRoute_cap (effortLevel low)]
RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}      [Derived from
postRoute_res (effortLevel low)]
RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
*Info: initialize multi-corner CTS.
Reading timing constraints file 'fa.sdc' ...
```

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```
Current (total cpu=0:00:30.0, real=0:04:00, peak res=1356.1M, current
mem=1356.1M)
**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
fa.sdc, Line 9).

**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
fa.sdc, Line 10).

fa
INFO (CTE): Reading of timing constraints file fa.sdc completed, with 2
WARNING
Ending "Constraint file reading stats" (total cpu=0:00:00.0,
real=0:00:00.0, peak res=1364.1M, current mem=1364.0M)
Current (total cpu=0:00:30.0, real=0:04:01, peak res=1364.1M, current
mem=1364.0M)
Total number of combinational cells: 234
Total number of sequential cells: 105
Total number of tristate cells: 9
Total number of level shifter cells: 0
Total number of power gating cells: 0
Total number of isolation cells: 0
Total number of power switch cells: 0
Total number of pulse generator cells: 0
Total number of always on buffers: 0
Total number of retention cells: 0
List of usable buffers: BUFX2 BUFX12 BUFX16 BUFX20 CLKBUFX2 BUFX3 BUFX4
CLKBUFX12 CLKBUFX16 CLKBUFX20 CLKBUFX4 CLKBUFX8 BUFX8 CLKBUFX3
Total number of usable buffers: 14
List of unusable buffers:
Total number of unusable buffers: 0
List of usable inverters: CLKINVX2 CLKINVX1 CLKINVX12 CLKINVX16 CLKINVX20
INVX1 CLKINVX3 CLKINVX4 INVX12 INVX2 INVX3 CLKINVX8 INVX20 INVX4 INVX16
INVXL INVX8
Total number of usable inverters: 17
List of unusable inverters:
Total number of unusable inverters: 0
List of identified usable delay cells: DLY1X1 DLY4X1 DLY2X1 DLY3X1
Total number of identified usable delay cells: 4
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0
**WARN: (IMPSYC-2): Timing information is not defined for cell
DFFHQXL; Check the timing library (.lib) file and make sure the timing
information exists for the cell and you can run the checkTimingLibrary
command to verify if the timing library has complete information after
the design is loaded.
Type 'man IMPSYC-2' for more detail.

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count  Summary
WARNING IMPLF-200      4  Pin '%s' in macro '%s' has no
ANTENNAGAT...
WARNING IMPLF-201      50  Pin '%s' in macro '%s' has no
ANTENNADIF...
```

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```
WARNING IMPFP-3961           2 The techSite '%s' has no related
standar...
WARNING IMPSYC-2             1 Timing information is not defined for
ce...
WARNING IMPVL-159            696 Pin '%s' of cell '%s' is defined in LEF
...
WARNING TCLCMD-1461          2 Skipped unsupported command: %s
*** Message Summary: 755 warning(s), 0 error(s)

innovus 1> Adjusting coreMargin left    to finFet grid (PlacementGrid) :
after adjusting :2.64
Adjusting coreMargin bottom   to finFet grid (PlacementGrid) : after
adjusting :2.8
Adjusting coreMargin right    to finFet grid (PlacementGrid) : after
adjusting :2.64
Adjusting coreMargin top      to finFet grid (PlacementGrid) : after
adjusting :2.8
Adjusting core size to PlacementGrid : width :24.42 height : 20.16
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
unless standard cell models of this type exist in the LEF/OA library.
Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 560 (derived)
Vertical Layer M2 offset = 660 (derived)
Start create_tracks
Generated pitch 0.99 in Metal6 is different from 1.32 defined in
technology file in preferred direction.
Generated pitch 0.56 in Metal5 is different from 1.12 defined in
technology file in preferred direction.
**WARN: (IMPFP-325): Floorplan of the design is resized. All current
floorplan objects are automatically derived based on specified new
floorplan. This may change blocks, fixed standard cells, existing routes
and blockages.
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

viaInitial starts at Thu Oct 10 11:22:28 2024
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM1 GENERATE.
Type 'man IMPPP-557' for more detail.
```

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```
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM2 GENERATE.
Type 'man IMPPP-557' for more detail.
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM3 GENERATE.
Type 'man IMPPP-557' for more detail.
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM4 GENERATE.
Type 'man IMPPP-557' for more detail.
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM5 GENERATE.
Type 'man IMPPP-557' for more detail.
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM6 GENERATE.
Type 'man IMPPP-557' for more detail.
viaInitial ends at Thu Oct 10 11:22:28 2024
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1503.3M)
**WARN: (IMPPP-136): The currently specified top spacing 0.200000 is
less than the required spacing 0.280000 for widths specified as 0.700000
and 0.700000.
**WARN: (IMPPP-136): The currently specified bottom spacing 0.200000
is less than the required spacing 0.280000 for widths specified as
0.700000 and 0.700000.
**WARN: (IMPPP-136): The currently specified left spacing 0.200000 is
less than the required spacing 0.460000 for widths specified as 0.700000
and 0.700000.
**WARN: (IMPPP-136): The currently specified right spacing 0.200000 is
less than the required spacing 0.460000 for widths specified as 0.700000
and 0.700000.
Ring generation is complete.
vias are now being generated.
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 1.68) (2.14, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 23.46) (2.14,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (27.56, 1.68) (28.00,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (27.56, 23.46) (28.00,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 1.68) (2.14, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (27.56, 1.68) (28.00,
2.30).
```

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```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 23.46) (2.14,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (27.56, 23.46) (28.00,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 0.70) (0.98, 1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 24.62) (1.24,
25.06).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (28.72, 0.70) (29.16,
1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (28.72, 24.36) (29.16,
25.06).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 0.70) (0.98, 1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (28.72, 0.70) (29.16,
1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 24.62) (1.24,
25.06).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (28.72, 24.36) (29.16,
25.06).
addRing created 8 wires.
ViaGen created 0 via, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+-----+
| Metal5 |        4       |      NA      |
| Metal6 |        4       |      NA      |
+-----+-----+-----+
innovus 1> addStripe will allow jog to connect padcore ring and block
ring.

Stripes will stop at the boundary of the specified area.
When breaking rings, the power planner will consider the existence of
blocks.
Stripes will not extend to closest target.
The power planner will set stripe antenna targets to none (no trimming
allowed).
Stripes will not be created over regions without power planning wires.
The entire stripe set will break at the domain if one of the nets is not
in the domain.
addStripe will break automatically at non-default domains when generating
global stripes over the core area or default domain.
Offset for stripe breaking is set to 0.

Initialize fgc environment(mem: 1508.4M) ... fail and won't use fgc to
check drc(cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1508.4M)
```

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```
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1508.4M)
Loading wires (cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1508.4M)
Loading via instances (cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1508.4M)
**WARN: (IMPPP-136): The currently specified spacing 0.200000 in -
spacing option is less than the required spacing 0.460000 for widths
specified as 0.700000 and 0.700000.
Starting stripe generation ...
Non-Default Mode Option Settings :
    NONE
Stripe generation is complete.
vias are now being generated.
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (3.64, 1.68) (4.08, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (3.64, 23.46) (4.08,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (8.64, 1.68) (9.08, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (8.64, 23.46) (9.08,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (13.64, 1.68) (14.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (13.64, 23.46) (14.08,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (18.64, 1.68) (19.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (18.64, 23.46) (19.08,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (23.64, 1.68) (24.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (23.64, 23.46) (24.08,
24.08).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (4.80, 0.70) (5.24, 1.32).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (4.80, 24.44) (5.24,
25.06).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (9.80, 0.70) (10.24, 1.32).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (9.80, 24.44) (10.24,
25.06).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (14.80, 0.70) (15.24,
1.32).
```

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```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (14.80, 24.44) (15.24,
25.06).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (19.80, 0.70) (20.24,
1.32).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (19.80, 24.44) (20.24,
25.06).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (24.80, 0.70) (25.24,
1.32).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (24.80, 24.44) (25.24,
25.06).
addStripe created 10 wires.
ViaGen created 0 via, deleted 0 via to avoid violation.
+-----+-----+
| Layer | Created | Deleted |
+-----+-----+
| Metal6 |     10    |      NA   |
+-----+-----+
innovus 1> **WARN: (IMPSR-4058): Sroute option: blockPinTarget should be
used in conjunction with option: -connect blockPin.
*** Begin SPECIAL ROUTE on Thu Oct 10 11:23:24 2024 ***
SPECIAL ROUTE ran on directory:
/home/student/Desktop/21bec1033/full_adder
SPECIAL ROUTE ran on machine: cad69 (Linux 4.18.0-425.19.2.el8_7.x86_64
x86_64 2.10Ghz)

Begin option processing ...
srouteConnectPowerBump set to false
routeSelectNet set to "VDD VSS"
routeSpecial set to true
srouteBottomLayerLimit set to 1
srouteBottomTargetLayerLimit set to 1
srouteConnectBlockPin set to false
srouteConnectConverterPin set to false
srouteConnectPadPin set to false
srouteConnectStripe set to false
srouteCrossoverViaBottomLayer set to 1
srouteCrossoverViaTopLayer set to 6
srouteFollowCorePinEnd set to 3
srouteFollowPadPin set to false
srouteJogControl set to "preferWithChanges differentLayer"
srouteNoViaOnWireShape set to "padring ring stripe blockring blockpin
coverpin blockwire corewire followpin iowire"
sroutePadPinAllPorts set to true
sroutePreserveExistingRoutes set to true
srouteRoutePowerBarPortOnBothDir set to true
srouteStopBlockPin set to "nearestTarget"
srouteTopLayerLimit set to 6
srouteTopTargetLayerLimit set to 6
End option processing: cpu: 0:00:00, real: 0:00:00, peak: 3025.00 megs.
```

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```
Reading DB technology information...
Finished reading DB technology information.
Reading floorplan and netlist information...
Finished reading floorplan and netlist information.
Read in 12 layers, 6 routing layers, 1 overlap layer
Read in 471 macros, 5 used
Read in 3 components
    3 core components: 3 unplaced, 0 placed, 0 fixed
Read in 6 logical pins
Read in 6 nets
Read in 2 special nets, 2 routed
2 nets selected.

Begin power routing ...
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the VDD net.
    Run the globalNetConnect command or change the CPF file to ensure that
    the netlist reflects the correct power ground connections. The standard
    cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
    connection.
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the VSS net.
    Run the globalNetConnect command or change the CPF file to ensure that
    the netlist reflects the correct power ground connections. The standard
    cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
    connection.
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VDD.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VDD.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VSS.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
VSS.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
```

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```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (27.56, 12.48) (27.93,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (27.56, 12.48) (28.00,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (27.56, 2.58) (28.00,
3.20).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 22.56) (2.14,
23.18).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (IMPPP-531): Message (IMPPP-531) has exceeded the current message
display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
    Number of Core ports routed: 10
    Number of Followpin connections: 5
End power routing: cpu: 0:00:00, real: 0:00:00, peak: 3032.00 megs.
```

```
Begin updating DB with routing results ...
Updating DB with 5 via definition ...Extracting standard cell pins and
blockage .....
Pin and blockage extraction finished
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
sroute post-processing starts at Thu Oct 10 11:23:24 2024
The viaGen is rebuilding shadow vias for net VDD.
sroute post-processing ends at Thu Oct 10 11:23:24 2024
sroute created 29 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+-----+
| Metall1 |      15       |      NA       |
| Via12  |       4        |      0        |
| Metal2  |       2        |      NA       |
| Via23  |       2        |      0        |
| Via34  |       2        |      0        |
| Metal4  |       2        |      NA       |
| Metal6  |      10       |      NA       |
+-----+-----+-----+
*** placeDesign #1 [begin] : totSession cpu/real = 0:00:41.7/0:06:44.4
(0.1), mem = 1507.1M
Extracting standard cell pins and blockage .....
Pin and blockage extraction finished
*** Starting placeDesign default flow ***
*** Start deleteBufferTree ***
Info: Detect buffers to remove automatically.
Analyzing netlist ...
Updating netlist

*summary: 0 instances (buffers/inverters) removed
*** Finish deleteBufferTree (0:00:00.1) ***
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
Set Default Input Pin Transition as 1 ps.
**INFO: Analyzing IO path groups for slack adjustment
Effort level <high> specified for reg2reg_tmp.53898 path_group
AAE_INFO: opIsDesignInPostRouteState() is 0
AAE DB initialization (MEM=1625.45 CPU=0:00:00.0 REAL=0:00:00.0)
#####
# Design Stage: PreRoute
# Design Name: fa
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=1628.46)
Total number of fetched objects 11
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1777.28 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1777.28 CPU=0:00:00.0
REAL=0:00:00.0)
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Input Pin Transition as 0.1 ps.
Set Default Net Load as 0.5 pF.
**INFO: Pre-place timing setting for timing analysis already disabled
Deleted 0 physical inst (cell - / prefix -).
INFO: #ExclusiveGroups=0
INFO: There are no Exclusive Groups.
*** Starting "NanoPlace(TM) placement v#6 (mem=1751.6M)" ...
*** Build Buffered Sizing Timing Model
(cpu=0:00:00.4 mem=1759.6M) ***
*** Build Virtual Sizing Timing Model
(cpu=0:00:00.4 mem=1759.6M) ***
No user-set net weight.
Net fanout histogram:
2          : 10 (90.9%) nets
3          : 0 (0.0%) nets
4          - 14    : 1 (9.1%) nets
15         - 39    : 0 (0.0%) nets
40         - 79    : 0 (0.0%) nets
80         - 159   : 0 (0.0%) nets
160        - 319   : 0 (0.0%) nets
320        - 639   : 0 (0.0%) nets
640        - 1279  : 0 (0.0%) nets
1280       - 2559  : 0 (0.0%) nets
2560       - 5119  : 0 (0.0%) nets
5120+      : 0 (0.0%) nets
Options: timingDriven clkGateAware ignoreScan pinGuide congEffort=auto
gpeffort=medium
**WARN: (IMPSP-9042): Scan chains were not defined, -
place_global_ignore_scan option will be ignored.
Define the scan chains before using this option.
Type 'man IMPSP-9042' for more detail.
#std cell=6 (0 fixed + 6 movable) #buf cell=0 #inv cell=0 #block=0 (0
floating + 0 preplaced)
#ioInst=0 #net=11 #term=26 #term/net=2.36, #fixedIo=0, #floatIo=0,
#fixedPin=0, #floatPin=6
stdCell: 6 single + 0 double + 0 multi
Total standard cell length = 0.0667 (mm), area = 0.0003 (mm^2)
Average module density = 0.682.
Density for the design = 0.682.
      = stdcell_area 101 sites (336 um^2) / alloc_area 148 sites (492
um^2).
Pin Density = 0.1757.
      = total # of pins 26 / total area 148.
== lastAutoLevel = 3
Clock gating cells determined by native netlist tracing.
Iteration 1: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
          Est.  stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
          cpu = 0:00:00.0 real = 0:00:00.0 mem = 1782.4M
Iteration 2: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
          Est.  stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
          cpu = 0:00:00.0 real = 0:00:00.0 mem = 1782.4M
Iteration 3: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
          Est.  stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
          cpu = 0:00:00.0 real = 0:00:00.0 mem = 1783.8M
Active setup views:
    worst_case
Iteration 4: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
          Est.  stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
          cpu = 0:00:00.0 real = 0:00:00.0 mem = 1783.8M
Iteration 5: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
          Est.  stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
          cpu = 0:00:00.0 real = 0:00:00.0 mem = 1783.8M
Iteration 6: Total net bbox = 1.120e+02 (1.05e+02 6.72e+00)
          Est.  stn bbox = 1.136e+02 (1.07e+02 6.72e+00)
          cpu = 0:00:00.1 real = 0:00:01.0 mem = 1783.8M
*** cost = 1.120e+02 (1.05e+02 6.72e+00) (cpu for global=0:00:00.1)
real=0:00:01.0 ***
Info: 0 clock gating cells identified, 0 (on average) moved 0/1
Solver runtime cpu: 0:00:00.0 real: 0:00:00.0
Core Placement runtime cpu: 0:00:00.0 real: 0:00:01.0
**WARN: (IMPSP-9025): No scan chain specified/traced.
Type 'man IMPSP-9025' for more detail.
*** Starting refinePlace (0:00:43.1 mem=1783.8M) ***
Total net bbox length = 1.419e+02 (1.251e+02 1.680e+01) (ext = 9.390e+01)
Move report: Detail placement moves 6 insts, mean move: 8.62 um, max
move: 13.17 um
      Max move on inst (sum_reg): (9.57, 10.36) --> (15.18, 17.92)
      Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 1807.8MB
Summary Report:
Instances move: 6 (out of 6 movable)
Instances flipped: 0
Mean displacement: 8.62 um
Max displacement: 13.17 um (Instance: sum_reg) (9.57, 10.36) -> (15.18,
17.92)
Length: 16 sites, height: 1 rows, site name: tsm3site, cell type:
DFFHQXL
Total net bbox length = 1.841e+02 (9.900e+01 8.512e+01) (ext = 1.005e+02)
Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 1807.8MB
*** Finished refinePlace (0:00:43.1 mem=1807.8M) ***
*** End of Placement (cpu=0:00:00.6, real=0:00:02.0, mem=1807.8M) ***
default core: bins with density > 0.750 = 0.00 % ( 0 / 1 )
Density distribution unevenness ratio = 0.000%
*** Free Virtual Timing Model ...(mem=1807.8M)
Starting IO pin assignment...
The design is not routed. Using placement based method for pin
assignment.
Completed IO pin assignment.
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
**INFO: Analyzing IO path groups for slack adjustment
Effort level <high> specified for reg2reg_tmp.53898 path_group
AAE_INFO: opIsDesignInPostRouteState() is 0
#####
# Design Stage: PreRoute
# Design Name: fa
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=1789.06)
Total number of fetched objects 11
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1840.48 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1840.48 CPU=0:00:00.0
REAL=0:00:00.0)
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Info: Disable timing driven in postCTS congRepair.

Starting congRepair ...
[NR-eGR] Num Prerouted Nets = 0  Num Prerouted Wires = 0
[NR-eGR] Read 11 nets ( ignored 0 )
[NR-eGR] There are 1 clock nets ( 0 with NDR ).
[NR-eGR] Layer group 1: route 11 net(s) in layer range [2, 6]
[NR-eGR] Early Global Route overflow of layer group 1: 0.00% H + 0.00% V.
EstWL: 1.310400e+02um
[NR-eGR] Overflow after Early Global Route 0.00% H + 0.00% V
Early Global Route congestion estimation runtime: 0.00 seconds, mem =
1830.8M
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00,
normalized total congestion hotspot area = 0.00 (area is in unit of 4
std-cell row bins)
Skipped repairing congestion.
[NR-eGR]                               Length (um)  Vias
[NR-eGR] -----
[NR-eGR] Metal1  (1H)                  0    20
[NR-eGR] Metal2  (2V)                  80   18
[NR-eGR] Metal3  (3H)                  50    1
[NR-eGR] Metal4  (4V)                  9    0
[NR-eGR] Metal5  (5H)                  0    0
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
[NR-eGR] Metal6 (6V) 0 0
[NR-eGR] -----
[NR-eGR] Total 139 39
[NR-eGR] -----
-----
[NR-eGR] Total half perimeter of net bounding box: 128um
[NR-eGR] Total length: 139um, number of vias: 39
[NR-eGR] -----
-----
[NR-eGR] Total eGR-routed clock nets wire length: 50um, number of vias:
11
[NR-eGR] -----
-----
Early Global Route wiring runtime: 0.00 seconds, mem = 1765.8M
Tdgp not successfully initied but do clear! skip clearing
End of congRepair (cpu=0:00:00.0, real=0:00:00.0)
*** Finishing placeDesign default flow ***
***** Total cpu 0:0:2
***** Total real time 0:0:2
**placeDesign ... cpu = 0: 0: 2, real = 0: 0: 2, mem = 1765.8M **
Tdgp not successfully initied but do clear! skip clearing

*** Summary of all messages that are not suppressed in this session:
Severity ID Count Summary
WARNING IMPDC-1629 2 The default delay limit was set to %d.
T...
WARNING IMPSP-9025 1 No scan chain specified/traced.
WARNING IMPSP-9042 1 Scan chains were not defined, -
place_glo...
*** Message Summary: 4 warning(s), 0 error(s)

*** placeDesign #1 [finish] : cpu/real = 0:00:01.6/0:00:02.7 (0.6),
totSession cpu/real = 0:00:43.3/0:06:47.0 (0.1), mem = 1765.8M
innovus 1> **ERROR: (IMPSYT-6000):No Object Selected.
**ERROR: (IMPSYT-6000): No Object Selected.
AAE DB initialization (MEM=1747.54 CPU=0:00:00.0 REAL=0:00:00.0)
*** timeDesign #1 [begin] : totSession cpu/real = 0:00:52.5/0:08:32.9
(0.1), mem = 1747.5M
Setting timing_disable_library_data_to_data_checks to 'true'.
Setting timing_disable_user_data_to_data_checks to 'true'.
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1737.5M)
Extraction called for design 'fa' of instances=6 and nets=13 using
extraction engine 'preRoute' .
**WARN: (IMPEXT-3530): The process node is not set. Use the command
setDesignMode -process <process node> prior to extraction for maximum
accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design fa.
RC Extraction called in multi-corner(1) mode.
RCMode: PreRoute
    RC Corner Indexes 0
    Capacitance Scaling Factor : 1.00000
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
Resistance Scaling Factor      : 1.00000
Clock Cap. Scaling Factor    : 1.00000
Clock Res. Scaling Factor    : 1.00000
Shrink Factor                : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0
MEM: 1737.543M)
Starting delay calculation for Setup views
AAE_INFO: opIsDesignInPostRouteState() is 0
#####
# Design Stage: PreRoute
# Design Name: fa
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=1750.11)
Total number of fetched objects 11
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1846.14 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1846.14 CPU=0:00:00.0
REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0
totSessionCpu=0:00:52.6 mem=1838.1M)
```

timeDesign Summary

Setup views included:
worst_case

Setup mode	all	reg2reg	default
WNS (ns):	9.917	N/A	9.917
TNS (ns):	0.000	N/A	0.000
Violating Paths:	0	N/A	0
All Paths:	3	N/A	3

DRVs	Real		Total
	Nr nets(terms)	Worst Vio	Nr nets(terms)

Lab-5: Logic synthesis & Physical Design of Full Adder

```
| max_cap | 0 (0) | 0.000 | 0 (0) |
| max_tran | 0 (0) | 0.000 | 0 (0) |
| max_fanout | 0 (0) | 0 | 0 (0) |
| max_length | 0 (0) | 0 | 0 (0) |
+-----+-----+-----+-----+
Density: 68.243%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.22 sec
Total Real time: 1.0 sec
Total Memory Usage: 1817.5625 Mbytes
*** timeDesign #1 [finish] : cpu/real = 0:00:00.2/0:00:00.8 (0.3),
totSession cpu/real = 0:00:52.7/0:08:33.6 (0.1), mem = 1817.6M
innovus 1> *** timeDesign #2 [begin] : totSession cpu/real =
0:00:52.8/0:08:35.1 (0.1), mem = 1817.6M
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1782.8M)
Starting delay calculation for Hold views
AAE_INFO: opIsDesignInPostRouteState() is 0
#####
#####
# Design Stage: PreRoute
# Design Name: fa
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
#####
Start delay calculation (fullDC) (1 T). (MEM=1792.63)
*** Calculating scaling factor for min_timing libraries using the default
operating condition of each library.
Total number of fetched objects 11
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1844.79 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1844.79 CPU=0:00:00.0
REAL=0:00:00.0)
Turning on fast DC mode.
*** Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0
totSessionCpu=0:00:52.9 mem=1844.8M)

-----
timeDesign Summary
-----
Hold views included:
best_case

+-----+-----+-----+-----+
| Hold mode | all | reg2reg | default |

```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
+-----+-----+-----+-----+
|           WNS (ns):| -0.018 |   N/A   | -0.018  |
|           TNS (ns):| -0.054 |   N/A   | -0.054  |
| Violating Paths:|    3    |   N/A   |    3    |
|     All Paths:   |    3    |   N/A   |    3    |
+-----+-----+-----+-----+
Density: 68.243%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.19 sec
Total Real time: 0.0 sec
Total Memory Usage: 1772.066406 Mbytes
*** timeDesign #2 [finish] : cpu/real = 0:00:00.2/0:00:00.2 (1.0),
totSession cpu/real = 0:00:53.0/0:08:35.2 (0.1), mem = 1772.1M
innovus 1> *** timeDesign #3 [begin] : totSession cpu/real =
0:00:53.1/0:08:37.1 (0.1), mem = 1772.1M
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1772.1M)
Starting delay calculation for Hold views
AAE_INFO: opIsDesignInPostRouteState() is 0
#####
# Design Stage: PreRoute
# Design Name: fa
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=1780.61)
*** Calculating scaling factor for min_timing libraries using the default
operating condition of each library.
Total number of fetched objects 11
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1848.03 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1848.03 CPU=0:00:00.0
REAL=0:00:00.0)
Turning on fast DC mode.
*** Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0
totSessionCpu=0:00:53.2 mem=1848.0M)

-----
timeDesign Summary
-----
Hold views included:
best_case
+-----+-----+-----+-----+
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
|      Hold mode      |    all    | reg2reg | default |
+-----+-----+-----+-----+
|          WNS (ns):| -0.018  | N/A     | -0.018  |
|          TNS (ns):| -0.054  | N/A     | -0.054  |
| Violating Paths:|      3   | N/A     |      3   |
| All Paths:       |      3   | N/A     |      3   |
+-----+-----+-----+-----+
Density: 68.243%
Routing Overflow: 0.00% H and 0.00% V
-----
Reported timing to dir timingReports
Total CPU time: 0.22 sec
Total Real time: 1.0 sec
Total Memory Usage: 1775.300781 Mbytes
*** timeDesign #3 [finish] : cpu/real = 0:00:00.2/0:00:00.2 (1.0),
totSession cpu/real = 0:00:53.3/0:08:37.4 (0.1), mem = 1775.3M
innovus 1>
innovus 1> source ccopt.spec
Extracting original clock gating for clk...
    clock tree clk contains 5 sinks and 0 clock gates.
Extracting original clock gating for clk done.
The skew group clk/constraints was created. It contains 5 sinks and 1
sources.
Checking clock tree convergence...
Checking clock tree convergence done.
innovus 2> ccopt_desgin-cts
invalid command name "ccopt_desgin-cts"
innovus 3> ccopt_desgin -cts
invalid command name "ccopt_desgin"
innovus 4> saveDesign DBS/cts.encl
#% Begin save design ... (date=10/10 11:27:58, mem=1643.5M)
% Begin Save ccopt configuration ... (date=10/10 11:27:58, mem=1643.5M)
% End Save ccopt configuration ... (date=10/10 11:27:58, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1644.3M, current mem=1644.3M)
% Begin Save netlist data ... (date=10/10 11:27:58, mem=1644.3M)
Writing Binary DB to DBS/cts.encl.dat/fa.v.bin in single-threaded mode...
% End Save netlist data ... (date=10/10 11:27:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1645.0M, current mem=1645.0M)
Saving symbol-table file ...
Saving congestion map file DBS/cts.encl.dat/fa.route.congmap.gz ...
% Begin Save AAE data ... (date=10/10 11:27:58, mem=1645.0M)
Saving AAE Data ...
% End Save AAE data ... (date=10/10 11:27:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1645.4M, current mem=1645.4M)
Saving preference file DBS/cts.encl.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=10/10 11:27:58, mem=1646.9M)
Saving floorplan file ...
% End Save floorplan data ... (date=10/10 11:27:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1647.0M, current mem=1647.0M)
Saving Drc markers ...
... 6 markers are saved ...
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
... 0 geometry drc markers are saved ...
... 0 antenna drc markers are saved ...
% Begin Save placement data ... (date=10/10 11:27:58, mem=1647.0M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=10/10 11:27:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1647.3M, current mem=1647.3M)
% Begin Save routing data ... (date=10/10 11:27:58, mem=1647.3M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1778.1M) ***
% End Save routing data ... (date=10/10 11:27:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1647.5M, current mem=1647.5M)
Saving property file DBS/cts.encl.dat/fa.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1781.1M) ***
% Begin Save power constraints data ... (date=10/10 11:27:58,
mem=1648.7M)
% End Save power constraints data ... (date=10/10 11:27:58, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1648.7M, current mem=1648.7M)
Generated self-contained design cts.encl.dat
#% End save design ... (date=10/10 11:27:58, total cpu=0:00:00.2,
real=0:00:00.0, peak res=1651.8M, current mem=1651.8M)
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 5> #WARNING (NRIF-91) Option setNanoRouteMode -
routeTopRoutingLayer is obsolete. It will continue to work for the
current release. To ensure compatibility with future releases, use option
setDesignMode -topRoutingLayer instead.
#WARNING (NRIF-90) Option setNanoRouteMode -routeBottomRoutingLayer is
obsolete. It will continue to work for the current release. To ensure
compatibility with future releases, use option setDesignMode -
bottomRoutingLayer instead.
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory =
1653.61 (MB), peak = 1683.08 (MB)
AAE_INFO: Pre Route call back at the beginning of routeDesign
***INFO: setDesignMode -flowEffort standard
***INFO: setDesignMode -powerEffort none
#WARNING (NRIG-96) Selected single pass global detail route --
globalDetail". Clock eco and post optimizations will not be run. See "man
NRIG-96" for more details.
#WARNING (NRIG-144) Cannot combine -viaOpt with -globalDetail option. The
-viaOpt will be ignored.
**INFO: User settings:
setNanoRouteMode -drouteEndIteration      1
setNanoRouteMode -droutePostRouteSpreadWire 1
setNanoRouteMode -extractThirdPartyCompatible false
setNanoRouteMode -routeBottomRoutingLayer   1
setNanoRouteMode -routeTopRoutingLayer      6
setNanoRouteMode -routeWithSiDriven        false
setNanoRouteMode -routeWithTimingDriven    false
setNanoRouteMode -timingEngine             {}
setExtractRCMode -engine                  preRoute
setDelayCalMode -enable_high_fanout       true
setDelayCalMode -engine                  aae
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
setDelayCalMode -ignoreNetLoad           false
setDelayCalMode -socv_accuracy_mode     low
setSIMode -separate_delta_delay_on_data true

/**INFO: multi-cut via swapping will not be performed after routing.
/**INFO: All auto set options tuned by routeDesign will be restored to
their original settings on command completion.
Begin checking placement ... (start mem=1817.7M, init mem=1817.7M)
*info: Placed = 6
*info: Unplaced = 0
Placement Density:68.24%(336/492)
Placement Density (including fixed std cells):68.24%(336/492)
Finished checkPlace (total: cpu=0:00:00.0, real=0:00:00.0; vio checks:
cpu=0:00:00.0, real=0:00:00.0; mem=1817.7M)
Turning off fast DC mode.

changeUseClockNetStatus Option : -noFixedNetWires
*** Changed status on (0) nets in Clock.
*** End changeUseClockNetStatus (cpu=0:00:00.0, real=0:00:00.0,
mem=1817.7M) ***

globalDetailRoute

#Start globalDetailRoute on Thu Oct 10 11:28:40 2024
#
#WARNING (NRIG-1303) The congestion map does not match the GCELL grid.
Clearing the map.
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
#num needed restored net=0
#need_extraction net=0 (total=13)
#WARNING (NRDB-2005) SPECIAL_NET VDD has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#WARNING (NRDB-2005) SPECIAL_NET VSS has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Total number of trivial nets (e.g. < 2 pins) = 2 (skipped).
#Total number of routable nets = 11.
#Total number of nets in the design = 13.
#11 routable nets do not have any wires.
#11 nets will be global routed.
#Start routing data preparation on Thu Oct 10 11:28:40 2024
#
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.320.
#Voltage range [0.000 - 1.320] has 11 nets.
#Voltage range [1.080 - 1.320] has 1 net.
#Voltage range [0.000 - 0.000] has 1 net.
#Build and mark too close pins for the same net.
#Rebuild pin access data for design.
#Initial pin access analysis.
#Detail pin access analysis.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```

# Metal1      H   Track-Pitch = 0.56000    Line-2-Via Pitch = 0.48500
# Metal2      V   Track-Pitch = 0.66000    Line-2-Via Pitch = 0.56000
# Metal3      H   Track-Pitch = 0.56000    Line-2-Via Pitch = 0.56000
# Metal4      V   Track-Pitch = 0.66000    Line-2-Via Pitch = 0.56000
# Metal5      H   Track-Pitch = 0.56000    Line-2-Via Pitch = 0.56000
# Metal6      V   Track-Pitch = 0.99000    Line-2-Via Pitch = 0.95000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1661.39 (MB),
peak = 1694.54 (MB)
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.56000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1664.20 (MB),
peak = 1694.54 (MB)
#
#Finished routing data preparation on Thu Oct 10 11:28:40 2024
#
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 8.56 (MB)
#Total memory = 1664.20 (MB)
#Peak memory = 1694.54 (MB)
#
#
#Start global routing on Thu Oct 10 11:28:40 2024
#
#
#Start global routing initialization on Thu Oct 10 11:28:40 2024
#
#Number of eco nets is 0
#
#Start global routing data preparation on Thu Oct 10 11:28:40 2024
#
#Start routing resource analysis on Thu Oct 10 11:28:40 2024
#
#Routing resource analysis is done on Thu Oct 10 11:28:40 2024
#
# Resource Analysis:
#
#          Routing #Avail     #Track      #Total      %Gcell
# Layer    Direction Track Blocked   Gcell    Blocked
# -----
# Metal1      H       15        31        12      16.67%
# Metal2      V       39         6        12      0.00%
# Metal3      H       44         2        12      0.00%
# Metal4      V       42         3        12      0.00%
# Metal5      H       38         8        12      0.00%
# Metal6      V        9        20        12      16.67%
# -----
# Total           188      29.13%      72      5.56%
#

```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
#  
#  
#  
#Global routing data preparation is done on Thu Oct 10 11:28:40 2024  
#  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1664.20 (MB),  
peak = 1694.54 (MB)  
#  
#  
#Global routing initialization is done on Thu Oct 10 11:28:40 2024  
#  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1664.20 (MB),  
peak = 1694.54 (MB)  
#  
#start global routing iteration 1...  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1665.95 (MB),  
peak = 1694.54 (MB)  
#  
#start global routing iteration 2...  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1665.95 (MB),  
peak = 1694.54 (MB)  
#  
#  
#Total number of trivial nets (e.g. < 2 pins) = 2 (skipped).  
#Total number of routable nets = 11.  
#Total number of nets in the design = 13.  
#  
#11 routable nets have routed wires.  
#  
#Routed nets constraints summary:  
#-----  
#      Rules    Unconstrained  
#-----  
#      Default     11  
#-----  
#      Total      11  
#-----  
#  
#Routing constraints summary of the whole design:  
#-----  
#      Rules    Unconstrained  
#-----  
#      Default     11  
#-----  
#      Total      11  
#-----  
#  
#  
# Congestion Analysis: (blocked Gcells are excluded)  
#  
#          OverCon  
#          #Gcell    %Gcell  
# Layer      (1)    OverCon  
# -----
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
#  Metall1      0 (0.00%)  (0.00%)
#  Metal2      0 (0.00%)  (0.00%)
#  Metal3      0 (0.00%)  (0.00%)
#  Metal4      0 (0.00%)  (0.00%)
#  Metal5      0 (0.00%)  (0.00%)
#  Metal6      0 (0.00%)  (0.00%)
#
#-----#
#      Total      0 (0.00%)  (0.00%)
#
#-----#
# The worst congested Gcell overcon (routing demand over resource in
# number of tracks) = 1
# Overflow after GR: 0.00% H + 0.00% V
#
#-----#
#Hotspot report including placement blocked areas
[hotspot] +-----+-----+-----+
-----+
[hotspot] |      layer   |      max hotspot   |      total hotspot   |
[hotspot bbox           |                   |
[hotspot] +-----+-----+-----+
-----+
[hotspot] |      Metal1(H)   |      0.00   |      0.00   |
|(none)          |                   |
[hotspot] |      Metal2(V)   |      0.00   |      0.00   |
|(none)          |                   |
[hotspot] |      Metal3(H)   |      0.00   |      0.00   |
|(none)          |                   |
[hotspot] |      Metal4(V)   |      0.00   |      0.00   |
|(none)          |                   |
[hotspot] |      Metal5(H)   |      0.00   |      0.00   |
|(none)          |                   |
[hotspot] |      Metal6(V)   |      0.00   |      0.00   |
|(none)          |                   |
[hotspot] +-----+-----+-----+
-----+
[hotspot] |      worst     |      0.00   |      0.00   |
|
[hotspot] +-----+-----+-----+
-----+
[hotspot] |      all layers |      0.00   |      0.00   |
|
[hotspot] +-----+-----+-----+
-----+
Local HotSpot Analysis (blockage included) (3d): normalized congestion
max/total hotspot area = 0.00/0.00 (area is in unit of 4 std-cell row
bins)
#Complete Global Routing.
#Total wire length = 94 um.
#Total half perimeter of net bounding box = 148 um.
#Total wire length on LAYER Metal1 = 0 um.
#Total wire length on LAYER Metal2 = 60 um.
#Total wire length on LAYER Metal3 = 34 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
#Total number of vias = 29
#Up-Via Summary (total 29):
#
#-----
# Metal1          19
# Metal2           9
# Metal3           1
#-----
#                  29
#
#Max overcon = 0 track.
#Total overcon = 0.00%.
#Worst layer Gcell overcon rate = 0.00%.
#
#Global routing statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.88 (MB)
#Total memory = 1666.08 (MB)
#Peak memory = 1694.54 (MB)
#
#Finished global routing on Thu Oct 10 11:28:40 2024
#
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1666.08 (MB),
peak = 1694.54 (MB)
#Start Track Assignment.
#Done with 4 horizontal wires in 1 hboxes and 6 vertical wires in 1
hboxes.
#Done with 0 horizontal wires in 1 hboxes and 0 vertical wires in 1
hboxes.
#Done with 1 horizontal wires in 1 hboxes and 1 vertical wires in 1
hboxes.
#
#Track assignment summary:
# layer      (wire length)    (overlap)    (long ovlp) (with obs/pg/clk)
#-----
# Metal1        0.00    0.00%    0.00%    0.00%
# Metal2       56.57    0.00%    0.00%    0.00%
# Metal3       35.51    0.00%    0.00%    0.00%
# Metal4        0.00    0.00%    0.00%    0.00%
# Metal5        0.00    0.00%    0.00%    0.00%
# Metal6        0.00    0.00%    0.00%    0.00%
#-----
# All          92.08    0.00%    0.00%    0.00%
#Complete Track Assignment.
#Total wire length = 89 um.
#Total half perimeter of net bounding box = 148 um.
#Total wire length on LAYER Metal1 = 0 um.
#Total wire length on LAYER Metal2 = 55 um.
#Total wire length on LAYER Metal3 = 34 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
#Total number of vias = 29
#Up-Via Summary (total 29):
#
#-----
# Metal1      19
# Metal2      9
# Metal3      1
#-----
#          29
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1666.19 (MB),
peak = 1694.54 (MB)
#
#Routing data preparation, pin analysis, global routing and track
assignment statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 10.55 (MB)
#Total memory = 1666.19 (MB)
#Peak memory = 1694.54 (MB)
#
#Start Detail Routing..
#start initial detail routing ...
#   number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1667.73 (MB),
peak = 1694.54 (MB)
#Complete Detail Routing.
#Total wire length = 132 um.
#Total half perimeter of net bounding box = 148 um.
#Total wire length on LAYER Metal1 = 5 um.
#Total wire length on LAYER Metal2 = 85 um.
#Total wire length on LAYER Metal3 = 34 um.
#Total wire length on LAYER Metal4 = 9 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 31
#Up-Via Summary (total 31):
#
#-----
# Metal1      20
# Metal2      10
# Metal3      1
#-----
#          31
#
#Total number of DRC violations = 0
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.54 (MB)
#Total memory = 1667.73 (MB)
#Peak memory = 1694.54 (MB)
#
#Start Post Route wire spreading..
#
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
#Start DRC checking..
#    number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1668.05 (MB),
peak = 1694.54 (MB)
#CELL_VIEW fa,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#
#Start data preparation for wire spreading...
#
#Data preparation is done on Thu Oct 10 11:28:40 2024
#
#
#Start Post Route Wire Spread.
#Done with 0 horizontal wires in 1 hboxes and 1 vertical wires in 1
hboxes.
#Complete Post Route Wire Spread.
#
#Total wire length = 133 um.
#Total half perimeter of net bounding box = 148 um.
#Total wire length on LAYER Metal1 = 5 um.
#Total wire length on LAYER Metal2 = 86 um.
#Total wire length on LAYER Metal3 = 34 um.
#Total wire length on LAYER Metal4 = 9 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 31
#Up-Via Summary (total 31):
#
#-----
# Metall1      20
# Metal2      10
# Metal3       1
#-----
#                  31
#
#
#Start DRC checking..
#    number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1667.87 (MB),
peak = 1694.54 (MB)
#CELL_VIEW fa,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#    number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1667.87 (MB),
peak = 1694.54 (MB)
#CELL_VIEW fa,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#Post Route wire spread is done.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
#Total wire length = 133 um.
#Total half perimeter of net bounding box = 148 um.
#Total wire length on LAYER Metal1 = 5 um.
#Total wire length on LAYER Metal2 = 86 um.
#Total wire length on LAYER Metal3 = 34 um.
#Total wire length on LAYER Metal4 = 9 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 31
#Up-Via Summary (total 31):
#
#-----
# Metal1      20
# Metal2      10
# Metal3      1
#-----
#          31
#
#detailRoute Statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.68 (MB)
#Total memory = 1667.87 (MB)
#Peak memory = 1694.54 (MB)
#    no debugging net set
#
#globaDetailRoute statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 21.95 (MB)
#Total memory = 1676.20 (MB)
#Peak memory = 1694.54 (MB)
#Number of warnings = 3
#Total number of warnings = 7
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Thu Oct 10 11:28:40 2024
#
#Default setup view is reset to worst_case.

detailRoute

#Start detailRoute on Thu Oct 10 11:28:40 2024
#
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
#num needed restored net=0
#need_extraction net=0 (total=13)
#WARNING (NRDB-2005) SPECIAL_NET VDD has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#WARNING (NRDB-2005) SPECIAL_NET VSS has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Start routing data preparation on Thu Oct 10 11:28:40 2024
#
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.320.
#Voltage range [0.000 - 1.320] has 11 nets.
#Voltage range [1.080 - 1.320] has 1 net.
#Voltage range [0.000 - 0.000] has 1 net.
#Build and mark too close pins for the same net.
#Initial pin access analysis.
#Detail pin access analysis.
# Metal1      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.48500
# Metal2      V  Track-Pitch = 0.66000   Line-2-Via Pitch = 0.56000
# Metal3      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.56000
# Metal4      V  Track-Pitch = 0.66000   Line-2-Via Pitch = 0.56000
# Metal5      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.56000
# Metal6      V  Track-Pitch = 0.99000   Line-2-Via Pitch = 0.95000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1674.68 (MB),
peak = 1694.54 (MB)
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.56000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1677.18 (MB),
peak = 1694.54 (MB)
#
#Start Post Route wire spreading..
#
#Start data preparation for wire spreading...
#
#Data preparation is done on Thu Oct 10 11:28:40 2024
#
#
#Start Post Route Wire Spread.
#Done with 0 horizontal wires in 1 hboxes and 0 vertical wires in 1
hboxes.
#Complete Post Route Wire Spread.
#
#Total wire length = 133 um.
#Total half perimeter of net bounding box = 148 um.
#Total wire length on LAYER Metal1 = 5 um.
#Total wire length on LAYER Metal2 = 86 um.
#Total wire length on LAYER Metal3 = 34 um.
#Total wire length on LAYER Metal4 = 9 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 31
#Up-Via Summary (total 31):
#
#-----
# Metal1          20
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
# Metal2          10
# Metal3          1
#-----
#                  31
#
#      number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1677.34 (MB),
peak = 1694.54 (MB)
#CELL_VIEW fa,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#Post Route wire spread is done.
#Total wire length = 133 um.
#Total half perimeter of net bounding box = 148 um.
#Total wire length on LAYER Metal1 = 5 um.
#Total wire length on LAYER Metal2 = 86 um.
#Total wire length on LAYER Metal3 = 34 um.
#Total wire length on LAYER Metal4 = 9 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 31
#Up-Via Summary (total 31):
#
#-----
# Metal1          20
# Metal2          10
# Metal3          1
#-----
#                  31
#
#      no debugging net set
#
#detailRoute statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.29 (MB)
#Total memory = 1674.18 (MB)
#Peak memory = 1694.54 (MB)
#Number of warnings = 2
#Total number of warnings = 9
#Number of fails = 0
#Total number of fails = 0
#Complete detailRoute on Thu Oct 10 11:28:40 2024
#
#Default setup view is reset to worst_case.
AAE_INFO: Post Route call back at the end of routeDesign
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory =
1674.19 (MB), peak = 1694.54 (MB)
*** Message Summary: 0 warning(s), 0 error(s)

innovus 5> **WARN: (IMPSP-5217): addFiller command is running on a
postRoute database. It is recommended to be followed by ecoRoute -target
command to make the DRC clean.
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
Type 'man IMPSP-5217' for more detail.
*INFO: Adding fillers to top-module.
*INFO: Added 0 filler inst (cell FILL64 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILL32 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILL16 / prefix FILLER).
*INFO: Added 4 filler insts (cell FILL8 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILL4 / prefix FILLER).
*INFO: Added 6 filler insts (cell FILL2 / prefix FILLER).
*INFO: Added 3 filler insts (cell FILL1 / prefix FILLER).
*INFO: Total 13 filler insts added - prefix FILLER (CPU: 0:00:00.0).
For 13 new insts, innovus 5> **WARN: (IMPSP-5217): addFiller command is
running on a postRoute database. It is recommended to be followed by
ecoRoute -target command to make the DRC clean.
Type 'man IMPSP-5217' for more detail.
*INFO: Adding fillers to top-module.
*INFO: Added 0 filler inst of any cell-type.
innovus 5> Performing RC Extraction ...
Extraction called for design 'fa' of instances=19 and nets=13 using
extraction engine 'preRoute'.
**WARN: (IMPEXT-3530): The process node is not set. Use the command
setDesignMode -process <process node> prior to extraction for maximum
accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design fa.
RC Extraction called in multi-corner(1) mode.
RCMode: PreRoute
    RC Corner Indexes          0
    Capacitance Scaling Factor : 1.00000
    Resistance Scaling Factor : 1.00000
    Clock Cap. Scaling Factor : 1.00000
    Clock Res. Scaling Factor : 1.00000
    Shrink Factor             : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0
MEM: 1844.973M)
innovus 5> Writing Netlist "fa.v" ...
innovus 5> #% Begin save design ... (date=10/10 11:31:58, mem=1677.9M)
% Begin Save ccopt configuration ... (date=10/10 11:31:58, mem=1677.9M)
% End Save ccopt configuration ... (date=10/10 11:31:58, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1678.1M, current mem=1678.1M)
% Begin Save netlist data ... (date=10/10 11:31:58, mem=1678.1M)
Writing Binary DB to fa.enc.dat/fa.v.bin in single-threaded mode...
% End Save netlist data ... (date=10/10 11:31:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1678.2M, current mem=1678.2M)
Saving symbol-table file ...
Saving congestion map file fa.enc.dat/fa.route.congmap.gz ...
% Begin Save AAE data ... (date=10/10 11:31:58, mem=1678.2M)
Saving AAE Data ...
AAE DB initialization (MEM=1844.51 CPU=0:00:00.0 REAL=0:00:00.0)
```

Lab-5: Logic synthesis & Physical Design of Full Adder

```
% End Save AAE data ... (date=10/10 11:31:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1678.8M, current mem=1678.8M)
Saving preference file fa.enc.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=10/10 11:31:58, mem=1679.4M)
Saving floorplan file ...
% End Save floorplan data ... (date=10/10 11:31:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1679.4M, current mem=1679.4M)
Saving Drc markers ...
... 6 markers are saved ...
... 0 geometry drc markers are saved ...
... 0 antenna drc markers are saved ...
% Begin Save placement data ... (date=10/10 11:31:58, mem=1679.4M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=10/10 11:31:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1679.4M, current mem=1679.4M)
% Begin Save routing data ... (date=10/10 11:31:58, mem=1679.4M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1844.0M) ***
% End Save routing data ... (date=10/10 11:31:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1679.5M, current mem=1679.5M)
Saving property file fa.enc.dat/fa.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1847.0M) ***
#Saving pin access data to file fa.enc.dat/fa.apa ...
#
% Begin Save power constraints data ... (date=10/10 11:31:58,
mem=1679.5M)
% End Save power constraints data ... (date=10/10 11:31:58, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1679.5M, current mem=1679.5M)
Generated self-contained design fa.enc.dat
#% End save design ... (date=10/10 11:31:58, total cpu=0:00:00.2,
real=0:00:00.0, peak res=1710.0M, current mem=1680.2M)
*** Message Summary: 0 warning(s), 0 error(s)

Parse flat map file...
Writing GDSII file ...
***** db unit per micron = 2000 *****
***** output gds2 file unit per micron = 2000 *****
***** unit scaling factor = 1 *****
Output for instance
Output for bump
Output for physical terminals
Output for logical terminals
Output for regular nets
Output for special nets and metal fills
Output for via structure generation total number 7
Statistics for GDS generated (version 3)
-----
Stream Out Layer Mapping Information:
GDS Layer Number      GDS Layer Name
-----
```

Lab-5: Logic synthesis & Physical Design of Full Adder

122	DIEAREA
58	Via34
57	Via34
50	Metal3
107	Metal6
46	Metal3
45	Metal3
44	Metal3
63	Via34
43	Metal3
62	Via34
41	Via23
22	Metal12
40	Via23
37	Via23
59	Via34
36	Via23
31	Metal12
88	Metal5
29	Metal12
86	Metal5
105	Via56
9	Metal11
66	Metal4
42	Via23
23	Metal12
99	Via56
19	Via12
8	Metal11
65	Metal4
84	Via45
30	Metal12
87	Metal5
7	Metal11
6	Metal11
64	Metal4
83	Via45
39	Via23
16	Via12
52	Metal3
109	Metal6
2	Metal11
21	Via12
78	Via45
10	Metal11
67	Metal4
51	Metal3
108	Metal6
28	Metal12
1	Metal11
20	Via12
38	Via23
15	Via12
5	Metal11

Lab-5: Logic synthesis & Physical Design of Full Adder

81	Via45
17	Via12
49	Metal3
18	Via12
47	Metal3
24	Metal12
100	Via56
48	Metal3
106	Metal6
25	Metal2
3	Metal1
79	Via45
26	Metal12
102	Via56
4	Metal1
27	Metal2
85	Metal5
104	Via56
60	Via34
61	Via34
68	Metal4
69	Metal4
70	Metal4
71	Metal4
72	Metal4
73	Metal4
80	Via45
82	Via45
90	Metal5
91	Metal5
92	Metal5
93	Metal5
94	Metal5
101	Via56
103	Via56
111	Metal6
112	Metal6
113	Metal6
114	Metal6
115	Metal6
110	Metal6
89	Metal5
117	Metal6
56	Metal3
55	Metal3
54	Metal3
53	Metal3
32	Metal12
98	Metal15
96	Metal15
76	Metal4
33	Metal2
75	Metal4
97	Metal5

Lab-5: Logic synthesis & Physical Design of Full Adder

74	Metal4
119	Metal6
12	Metal1
77	Metal4
118	Metal6
11	Metal1
34	Metal2
116	Metal6
35	Metal2
13	Metal1
14	Metal1
95	Metal5

Stream Out Information Processed for GDS version 3:
Units: 2000 DBU

Object	Count
Instances	19
Ports/Pins	6
metal layer Metal2	4
metal layer Metal3	1
metal layer Metal4	1
Nets	31
metal layer Metal1	1
metal layer Metal2	23
metal layer Metal3	6
metal layer Metal4	1
Via Instances	31
Special Nets	47
metal layer Metal1	15
metal layer Metal2	2
metal layer Metal4	2
metal layer Metal5	4
metal layer Metal6	24
Via Instances	8
Metal Fills	0
Via Instances	0
Metal FillOPCs	0
Via Instances	0
Metal FillDRCs	0
Via Instances	0

Lab-5: Logic synthesis & Physical Design of Full Adder

```
Text                                19
    metal layer Metal2                12
    metal layer Metal3                3
    metal layer Metal4                2
    metal layer Metal6                2

Blockages                            0

Custom Text                           0

Custom Box                            0

Trim Metal                            0

#####Streamout is finished!
innovus 5> Parse flat map file...
Writing GDSII file ...
***** db unit per micron = 2000 *****
***** output gds2 file unit per micron = 2000 *****
***** unit scaling factor = 1 *****
Output for instance
Output for bump
Output for physical terminals
Output for logical terminals
Output for regular nets
Output for special nets and metal fills
Output for via structure generation total number 7
Statistics for GDS generated (version 3)
-----
Stream Out Layer Mapping Information:
GDS Layer Number      GDS Layer Name
-----
  121                  COMP
  122                  DIEAREA
   58                  Via34
   57                  Via34
   50                  Metal3
  107                  Metal6
   46                  Metal3
   45                  Metal3
   44                  Metal3
   63                  Via34
   43                  Metal3
   62                  Via34
   41                  Via23
   22                  Metal2
   40                  Via23
   37                  Via23
   59                  Via34
   36                  Via23
```

Lab-5: Logic synthesis & Physical Design of Full Adder

31	Metal2
88	Metal5
29	Metal2
86	Metal5
105	Via56
9	Metal11
66	Metal4
42	Via23
23	Metal2
99	Via56
19	Via12
8	Metal11
65	Metal4
84	Via45
30	Metal2
87	Metal5
7	Metal11
6	Metal11
64	Metal4
83	Via45
39	Via23
16	Via12
52	Metal3
109	Metal6
2	Metal11
21	Via12
78	Via45
10	Metal11
67	Metal4
51	Metal3
108	Metal6
28	Metal2
1	Metal11
20	Via12
38	Via23
15	Via12
5	Metal11
81	Via45
17	Via12
49	Metal3
18	Via12
47	Metal3
24	Metal2
100	Via56
48	Metal3
106	Metal6
25	Metal2
3	Metal11
79	Via45
26	Metal2
102	Via56
4	Metal11
27	Metal2
85	Metal5

Lab-5: Logic synthesis & Physical Design of Full Adder

104	Via56
60	Via34
61	Via34
68	Metal4
69	Metal4
70	Metal4
71	Metal4
72	Metal4
73	Metal4
80	Via45
82	Via45
90	Metal5
91	Metal5
92	Metal5
93	Metal5
94	Metal5
101	Via56
103	Via56
111	Metal6
112	Metal6
113	Metal6
114	Metal6
115	Metal6
110	Metal6
89	Metal5
117	Metal6
56	Metal3
55	Metal3
54	Metal3
53	Metal3
32	Metal2
98	Metal5
96	Metal5
76	Metal4
33	Metal2
75	Metal4
97	Metal5
74	Metal4
119	Metal6
12	Metal1
77	Metal4
118	Metal6
11	Metal1
34	Metal2
116	Metal6
35	Metal2
13	Metal1
14	Metal1
95	Metal5

Stream Out Information Processed for GDS version 3:
Units: 2000 DBU

Lab-5: Logic synthesis & Physical Design of Full Adder

Object	Count
<hr/>	
Instances	19
Ports/Pins	6
metal layer Metal2	4
metal layer Metal3	1
metal layer Metal4	1
Nets	31
metal layer Metal1	1
metal layer Metal2	23
metal layer Metal3	6
metal layer Metal4	1
Via Instances	31
Special Nets	47
metal layer Metal1	15
metal layer Metal2	2
metal layer Metal4	2
metal layer Metal5	4
metal layer Metal6	24
Via Instances	8
Metal Fills	0
Via Instances	0
Metal FillOPCs	0
Via Instances	0
Metal FillDRCs	0
Via Instances	0
Text	19
metal layer Metal2	12
metal layer Metal3	3
metal layer Metal4	2
metal layer Metal6	2
Blockages	0
Custom Text	0
Custom Box	0
Trim Metal	0

Lab-5: Logic synthesis & Physical Design of Full Adder

```
#####Streamout is finished!
innovus 5> Parse flat map file...
Writing GDSII file ...
***** db unit per micron = 2000 *****
***** output gds2 file unit per micron = 2000 *****
***** unit scaling factor = 1 *****

Output for instance
Output for bump
Output for physical terminals
Output for logical terminals
Output for regular nets
Output for special nets and metal fills
Output for via structure generation total number 7
Statistics for GDS generated (version 3)
-----
Stream Out Layer Mapping Information:
GDS Layer Number          GDS Layer Name
-----
121                         COMP
122                         DIEAREA
58                          Via34
57                          Via34
50                          Metal3
107                         Metal6
46                          Metal3
45                          Metal3
44                          Metal3
63                          Via34
43                          Metal3
62                          Via34
41                          Via23
22                          Metal2
40                          Via23
37                          Via23
59                          Via34
36                          Via23
31                          Metal2
88                          Metal5
29                          Metal2
86                          Metal5
105                         Via56
9                           Metal1
66                         Metal4
42                         Via23
23                         Metal2
99                         Via56
19                         Via12
8                           Metal1
65                         Metal4
84                         Via45
30                         Metal2
87                         Metal5
7                           Metal1
```

Lab-5: Logic synthesis & Physical Design of Full Adder

6	Metall1
64	Metal4
83	Via45
39	Via23
16	Via12
52	Metal3
109	Metal6
2	Metall1
21	Via12
78	Via45
10	Metall1
67	Metal4
51	Metal3
108	Metal6
28	Metal2
1	Metall1
20	Via12
38	Via23
15	Via12
5	Metall1
81	Via45
17	Via12
49	Metal3
18	Via12
47	Metal3
24	Metal2
100	Via56
48	Metal3
106	Metal6
25	Metal2
3	Metall1
79	Via45
26	Metal2
102	Via56
4	Metall1
27	Metal2
85	Metal5
104	Via56
60	Via34
61	Via34
68	Metal4
69	Metal4
70	Metal4
71	Metal4
72	Metal4
73	Metal4
80	Via45
82	Via45
90	Metal5
91	Metal5
92	Metal5
93	Metal5
94	Metal5
101	Via56

Lab-5: Logic synthesis & Physical Design of Full Adder

103	Via56
111	Metal6
112	Metal6
113	Metal6
114	Metal6
115	Metal6
110	Metal6
89	Metal5
117	Metal6
56	Metal3
55	Metal3
54	Metal3
53	Metal3
32	Metal2
98	Metal5
96	Metal5
76	Metal4
33	Metal2
75	Metal4
97	Metal5
74	Metal4
119	Metal6
12	Metal1
77	Metal4
118	Metal6
11	Metal1
34	Metal2
116	Metal6
35	Metal2
13	Metal1
14	Metal1
95	Metal5

Stream Out Information Processed for GDS version 3:
Units: 2000 DBU

Object	Count

Instances	19

Ports/Pins	6
metal layer Metal2	4
metal layer Metal3	1
metal layer Metal4	1

Nets	31
metal layer Metal1	1
metal layer Metal2	23
metal layer Metal3	6
metal layer Metal4	1

Via Instances	31

Lab-5: Logic synthesis & Physical Design of Full Adder

Special Nets	47
metal layer Metal1	15
metal layer Metal2	2
metal layer Metal4	2
metal layer Metal5	4
metal layer Metal6	24
Via Instances	8
Metal Fills	0
Via Instances	0
Metal FillOPCs	0
Via Instances	0
Metal FillDRCs	0
Via Instances	0
Text	19
metal layer Metal2	12
metal layer Metal3	3
metal layer Metal4	2
metal layer Metal6	2
Blockages	0
Custom Text	0
Custom Box	0
Trim Metal	0
#####Streamout is finished!	
innovus 5>	

Lab-5: Logic synthesis & Physical Design of Full Adder

Inference: A total of 3 leaf instance count is present in the gate level netlist with total area of 16.074, total power of 564.62nW.

Result: Hence a Full Adder is physically designed, synthesized and the gate level netlist with timing, area and power report has been generated.