

DA3: Logic synthesis and Functional Verification of restoring binary division algorithm

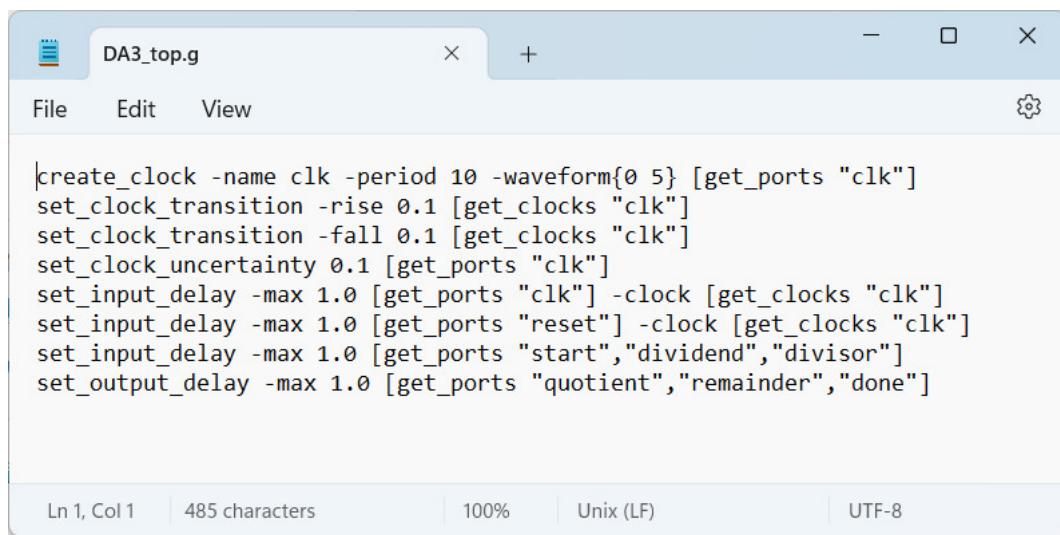
Aim: To synthesize a restoring binary division algorithm and to get the gate level netlist with timing, area, and power reports.

EDA Tools Used: Cadence NC Launch, Genus (Logic synthesis tool) .

Description: The restoring binary division algorithm is a method for dividing two binary numbers, similar to long division in decimal. It operates by iteratively subtracting the divisor from the most significant bits of the dividend (shifted left) and checking if the result is non-negative. If the result is positive or zero, the quotient bit is set to 1, and the remainder retains the subtraction result. If the result is negative, the quotient bit is set to 0, and the original value is restored (hence "restoring") before proceeding to the next step. This process repeats until all bits of the quotient are determined.

Procedure:

1. Write the verilog file for the design and do the functional verification in NC Launch.
2. Copy the fast.lib and slow.lib files into the folder where (.v) files are located.
3. Create a Synopsys design constraint file (.SDC file) by entering the design constraints required for the synthesis.

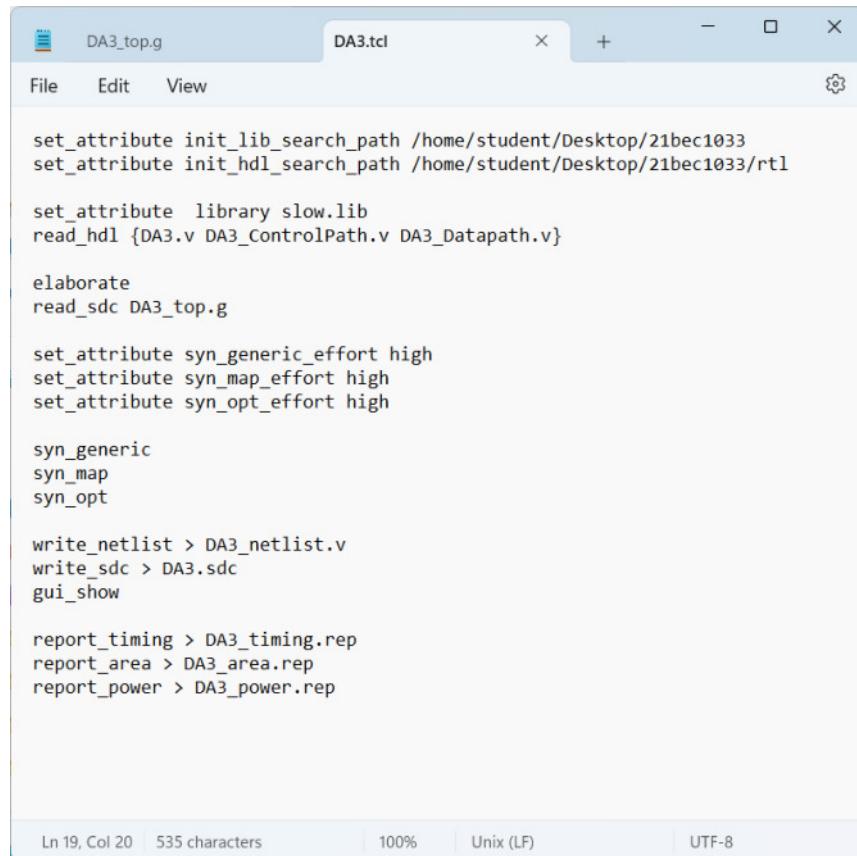


```
create_clock -name clk -period 10 -waveform{0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.1 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "clk"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "start","dividend","divisor"]
set_output_delay -max 1.0 [get_ports "quotient","remainder","done"]
```

Ln 1, Col 1 | 485 characters | 100% | Unix (LF) | UTF-8

DA3 Logic synthesis & Physical design of restoring binary division algorithm

4. Create a (.tcl) file containing all the commands for performing the logic synthesis.
Synthesis effort can be medium or high.



The screenshot shows a text editor window with the title bar 'DA3.tcl'. The window contains a Tcl script for performing logic synthesis. The script includes commands for setting search paths, reading HDL files, elaborating the design, and specifying synthesis efforts (syn_generic_effort, syn_map_effort, syn_opt_effort). It also includes commands for writing netlists, generating SDC files, and displaying GUIs. Finally, it generates timing, area, and power reports.

```
set_attribute init_lib_search_path /home/student/Desktop/21bec1033
set_attribute init_hdl_search_path /home/student/Desktop/21bec1033/rtl

set_attribute library slow.lib
read_hdl {DA3.v DA3_ControlPath.v DA3_Datapath.v}

elaborate
read_sdc DA3_top.g

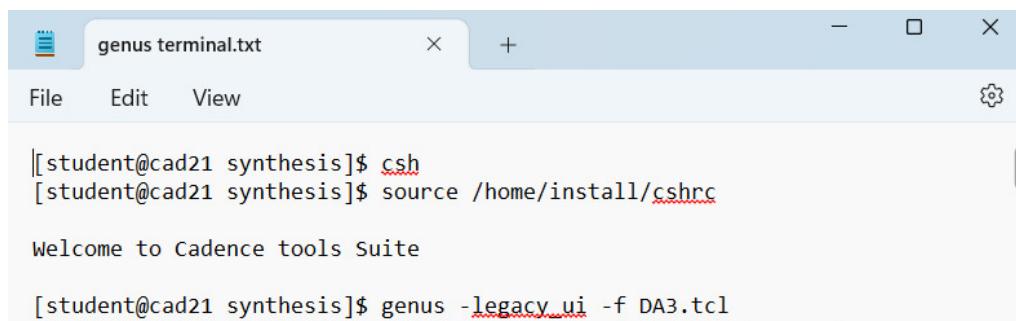
set_attribute syn_generic_effort high
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > DA3_netlist.v
write_sdc > DA3.sdc
gui_show

report_timing > DA3_timing.rep
report_area > DA3_area.rep
report_power > DA3_power.rep
```

5. Invoke the C shell and launch the Genus tool by entering the below commands.



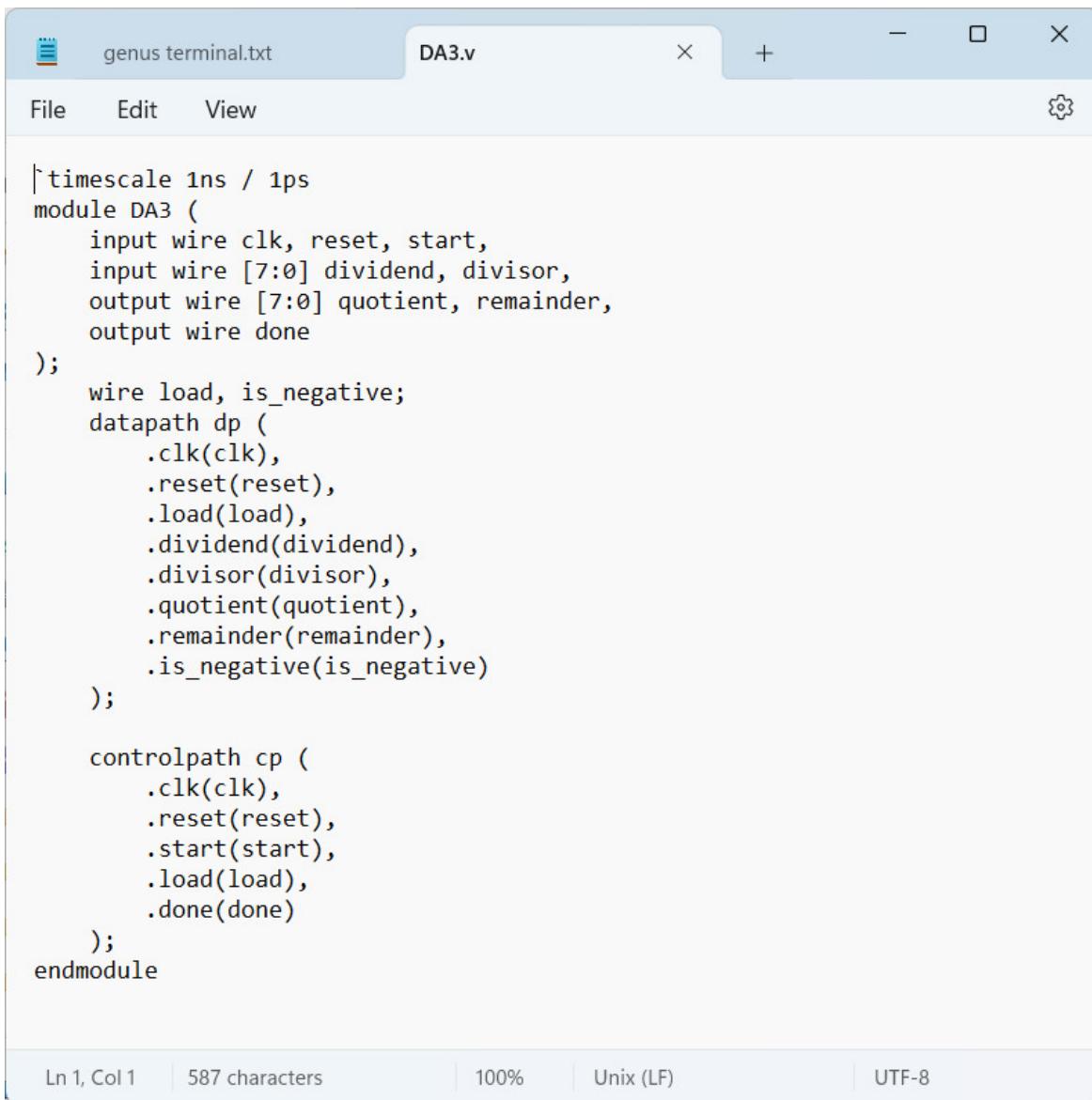
The screenshot shows a terminal window with the title 'genus terminal.txt'. The window displays a sequence of commands entered in the C shell to launch the Cadence tools suite and the Genus tool. The commands include 'csh', 'source /home/install/cshrc', and 'genus -legacy_ui -f DA3.tcl'.

```
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc
Welcome to Cadence tools Suite
[student@cad21 synthesis]$ genus -legacy_ui -f DA3.tcl
```

6. Execute the commands in the (.tcl file) by entering **source DA3.tcl** command in the command line window.
7. Check for the area, timing and power reports generated in the respective folder.
Also check the gate level netlist generated in the Genus synthesis solution window.
8. Now do the physical design using innovus.

Pre Synthesis Verilog Programs:

//Verilog Program of Top Module



The screenshot shows a terminal window titled "genus terminal.txt" with the file name "DA3.v" highlighted. The window contains Verilog code for a top module named DA3. The code defines a module with inputs clk, reset, start, dividend, divisor, and outputs quotient, remainder, done, and is_negative. It uses two data paths (dp) and one control path (cp) to handle the division process. The Verilog code is as follows:

```
timescale 1ns / 1ps
module DA3 (
    input wire clk, reset, start,
    input wire [7:0] dividend, divisor,
    output wire [7:0] quotient, remainder,
    output wire done
);
    wire load, is_negative;
    datapath dp (
        .clk(clk),
        .reset(reset),
        .load(load),
        .dividend(dividend),
        .divisor(divisor),
        .quotient(quotient),
        .remainder(remainder),
        .is_negative(is_negative)
    );
    controlpath cp (
        .clk(clk),
        .reset(reset),
        .start(start),
        .load(load),
        .done(done)
    );
endmodule
```

At the bottom of the terminal window, status information is displayed: Ln 1, Col 1 | 587 characters | 100% | Unix (LF) | UTF-8.

//Verilog Program of the Control Path

The screenshot shows a Verilog code editor window titled "DA3_ControlPath.v". The code defines a module named "controlpath" with inputs "clk", "reset", and "start", and outputs "load" and "done". It contains a register "count" and an always block that handles three cases: reset, start, and a general loop. The general loop increments "count" if it is less than 8, or sets "done" to 1 if it is 8 or more. The code ends with an endmodule statement. The status bar at the bottom indicates the code length (619 characters), zoom level (100%), line endings (Unix (LF)), and encoding (UTF-8).

```
`timescale 1ns / 1ps
module controlpath (
    input wire clk, reset, start,
    output reg load, done
);
    reg [3:0] count;

    always @(posedge clk or posedge reset) begin
        if (reset) begin
            load <= 0;
            done <= 0;
            count <= 0;
        end
        else if (start) begin
            load <= 1;
            done <= 0;
            count <= 0;
        end
        else begin
            load <= 0;
            if (count < 8) begin
                count <= count + 1;
            end
            else begin
                done <= 1;
            end
        end
    end
end
endmodule
```

Ln 1, Col 1 | 619 characters | 100% | Unix (LF) | UTF-8

//Verilog Program of the Data Path

The screenshot shows a code editor window with the title bar "DA3_Datopath.v". The menu bar includes "File", "Edit", "View", and a settings gear icon. The code itself is a Verilog module named "datapath" with the following structure:

```
timescale 1ns / 1ps
module datapath (
    input wire clk, reset, load,
    input wire [7:0] dividend, divisor,
    output reg [7:0] quotient, remainder,
    output wire is_negative
);

reg [15:0] A;
reg [7:0] Q;
reg [7:0] M;
assign is_negative = A[15];

always @(posedge clk or posedge reset) begin
    if (reset) begin
        A <= 0;
        Q <= 0;
        M <= 0;
        quotient <= 0;
        remainder <= 0;
    end
    else if (load) begin
        Q <= dividend;
        M <= divisor;
        A <= 0;
    end
end

always @(posedge clk) begin
    if (!reset && !load) begin
        A <= {A[14:0], Q[7]};
        Q <= {Q[6:0], 1'b0};

        A <= A - {M, 8'b0};

        if (is_negative) begin
            A <= A + {M, 8'b0};
            Q[0] <= 0;
        end
        else begin
            Q[0] <= 1;
        end
    end
end

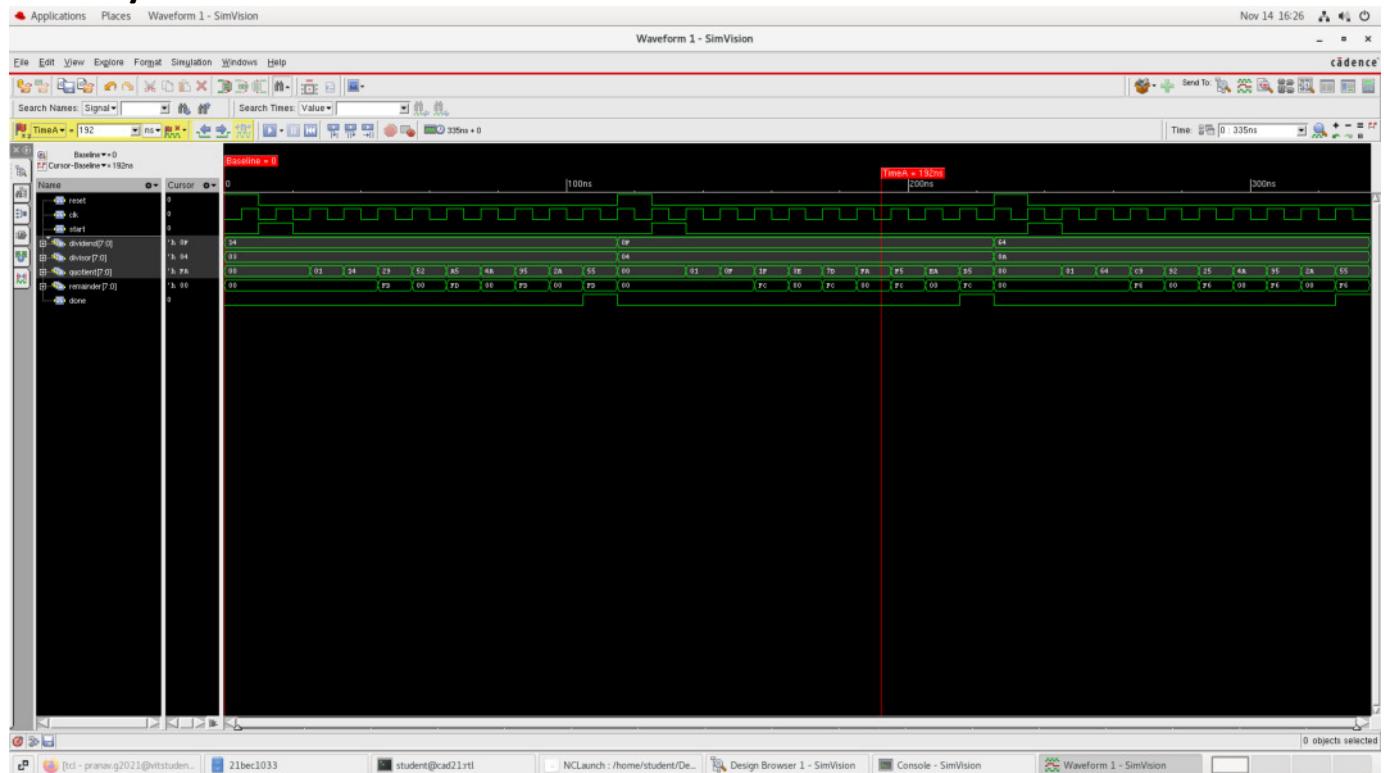
always @(posedge clk) begin
    quotient <= Q;
    remainder <= A[15:8];
end
endmodule
```

The status bar at the bottom indicates "Ln 1, Col 1 | 1,072 characters | 70% | Unix (LF) | UTF-8".

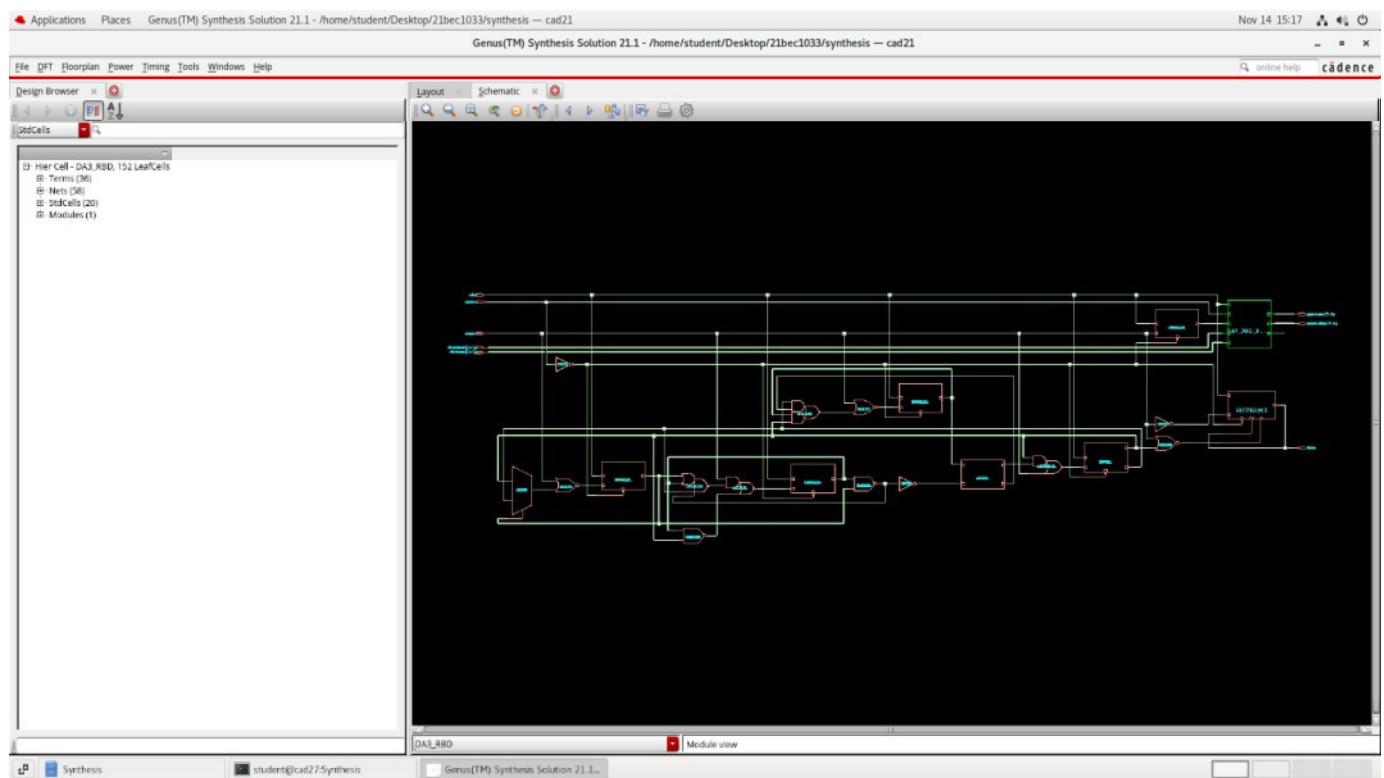
//Verilog Program of the Test Bench

<pre>DA3_tb.v</pre> <p>File Edit View</p> <pre>'timescale 1ns / 1ps module DA3_tb; reg clk, reset, start; reg [7:0] dividend, divisor; wire [7:0] quotient, remainder; wire done; DA3_netlist uut (.clk(clk), .reset(reset), .start(start), .dividend(dividend), .divisor(divisor), .quotient(quotient), .remainder(remainder), .done(done)); initial begin clk = 0; forever #5 clk = ~clk; end initial begin dividend = 8'd20; divisor = 8'd3; reset = 1; start = 0; #10; reset = 0; start = 1; #10; start = 0; wait(done); #10; \$display("Test Case 1: 20 / 3"); \$display("Quotient: %d, Remainder: %d", quotient, remainder); if (quotient == 6 && remainder == 2) \$display("PASS"); else \$display("FAIL"); dividend = 8'd15;</pre>	<pre>DA3_tb.v</pre> <p>File Edit View</p> <pre> \$display("Quotient: %d, Remainder: %d", quotient, remainder); if (quotient == 6 && remainder == 2) \$display("PASS"); else \$display("FAIL"); dividend = 8'd15; divisor = 8'd4; reset = 1; start = 0; #10; reset = 0; start = 1; #10; start = 0; wait(done); #10; \$display("Test Case 2: 15 / 4"); \$display("Quotient: %d, Remainder: %d", quotient, remainder); if (quotient == 3 && remainder == 3) \$display("PASS"); else \$display("FAIL"); dividend = 8'd100; divisor = 8'd10; reset = 1; start = 0; #10; reset = 0; start = 1; #10; start = 0; wait(done); #10; \$display("Test Case 3: 100 / 10"); \$display("Quotient: %d, Remainder: %d", quotient, remainder); if (quotient == 10 && remainder == 0) \$display("PASS"); else \$display("FAIL"); \$stop; end endmodule</pre> <p>Ln 1, Col 1 1,828 characters 90% Unix (LF)</p>
<p>Ln 1, Col 1 1,828 characters</p>	<p>80% Unix (LF) UTF-8</p>

Pre Synthesis Verification:



Gate level Netlist:



Observations:

Synthesis effort: High

a) Netlist :

```

// Generated by Cadence Genus(TM) Synthesis Solution 21.
// Generated on: Nov 14 2024 16:28:47 IST (Nov 14 2024 16:28:47)
// Verification Directory fv/restoring_division

module datapath(clk, reset, load, dividend, divisor, quotient, remainder, is_negative);
    input clk, reset, load;
    input [7:0] dividend, divisor;
    output [7:0] quotient, remainder;
    output is_negative;
    wire clk, reset, load;
    wire [7:0] dividend, divisor;
    wire [7:0] quotient, remainder;
    wire is_negative;
    wire [7:0] Q;
    wire [15:0] A;
    wire [7:0] M;
    wire n_0, n_1, n_2, n_4, n_5, n_6, n_7, n_8;
    wire n_10, n_11, n_12, n_13, n_14, n_15, n_16, n_17;
    wire n_18, n_19, n_20, n_21, n_22, n_23, n_24, n_25;
    wire n_26, n_27, n_28, n_29, n_30, n_31, n_32, n_33;
    wire n_34, n_35, n_36, n_37, n_38, n_39, n_40, n_41;
    wire n_42, n_43, n_44, n_45, n_46, n_47, n_48, n_49;
    wire n_50, n_51, n_52, n_53, n_54, n_55, n_56, n_57;
    wire n_58, n_59, n_60, n_61, n_62, n_63, n_64, n_65;
    wire n_66, n_67, n_68, n_69, n_70, n_71, n_72, n_73;
    wire n_74, n_75, n_76, n_77, n_78, n_79, n_80, n_81;
    wire n_82, n_83, n_84, n_85, n_86, n_87, n_88, n_89;
    wire n_125;
    assign A[14] = 1'b0;
    assign A[13] = 1'b0;
    assign A[10] = 1'b0;
    assign A[11] = 1'b0;
    assign A[12] = 1'b0;
    assign A[9] = 1'b0;
    assign A[8] = 1'b0;
    ...

```

Ln 12, Col 22 | 13,868 characters

```

assign remainder[1] = 1'b0;
assign remainder[2] = 1'b0;
assign remainder[3] = 1'b0;
assign remainder[4] = 1'b0;
assign remainder[5] = 1'b0;
assign remainder[6] = 1'b0;
assign remainder[7] = 1'b0;
assign quotient[0] = 1'b0;
assign quotient[1] = 1'b0;
assign quotient[2] = 1'b0;
assign quotient[3] = 1'b0;
assign quotient[4] = 1'b0;
assign quotient[5] = 1'b0;
assign quotient[6] = 1'b0;
assign quotient[7] = 1'b0;
INVXL g1142(.A (reset), .Y (n_89));
DFFQXL \remainder_reg[7]122 (.CK (clk), .D (is_negative), .Q
(remainder[7]));
DFFQXL \quotient_reg[1]108 (.CK (clk), .D (Q[1]), .Q
(quotient[1]));
DFFQXL \quotient_reg[3]110 (.CK (clk), .D (Q[3]), .Q
(quotient[3]));
DFFQXL \quotient_reg[7]114 (.CK (clk), .D (Q[7]), .Q
(quotient[7]));
DFFQXL \quotient_reg[0]107 (.CK (clk), .D (Q[0]), .Q
(quotient[0]));
DFFQXL \remainder_reg[0]115 (.CK (clk), .D (A[8]), .Q
(remainder[0]));
DFFQXL \quotient_reg[4]111 (.CK (clk), .D (Q[4]), .Q
(quotient[4]));
DFFQXL \remainder_reg[1]116 (.CK (clk), .D (A[9]), .Q
(remainder[1]));
DFFQXL \remainder_reg[4]119 (.CK (clk), .D (A[12]), .Q
(remainder[4]));
DFFQXL \quotient_reg[2]109 (.CK (clk), .D (Q[2]), .Q
(quotient[2]));
DFFQXL \quotient_reg[5]112 (.CK (clk), .D (Q[5]), .Q
(quotient[5]));

```

Ln 80, Col 69 | 3,205 characters

```

.C0 (n_86), .C1 (n_32), .Y (n_88);
DFFQX1 \A_reg[14]77 (.CK (clk), .D (n_87), .Q (A[14]));
OAI21XL g2123_5107(.A0 (n_76), .A1 (n_27), .B0 (n_84), .Y (n_87));
DFFQX1 \A_reg[13]76 (.CK (clk), .D (n_81), .Q (A[13]));
AOI21XL g2125_6260(.A0 (n_79), .A1 (n_25), .B0 (n_83), .Y (n_86));
AOI21XL g2126_4319(.A0 (n_25), .A1 (n_80), .B0 (n_82), .Y (n_85));
AOI22XL g2127_8428(.A0 (n_77), .A1 (n_27), .B0 (n_125), .B1 (A[14]),
.Y (n_84));
NOR2XL g2128_5526(.A (n_79), .B (n_25), .Y (n_83));
NOR2XL g2129_6783(.A (n_25), .B (n_80), .Y (n_82));
OAI21XL g2130_3680(.A0 (n_67), .A1 (n_28), .B0 (n_78), .Y (n_81));
DFFQX1 \A_reg[12]75 (.CK (clk), .D (n_73), .Q (A[12]));
OAI21XL g2132_1617(.A0 (n_72), .A1 (n_21), .B0 (n_12), .Y (n_80));
OAI21XL g2133_2802(.A0 (M[6]), .A1 (A[14]), .B0 (n_74), .Y (n_79));
AOI22XL g2134_1705(.A0 (n_68), .A1 (n_28), .B0 (n_125), .B1 (A[13]),
.Y (n_78));
OAI21XL g2135_5122(.A0 (n_32), .A1 (n_71), .B0 (n_75), .Y (n_77));
OA22XL g2136_8246(.A0 (n_30), .A1 (n_72), .B0 (n_70), .B1 (n_32),
.Y (n_76));
NAND2XL g2137_7098(.A (n_29), .B (n_72), .Y (n_75));
OAI2BB1XL g2138_6131(.A0N (A[14]), .A1N (M[6]), .B0 (n_71), .Y
(n_74));
OAI21XL g2139_1881(.A0 (n_60), .A1 (n_35), .B0 (n_69), .Y (n_73));
INVXL g2140 (.A (n_71), .Y (n_70));
DFFQX1 \A_reg[11]74 (.CK (clk), .D (n_65), .Q (A[11]));
AOI21XL g2142_5115(.A0 (n_23), .A1 (n_64), .B0 (n_10), .Y (n_72));
OAI21XL g2143_7482(.A0 (M[5]), .A1 (A[13]), .B0 (n_66), .Y (n_71));
AOI22XL g2144_4733(.A0 (n_61), .A1 (n_35), .B0 (n_125), .B1 (A[12]),
.Y (n_69));
OAI22XL g2145_6161(.A0 (n_64), .A1 (n_30), .B0 (n_32), .B1 (n_63),
.Y (n_68));
AOI22XL g2146_9315(.A0 (n_64), .A1 (n_29), .B0 (n_31), .B1 (n_63),
.Y (n_67));
OAI2BB1XL g2147_9945(.A0N (A[13]), .A1N (M[5]), .B0 (n_63), .Y
(n_66));
OAI21XL g2148_2883(.A0 (n_50), .A1 (n_26), .B0 (n_62), .Y (n_65));
DFFQX1 \A_reg[10]73 (.CK (clk), .D (n_56), .Q (A[10]));
OAI21XL g2150_2346(.A0 (n_55), .A1 (n_16), .B0 (n_19), .Y (n_64));
OAI21XL g2151_1666(.A0 (M[4]), .A1 (A[12]), .B0 (n_57), .Y (n_63));
AOI22XL g2152_7410(.A0 (n_51), .A1 (n_26), .B0 (n_125), .B1 (A[11]),
.Y (n_55));

```

Ln 41, Col 72 | 2,225 characters

90% Windows (CRLF) UTF-8

Ln 40, Col 19 | 1,949 characters

90% Windows (CRLF) UTF-8

DA3 Logic synthesis & Physical design of restoring binary division algorithm

Untitled Untitled

File Edit View

```

SDFFQX1 \_reg[5]96 (.CK (clk), .D (Q[4]), .SI (Q[5]), .SE (n_125),
.Q (Q[5]));
AOI22XL g2179_5115(.A0 (n_29), .A1 (n_17), .B0 (n_18), .B1 (n_31),
.Y (n_43));
OAI21XL g2180_7482(.A0 (n_125), .A1 (n_17), .B0 (n_36), .Y (n_42));
OAI2BB1XL g2181_4733(.A0N (A[10]), .A1N (M[2]), .B0 (n_39), .Y
(n_41));
OAI22XL g2182_6161(.A0 (n_30), .A1 (n_17), .B0 (n_18), .B1 (n_32),
.Y (n_40));
SDFFQX1 \_reg[6]97 (.CK (clk), .D (Q[5]), .SI (Q[6]), .SE (n_125),
.Q (Q[6]));
SDFFQX1 \_reg[7]98 (.CK (clk), .D (Q[6]), .SI (Q[7]), .SE (n_125),
.Q (Q[7]));
SDFFRHQX1 \_reg[7] (.RN (n_89), .CK (clk), .D (Q[7]), .SI
(dividend[7])), .SE (load), .Q (Q[7]));
SDFFRHQX1 \_reg[3] (.RN (n_89), .CK (clk), .D (Q[3]), .SI
(dividend[3])), .SE (load), .Q (Q[3]));
SDFFRHQX1 \_reg[4] (.RN (n_89), .CK (clk), .D (Q[4]), .SI
(dividend[4])), .SE (load), .Q (Q[4]));
SDFFRHQX1 \_reg[5] (.RN (n_89), .CK (clk), .D (Q[5]), .SI
(dividend[5])), .SE (load), .Q (Q[5]));
SDFFRHQX1 \_reg[1] (.RN (n_89), .CK (clk), .D (Q[1]), .SI
(dividend[1])), .SE (load), .Q (Q[1]));
SDFFRHQX1 \_reg[6] (.RN (n_89), .CK (clk), .D (Q[6]), .SI
(dividend[6])), .SE (load), .Q (Q[6]));
SDFFRHQX1 \_reg[0] (.RN (n_89), .CK (clk), .D (Q[0]), .SI
(dividend[0])), .SE (load), .Q (Q[0]));
SDFFRHQX1 \_reg[2] (.RN (n_89), .CK (clk), .D (Q[2]), .SI
(dividend[2])), .SE (load), .Q (Q[2]));
SDFFRHQX1 \_M_reg[0] (.RN (n_89), .CK (clk), .D (M[0]), .SI
(divisor[0])), .SE (load), .Q (M[0]));
CLKINVX1 g2194(A (n_37), .Y (n_38));
OAI2BB1XL g2195_9315(.A0N (M[0]), .A1N (n_8), .B0 (A[8]), .Y (n_36));
OAI21XL g2196_9945(.A0 (M[1]), .A1 (n_9), .B0 (n_24), .Y (n_39));
SDFFRHQX1 \_M_reg[7] (.RN (n_89), .CK (clk), .D (M[7]), .SI
(divisor[7])), .SE (load), .Q (M[7]));
AOI21XL g2198_2883(.A0 (n_22), .A1 (n_17), .B0 (n_13), .Y (n_37));
SDFFRHQX1 \_M_reg[5] (.RN (n_89), .CK (clk), .D (M[5]), .SI
(divisor[5])), .SE (load), .Q (M[5]));

```

Untitled

File Edit View

```

NAND2BXL g2(.AN (load), .B (n_89), .Y (n_125));
endmodule

module restoring_division(clk, reset, start, dividend, divisor,
quotient, remainder, done);
input clk, reset, start;
input [7:0] dividend, divisor;
output [7:0] quotient, remainder;
output done;
wire clk, reset, start;
wire [7:0] dividend, divisor;
wire [7:0] quotient, remainder;
wire done;
wire [3:0] cp_count;
wire is_negative, load, n_0, n_1, n_2, n_3, n_4, n_5;
wire n_6, n_7, n_8, n_9, n_10, n_11, n_12, n_13;
wire n_14, n_15;
datapath dp(.clk (clk), .reset (reset), .load (load), .dividend
(dividend), .divisor (divisor), .quotient (quotient), .remainder
(remainder), .is_negative (is_negative));
DFFRHQX1 cp_load_reg(.RN (n_1), .CK (clk), .D (start), .Q (load));
INVXL g55(.A (reset), .Y (n_1));
DFFRHQX1 \cp_count_reg[2] (.RN (n_1), .CK (clk), .D (n_15), .Q
(cp_count[2]));
NOR2XL g89_9315(.A (start), .B (n_13), .Y (n_15));
AOI2BB1XL g90_9945(.A0N (cp_count[3]), .A1N (n_11), .B0 (start), .Y
(n_14));
MXI2XL g91_2883(.A (n_12), .B (cp_count[2]), .S0 (cp_count[3]), .Y
(n_13));
DFFRHQX1 \cp_count_reg[1] (.RN (n_1), .CK (clk), .D (n_10), .Q
(cp_count[1]));
ADDHXL g93_2346(.A (cp_count[2]), .B (n_8), .C0 (n_11), .S (n_12));
AOI21XL g94_1666(.A0 (n_3), .A1 (n_9), .B0 (start), .Y (n_10));
DFFRHQX1 \cp_count_reg[0] (.RN (n_1), .CK (clk), .D (n_7), .Q
(cp_count[0]));
OAI21XL g96_7410(.A0 (cp_count[0]), .A1 (cp_count[1]), .B0 (n_0),
.C0 (n_4), .Y (n_9));
SDFFRHQX1 cp_done_reg(.RN (n_1), .CK (clk), .D (n_2), .SI (done), .SE
(n_5), .Q (done));
CLKINVX1 g98(.A (n_4), .Y (n_8));
NOR2XL g99_6417(.A (start), .B (n_6), .Y (n_7));
MXI2XL g100_5477(.A (n_0), .B (cp_count[3]), .S0 (cp_count[0]), .Y
(n_6));
NOR2XL g101_2398(.A (start), .B (cp_count[3]), .Y (n_5));
NAND2XL g102_5107(.A (cp_count[1]), .B (cp_count[3]), .Y (n_3));
NAND2XL g103_6260(.A (cp_count[1]), .B (cp_count[0]), .Y (n_4));
INVXL g104(.A (start), .Y (n_2));
DFFRX1 \cp_count_reg[3] (.RN (n_1), .CK (clk), .D (n_14), .Q
(cp_count[3]), .QN (n_0));
endmodule

```

Untitled

File Edit View

```


```

Ln 40, Col 45 2,025 characters

File Edit View

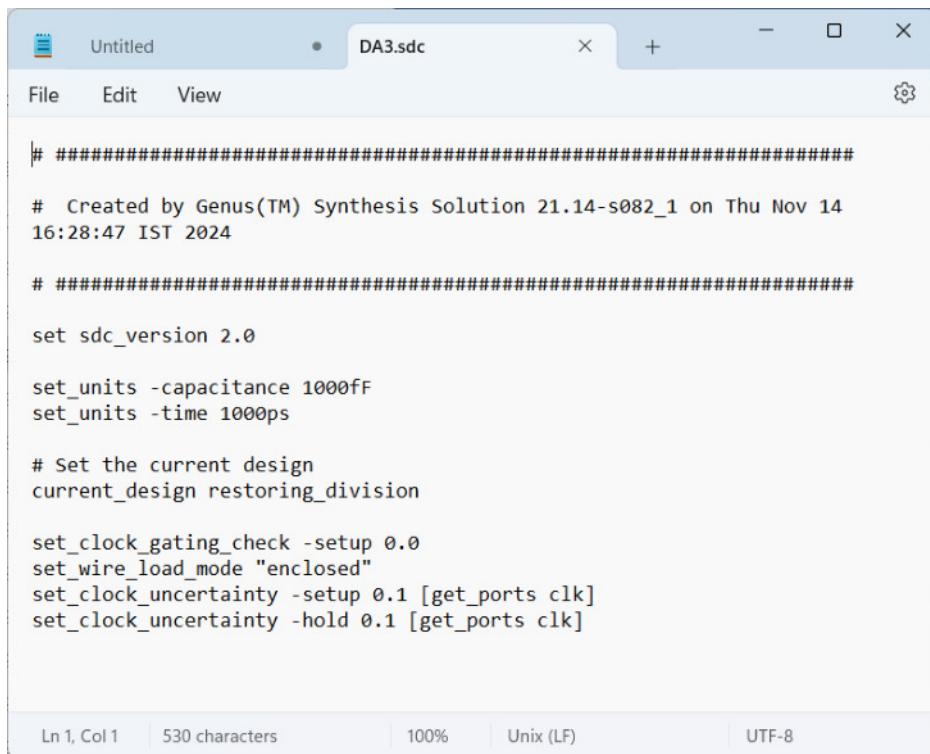
```


```

Ln 57, Col 10 2,391 characters

DA3 Logic synthesis & Physical design of restoring binary division algorithm

b) Constraint_created file



```
# #####
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Nov 14
# 16:28:47 IST 2024
#
# #####
set sdc_version 2.0

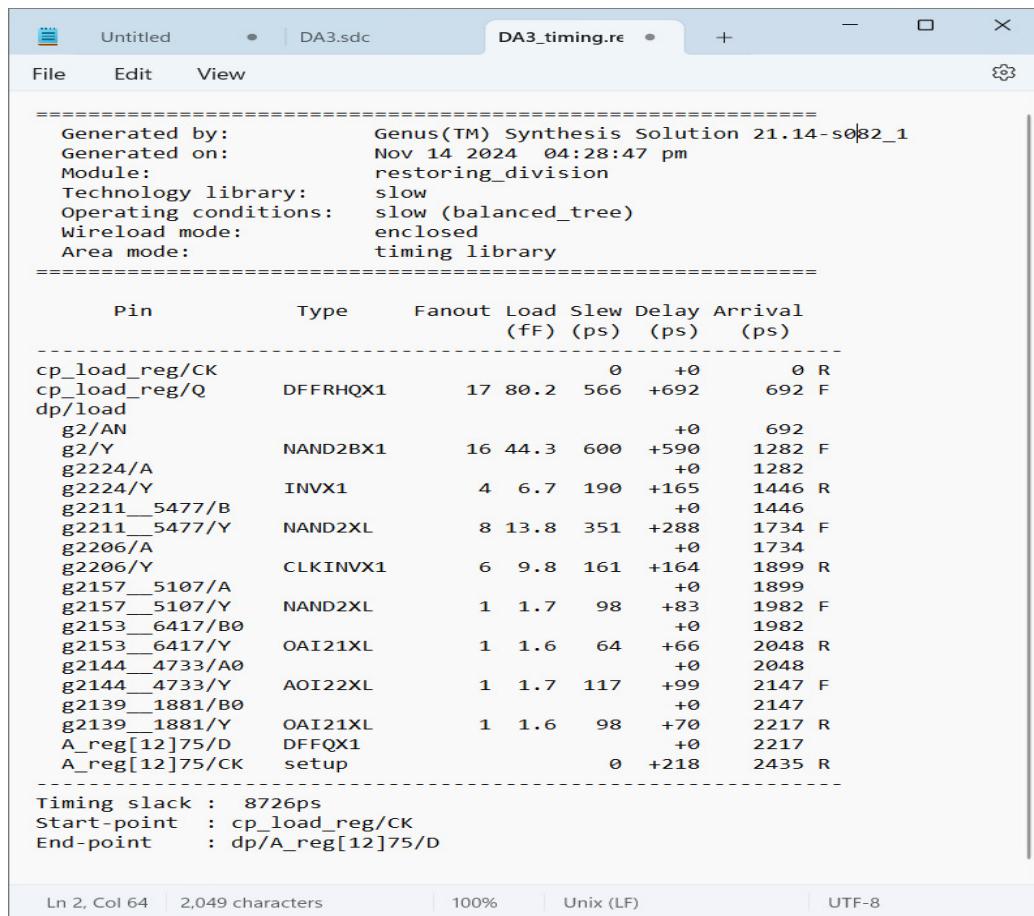
set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design restoring_division

set_clock_gating_check -setup 0.0
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.1 [get_ports clk]
set_clock_uncertainty -hold 0.1 [get_ports clk]
```

Ln 1, Col 1 | 530 characters | 100% | Unix (LF) | UTF-8

c) Timing_report file



```
=====
Generated by:          Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:         Nov 14 2024 04:28:47 pm
Module:               restoring_division
Technology library:   slow
Operating conditions: slow (balanced_tree)
Wireload mode:        enclosed
Area mode:            timing library
=====

Pin           Type      Fanout Load Slew Delay Arrival
             (fF)    (ps)  (ps)  (ps)  (ps)
-----
cp_load_reg/CK          DFFRHQX1       17 80.2   566 +692    0 R
cp_load_reg/Q          DFFRHQX1       17 80.2   566 +692   692 F
dp/load
g2/AN                  NAND2BX1       16 44.3   600 +590    +0   692
g2/Y                   INVX1          4   6.7    190 +165    +0   1282
g2224/A                INVX1          4   6.7    190 +165    +0   1282
g2224/Y                INVX1          4   6.7    190 +165    +0   1446
g2211_5477/B           NAND2XL        8  13.8   351 +288    +0   1446
g2211_5477/Y           NAND2XL        8  13.8   351 +288    +0   1734
g2206/A                CLKINVX1       6   9.8    161 +164    +0   1734
g2206/Y                CLKINVX1       6   9.8    161 +164    +0   1899
g2157_5107/A           NAND2XL        1   1.7    98  +83     +0   1899
g2157_5107/Y           NAND2XL        1   1.7    98  +83     +0   1982
g2153_6417/B0          OAI21XL        1   1.6    64  +66     +0   2048
g2153_6417/Y           OAI21XL        1   1.6    64  +66     +0   2048
g2144_4733/A0          AOI22XL        1   1.7   117  +99     +0   2147
g2144_4733/Y           AOI22XL        1   1.7   117  +99     +0   2147
g2139_1881/B0          OAI21XL        1   1.6    98  +70     +0   2217
g2139_1881/Y           OAI21XL        1   1.6    98  +70     +0   2217
A_reg[12]75/D          DFFQX1         0   0.0     0  +218    +0   2435
A_reg[12]75/CK          setup          0   0.0     0  +218    +0   2435

Timing slack : 8726ps
Start-point  : cp_load_reg/CK
End-point    : dp/A_reg[12]75/D
```

Ln 2, Col 64 | 2,049 characters | 100% | Unix (LF) | UTF-8

DA3 Logic synthesis & Physical design of restoring binary division algorithm

d) Area_report file

DA3_area.rep

File Edit View

```
=====
Generated by:          Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:         Nov 14 2024 04:28:47 pm
Module:               restoring_division
Technology library:   slow
Operating conditions: slow (balanced_tree)
Wireload mode:        enclosed
Area mode:            timing library
=====
```

Instance	Module	Cell Count	Cell Area	Net Area	Total Area
restoring_division		157	1514.557	0.000	1514.557
<none> (D)	dp	datopath	137	1323.818	0.000
<none> (D)					1323.818

(D) = wireload is default in technology library

Ln 1, Col 1 | 840 characters | 100% | Unix (LF) | UTF-8

e) Power_report file

DA3_area.rep DA3_power.rep

File Edit View

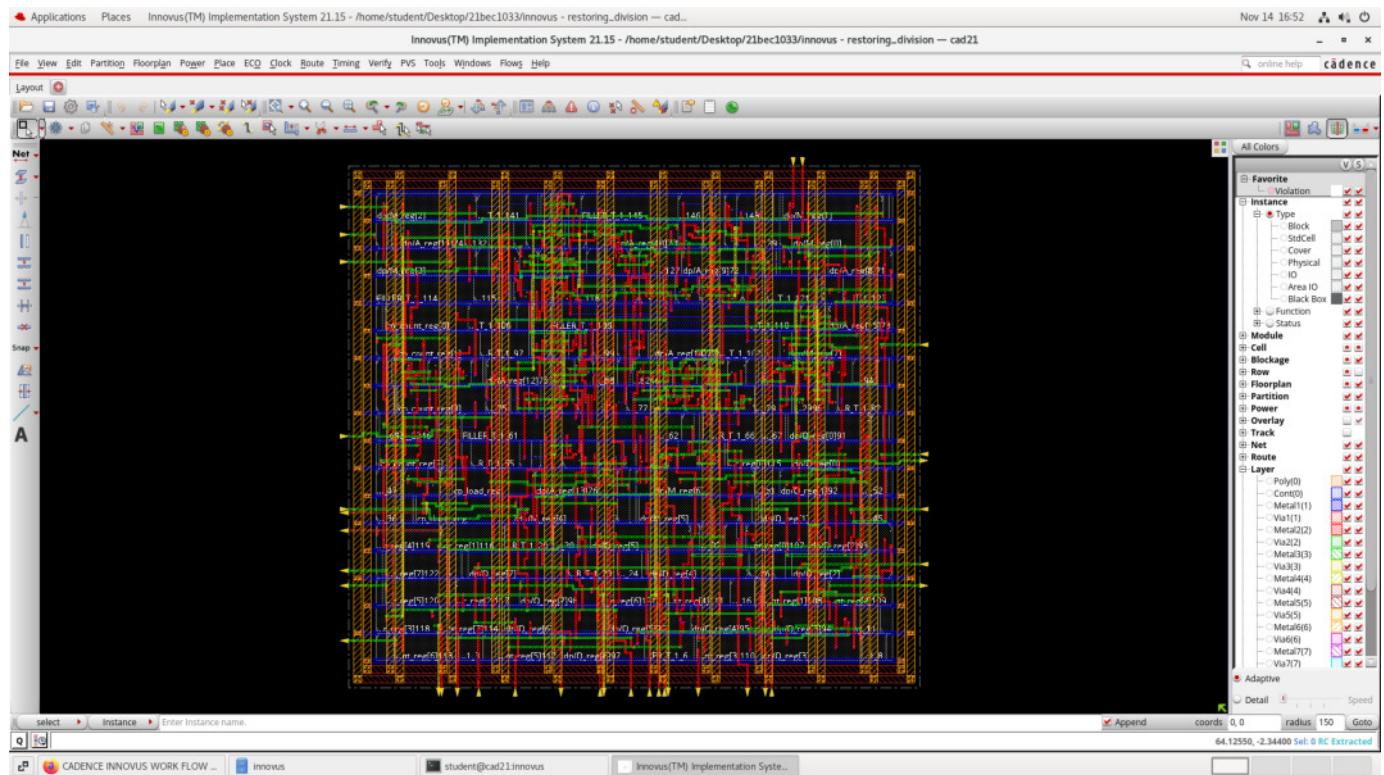
```
Instance: /restoring_division
Power Unit: W
PDB Frames: /stim#0/frame#0
```

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	6.47760e-06	1.83460e-05	2.14174e-06	2.69654e-05	80.87%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	1.44301e-06	3.27454e-06	1.66125e-06	6.37880e-06	19.13%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	7.92061e-06	2.16206e-05	3.80299e-06	3.33442e-05	100.00%
Percentage	23.75%	64.84%	11.41%	100.00%	100.00%

Ln 1, Col 1 | 1,212 characters | 100% | Unix (LF) | UTF-8

DA3 Logic synthesis & Physical design of restoring binary division algorithm

Physical design of the Multiplier:



DA3 Logic synthesis & Physical design of restoring binary division algorithm

Genus Terminal:

```
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -legacy_ui -f DA3.tcl
2024/11/14 16:28:39 WARNING This OS does not appear to be a Cadence
supported Linux configuration.
2024/11/14 16:28:39 For more info, please run CheckSysConf in
<cdsRoot/tools.lnx86/bin/checkSysConf <productId>
TMPDIR is being set to /tmp/genus_temp_34291_cad21_student_NQH68u
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved
worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a
trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[16:28:39.095721] Configured Lic search path (21.01-s002): 5280@cadence

Version: 21.14-s082_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files DA3.tcl
Date:    Thu Nov 14 16:28:39 2024
Host:    cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64)
(12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700
25600KB) (32402340KB)
PID:     34291
OS:      Red Hat Enterprise Linux release 8.8 (Ootpa)

[16:28:40.025611] Periodic Lic check successful
[16:28:40.025619] Feature usage summary:
[16:28:40.025619] Genus_Synthesis
Checking out license: Genus_Synthesis

*****
*****
```



```
***** Loading tool scripts...
***** Finished loading tool scripts (3 seconds elapsed).

#@ Processing -files option
@genus 1> source DA3.tcl
Setting attribute of root '/': 'init_lib_search_path' =
/home/student/Desktop/21bec1033
Setting attribute of root '/': 'init_hdl_search_path' =
/home/student/Desktop/21bec1033/rtl

Threads Configured:3

Message Summary for Library slow.lib:
*****
Missing a function attribute in the output pin definition. [LBR-518]: 1
Missing library level attribute. [LBR-516]: 1
*****
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Info      : Created nominal operating condition. [LBR-412]
            : Operating condition '_nominal_' was created for the PVT values
(1.000000, 0.900000, 125.000000) in library 'slow.lib'.
            : The nominal operating condition is represented, either by the
nominal PVT values specified in the library source (via
nom_process,nom_voltage and nom_temperature respectively), or by the
default PVT values (1.0,1.0,1.0).
            Setting attribute of root '/': 'library' = slow.lib
            Library has 324 usable logic and 128 usable sequential lib-cells.
Info      : Elaborating Design. [ELAB-1]
            : Elaborating top-level block 'restoring_division' from file
'/home/student/Desktop/21bec1033/rtl/DA3.v'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[0]' in module 'datapath'.
            : This may cause simulation mismatches between the original and
synthesized designs.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[1]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[2]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[3]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[4]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[5]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[6]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[7]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[8]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[9]' in module 'datapath'.
Warning   : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[10]' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[11]' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[12]' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[13]' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'A[14]' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'is_negative' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'Q[0]' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'Q[1]' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'Q[2]' in module 'datapath'.
Warning  : Signal or variable has multiple drivers. [CDFG2G-622]
            : 'Q[3]' in module 'datapath'.
Warning  : Maximum message print count reached. [MESG-11]
            : Maximum print count of '20' reached for message 'CDFG2G-622'.
Info      : Done Elaborating Design. [ELAB-3]
            : Done elaborating 'restoring_division'.
Checking for analog nets...
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
: An object of type 'clock' named '' could not be found.
Error  : Could not interpret SDC command. [SDC-202] [read_sdc]
        : The 'read_sdc' command encountered an error while processing
this command on line '3' of the SDC file 'DA3_top.g':
set_clock_transition -fall 0.1 [get_clocks 'clk'].
Warning : Could not find requested search value. [SDC-208] [get_clocks]
        : The 'get_clocks' command on line '5' of the SDC file
'DA3_top.g' cannot find any clocks named 'clk'
Error  : Invalid SDC command option combination. [SDC-204]
[set_io_delay]
        : The set_io_delay command does not accept any invalid clock
        : This option is not valid for the indicated SDC command. Check
the SDC command and contact Cadence customer support if you believe this
option combination should be supported.
Error  : Could not interpret SDC command. [SDC-202] [read_sdc]
        : The 'read_sdc' command encountered an error while processing
this command on line '5' of the SDC file 'DA3_top.g': set_input_delay -
max 1.0 [get_ports 'clk'] -clock [get_clocks 'clk'].
Warning : Could not find requested search value. [SDC-208] [get_clocks]
        : The 'get_clocks' command on line '6' of the SDC file
'DA3_top.g' cannot find any clocks named 'clk'
Error  : Could not interpret SDC command. [SDC-202] [read_sdc]
        : The 'read_sdc' command encountered an error while processing
this command on line '6' of the SDC file 'DA3_top.g': set_input_delay -
max 1.0 [get_ports 'reset'] -clock [get_clocks 'clk'].
Error  : Could not interpret SDC command. [SDC-202] [read_sdc]
        : The TCL interpreter encountered the following error while
processing line '7' of the SDC file 'DA3_top.g': extra characters after
close-quote.
Error  : Could not interpret SDC command. [SDC-202] [read_sdc]
        : The TCL interpreter encountered the following error while
processing line '8' of the SDC file 'DA3_top.g': extra characters after
close-quote.
Statistics for commands executed by read_sdc:
  "create_clock"           - successful      0 , failed      1 (runtime
0.00)
  "get_clocks"             - successful      0 , failed      4 (runtime
0.00)
  "get_ports"              - successful      4 , failed      0 (runtime
0.00)
  "set_clock_transition"   - successful      0 , failed      2 (runtime
0.00)
  "set_clock_uncertainty"  - successful      1 , failed      0 (runtime
0.00)
  "set_input_delay"        - successful      0 , failed      2 (runtime
0.00)
Warning : Total failed commands during read_sdc are 9
Warning : One or more commands failed when these constraints were
applied. [SDC-209]
        : The 'read_sdc' command encountered a problem while processing
commands.
        : You can examine the failed commands or save them to a file by
querying the Tcl variable $::dc::sdc_failed_commands.
read_sdc completed in 00:00:00 (hh:mm:ss)
Setting attribute of root '/': 'syn_generic_effort' = high
Setting attribute of root '/': 'syn_map_effort' = high
Setting attribute of root '/': 'syn_opt_effort' = high

Stage: pre_early_cg
-----
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_elab
-----
| Trick           | Accepts | Rejects | Runtime (ms) |
-----
| ume_constant_bmux |      0 |      0 |      0.00 |
-----
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: restoring_division, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: restoring_division, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
-----
| Transform       | Accepts | Rejects | Runtime (ms) |
-----
| hlo_clip_mux_input |      0 |      0 |      0.00 |
| hlo_clip          |      0 |      0 |      0.00 |
-----
Error   : An invalid option was specified. [TUI-204] [create_clock]
          : An option named '-waveform{0}' could not be found.
          : Run 'command_name -help' to check all valid options. To correct
the option and rerun the command.
Error   : Could not interpret SDC command. [SDC-202] [read_sdc]
          : The 'read_sdc' command encountered an error while processing
this command on line '1' of the SDC file 'DA3_top.g': create_clock -name
clk -period 10 -waveform{0 5} [get_ports 'clk'].
          : The 'read_sdc' command encountered a problem while trying to
evaluate an SDC command. This SDC command will be added to the Tcl
variable $::dc::sdc_failed_commands.
Warning : Could not find requested search value. [SDC-208] [get_clocks]
          : The 'get_clocks' command on line '2' of the SDC file
'DA3_top.g' cannot find any clocks named 'clk'
          : Use get_* commands to find the objects along with a wild card
entry in the name of the object to check if the object is existing with
different naming style.
Error   : A required object parameter could not be found. [TUI-61]
[parse_options]
          : An object of type 'clock' named '' could not be found.
          : Check to make sure that the object exists and is of the correct
type. The 'what_is' command can be used to determine the type of an
object.
Error   : Could not interpret SDC command. [SDC-202] [read_sdc]
          : The 'read_sdc' command encountered an error while processing
this command on line '2' of the SDC file 'DA3_top.g':
set_clock_transition -rise 0.1 [get_clocks 'clk'].
Warning : Could not find requested search value. [SDC-208] [get_clocks]
          : The 'get_clocks' command on line '3' of the SDC file
'DA3_top.g' cannot find any clocks named 'clk'
Error   : A required object parameter could not be found. [TUI-61]
[parse_options]
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

| Transform | Accepts | Rejects | Runtime (ms) |
-----
##Generic Timing Info for library domain: _default_ typical gate delay:
127.0 ps std_slew: 15.5 ps std_load: 7.0 fF
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup,
startdef: restoring_division, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime:
0.000s)

Stage: pre_to_gen_setup
-----
| Transform | Accepts | Rejects | Runtime (ms) |
-----
| hlo_mux_reorder | 0 | 0 | 0.00 |
-----
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[0]'.
            : To prevent this optimization, set the
'optimize_constant_0_flops' root attribute to 'false' or
'optimize_constant_0_seq' instance attribute to 'false'. You can also see
the complete list of deleted sequential with command "report sequential -
deleted" (on Reason "constant0").
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[1]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[2]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[3]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[4]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[5]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[6]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[7]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[8]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[9]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[10]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[11]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[12]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[13]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[14]'.
Info      : Replacing a flip-flop with a logic constant 0. [GLO-12]
            : The instance is 'dp/A_reg[15]'.
Info      : Deleting instances not driving any primary outputs. [GLO-34]
            : Deleting 16 sequential instances.
            : Optimizations such as constant propagation or redundancy
removal could change the connections so a hierarchical instance does not
drive any primary outputs anymore. To see the list of deleted
hierarchical instances, set the 'information_level' attribute to 2 or
above. If the message is truncated set the message attribute 'truncate'

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Starting decode mux sandwich optimization [v2.0] (stage: pre_rtlopt,
startdef: restoring_division, recur: true)
Completed decode mux sandwich optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting decode mux optimization [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed decode mux optimization (accepts: 0, rejects: 0, runtime:
0.000s)
Starting chop wide muxes [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed chop wide muxes (accepts: 0, rejects: 0, runtime: 0.000s)
Starting common data mux cascade opt [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed common data mux cascade opt (accepts: 0, rejects: 0, runtime:
0.000s)
Starting mux input consolidation [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed mux input consolidation (accepts: 0, rejects: 0, runtime:
0.000s)
Starting constant-data mux optimization [v1.0] (stage: pre_rtlopt,
startdef: restoring_division, recur: true)
Completed constant-data mux optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting chain-to-tree inequality transform [v2.0] (stage: pre_rtlopt,
startdef: restoring_division, recur: true)
Completed chain-to-tree inequality transform (accepts: 0, rejects: 0,
runtime: 0.001s)
Starting reconvergence optimization [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed reconvergence optimization (accepts: 0, rejects: 0, runtime:
0.000s)
Starting logic restructure optimization [v1.0] (stage: pre_rtlopt,
startdef: restoring_division, recur: true)
Completed logic restructure optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting common select mux optimization [v1.0] (stage: pre_rtlopt,
startdef: restoring_division, recur: true)
Completed common select mux optimization (accepts: 0, rejects: 0,
runtime: 0.000s)
Starting identity transform [v3.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed identity transform (accepts: 0, rejects: 0, runtime: 0.000s)
Starting reduce operator chain [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed reduce operator chain (accepts: 0, rejects: 0, runtime: 0.000s)
Starting common data mux cascade opt [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed common data mux cascade opt (accepts: 0, rejects: 0, runtime:
0.000s)
Starting mux input consolidation [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed mux input consolidation (accepts: 0, rejects: 0, runtime:
0.000s)
Starting optimize datapath elements [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed optimize datapath elements (accepts: 0, rejects: 0, runtime:
0.000s)
Starting datapath recasting [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed datapath recasting (accepts: 0, rejects: 0, runtime: 0.000s)
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
to false to see the complete list. To prevent this optimization, set the
'delete_unloaded_insts' root/subdesign attribute to 'false' or 'preserve'
instance attribute to 'true'.
Info      : Synthesizing. [SYNTH-1]
            : Synthesizing 'restoring_division' to generic gates using 'high'
effort.
PBS_Generic-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Start' being created for table 'pbs_debug'

    Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
    | Memory   | Stage
    -----+-----+-----+-----+
    00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:44
(Nov14) | 242.2 MB | PBS_Generic-Start
    -----+-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
TNS Restructuring config: no_value at stage: generic applied.
Info      : Partition Based Synthesis execution skipped. [PHYS-752]
            : Design size is less than the partition size '100000' for
distributed generic optimization to kick in.
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup,
startdef: restoring_division, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime:
0.001s)

Stage: pre_to_gen_setup
-----+
| Transform      | Accepts | Rejects | Runtime (ms) |
-----+
| hlo_mux_reorder |      0 |      0 |       1.00 |
-----+
Starting mux data reorder optimization [v1.0] (stage: post_to_gen_setup,
startdef: restoring_division, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime:
0.000s)

Stage: post_to_gen_setup
-----+
| Transform      | Accepts | Rejects | Runtime (ms) |
-----+
| hlo_mux_reorder |      0 |      0 |       0.00 |
-----+
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: pre_hlo_rtlopt
-----+
| Trick | Accepts | Rejects | Runtime (ms) |
-----+
Starting infer macro optimization [v1.0] (stage: pre_rtlopt, startdef:
restoring_division, recur: true)
Completed infer macro optimization (accepts: 0, rejects: 2, runtime:
0.001s)
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

Starting clip mux common data inputs [v1.0] (stage: pre_rtlopt, startdef: restoring_division, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: pre_rtlopt, startdef: restoring_division, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_rtlopt
-----
| Transform | Accepts | Rejects | Runtime (ms) |
|-----|
| hlo_infer_macro | 0 | 2 | 1.00 |
| hlo_decode_mux_sandwich | 0 | 0 | 0.00 |
| hlo_mux_decode | 0 | 0 | 0.00 |
| hlo_chop_mux | 0 | 0 | 0.00 |
| hlo_mux_cascade_opt | 0 | 0 | 0.00 |
| hlo_mux_consolidation | 0 | 0 | 0.00 |
| hlo_constant_mux_opt | 0 | 0 | 0.00 |
| hlo_inequality_transform | 0 | 0 | 1.00 |
| hlo_reconv_opt | 0 | 0 | 0.00 |
| hlo_restructure | 0 | 0 | 0.00 |
| hlo_common_select_muxopto | 0 | 0 | 0.00 |
| hlo_identity_transform | 0 | 0 | 0.00 |
| hlo_reduce_operator_chain | 0 | 0 | 0.00 |
| hlo_mux_cascade_opt | 0 | 0 | 0.00 |
| hlo_mux_consolidation | 0 | 0 | 0.00 |
| hlo_optimize_datapath | 0 | 0 | 0.00 |
| hlo_datapath_recast | 0 | 0 | 0.00 |
| hlo_clip_mux_input | 0 | 0 | 0.00 |
| hlo_clip | 0 | 0 | 0.00 |
|-----|
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_hlo_rtlopt
-----
| Trick | Accepts | Rejects | Runtime (ms) |
|-----|
| ume_runtime | 0 | 0 | 0.00 |
|-----|
Number of big hc bmuxes before = 0
Info : Pre-processed datapath logic. [DPOPT-6]
      : No pre-processing optimizations applied to datapath logic in 'restoring_division'.
Info : Optimizing datapath logic. [DPOPT-1]
      : Optimizing datapath logic in 'restoring_division'.
Info : Implementing datapath configurations. [DPOPT-3]
      : Implementing datapath configurations for 'CDN_DP_region_1_0'
CSAGen Prep Share:0 Re-Write:0 Speculation: 0
MaxCSA: Successfully built Maximal CSA Expression Expr0
Info : Accepted resource sharing opportunity. [RTLOPT-30]
      : Merged the following sets of instances in 'CDN_DP_region_1_0_c7' in datapath':
          (final_adder_SUB_TC_OP_3, final_adder_ADD_TC_OP_1)
          (csa_tree_SUB_TC_OP_3, csa_tree_ADD_TC_OP_1)

CDN_DP_region_1_0 level = 0 loads = 0 drivers = 0

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
Smallest config area : 1361810415. Fastest config wns; 0
##>+-----+
-----+
##>Summary table of configs (Best config is CDN_DP_region_1_0_c6)
##>+-----+
-----+
##>          0           1           2
3           4           5           6
7
##>+-----+
-----+
##>          Area      1377068795      1361810415      1361810415
1361810415      1361810415      1361810415      1361810415
1831005600
##>          WNS      +214748364.70      +214748364.70      +214748364.70
+214748364.70      +214748364.70      +214748364.70      +214748364.70
+214748364.70
##>          TNS          0           0           0           0
0           0           0           0           0
0
##>          Num Rewrite      0           1           1           1
1           1           1           1
##>          Num Factor      0           0           0           0
0           0           0           0
0
##>          Num Share      0           0           0           0
0           0           0           0
2
##>          Num CmultCse      0           0           0           0
0           0           0           0
0
##>          Num Downsize      0           0           0           0
0           0           0           0
0
##>          Num Speculate      0           0           0           0
0           0           0           0
0
##>          Runtime(s)      0           0           0           0
0           0           0           0
0
+-----+
-----+
##>
##>
##>+-----+
-----+
##>Optimization Step DEBUG Table for config CDN_DP_region_1_0_c6
##>
##>          Step          Area   ( % Chg)
WNS (Change)      TNS (Change)      Runtime (s)      Comment

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
CDN_DP_region_1_0_c0 in datapath: area: 1377068795 ,dp = 2 mux = 2 sg =
slow          worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
tns: 0  tns_per_endp:  -1.0000  norm_tns_per_endp:  -1.0000
tns_sense_max:  -1.0000  tns_sense_avg:  -1.0000  tns_sense_num: -1
skipped
CDN_DP_region_1_0_c1 in datapath: area: 1361810415 ,dp = 2 mux = 1 sg =
fast          worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
tns: 0  tns_per_endp:  -1.0000  norm_tns_per_endp:  -1.0000
tns_sense_max:  -1.0000  tns_sense_avg:  -1.0000  tns_sense_num: -1
is current best
CDN_DP_region_1_0_c2 in datapath: area: 1361810415 ,dp = 2 mux = 1 sg =
very_slow      worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
tns: 0  tns_per_endp:  -1.0000  norm_tns_per_endp:  -1.0000
tns_sense_max:  -1.0000  tns_sense_avg:  -1.0000  tns_sense_num: -1
is current best
CDN_DP_region_1_0_c3 in datapath: area: 1361810415 ,dp = 2 mux = 1 sg =
very_fast       worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
tns: 0  tns_per_endp:  -1.0000  norm_tns_per_endp:  -1.0000
tns_sense_max:  -1.0000  tns_sense_avg:  -1.0000  tns_sense_num: -1
is current best
CDN_DP_region_1_0_c4 in datapath: area: 1361810415 ,dp = 2 mux = 1 sg =
very_fast       worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
tns: 0  tns_per_endp:  -1.0000  norm_tns_per_endp:  -1.0000
tns_sense_max:  -1.0000  tns_sense_avg:  -1.0000  tns_sense_num: -1
is current best
CDN_DP_region_1_0_c5 in datapath: area: 1361810415 ,dp = 2 mux = 1 sg =
very_fast       worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
tns: 0  tns_per_endp:  -1.0000  norm_tns_per_endp:  -1.0000
tns_sense_max:  -1.0000  tns_sense_avg:  -1.0000  tns_sense_num: -1
is current best
CDN_DP_region_1_0_c6 in datapath: area: 1361810415 ,dp = 2 mux = 1 sg =
very_fast       worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
tns: 0  tns_per_endp:  -1.0000  norm_tns_per_endp:  -1.0000
tns_sense_max:  -1.0000  tns_sense_avg:  -1.0000  tns_sense_num: -1
is current best
CDN_DP_region_1_0_c7 in datapath: area: 1831005600 ,dp = 3 mux = 3 sg =
very_fast       worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
tns: 0  tns_per_endp:  -1.0000  norm_tns_per_endp:  -1.0000
tns_sense_max:  -1.0000  tns_sense_avg:  -1.0000  tns_sense_num: -1

Best config: CDN_DP_region_1_0_c6 in datapath: area: 1361810415 ,dp = 2
mux = 1 sg = very_fast      worst_clk_period: -1.0000
wns: 0  norm_wns:  -1.0000
fail_endp: -1
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

##>+-----
-----+
##>>createMaxCarrySave           START      1377068795 (      )
214748364.70 (      )          0 (      )      1377068795 ( +0.00)
##> datapath_rewrite_one_def   START      1377068795 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      1377068795 ( +0.00)
##> fast_cse_elim             START      1377068795 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      1377068795 ( +0.00)
##>                               END       1377068795 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> fast_cse_elim             START      1377068795 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      1377068795 ( +0.00)
##>                               END       1377068795 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> rewrite                   START      1377068795 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      (a,csaa)
dissolve_1bit_const_2x1mux_from --> dissolve_1bit_const_2x1mux_to
##>                               END       1365625010 ( -0.83)
214748364.70 ( +0.00)        0 (      0)      0
##> fast_cse_elim             START      1365625010 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      1361810415 ( -0.28)
##>                               END       1361810415 ( -1.11)
214748364.70 ( +0.00)        0 (      0)      0
##>                               END       1361810415 ( +0.00)
##> dpopt_share_one_def       START      1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      1361810415 ( +0.00)
##>                               END       1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> csa_opto                  START      1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      1361810415 ( +0.00)
##>                               END       1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> canonicalize_by_names    START      1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      1361810415 ( +0.00)
##>                               END       1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> datapath_rewrite_post_csa_one_
214748364.70 ( +0.00)        0 (      0)      1361810415 ( +0.00)
##>                               END       1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> datapath_csa_factoring_one_gde
214748364.70 ( +0.00)        0 (      0)      1361810415 ( +0.00)
##>                               END       1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> dpopt_share_one_def       START      1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      1361810415 ( +0.00)
##>                               END       1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> datapath_rewrite_post_share
214748364.70 ( +0.00)        0 (      0)      1361810415 ( +0.00)
##>                               END       1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0
##> dp_combine_const_mult_with_com
214748364.70 ( +0.00)        0 (      0)      1361810415 ( +0.00)
##>                               END       1361810415 ( +0.00)
214748364.70 ( +0.00)        0 (      0)      0

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
CSAGen Prep Share:0 Re-Write:0 Speculation: 0
MaxCSA: Successfully built Maximal CSA Expression Expr1
CDN_DP_region_0_0 level = 0 loads = 0 drivers = 0
CDN_DP_region_0_0_c0 in controlpath: area: 64848115 ,dp = 2 mux = 0 sg =
slow      worst_clk_period: -1.0000
wns: 0 norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
skipped
CDN_DP_region_0_0_c1 in controlpath: area: 45775140 ,dp = 2 mux = 0 sg =
fast      worst_clk_period: -1.0000
wns: 0 norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
is current best
CDN_DP_region_0_0_c2 in controlpath: area: 45775140 ,dp = 2 mux = 0 sg =
very_slow    worst_clk_period: -1.0000
wns: 0 norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
is current best
CDN_DP_region_0_0_c3 in controlpath: area: 45775140 ,dp = 2 mux = 0 sg =
very_fast     worst_clk_period: -1.0000
wns: 0 norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
is current best
CDN_DP_region_0_0_c4 in controlpath: area: 45775140 ,dp = 2 mux = 0 sg =
very_fast     worst_clk_period: -1.0000
wns: 0 norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
is current best
CDN_DP_region_0_0_c5 in controlpath: area: 45775140 ,dp = 2 mux = 0 sg =
very_fast     worst_clk_period: -1.0000
wns: 0 norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
is current best
CDN_DP_region_0_0_c6 in controlpath: area: 45775140 ,dp = 2 mux = 0 sg =
very_fast     worst_clk_period: -1.0000
wns: 0 norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
is current best
CDN_DP_region_0_0_c7 in controlpath: area: 64848115 ,dp = 2 mux = 0 sg =
very_fast     worst_clk_period: -1.0000
wns: 0 norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000 norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000 tns_sense_avg: -1.0000 tns_sense_num: -1
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

##>dp_operator_level_decomposition      START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>selective_flatten_dp_config        START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>createMaxCarrySave                START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>datapath_rewrite_one_def          START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>fast_cse_elim                    START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>fast_cse_elim                    START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>dpopt_share_one_def              START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>csa_opto                         START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>context_based_simplify            START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>group_csa_final_adder_dp         START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>dpopt_flatten_critical_muxes_i   START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>create_score                      START          1361810415 ( +0.00)
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>                                         END          0
214748364.70 ( +0.00)                 0 ( 0)           1361810415 ( +0.00)
##>+-----+
-----+
Committed config: CDN_DP_region_1_0_c6
Info    : Done implementing datapath configurations. [DPOPT-4]
         : Selected 'very_fast' configuration 6 for module
'CDN_DP_region_1_0'.
Optimizations applied to 'very_fast' configuration:
         rewriting(1), factoring(0), sharing(0), cmultcse(0),
downsizing(0), speculation(0)
Info    : Implementing datapath configurations. [DPOPT-3]
         : Implementing datapath configurations for 'CDN_DP_region_0_0'

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

Best config: CDN_DP_region_0_0_c6 in controlpath: area: 45775140 ,dp = 2
mux = 0 sg = very_fast      worst_clk_period: -1.0000
wns: 0  norm_wns: -1.0000
fail_endp: -1
tns: 0 tns_per_endp: -1.0000  norm_tns_per_endp: -1.0000
tns_sense_max: -1.0000  tns_sense_avg: -1.0000  tns_sense_num: -1
Smallest config area : 45775140.  Fastest config wns; 0
##>+-----+
-----+
##>Summary table of configs (Best config is CDN_DP_region_0_0_c6)
##>+-----+
-----+
##>          0           1           2
3          4           5           6
7
##>+-----+
-----+
##>          Area       64848115       45775140       45775140
45775140        45775140        45775140        45775140
64848115
##>          WNS      +214748364.70      +214748364.70      +214748364.70
+214748364.70        +214748364.70        +214748364.70        +214748364.70
+214748364.70
##>          TNS          0           0           0
0          0           0           0
0
##>          Num Rewrite        0           0           0
0          0           0           0
0
##>          Num Factor         0           0           0
0          0           0           0
0
##>          Num Share          0           0           0
0          0           0           0
0
##>          Num CmultCse        0           0           0
0          0           0           0
0
##>          Num Downsize        0           0           0
0          0           0           0
0
##>          Num Speculate        0           0           0
0          0           0           0
0
##>          Runtime(s)          0           0           0
0          0           0           0
0
+-----+
-----+
##>
##>
##>+-----+
-----+
##>Optimization Step DEBUG Table for config CDN_DP_region_0_0_c6
##>
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

##>                                         END      68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##>createMaxCarrySave                         START    68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          68662710 ( +0.00)
##> datapath_rewrite_one_def                 START    68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          68662710 ( +0.00)
##> fast_cse_elim                            START    68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##>                                         END      68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##> fast_cse_elim                            START    68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          68662710 ( +0.00)
##>                                         END      68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##>                                         END      68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##> dpopt_share_one_def                      START    68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          68662710 ( +0.00)
##>                                         END      68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##> csa_opto                                 START    68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          68662710 ( +0.00)
##>                                         END      68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##>                                         END      68662710 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##> context_based_simplify                  START    53404330 (-22.22)
214748364.70 ( +0.00)                      0 ( 0)          45775140 (-14.29)
##>                                         END      45775140 (-14.29)
214748364.70 ( +0.00)                      0 ( 0)          0
##>group_csa_final_adder_dp                START    45775140 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          45775140 ( +0.00)
##>                                         END      45775140 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##>dpopt_flatten_critical_muxes_i         START    45775140 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          45775140 ( +0.00)
##>                                         END      45775140 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##>create_score                             START    45775140 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          45775140 ( +0.00)
##>                                         END      45775140 ( +0.00)
214748364.70 ( +0.00)                      0 ( 0)          0
##>+-----+
-----+
Committed config: CDN_DP_region_0_0_c6
Info   : Done implementing datapath configurations. [DPOPT-4]
        : Selected 'very_fast' configuration 6 for module
'CDN_DP_region_0_0'.
        Optimizations applied to 'very_fast' configuration:
        rewriting(0), factoring(0), sharing(0), cmultcse(0),
downsizing(0), speculation(0)
Info   : Done optimizing datapath logic. [DPOPT-2]
        : Done optimizing datapath logic in 'restoring_division'.
Number of big hc bmxes after = 0
Starting logic reduction [v1.0] (stage: post_rtlopt, startdef:
restoring_division, recur: true)
Completed logic reduction (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux data reorder optimization [v1.0] (stage: post_rtlopt,
startdef: restoring_division, recur: true)

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

##>	Step	Area (% Chg)
WNS (Change)	TNS (Change)	Runtime (s) Comment
<hr/>		
##>+-----		
##>createMaxCarrySave	START	64848115 ()
214748364.70 ()	0 ()	64848115 (+0.00)
##> datapath_rewrite_one_def	START	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	64848115 (+0.00)
##> fast_cse_elim	START	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	64848115 (+0.00)
##>	END	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##> fast_cse_elim	START	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	64848115 (+0.00)
##>	END	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##>	END	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##> dpopt_share_one_def	START	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	64848115 (+0.00)
##>	END	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##> csa_opto	START	64848115 (+0.00)
214748364.70 (+0.00)	0 (0)	64848115 (+0.00)
##>	END	68662710 (+5.88)
214748364.70 (+0.00)	0 (0)	0
##>	END	68662710 (+5.88)
214748364.70 (+0.00)	0 (0)	0
##>canonicalize_by_names	START	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	68662710 (+0.00)
##>	END	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##>datapath_rewrite_post_csa_one_	START	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	68662710 (+0.00)
##>	END	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##>datapath_csa_factoring_one_gde	START	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	68662710 (+0.00)
##>	END	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##>dpopt_share_one_def	START	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	68662710 (+0.00)
##>	END	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##>datapath_rewrite_post_share	START	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	68662710 (+0.00)
##>	END	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##>dp_combine_const_mult_with_com	START	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	68662710 (+0.00)
##>	END	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##>dp_operator_level_decompositio	START	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	68662710 (+0.00)
##>	END	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	0
##>selective_flatten_dp_config	START	68662710 (+0.00)
214748364.70 (+0.00)	0 (0)	68662710 (+0.00)

DA3 Logic synthesis & Physical design of restoring binary division algorithm

Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_rtlopt

Transform	Accepts	Rejects	Runtime (ms)
hlo_logic_reduction	0	0	0.00
hlo_mux_reorder	0	0	0.00

```

Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/quotient_reg[0]'.
          : This optimization was enabled by the root attribute
'optimize_constant_latches'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/quotient_reg[1]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/quotient_reg[2]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/quotient_reg[3]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/quotient_reg[4]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/quotient_reg[5]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/quotient_reg[6]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/quotient_reg[7]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/remainder_reg[0]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/remainder_reg[1]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/remainder_reg[2]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/remainder_reg[3]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/remainder_reg[4]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/remainder_reg[5]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/remainder_reg[6]'.
Info    : Replacing a latch with a logic constant 0. [GLO-14]
          : The instance is 'dp/remainder_reg[7]'.
Info    : Deleting instances not driving any primary outputs. [GLO-34]
          : Deleting 8 sequential instances.
Starting mux speculation [v1.0] (stage: post_muxopt, startdef:
restoring_division, recur: true)
Starting speculation optimization
Completed speculation optimization (accepts:0)
Completed mux speculation (accepts: 0, rejects: 0, runtime: 0.004s)

```

Stage: post_muxopt

Transform	Accepts	Rejects	Runtime (ms)
hlo_speculation	0	0	4.00

```
=====
Stage : to_generic
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
| CDFG2G-622 |Warning| 40 |Signal or variable has multiple drivers.  
|             |       |  
|             |       |     |This may cause simulation mismatches  
between the |       |  
|             |       |     | original and synthesized designs.  
| CWD-19    |Info| 32 |An implementation was inferred.  
| DPOPT-1   |Info| 1  |Optimizing datapath logic.  
| DPOPT-2   |Info| 1  |Done optimizing datapath logic.  
| DPOPT-3   |Info| 2  |Implementing datapath configurations.  
| DPOPT-4   |Info| 2  |Done implementing datapath configurations.  
| DPOPT-6   |Info| 1  |Pre-processed datapath logic.  
| ELAB-1    |Info| 1  |Elaborating Design.  
| ELAB-2    |Info| 2  |Elaborating Subdesign.  
| ELAB-3    |Info| 1  |Done Elaborating Design.  
| GB-6      |Info| 2  |A datapath component has been ungrouped.  
| GLO-12   |Info| 16 |Replacing a flip-flop with a logic constant  
0.  |  
|             |       |  
|             |       |     |To prevent this optimization, set the  
| to        |       |     | 'optimize_constant_0_flops' root attribute  
| instance  |       |     | 'false' or 'optimize_constant_0_seq'  
|           |       |     | attribute to 'false'. You can also see the  
|           |       |     | complete list of deleted sequential with  
|           |       |     | command 'report sequential -deleted'  
|           |       |     | (on Reason 'constant0').  
| GLO-14   |Info| 16 |Replacing a latch with a logic constant 0.  
|             |       |  
|             |       |     |This optimization was enabled by the root  
|             |       |     | attribute 'optimize_constant_latches'.  
| GLO-34   |Info| 2  |Deleting instances not driving any primary  
|             |       |  
|             |       |     | outputs.  
|             |       |  
|             |       |     |Optimizations such as constant propagation  
or     |  
|             |       |     | redundancy removal could change the  
connections |  
|             |       |     | so a hierarchical instance does not drive  
any     |  
|             |       |     | primary outputs anymore. To see the list  
of      |
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

=====			
=====			
Message Summary			
=====			
Id	Sev	Count	Message Text
CDFG-372	Info	17	Bitwidth mismatch in assignment. Review and make sure the mismatch is unintentional. Genus can possibly issue bitwidth mismatch warning for explicit assignments present in RTL as-well-as for implicit assignments inferred by the tool. For without value to warning this example, in case of enum declaration value, the tool will implicitly assign the enum variables. It also issues the for any bitwidth mismatch that appears in implicit assignment.
CDFG-738	Info	1	Common subexpression eliminated.
CDFG-739	Info	1	Common subexpression kept.
CDFG2G-616	Info	2	Latch inferred. Check and revisit your RTL if this is not the intended behavior. Use the attributes 'set_attribute hdl_error_on_latch true' (LUI) or 'set_db hdl_error_on_latch true' (CUI) to issue an error when a latch is inferred. Use the attributes 'set_attributes hdl_latch_keep_feedback true' (LUI) or 'set_db hdl_latch_keep_feedback true' (CUI) to infer combinational logic rather than a assigned latch in case a variable is explicitly to itself.

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
|           |           | deleted hierarchical instances, set the
|           |           | 'information_level' attribute to 2 or
above. If |           | the message is truncated set the message
|           |           | attribute 'truncate' to false to see the
|           |           | complete list. To prevent this
optimization, |           | set the 'delete_unloaded_insts'
root/subdesign |           | attribute to 'false' or 'preserve'
instance      |           | attribute to 'true'.
|
| LBR-41     |Info    | 1 |An output library pin lacks a function
|           |           | attribute.
|
|           |           | |If the remainder of this library cell's
semantic   |           | checks are successful, it will be
considered as |           | a timing-model
|
|           |           | |(because one of its outputs does not have
a val     |           | id function.
|
| LBR-155    |Info    | 372 |Mismatch in unateness between
'timing_sense' |           | attribute and the function.
|
|           |           | |The 'timing_sense' attribute will be
respected. |
| LBR-161    |Info    | 1 |Setting the maximum print count of this
message    |           | to 10 if information_level is less than 9.
|
| LBR-162    |Info    | 124 |Both 'pos_unate' and 'neg_unate'
timing_sense |           | arcs have been processed.
|
|           |           | |Setting the 'timing_sense' to non_unate.
|
| LBR-170    |Info    | 32 |Ignoring specified timing sense.
|
|           |           | |Timing sense should never be set with
|           |           | 'rising_edge' or 'falling_edge' timing
type.      |
| LBR-412    |Info    | 1 |Created nominal operating condition.
|
|           |           | |The nominal operating condition is
represented, |
|           |           | either by the nominal PVT values specified
in       |           | the library source
|
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
| TUI-61      |Error   | 2 |A required object parameter could not be
found.  |
|           |       |     |Check to make sure that the object exists
and is |
|           |       |     | of the correct type. The 'what_is'
command can |
|           |       |     | be used to determine the type of an
object.    |
| TUI-204    |Error   | 1 |An invalid option was specified.
|
|           |       |     |Run 'command_name -help' to check all valid
|
|           |       |     | options. To correct the option and rerun
the     |
|           |       |     | command.
|
-----  
Mapper: Libraries have:  
    domain _default_: 324 combo usable cells and 128 sequential usable  
cells  
Multi-threaded constant propagation [1|0] ...  
Multi-threaded Virtual Mapping     (8 threads, 8 of 20 CPUs usable)  
=====  
Stage : first_condense  
=====  
=====  
Message Summary  
=====  
-----  
| Id    |Sev  |Count |                                     Message Text
|  
-----  
| GB-6  |Info  |  4 |A datapath component has been ungrouped.  
|  
| GLO-51 |Info  |  1 |Hierarchical instance automatically ungrouped.  
|  
|       |       |     |Hierarchical instances can be automatically  
ungrouped  |
|       |       |     |to allow for better area or timing optimization.  
To     |
|       |       |     |prevent this ungroup, set the root-level  
attribute  |
|       |       |     |'auto_ungroup' to 'none'. You can also prevent  
|       |       |individual ungroup with setting the attribute  
|       |       |'ungroup_ok' of instances or modules to 'false'.
|  
-----  
Global mapping target info  
=====  
Cost Group 'default' target slack: Unconstrained  
  
State Retention Synthesis Status
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
|           |           | (via nom_process,nom_voltage and
nom_temperatur |           | e respectively)
|
|           |           | , or by the default PVT values
(1.0,1.0,1.0). |
| LBR-516    |Info  | 1 |Missing library level attribute.
|
| LBR-518    |Info  | 1 |Missing a function attribute in the output
pin      |           | definition.
|
| PHYS-752   |Info  | 1 |Partition Based Synthesis execution
skipped.    |
| RTLOPT-30   |Info  | 1 |Accepted resource sharing opportunity.
|
| RTLOPT-40   |Info  | 7 |Transformed datapath macro.
|
| SDC-202    |Error  | 7 |Could not interpret SDC command.
|
|           |           | The 'read_sdc' command encountered a
problem     |
|           |           | while trying to evaluate an SDC command.
This       |
|           |           | SDC command will be added to the Tcl
variable   |
|           |           | $::dc::sdc_failed_commands.
|
| SDC-204    |Error  | 1 |Invalid SDC command option combination.
|
|           |           | This option is not valid for the indicated
SDC        |
|           |           | command. Check the SDC command and contact
|
|           |           | Cadence customer support if you believe
this       |
|           |           | option combination should be supported.
|
| SDC-208    |Warning | 4 |Could not find requested search value.
|
|           |           | Use get_* commands to find the objects
along     |
|           |           | with a wild card entry in the name of the
|
|           |           | object to check if the object is existing
with      |
|           |           | different naming style.
|
| SDC-209    |Warning | 1 |One or more commands failed when these
|
|           |           | constraints were applied.
|
|           |           | You can examine the failed commands or save
them     |
|           |           | to a file by querying the Tcl variable
|
|           |           | $::dc::sdc_failed_commands.
|
| SYNTH-1   |Info   | 1 |Synthesizing.
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

=====

Category	Flops	Percentage
Total instances	54	100.0
Excluded from State Retention	54	100.0
- Will not convert	54	100.0
- Preserved	0	0.0
- Power intent excluded	54	100.0
- Could not convert	0	0.0
- Scan type	0	0.0
- No suitable cell	0	0.0
State Retention instances	0	0.0

PBS_Generic_Opt-Post - Elapsed_Time 1, CPU_Time 1.8599680000000003
stamp 'PBS_Generic_Opt-Post' being created for table 'pbs_debug'

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time
Memory	Stage		
00:00:04(00:00:03)	00:00:00(00:00:00)	0.0(0.0)	16:28:44 (Nov14) 242.2 MB PBS_Generic-Start
00:00:05(00:00:04)	00:00:01(00:00:01)	100.0(100.0)	16:28:45 (Nov14) 756.7 MB PBS_Generic_Opt-Post

Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_Generic-Postgen HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Postgen HBO Optimizations' being created for table
'pbs_debug'

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time
Memory	Stage		
00:00:04(00:00:03)	00:00:00(00:00:00)	0.0(0.0)	16:28:44 (Nov14) 242.2 MB PBS_Generic-Start
00:00:05(00:00:04)	00:00:01(00:00:01)	100.0(100.0)	16:28:45 (Nov14) 756.7 MB PBS_Generic_Opt-Post
00:00:05(00:00:04)	00:00:00(00:00:00)	0.0(0.0)	16:28:45 (Nov14) 756.7 MB PBS_Generic-Postgen HBO Optimizations

Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
##>===== Cadence Confidential (Generic-Logical)
=====

DA3 Logic synthesis & Physical design of restoring binary division algorithm

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time
Memory	Stage		
00:00:04 (00:00:03) (Nov14)	00:00:00 (00:00:00) PBS_Generic-Start	0.0(0.0)	16:28:44
00:00:05 (00:00:04) (Nov14)	00:00:01 (00:00:01) PBS_Generic_Opt-Post	100.0(100.0)	16:28:45
00:00:05 (00:00:04) (Nov14)	00:00:00 (00:00:00) PBS_Generic-Postgen HBO Optimizations	0.0(0.0)	16:28:45
00:00:05 (00:00:04) (Nov14)	00:00:00 (00:00:00) PBS_TechMap-Start	0.0(0.0)	16:28:45
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)			
Info: (*N*) indicates data that was populated from previously saved time_info database			
Info: CPU time includes time of parent + longest thread			
PBS_TechMap-Premap HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0 stamp 'PBS_TechMap-Premap HBO Optimizations' being created for table 'pbs_debug'			
Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time
Memory	Stage		
00:00:04 (00:00:03) (Nov14)	00:00:00 (00:00:00) PBS_Generic-Start	0.0(0.0)	16:28:44
00:00:05 (00:00:04) (Nov14)	00:00:01 (00:00:01) PBS_Generic_Opt-Post	100.0(100.0)	16:28:45
00:00:05 (00:00:04) (Nov14)	00:00:00 (00:00:00) PBS_Generic-Postgen HBO Optimizations	0.0(0.0)	16:28:45
00:00:05 (00:00:04) (Nov14)	00:00:00 (00:00:00) PBS_TechMap-Start	0.0(0.0)	16:28:45
00:00:05 (00:00:04) (Nov14)	00:00:00 (00:00:00) PBS_TechMap-Premap HBO Optimizations	0.0(0.0)	16:28:45
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)			
Info: (*N*) indicates data that was populated from previously saved time_info database			
Info: CPU time includes time of parent + longest thread			
Info : Partition Based Synthesis execution skipped. [PHYS-752]			
: Design size is less than the partition size '100000' for distributed mapping optimization to kick in.			
Mapper: Libraries have:			

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
##>===== Cadence Confidential (Generic-Logical)
=====
##>Main Thread Summary:
##>-----
-----  
##>STEP                               Elapsed      WNS      TNS      Insts
Area     Memory  
##>-----  
-----  
##>G:Initial                         0          -          -          487
4749     242
##>G:Setup                            0          -          -          -
-          -
##>G:Launch ST                         0          -          -          -
-          -
##>G:Design Partition                  0          -          -          -
-          -
##>G>Create Partition Netlists         0          -          -          -
-          -
##>G:Init Power                        0          -          -          -
-          -
##>G:Budgeting                          0          -          -          -
-          -
##>G:Derenv-DB                         0          -          -          -
-          -
##>G:Debug Outputs                     0          -          -          -
-          -
##>G:ST loading                        0          -          -          -
-          -
##>G:Distributed                       0          -          -          -
-          -
##>G:Timer                            0          -          -          -
-          -
##>G:Assembly                          0          -          -          -
-          -
##>G:DFT                             0          -          -          -
-          -
##>G:Const Prop                        0          -          -          212
2628     756
##>G:Misc                            1
##>-----  
-----  
##>Total Elapsed                      1
##>=====  
=====  
Info      : Done synthesizing. [SYNTH-2]
          : Done synthesizing 'restoring_division' to generic gates.
##Generic Timing Info for library domain: _default_ typical gate delay:
127.0 ps std_slew: 15.5 ps std_load: 7.0 fF
Info      : Mapping. [SYNTH-4]
          : Mapping 'restoring_division' using 'high' effort.
Mapper: Libraries have:
        domain _default_: 324 combo usable cells and 128 sequential usable
cells
Configuring mapper costing (none)
TNS Restructuring config: no_value at stage: map applied.
PBS_TechMap-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Start' being created for table 'pbs_debug'
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
domain _default_: 324 combo usable cells and 128 sequential usable
cells
Multi-threaded Virtual Mapping      (8 threads, 8 of 20 CPUs usable)

Global mapping target info
=====
Cost Group 'default' target slack: Unconstrained

Multi-threaded Technology Mapping (8 threads, 8 of 20 CPUs usable)

Global mapping status
=====
          Worst
          Total  Weighted
Operation      Area  Neg Slk Worst Path
global_map      1520    0   N/A

Cost Group      Target  Slack  Diff. Constr.
-----
default        unconst. unconst.           N.A.

Global incremental target info
=====
Cost Group 'default' target slack: Unconstrained
=====
Stage : global_incr_map
=====
Message Summary
=====
|   Id   |Sev  |Count |           Message Text |
|-----|
| PA-7   |Info  |    8 |Resetting power analysis results. |
|       |      |      |All computed switching activities are removed. |
| PHYS-752 |Info  |    1 |Partition Based Synthesis execution skipped. |
| SYNTH-2  |Info  |    1 |Done synthesizing. |
| SYNTH-4  |Info  |    1 |Mapping. |
|-----|

Global incremental optimization status
=====
          Worst
          Total  Weighted
Operation      Area  Neg Slk Worst Path
global_incr     1518    0   N/A

Cost Group      Target  Slack  Diff. Constr.
-----
default        unconst. unconst.           N.A.

State Retention Synthesis Status
=====
Category          Flops  Percentage
-----
Total instances      54        100.0
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time
Memory	Stage		
00:00:04(00:00:03)	00:00:00(00:00:00)	0.0(0.0)	16:28:44 (Nov14) 242.2 MB PBS_Generic-Start
00:00:05(00:00:04)	00:00:01(00:00:01)	73.0(50.0)	16:28:45 (Nov14) 756.7 MB PBS_Generic_Opt-Post
00:00:05(00:00:04)	00:00:00(00:00:00)	0.0(0.0)	16:28:45 (Nov14) 756.7 MB PBS_Generic-Postgen HBO Optimizations
00:00:05(00:00:04)	00:00:00(00:00:00)	0.0(0.0)	16:28:45 (Nov14) 756.7 MB PBS_TechMap-Start
00:00:05(00:00:04)	00:00:00(00:00:00)	0.0(0.0)	16:28:45 (Nov14) 756.7 MB PBS_TechMap-Premap HBO Optimizations
00:00:05(00:00:05)	00:00:00(00:00:01)	-12.3(50.0)	16:28:46 (Nov14) 756.7 MB PBS_Techmap-Global Mapping
00:00:06(00:00:05)	00:00:01(00:00:00)	39.3(0.0)	16:28:46 (Nov14) 756.7 MB PBS_TechMap-Datapath Postmap Operations
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57) Info: (*N*) indicates data that was populated from previously saved time_info database Info: CPU time includes time of parent + longest thread PBS_TechMap-Postmap HBO Optimizations - Elapsed_Time 0, CPU_Time - 0.002587000000000117 stamp 'PBS_TechMap-Postmap HBO Optimizations' being created for table 'pbs_debug'			
Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time
Memory	Stage		
00:00:04(00:00:03)	00:00:00(00:00:00)	0.0(0.0)	16:28:44 (Nov14) 242.2 MB PBS_Generic-Start
00:00:05(00:00:04)	00:00:01(00:00:01)	73.1(50.0)	16:28:45 (Nov14) 756.7 MB PBS_Generic_Opt-Post
00:00:05(00:00:04)	00:00:00(00:00:00)	0.0(0.0)	16:28:45 (Nov14) 756.7 MB PBS_Generic-Postgen HBO Optimizations
00:00:05(00:00:04)	00:00:00(00:00:00)	0.0(0.0)	16:28:45 (Nov14) 756.7 MB PBS_TechMap-Start

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

Excluded from State Retention      54      100.0
  - Will not convert              54      100.0
    - Preserved                  0       0.0
    - Power intent excluded     54      100.0
  - Could not convert             0       0.0
    - Scan type                  0       0.0
    - No suitable cell            0       0.0
State Retention instances          0       0.0
-----
INFO: skipping constant propagation
PBS_Techmap-Global Mapping - Elapsed_Time 1, CPU_Time -0.31352500000000003
stamp 'PBS_Techmap-Global Mapping' being created for table 'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
  | Memory   | Stage
  -----+-----+-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:44
(Nov14) | 242.2 MB | PBS_Generic-Start
  -----+-----+-----+
  00:00:05(00:00:04) | 00:00:01(00:00:01) | 120.3( 50.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_Generic_Opt-Post
  -----+-----+-----+
  00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_Generic-Postgen HBO Optimizations
  -----+-----+-----+
  00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_TechMap-Start
  -----+-----+-----+
  00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_TechMap-Premap HBO Optimizations
  -----+-----+-----+
  00:00:05(00:00:05) | 00:00:00(00:00:01) | -20.3( 50.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_Techmap-Global Mapping
  -----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
Warning : Command 'commit_power_intent' cannot proceed as there is no
power intent loaded. [CPI-506]
      : Command 'commit_power_intent' requires a valid power_intent to
be loaded.
Info   : Wrote formal verification information. [CFM-5]
      : Wrote 'fv/restoring_division/fv_map.fv.json' for netlist
'fv/restoring_division/fv_map.v.gz'.
Info   : Wrote dofile. [CFM-1]
      : Dofile is 'fv/restoring_division/rtl_to_fv_map.do'.
      : Alias mapping flow is enabled.
PBS_TechMap-Datapath Postmap Operations - Elapsed_Time 0, CPU_Time 1.0
stamp 'PBS_TechMap-Datapath Postmap Operations' being created for table
'pbs_debug'

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
-----+-----+-----+
-----+-----+
00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+
-----+-----+
00:00:05(00:00:05) | 00:00:00(00:00:01) | -12.3( 50.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_Techmap-Global Mapping
-----+-----+
-----+-----+
00:00:06(00:00:05) | 00:00:01(00:00:00) | 39.3( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+
-----+-----+
00:00:06(00:00:05) | 00:00:00(00:00:00) | -0.1( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Postmap HBO Optimizations
-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
Doing ConstProp on /designs/restoring_division ...

Time taken by ConstProp Step: 00:00:00
PBS_TechMap-Postmap Clock Gating - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Postmap Clock Gating' being created for table
'pbs_debug'

      Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
      | Memory | Stage
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:44
(Nov14) | 242.2 MB | PBS_Generic-Start
-----+-----+
-----+-----+
00:00:05(00:00:04) | 00:00:01(00:00:01) | 73.1( 50.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_Generic_Opt-Post
-----+-----+
-----+-----+
00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+
-----+-----+
00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_TechMap-Start
-----+-----+
-----+-----+
00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+
-----+-----+
00:00:05(00:00:05) | 00:00:00(00:00:01) | -12.3( 50.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_Techmap-Global Mapping
-----+-----+
-----+-----+
00:00:06(00:00:05) | 00:00:01(00:00:00) | 39.3( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Datapath Postmap Operations
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
plc_laf_lo_st      0 (      0 /      0 )  0.00
plc_lo_st          0 (      0 /      0 )  0.00
fopt               0 (      0 /      0 )  0.00
crit_dnsz          0 (      0 /      0 )  0.00
dup                0 (      0 /      0 )  0.00
setup_dn           0 (      0 /      0 )  0.00
mb_split            0 (      0 /      0 )  0.00

PBS_TechMap-Postmap Cleanup - Elapsed_Time 0, CPU_Time -
0.0017360000000001818
stamp 'PBS_TechMap-Postmap Cleanup' being created for table 'pbs_debug'

  Total Time (Wall) |  Stage Time (Wall) |  % (Wall) |  Date - Time
|  Memory   |  Stage
-----+-----+-----+-----+
-----+-----+
  00:00:04(00:00:03) |  00:00:00(00:00:00) |  0.0( 0.0) |  16:28:44
(Nov14) |  242.2 MB | PBS_Generic-Start
-----+-----+-----+
-----+-----+
  00:00:05(00:00:04) |  00:00:01(00:00:01) |  73.2( 50.0) |  16:28:45
(Nov14) |  756.7 MB | PBS_Generic_Opt-Post
-----+-----+-----+
-----+-----+
  00:00:05(00:00:04) |  00:00:00(00:00:00) |  0.0( 0.0) |  16:28:45
(Nov14) |  756.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
-----+-----+
  00:00:05(00:00:04) |  00:00:00(00:00:00) |  0.0( 0.0) |  16:28:45
(Nov14) |  756.7 MB | PBS_TechMap-Start
-----+-----+-----+
-----+-----+
  00:00:05(00:00:04) |  00:00:00(00:00:00) |  0.0( 0.0) |  16:28:45
(Nov14) |  756.7 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+-----+
-----+-----+
  00:00:05(00:00:05) |  00:00:00(00:00:01) | -12.3( 50.0) |  16:28:46
(Nov14) |  756.7 MB | PBS_Techmap-Global Mapping
-----+-----+-----+
-----+-----+
  00:00:06(00:00:05) |  00:00:01(00:00:00) |  39.3( 0.0) |  16:28:46
(Nov14) |  756.7 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+-----+
-----+-----+
  00:00:06(00:00:05) |  00:00:00(00:00:00) | -0.1( 0.0) |  16:28:46
(Nov14) |  756.7 MB | PBS_TechMap-Postmap HBO Optimizations
-----+-----+-----+
-----+-----+
  00:00:06(00:00:05) |  00:00:00(00:00:00) |  0.0( 0.0) |  16:28:46
(Nov14) |  756.7 MB | PBS_TechMap-Postmap Clock Gating
-----+-----+-----+
-----+-----+
  00:00:06(00:00:05) |  00:00:00(00:00:00) | -0.1( 0.0) |  16:28:46
(Nov14) |  756.7 MB | PBS_TechMap-Postmap Cleanup
-----+-----+-----+
-----+-----+
Number of threads: 8 * 1  (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

-----+-----+-----+
-----+-----+
00:00:06(00:00:05) | 00:00:00(00:00:00) | -0.1( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Postmap HBO Optimizations
-----+-----+
-----+-----+
00:00:06(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Postmap Clock Gating
-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
-----
-----+-----+
hi_fo_buf           1518      0      0      0
-----+-----+
Trick    Calls   Accepts  Attempts  Time (secs)
-----+-----+
hi_fo_buf          0 ( 0 / 0 ) 0.00
-----+-----+
Incremental optimization status
=====
                               Worst      Total DRC Total
                               Total Weighted Neg Max
Operation          Area Neg Slk Slack Cap
init_delay        1518     0       0       0       0
-----+-----+
Trick    Calls   Accepts  Attempts  Time (secs)
-----+-----+
crit_upsz          0 ( 0 / 0 ) 0.00
plc_bal_star       0 ( 0 / 0 ) 0.00
drc_buftimb        0 ( 0 / 0 ) 0.00
plc_st             0 ( 0 / 0 ) 0.00
plc_st_fence       0 ( 0 / 0 ) 0.00
plc_star           0 ( 0 / 0 ) 0.00
plc_laf_st         0 ( 0 / 0 ) 0.00
plc_laf_st_fence  0 ( 0 / 0 ) 0.00
drc_buftims        0 ( 0 / 0 ) 0.00
fopt               0 ( 0 / 0 ) 0.00
plc_laf_lo_st     0 ( 0 / 0 ) 0.00
plc_lo_st          0 ( 0 / 0 ) 0.00
mb_split           0 ( 0 / 0 ) 0.00
-----+-----+
Local TNS optimization status
=====
                               Worst      Total DRC Total
                               Total Weighted Neg Max
Operation          Area Neg Slk Slack Cap
init_tns          1518     0       0       0       0
-----+-----+
Trick    Calls   Accepts  Attempts  Time (secs)
-----+-----+
plc_bal_star       0 ( 0 / 0 ) 0.00
drc_buftimb        0 ( 0 / 0 ) 0.00
drc_buftims        0 ( 0 / 0 ) 0.00
crit_upsz          0 ( 0 / 0 ) 0.00

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
PBS_Techmap-Post_MBCI - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Techmap-Post_MBCI' being created for table 'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
  | Memory | Stage
-----
+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:44
(Nov14) | 242.2 MB | PBS_Generic-Start
+-----+
+-----+
00:00:05(00:00:04) | 00:00:01(00:00:01) | 73.2( 50.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_Generic_Opt-Post
+-----+
+-----+
00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_Generic-Postgen HBO Optimizations
+-----+
+-----+
00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_TechMap-Start
+-----+
+-----+
00:00:05(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:45
(Nov14) | 756.7 MB | PBS_TechMap-Premap HBO Optimizations
+-----+
+-----+
00:00:05(00:00:05) | 00:00:00(00:00:01) | -12.3( 50.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_Techmap-Global Mapping
+-----+
+-----+
00:00:06(00:00:05) | 00:00:01(00:00:00) | 39.3( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Datapath Postmap Operations
+-----+
+-----+
00:00:06(00:00:05) | 00:00:00(00:00:00) | -0.1( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Postmap HBO Optimizations
+-----+
+-----+
00:00:06(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Postmap Clock Gating
+-----+
+-----+
00:00:06(00:00:05) | 00:00:00(00:00:00) | -0.1( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_TechMap-Postmap Cleanup
+-----+
+-----+
00:00:06(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 16:28:46
(Nov14) | 756.7 MB | PBS_Techmap-Post_MBCI
+-----+
+-----+
Number of threads: 8 * 1  (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
##>===== Cadence Confidential (Mapping-Logical)
=====
##>Main Thread Summary:
##>-----
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

Operation	Area	Neg	Slk	Slack	Cap
init_iopt	1518	0	0	0	0
const_prop	1518	0	0	0	0
hi_fo_buf	1518	0	0	0	0
Trick	Calls	Accepts	Attempts	Time (secs)	
hi_fo_buf	0 (0 /	0)	0.00	
 Incremental optimization status					
Operation	Total	Worst	Total	DRC	Total
init_delay	1518	Weighted	Neg	Max	
		Area	Slk	Slack	Cap
Trick	Calls	Accepts	Attempts	Time (secs)	
crit_msz	0 (0 /	0)	0.00	
crit_upsz	0 (0 /	0)	0.00	
crit_slew	0 (0 /	0)	0.00	
setup_dn	0 (0 /	0)	0.00	
plc_bal_star	0 (0 /	0)	0.00	
drc_buftimb	0 (0 /	0)	0.00	
plc_st	0 (0 /	0)	0.00	
plc_st_fence	0 (0 /	0)	0.00	
plc_star	0 (0 /	0)	0.00	
plc_laf_st	0 (0 /	0)	0.00	
plc_laf_st_fence	0 (0 /	0)	0.00	
drc_buftims	0 (0 /	0)	0.00	
plc_laf_lo_st	0 (0 /	0)	0.00	
plc_lo_st	0 (0 /	0)	0.00	
fopt	0 (0 /	0)	0.00	
crit_swap	0 (0 /	0)	0.00	
mux2_swap	0 (0 /	0)	0.00	
crit_dnsz	0 (0 /	0)	0.00	
load_swap	0 (0 /	0)	0.00	
fopt	0 (0 /	0)	0.00	
setup_dn	0 (0 /	0)	0.00	
load_isol	0 (0 /	0)	0.00	
load_isol	0 (0 /	0)	0.00	
move_for	0 (0 /	0)	0.00	
move_for	0 (0 /	0)	0.00	
rem_bi	0 (0 /	0)	0.00	
offload	0 (0 /	0)	0.00	
rem_bi	0 (0 /	0)	0.00	
offload	0 (0 /	0)	0.00	
phase	0 (0 /	0)	0.00	
in_phase	0 (0 /	0)	0.00	
merge_bit	0 (0 /	0)	0.00	
merge_idrvr	0 (0 /	0)	0.00	
merge_iload	0 (0 /	0)	0.00	
merge_idload	0 (0 /	0)	0.00	
merge_drvr	0 (0 /	0)	0.00	
merge_load	0 (0 /	0)	0.00	

DA3 Logic synthesis & Physical design of restoring binary division algorithm

##>STEP	Area	Memory	Elapsed	WNS	TNS	Insts
##>-----						
##>M:Initial	2628	756	0	-	-	212
##>M:Pre Cleanup	2628	756	0	-	-	212
##>M:Setup	-	-	0	-	-	-
##>M:Launch ST	-	-	0	-	-	-
##>M:Design Partition	-	-	0	-	-	-
##>M>Create Partition Netlists	-	-	0	-	-	-
##>M:Init Power	-	-	0	-	-	-
##>M:Budgeting	-	-	0	-	-	-
##>M:Derenv-DB	-	-	0	-	-	-
##>M:Debug Outputs	-	-	0	-	-	-
##>M:ST loading	-	-	0	-	-	-
##>M:Distributed	-	-	0	-	-	-
##>M:Timer	-	-	0	-	-	-
##>M:Assembly	-	-	0	-	-	-
##>M:DFT	-	-	0	-	-	-
##>M:DP Operations	1518	756	0	-	-	160
##>M:Const Prop	1518	756	0	-	0	160
##>M:Cleanup	1518	756	0	-	0	160
##>M:MBCI	1518	756	0	-	-	160
##>M:Const Gate Removal	-	-	0	-	-	-
##>M:Misc	-	-	1			
##>-----						
##>Total Elapsed			1			
##>=====						
Info : Done mapping. [SYNTH-5]						
Info : Done mapping 'restoring_division'.						
Info : Incrementally optimizing. [SYNTH-7]						
Info : Incrementally optimizing 'restoring_division' using 'high' effort.						
Incremental optimization status						
=====						
			Worst Total	Total DRC Weighted Neg	Total Max	

DA3 Logic synthesis & Physical design of restoring binary division algorithm

decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
exp	0 (0 /	0)	0.00
gate_deco	0 (0 /	0)	0.00
gcomp_tim	0 (0 /	0)	0.00
inv_pair_2_buf	0 (0 /	0)	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
<hr/>				
crr_220	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_200	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_300	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_400	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_111	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_210	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_110	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_101	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_201	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_211	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crit_msz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
crit_slew	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
plc_bal_star	0 (0 /	0)	0.00
drc_buftimb	0 (0 /	0)	0.00
plc_st	0 (0 /	0)	0.00
plc_st_fence	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
plc_laf_st	0 (0 /	0)	0.00
plc_laf_st_fence	0 (0 /	0)	0.00
drc_buftims	0 (0 /	0)	0.00
plc_lo_st	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
crit_swap	0 (0 /	0)	0.00
mux2_swap	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
load_swap	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00

DA3 Logic synthesis & Physical design of restoring binary division algorithm

offload	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
merge_bit	0 (0 /	0)	0.00
merge_idrvr	0 (0 /	0)	0.00
merge_iload	0 (0 /	0)	0.00
merge_idload	0 (0 /	0)	0.00
merge_drvr	0 (0 /	0)	0.00
merge_load	0 (0 /	0)	0.00
phase	0 (0 /	0)	0.00
decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
in_phase	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
exp	0 (0 /	0)	0.00
gate_deco	0 (0 /	0)	0.00
gcomp_tim	0 (0 /	0)	0.00
inv_pair_2_buf	0 (0 /	0)	0.00
init_drc	1518	0	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
crit_slew	0 (0 /	0)	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_buf_sp	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_buf_sp	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00

DA3 Logic synthesis & Physical design of restoring binary division algorithm

gate_comp	6	(0 /	0)	0.01
gcomp_mog	0	(0 /	0)	0.00
glob_area	17	(0 /	17)	0.00
area_down	0	(0 /	0)	0.00
size_n_buf	0	(0 /	0)	0.00
gate_deco_area	0	(0 /	0)	0.00
rem_buf	0	(0 /	0)	0.00
rem_inv	0	(0 /	0)	0.00
merge_bi	0	(0 /	0)	0.00
rem_inv_qb	0	(0 /	0)	0.00

Incremental optimization status

Operation	Worst			Total	DRC	Total
	Total	Weighted		Neg	Max	
init_delay	1515	0		0	0	

Trick	Calls	Accepts	Attempts	Time (secs)
crr_220	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_200	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_300	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_400	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_111	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_210	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_110	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_101	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_201	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crr_211	0	(0 /	0)	0.00
crr_glob	0	(0 /	0)	0.00
crit_msz	0	(0 /	0)	0.00
crit_upsz	0	(0 /	0)	0.00
crit_slew	0	(0 /	0)	0.00
setup_dn	0	(0 /	0)	0.00
plc_bal_star	0	(0 /	0)	0.00
drc_buftimb	0	(0 /	0)	0.00
plc_st	0	(0 /	0)	0.00
plc_st_fence	0	(0 /	0)	0.00
plc_star	0	(0 /	0)	0.00
plc_laf_st	0	(0 /	0)	0.00
plc_laf_st_fence	0	(0 /	0)	0.00
drc_buftims	0	(0 /	0)	0.00
plc_lo_st	0	(0 /	0)	0.00
fopt	0	(0 /	0)	0.00
crit_swap	0	(0 /	0)	0.00
mux2_swap	0	(0 /	0)	0.00
crit_dnsz	0	(0 /	0)	0.00
load_swap	0	(0 /	0)	0.00
fopt	0	(0 /	0)	0.00

DA3 Logic synthesis & Physical design of restoring binary division algorithm

dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
init_tns	1518	0	0	0
Trick	Calls	Accepts	Attempts	Time (secs)
fopt	0 (0 /	0)	0.00
plc_bal_star	0 (0 /	0)	0.00
drc_buftimb	0 (0 /	0)	0.00
drc_buftims	0 (0 /	0)	0.00
crit_msz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
plc_laf_lo_st	0 (0 /	0)	0.00
plc_lo_st	0 (0 /	0)	0.00
crit_swap	0 (0 /	0)	0.00
mux2_swap	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
load_swap	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
merge_bit	0 (0 /	0)	0.00
merge_idrvr	0 (0 /	0)	0.00
merge_iload	0 (0 /	0)	0.00
merge_idload	0 (0 /	0)	0.00
merge_drvr	0 (0 /	0)	0.00
merge_load	0 (0 /	0)	0.00
phase	0 (0 /	0)	0.00
decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00
crr_local	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
init_area	1518	0	0	0
merge_bi	1516	0	0	0
rem_inv_qb	1515	0	0	0
io_phase	1515	0	0	0
Trick	Calls	Accepts	Attempts	Time (secs)
undup	0 (0 /	0)	0.00
rem_buf	0 (0 /	0)	0.00
rem_inv	0 (0 /	0)	0.00
merge_bi	1 (1 /	1)	0.00
rem_inv_qb	1 (1 /	1)	0.00
seq_res_area	4 (0 /	0)	0.07
io_phase	1 (1 /	1)	0.00

DA3 Logic synthesis & Physical design of restoring binary division algorithm

setup_dn	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
merge_bit	0 (0 /	0)	0.00
merge_idrvr	0 (0 /	0)	0.00
merge_iload	0 (0 /	0)	0.00
merge_idload	0 (0 /	0)	0.00
merge_drvr	0 (0 /	0)	0.00
merge_load	0 (0 /	0)	0.00
phase	0 (0 /	0)	0.00
decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
in_phase	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
exp	0 (0 /	0)	0.00
gate_deco	0 (0 /	0)	0.00
gcomp_tim	0 (0 /	0)	0.00
inv_pair_2_buf	0 (0 /	0)	0.00
init_drc	1515	0	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
crit_slew	0 (0 /	0)	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00

DA3 Logic synthesis & Physical design of restoring binary division algorithm

plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
 init_tns	 1515	 0	 0	 0
 Trick	 Calls	 Accepts	 Attempts	 Time (secs)
-----	-----	-----	-----	-----
fopt	0 (0 /	0)	0.00
plc_bal_star	0 (0 /	0)	0.00
drc_buftimb	0 (0 /	0)	0.00
drc_buftims	0 (0 /	0)	0.00
crit_msz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
plc_laf_lo_st	0 (0 /	0)	0.00
plc_lo_st	0 (0 /	0)	0.00
crit_swap	0 (0 /	0)	0.00
mux2_swap	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
load_swap	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
merge_bit	0 (0 /	0)	0.00
merge_idrvr	0 (0 /	0)	0.00
merge_iload	0 (0 /	0)	0.00
merge_idload	0 (0 /	0)	0.00
merge_drvr	0 (0 /	0)	0.00
merge_load	0 (0 /	0)	0.00
phase	0 (0 /	0)	0.00
decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00
crr_local	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
 init_area	 1515	 0	 0	 0
 Trick	 Calls	 Accepts	 Attempts	 Time (secs)
-----	-----	-----	-----	-----
undup	0 (0 /	0)	0.00
rem_buf	0 (0 /	0)	0.00
rem_inv	0 (0 /	0)	0.00
merge_bi	0 (0 /	0)	0.00
rem_inv_qb	0 (0 /	0)	0.00
io_phase	0 (0 /	0)	0.00

DA3 Logic synthesis & Physical design of restoring binary division algorithm

buf2inv	0 (0 /	0)	0.00
exp	0 (0 /	0)	0.00
gate_deco	0 (0 /	0)	0.00
gcomp_tim	0 (0 /	0)	0.00
inv_pair_2_buf	0 (0 /	0)	0.00
 init_drc		1515	0	0
 Trick	Calls	Accepts	Attempts	Time (secs)

plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
crit_slew	0 (0 /	0)	0.00
 Trick	Calls	Accepts	Attempts	Time (secs)

plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
 Trick	Calls	Accepts	Attempts	Time (secs)

plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
 =====				
Stage : incr_opt				
 =====				
=====				
Message Summary				
=====				

Id Sev Count			Message Text	

CFM-1 Info 1 Wrote dofile.				

DA3 Logic synthesis & Physical design of restoring binary division algorithm

gate_comp	6	(0 /	0)	0.01
gcomp_mog	0	(0 /	0)	0.00
glob_area	17	(0 /	17)	0.00
area_down	0	(0 /	0)	0.00
size_n_buf	0	(0 /	0)	0.00
gate_deco_area	0	(0 /	0)	0.00

Incremental optimization status

Operation	Worst			Total	DRC	Total
	Total	Weighted	Neg Slk	Slack	Neg	Max Cap
init_delay	1515		0	0	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
crit_msz	0	(0 /	0)	0.00
crit_upsz	0	(0 /	0)	0.00
crit_slew	0	(0 /	0)	0.00
setup_dn	0	(0 /	0)	0.00
plc_bal_star	0	(0 /	0)	0.00
drc_buftimb	0	(0 /	0)	0.00
plc_st	0	(0 /	0)	0.00
plc_st_fence	0	(0 /	0)	0.00
plc_star	0	(0 /	0)	0.00
plc_laf_st	0	(0 /	0)	0.00
plc_laf_st_fence	0	(0 /	0)	0.00
drc_buftims	0	(0 /	0)	0.00
plc_laf_lo_st	0	(0 /	0)	0.00
plc_lo_st	0	(0 /	0)	0.00
fopt	0	(0 /	0)	0.00
crit_swap	0	(0 /	0)	0.00
mux2_swap	0	(0 /	0)	0.00
crit_dnsz	0	(0 /	0)	0.00
load_swap	0	(0 /	0)	0.00
fopt	0	(0 /	0)	0.00
setup_dn	0	(0 /	0)	0.00
load_isol	0	(0 /	0)	0.00
load_isol	0	(0 /	0)	0.00
move_for	0	(0 /	0)	0.00
move_for	0	(0 /	0)	0.00
rem_bi	0	(0 /	0)	0.00
offload	0	(0 /	0)	0.00
rem_bi	0	(0 /	0)	0.00
offload	0	(0 /	0)	0.00
phase	0	(0 /	0)	0.00
in_phase	0	(0 /	0)	0.00
merge_bit	0	(0 /	0)	0.00
merge_idrvr	0	(0 /	0)	0.00
merge_iload	0	(0 /	0)	0.00
merge_idload	0	(0 /	0)	0.00
merge_drvr	0	(0 /	0)	0.00
merge_load	0	(0 /	0)	0.00
decomp	0	(0 /	0)	0.00
p_decomp	0	(0 /	0)	0.00
levelize	0	(0 /	0)	0.00
mb_split	0	(0 /	0)	0.00
dup	0	(0 /	0)	0.00
mux_retime	0	(0 /	0)	0.00

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
| CFM-5 |Info| 1 |Wrote formal verification information.  
|  
| CPI-506 |Warning| 1 |Command 'commit_power_intent' cannot proceed  
as |  
| | | there is no power intent loaded.  
|  
| PA-7 |Info| 4 |Resetting power analysis results.  
|  
| | | All computed switching activities are removed.  
|  
| SYNTH-5 |Info| 1 |Done mapping.  
|  
| SYNTH-7 |Info| 1 |Incrementally optimizing.  
  
-----  
Info : Done incrementally optimizing. [SYNTH-8]  
      : Done incrementally optimizing 'restoring_division'.  
Finished SDC export (command execution time mm:ss (real) = 00:00).  
Info : Joules engine is used. [RPT-16]  
      : Joules engine is being used for the command report_power.  
Info : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0  
netlist  
      : restoring_division  
Info : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%  
Info : ACTP-0001 Activity propagation ended for stim#0  
Info : PWRA-0001 [PwrInfo] compute_power effective options  
      : -mode : vectorless  
      : -skip_propagation : 1  
      : -frequency_scaling_factor : 1.0  
      : -use_clock_freq : stim  
      : -stim :/stim#0  
      : -fromGenus : 1  
Info : ACTP-0001 Timing initialization started  
Info : ACTP-0001 Timing initialization ended  
Info : PWRA-0002 [PwrInfo] Skipping activity propagation due to -  
skip_ap  
      : option....  
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for  
vectorless  
      : flow. Ignoring frequency scaling.  
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with  
vectorless mode  
      : of power analysis, ignored this option.  
Info : PWRA-0002 Started 'vectorless' power computation.  
Info : PWRA-0009 [PwrInfo] Power Computation Progress Report : 100%  
Info : PWRA-0002 Finished power computation.  
Info : PWRA-0007 [PwrInfo] Completed successfully.  
      : Info=6, Warn=2, Error=0, Fatal=0  
Output file: DA3_power.rep  
WARNING: This version of the tool is 875 days old.  
legacy_genus:/>
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

Innovus Terminal:

```
[student@cad21 innovus]$ csh
[student@cad21 innovus]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 innovus]$ innovus
Cadence Innovus(TM) Implementation System.
Copyright 2021 Cadence Design Systems, Inc. All rights reserved
worldwide.

Version: v21.15-s110_1, built Fri Sep 23 13:08:12 PDT 2022
Options:
Date: Thu Nov 14 16:42:37 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64)
(12cores*20cpus*12th Gen Intel(R) Core(TM) i7-12700 25600KB)
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

License:
[16:42:37.095673] Configured Lic search path (21.01-s002):
5280@cadence

      invs Innovus Implementation System      21.1 checkout
succeeded
      8 CPU jobs allowed with the current license(s). Use
setMultiCpuUsage to set your required CPU count.
Create and set the environment variable TMPDIR to
/tmp/innovus_temp_38079_cad21_student_Igezgi.

Change the soft stacksize limit to 0.2%RAM (63 mbytes). Set global
soft_stack_size_limit to change the value.

**INFO: MMMC transition support version v31-84

[INFO] Loading PVS 22.20 fill procedures
innovus 1> #% Begin Load MMMC data ... (date=11/14 16:46:32, mem=1020.2M)
#% End Load MMMC data ... (date=11/14 16:46:32, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1020.9M, current mem=1020.9M)

Loading LEF file
../../../../install/FOUNDRY/digital/90nm/dig/lef/gsclib090_translated.lef
...
**WARN: (IMPLF-105): The layer 'Oxide' specified in SAMENET spacing
rule is neither a routing layer nor a cut layer. The rule is ignored.
**WARN: (IMPLF-105): The layer 'Poly' specified in SAMENET spacing
rule is neither a routing layer nor a cut layer. The rule is ignored.
Set DBUPERIGU to M2 pitch 580.
**WARN: (IMPLF-200): Pin 'A' in macro 'ANTENNA' has no ANTENNAGATEAREA
value defined. The library data is incomplete and some process antenna
rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.

## Check design process and node:
## Both design process and tech node are not set.

Loading view definition file from Default.view
Reading maxt timing library
'/home/install/FOUNDRY/digital/90nm/dig/lib/slow.lib' ...
Read 479 cells in library 'slow'
Reading mint timing library
'/home/install/FOUNDRY/digital/90nm/dig/lib/fast.lib' ...
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Read 479 cells in library 'fast'
*** End library_loading (cpu=0.01min, real=0.00min, mem=31.0M,
fe_cpu=0.61min, fe_real=3.92min, fe_mem=1063.2M) ***
#% Begin Load netlist data ... (date=11/14 16:46:32, mem=1042.7M)
*** Begin netlist parsing (mem=1063.2M) ***
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR3X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR3X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR3X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (EMS-27): Message (IMPVL-159) has exceeded the current
message display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
Created 479 new cells from 2 timing libraries.
Reading netlist ...
Backslashed names will retain backslash and a trailing blank character.
Reading verilog netlist 'DA3_netlist.v'

*** Memory Usage v#1 (Current mem = 1063.219M, initial mem = 483.863M)
***
*** End netlist parsing (cpu=0:00:00.0, real=0:00:00.0, mem=1063.2M) ***
#% End Load netlist data ... (date=11/14 16:46:32, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1056.8M, current mem=1056.8M)
Top level cell is restoring_division.
Hooked 958 DB cells to tlib cells.
Starting recursive module instantiation check.
No recursion found.
Building hierarchical netlist for Cell restoring_division ...
*** Netlist is unique.
** info: there are 968 modules.
** info: there are 157 stdCell insts.

*** Memory Usage v#1 (Current mem = 1119.633M, initial mem = 483.863M)
***
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
unless standard cell models of this type exist in the LEF/OA library.
Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 290 (derived)
Vertical Layer M2 offset = 290 (derived)
Start create_tracks
Generated pitch 0.29 in Metal8 is different from 0.87 defined in
technology file in unpreferred direction.
Extraction setup Started
Initializing multi-corner RC extraction with 1 active RC Corners ...
Reading Capacitance Table File
../../../../install/FOUNDRY/digital/90nm/dig/captable/gpdk090.lef.extende
d.CapTbl ...
Cap table was created using Encounter 05.20-s112_1.
Process name: gpdk090_91.
Importing multi-corner RC tables ...
Summary of Active RC-Corners :
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Analysis View: worst
  RC-Corner Name      : rc
  RC-Corner Index     : 0
  RC-Corner Temperature : 25 Celsius
  RC-Corner Cap Table  :
'.../.../.../install/FOUNDRY/digital/90nm/dig/captable/gpdk090.lef.extend
ed.CapTbl'
  RC-Corner PreRoute Res Factor      : 1
  RC-Corner PreRoute Cap Factor     : 1
  RC-Corner PostRoute Res Factor    : 1 {1 1 1}
  RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
  RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
  RC-Corner PreRoute Clock Res Factor : 1      [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PreRoute Clock Cap Factor : 1      [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}  [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}  [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}

Analysis View: best
  RC-Corner Name      : rc
  RC-Corner Index     : 0
  RC-Corner Temperature : 25 Celsius
  RC-Corner Cap Table  :
'.../.../.../install/FOUNDRY/digital/90nm/dig/captable/gpdk090.lef.extend
ed.CapTbl'
  RC-Corner PreRoute Res Factor      : 1
  RC-Corner PreRoute Cap Factor     : 1
  RC-Corner PostRoute Res Factor    : 1 {1 1 1}
  RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
  RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
  RC-Corner PreRoute Clock Res Factor : 1      [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PreRoute Clock Cap Factor : 1      [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}  [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}  [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
*Info: initialize multi-corner CTS.
Reading timing constraints file 'DA3.sdc' ...
Current (total cpu=0:00:36.9, real=0:03:56, peak res=1355.7M, current
mem=1355.7M)
**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
DA3.sdc, Line 9).

**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
DA3.sdc, Line 10).

restoring_division
INFO (CTE): Reading of timing constraints file DA3.sdc completed, with 2
WARNING
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Ending "Constraint file reading stats" (total cpu=0:00:00.0,
real=0:00:00.0, peak res=1363.4M, current mem=1363.4M)
Current (total cpu=0:00:36.9, real=0:03:56, peak res=1363.4M, current
mem=1363.4M)
Total number of combinational cells: 317
Total number of sequential cells: 152
Total number of tristate cells: 10
Total number of level shifter cells: 0
Total number of power gating cells: 0
Total number of isolation cells: 0
Total number of power switch cells: 0
Total number of pulse generator cells: 0
Total number of always on buffers: 0
Total number of retention cells: 0
List of usable buffers: BUFX2 BUFX12 BUFX16 BUFX20 CLKBUFX2 BUFX3 BUFX4
BUFX6 BUFX8 CLKBUFX12 CLKBUFX16 CLKBUFX20 CLKBUFX3 CLKBUFX4 CLKBUFX6
CLKBUFX8
Total number of usable buffers: 16
List of unusable buffers:
Total number of unusable buffers: 0
List of usable inverters: CLKINVX1 CLKINVX2 CLKINVX12 CLKINVX16 CLKINVX20
CLKINVX3 CLKINVX4 CLKINVX6 CLKINVX8 INVX1 INVX2 INVX12 INVX16 INVX20
INVXL INVX3 INVX4 INVX6 INVX8
Total number of usable inverters: 19
List of unusable inverters:
Total number of unusable inverters: 0
List of identified usable delay cells: DLY1X1 DLY1X4 DLY2X1 DLY2X4 DLY3X1
DLY3X4 DLY4X1 DLY4X4
Total number of identified usable delay cells: 8
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count  Summary
WARNING IMPLF-200      1  Pin '%s' in macro '%s' has no
ANTENNAGAT...
WARNING IMPLF-105      2  The layer '%s' specified in SAMENET
spac...
WARNING IMPFP-3961     2  The techSite '%s' has no related
standar...
WARNING IMPVLS-159     958  Pin '%s' of cell '%s' is defined in LEF
...
WARNING TCLCMD-1461     2  Skipped unsupported command: %s
*** Message Summary: 965 warning(s), 0 error(s)

innovus 1> Adjusting coreMargin left    to finFet grid (PlacementGrid) :
after adjusting :2.61
Adjusting coreMargin bottom  to finFet grid (PlacementGrid) : after
adjusting :2.61
Adjusting coreMargin right   to finFet grid (PlacementGrid) : after
adjusting :2.61
Adjusting coreMargin top     to finFet grid (PlacementGrid) : after
adjusting :2.61
Adjusting core size to PlacementGrid : width :49.01 height : 44.37
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
unless standard cell models of this type exist in the LEF/OA library.
Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 290 (derived)
Vertical Layer M2 offset = 290 (derived)
Start create_tracks
Generated pitch 0.29 in Metal8 is different from 0.87 defined in
technology file in unpreferred direction.
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

viaInitial starts at Thu Nov 14 16:47:43 2024
viaInitial ends at Thu Nov 14 16:47:43 2024
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1720.0M)
Ring generation is complete.
vias are now being generated.
addRing created 8 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+
| Metal5 |         4        |      NA       |
| Via5  |         8        |      0        |
| Metal6 |         4        |      NA       |
+-----+-----+
innovus 1> addStripe will allow jog to connect padcore ring and block
ring.

Stripes will stop at the boundary of the specified area.
When breaking rings, the power planner will consider the existence of
blocks.
Stripes will not extend to closest target.
The power planner will set stripe antenna targets to none (no trimming
allowed).
Stripes will not be created over regions without power planning wires.
The entire stripe set will break at the domain if one of the nets is not
in the domain.
addStripe will break automatically at non-default domains when generating
global stripes over the core area or default domain.
Offset for stripe breaking is set to 0.

Initialize fgc environment(mem: 1720.0M) ... fail and won't use fgc to
check drc(cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1720.0M)
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1720.0M)
Loading wires (cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1720.0M)
Loading via instances (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1720.0M)
Starting stripe generation ...
Non-Default Mode Option Settings :
    NONE
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Completing 10% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 20% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 30% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 40% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 50% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 60% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 70% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 80% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 90% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Completing 100% stripe generation(cpu: 0:00:00.0, real: 0:00:00.0, peak
mem: 1720.0M)
Stripe generation is complete.
vias are now being generated.
addStripe created 20 wires.
ViaGen created 40 vias, deleted 0 via to avoid violation.
+-----+
| Layer |     Created    |     Deleted   |
+-----+
| Via5  |        40       |         0      |
| Metal6 |        20       |        NA      |
+-----+
innovus 1> **WARN: (IMPSR-4058): Sroute option: blockPinTarget should be
used in conjunction with option: -connect blockPin.
*** Begin SPECIAL ROUTE on Thu Nov 14 16:48:15 2024 ***
SPECIAL ROUTE ran on directory: /home/student/Desktop/21bec1033/innovus
SPECIAL ROUTE ran on machine: cad21 (Linux 4.18.0-425.19.2.e18_7.x86_64
x86_64 2.10Ghz)

Begin option processing ...
srouteConnectPowerBump set to false
routeSelectNet set to "vdd vss"
routeSpecial set to true
srouteBottomLayerLimit set to 1
srouteBottomTargetLayerLimit set to 1
srouteConnectBlockPin set to false
srouteConnectConverterPin set to false
srouteConnectPadPin set to false
srouteConnectStripe set to false
srouteCrossoverViaBottomLayer set to 1
srouteCrossoverViaTopLayer set to 9
srouteFollowCorePinEnd set to 3
srouteFollowPadPin set to false
srouteJogControl set to "preferWithChanges differentLayer"
srouteNoViaOnWireShape set to "padring ring stripe blockring blockpin
coverpin blockwire corewire followpin iowire"
sroutePadPinAllPorts set to true
sroutePreserveExistingRoutes set to true
srouteRoutePowerBarPortOnBothDir set to true
srouteStopBlockPin set to "nearestTarget"
srouteTopLayerLimit set to 9
srouteTopTargetLayerLimit set to 9
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
End option processing: cpu: 0:00:00, real: 0:00:00, peak: 3222.00 megs.

Reading DB technology information...
Finished reading DB technology information.
Reading floorplan and netlist information...
Finished reading floorplan and netlist information.
Read in 19 layers, 9 routing layers, 1 overlap layer
Read in 2 nondefault rules, 0 used
Read in 487 macros, 26 used
Read in 25 components
    25 core components: 25 unplaced, 0 placed, 0 fixed
Read in 36 logical pins
Read in 36 nets
Read in 2 special nets, 2 routed
2 nets selected.

Begin power routing ...
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the vdd net.
    Run the globalNetConnect command or change the CPF file to ensure that
    the netlist reflects the correct power ground connections. The standard
    cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
    connection.
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the vss net.
    Run the globalNetConnect command or change the CPF file to ensure that
    the netlist reflects the correct power ground connections. The standard
    cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
    connection.
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vss.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vss.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vss.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
CPU time for vdd FollowPin 0 seconds
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vss.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
CPU time for vss FollowPin 0 seconds
    Number of Core ports routed: 36
    Number of Followpin connections: 18
End power routing: cpu: 0:00:00, real: 0:00:00, peak: 3224.00 megs.
```

```
Begin updating DB with routing results ...
Updating DB with 0 via definition ...Extracting standard cell pins and
blockage .....
Pin and blockage extraction finished
```

```
sroute created 54 wires.
ViaGen created 180 vias, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created   |     Deleted   |
+-----+-----+-----+
| Metall1 |      54       |      NA        |
| Vial    |      36       |      0         |
| Via2    |      36       |      0         |
| Via3    |      36       |      0         |
| Via4    |      36       |      0         |
| Via5    |      36       |      0         |
+-----+-----+-----+
*** placeDesign #1 [begin] : totSession cpu/real = 0:00:47.8/0:06:10.3
(0.1), mem = 1718.5M
**ERROR: (IMPSP-9099): Scan chains exist in this design but are not
defined for 29.63% flops. Placement and timing QoR can be severely
impacted in this case!
It is highly recommend to define scan chains either through input scan
def (preferred) or specifyScanChain.
Extracting standard cell pins and blockage .....
Pin and blockage extraction finished
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
*** Starting placeDesign default flow ***
*** Start deleteBufferTree ***
Info: Detect buffers to remove automatically.
Analyzing netlist ...
Updating netlist

*summary: 2 instances (buffers/inverters) removed
*** Finish deleteBufferTree (0:00:00.1) ***
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
Set Default Input Pin Transition as 1 ps.
**INFO: Analyzing IO path groups for slack adjustment
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Input Pin Transition as 0.1 ps.
Set Default Net Load as 0.5 pF.
**INFO: Pre-place timing setting for timing analysis already disabled
Deleted 0 physical inst (cell - / prefix -).
INFO: #ExclusiveGroups=0
INFO: There are no Exclusive Groups.
*** Starting "NanoPlace(TM) placement v#6 (mem=1822.0M)" ...
*** Build Buffered Sizing Timing Model
(cpu=0:00:00.8 mem=1825.0M) ***
*** Build Virtual Sizing Timing Model
(cpu=0:00:00.9 mem=1833.0M) ***
No user-set net weight.
Net fanout histogram:
2          : 71 (49.0%) nets
3          : 33 (22.8%) nets
4      -    14    : 37 (25.5%) nets
15     -    39    : 3 (2.1%) nets
40     -    79    : 1 (0.7%) nets
80     -   159    : 0 (0.0%) nets
160    -   319    : 0 (0.0%) nets
320    -   639    : 0 (0.0%) nets
640    -  1279    : 0 (0.0%) nets
1280   -  2559    : 0 (0.0%) nets
2560   -  5119    : 0 (0.0%) nets
5120+   : 0 (0.0%) nets
Options: timingDriven clkGateAware ignoreScan pinGuide congEffort=auto
gpeffort=medium
**WARN: (IMPSP-9042): Scan chains were not defined, -
place_global_ignore_scan option will be ignored.
Define the scan chains before using this option.
Type 'man IMPSP-9042' for more detail.
**WARN: (IMPDB-2078): Output pin Q of instance dp/quotient_reg[7]114 is
connected to ground net quotient[7]. Usually it is not right to connect
an output signal pin to a P/G net, unless the pin is meant to be the
driver of the net. This can create a short circuit if the output is
power. Check the connectivity in the netlist.
**WARN: (IMPDB-2078): Output pin Q of instance dp/quotient_reg[6]113 is
connected to ground net quotient[6]. Usually it is not right to connect
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/quotient_reg[5]112 is connected to ground net quotient[5]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/quotient_reg[4]111 is connected to ground net quotient[4]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/quotient_reg[3]110 is connected to ground net quotient[3]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/quotient_reg[2]109 is connected to ground net quotient[2]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/quotient_reg[1]108 is connected to ground net quotient[1]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/quotient_reg[0]107 is connected to ground net quotient[0]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/remainder_reg[7]122 is connected to ground net remainder[7]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/remainder_reg[6]121 is connected to ground net remainder[6]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/remainder_reg[5]120 is connected to ground net remainder[5]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/remainder_reg[4]119 is connected to ground net remainder[4]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/remainder_reg[3]118 is connected to ground net remainder[3]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/remainder_reg[2]117 is connected to ground net remainder[2]. Usually it is not right to connect

DA3 Logic synthesis & Physical design of restoring binary division algorithm

an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/remainder_reg[1]116 is connected to ground net remainder[1]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/remainder_reg[0]115 is connected to ground net remainder[0]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/A_reg[15]78 is connected to ground net is_negative. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/A_reg[14]77 is connected to ground net dp/A[14]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/A_reg[13]76 is connected to ground net dp/A[13]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (IMPDB-2078): Output pin Q of instance dp/A_reg[12]75 is connected to ground net dp/A[12]. Usually it is not right to connect an output signal pin to a P/G net, unless the pin is meant to be the driver of the net. This can create a short circuit if the output is power. Check the connectivity in the netlist.

**WARN: (EMS-27): Message (IMPDB-2078) has exceeded the current message display limit of 20.

To increase the message display limit, refer to the product command reference manual.

```
#std cell=156 (0 fixed + 156 movable) #buf cell=0 #inv cell=15 #block=0
(0 floating + 0 preplaced)
#ioInst=0 #net=145 #term=554 #term/net=3.82, #fixedIo=0, #floatIo=0,
#fixedPin=0, #floatPin=20
stdCell: 156 single + 0 double + 0 multi
Total standard cell length = 0.5794 (mm), area = 0.0015 (mm^2)
Average module density = 0.695.
Density for the design = 0.695.
    = stdcell_area 1998 sites (1512 um^2) / alloc_area 2873 sites
(2175 um^2).
Pin Density = 0.1928.
    = total # of pins 554 / total area 2873.
==== lastAutoLevel = 5
**WARN: (IMPDC-348): The output pin dp/\A_reg[8]71 /Q is connected to power/ground net dp/A[8]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.
**WARN: (IMPDC-348): The output pin dp/\A_reg[9]72 /Q is connected to power/ground net dp/A[9]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[10]73 /Q is connected to power/ground net dp/A[10]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[11]74 /Q is connected to power/ground net dp/A[11]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[12]75 /Q is connected to power/ground net dp/A[12]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[13]76 /Q is connected to power/ground net dp/A[13]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[14]77 /Q is connected to power/ground net dp/A[14]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[15]78 /Q is connected to power/ground net is_negative. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[8]71 /Q is connected to power/ground net dp/A[8]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[9]72 /Q is connected to power/ground net dp/A[9]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[10]73 /Q is connected to power/ground net dp/A[10]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[11]74 /Q is connected to power/ground net dp/A[11]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 1926.0MB
Summary Report:
Instances move: 156 (out of 156 movable)
Instances flipped: 0
Mean displacement: 3.10 um
Max displacement: 27.54 um (Instance: dp/remainder_reg[0]115) (45.53,
2.9095) -> (35.96, 20.88)
Length: 21 sites, height: 1 rows, site name: gsclib090site, cell
type: DFFQXL
Total net bbox length = 1.563e+03 (7.829e+02 7.802e+02) (ext = 1.949e+02)
Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 1926.0MB
*** Finished refinePlace (0:00:49.3 mem=1926.0M) ***
*** End of Placement (cpu=0:00:01.2, real=0:00:02.0, mem=1926.0M) ***
default core: bins with density > 0.750 = 25.00 % ( 1 / 4 )
Density distribution unevenness ratio = 4.039%
*** Free Virtual Timing Model ...(mem=1926.0M)
Starting IO pin assignment...
The design is not routed. Using placement based method for pin
assignment.
Completed IO pin assignment.
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
**INFO: Analyzing IO path groups for slack adjustment
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Info: Disable timing driven in postCTS congRepair.

Starting congRepair ...
[NR-eGR] Num Prerouted Nets = 0 Num Prerouted Wires = 0
[NR-eGR] Read 145 nets ( ignored 0 )
[NR-eGR] Layer group 1: route 145 net(s) in layer range [2, 9]
[NR-eGR] Early Global Route overflow of layer group 1: 0.00% H + 0.00% V.
EstWL: 1.970550e+03um
[NR-eGR] Overflow after Early Global Route 0.00% H + 0.00% V
Early Global Route congestion estimation runtime: 0.01 seconds, mem =
1909.2M
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00,
normalized total congestion hotspot area = 0.00 (area is in unit of 4
std-cell row bins)
Skipped repairing congestion.
[NR-eGR]          Length (um)    Vias
[NR-eGR] -----
[NR-eGR] Metal1   (1H)           0    534
[NR-eGR] Metal2   (2V)          1112   761
[NR-eGR] Metal3   (3H)           999    12
[NR-eGR] Metal4   (4V)           25     1
[NR-eGR] Metal5   (5H)            7     0
[NR-eGR] Metal6   (6V)           0     0
[NR-eGR] Metal7   (7H)           0     0
[NR-eGR] Metal8   (8V)           0     0
[NR-eGR] Metal9   (9H)           0     0
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[12]75 /Q is connected to power/ground net dp/A[12]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[13]76 /Q is connected to power/ground net dp/A[13]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[14]77 /Q is connected to power/ground net dp/A[14]. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

**WARN: (IMPDC-348): The output pin dp/\A_reg[15]78 /Q is connected to power/ground net is_negative. This can compromise the delay calculation. Fix the issue by correcting the netlist and rerun. An output pin should not be connected to a power/ground net. In some cases, the pin direction may be incorrect, correcting pin direction to input instead of output fixes the issue in these cases.

Clock gating cells determined by native netlist tracing.

Iteration 1: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
Est. stn bbox = 0.000e+00 (0.00e+00 0.00e+00)

cpu = 0:00:00.0 real = 0:00:00.0 mem = 1900.5M

Iteration 2: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
Est. stn bbox = 0.000e+00 (0.00e+00 0.00e+00)

cpu = 0:00:00.0 real = 0:00:00.0 mem = 1900.5M

Iteration 3: Total net bbox = 2.436e+01 (1.47e+01 9.68e+00)
Est. stn bbox = 3.617e+01 (2.18e+01 1.44e+01)

cpu = 0:00:00.0 real = 0:00:00.0 mem = 1902.0M

Active setup views:

worst

Iteration 4: Total net bbox = 7.343e+02 (4.71e+02 2.64e+02)
Est. stn bbox = 9.929e+02 (6.18e+02 3.75e+02)

cpu = 0:00:00.0 real = 0:00:00.0 mem = 1902.0M

Iteration 5: Total net bbox = 1.012e+03 (5.27e+02 4.84e+02)

Est. stn bbox = 1.328e+03 (6.93e+02 6.35e+02)

cpu = 0:00:00.0 real = 0:00:00.0 mem = 1902.0M

Iteration 6: Total net bbox = 1.344e+03 (7.58e+02 5.85e+02)

Est. stn bbox = 1.691e+03 (9.45e+02 7.46e+02)

cpu = 0:00:00.1 real = 0:00:01.0 mem = 1902.0M

*** cost = 1.344e+03 (7.58e+02 5.85e+02) (cpu for global=0:00:00.1)

real=0:00:01.0***

Info: 0 clock gating cells identified, 0 (on average) moved 0/1

Solver runtime cpu: 0:00:00.1 real: 0:00:00.1

Core Placement runtime cpu: 0:00:00.1 real: 0:00:01.0

**WARN: (IMPSP-9025): No scan chain specified/traced.

Type 'man IMPSP-9025' for more detail.

*** Starting refinePlace (0:00:49.3 mem=1902.0M) ***

Total net bbox length = 1.444e+03 (8.268e+02 6.170e+02) (ext = 2.867e+02)

Move report: Detail placement moves 156 insts, mean move: 3.10 um, max move: 27.54 um

Max move on inst (dp/remainder_reg[0]115): (45.53, 2.91) -->
(35.96, 20.88)

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
[NR-eGR] -----
[NR-eGR]           Total      2144  1308
[NR-eGR] -----
-----
[NR-eGR] Total half perimeter of net bounding box: 1538um
[NR-eGR] Total length: 2144um, number of vias: 1308
[NR-eGR] -----
-----
[NR-eGR] Total eGR-routed clock nets wire length: 0um, number of vias: 0
[NR-eGR] -----
-----
Early Global Route wiring runtime: 0.00 seconds, mem = 1891.2M
Tdg not successfully initied but do clear! skip clearing
End of congRepair (cpu=0:00:00.0, real=0:00:00.0)
*** Finishing placeDesign default flow ***
**ERROR: (IMPSP-9099): Scan chains exist in this design but are not
defined for 29.63% flops. Placement and timing QoR can be severely
impacted in this case!
It is highly recommend to define scan chains either through input scan
def (preferred) or specifyScanChain.
***** Total cpu 0:0:2
***** Total real time 0:0:2
**placeDesign ... cpu = 0: 0: 2, real = 0: 0: 2, mem = 1891.2M **
Tdg not successfully initied but do clear! skip clearing

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPDB-2078      48 Output pin %s of instance %s is
connecte...
WARNING IMPDC-1629      2 The default delay limit was set to %d.
T...
WARNING IMPDC-348       16 The output pin %s is connected to
power/...
WARNING IMPSP-9025       1 No scan chain specified/traced.
WARNING IMPSP-9042       1 Scan chains were not defined, -
place_glo...
ERROR   IMPSP-9099       2 Scan chains exist in this design but
are...
*** Message Summary: 68 warning(s), 2 error(s)

*** placeDesign #1 [finish] : cpu/real = 0:00:01.6/0:00:02.6 (0.6),
totSession cpu/real = 0:00:49.4/0:06:12.9 (0.1), mem = 1891.2M
innovus 1>
innovus 1> source ccopt.spec
Extracting original clock gating for clk...
clock_tree clk contains 54 sinks and 0 clock gates.
Extracting original clock gating for clk done.
The skew group clk/cont was created. It contains 54 sinks and 1 sources.
Checking clock tree convergence...
Checking clock tree convergence done.
innovus 2> saveDesign DBS/cts.encl
% Begin save design ... (date=11/14 16:50:46, mem=1773.4M)
% Begin Save ccopt configuration ... (date=11/14 16:50:46, mem=1773.4M)
% End Save ccopt configuration ... (date=11/14 16:50:46, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1774.1M, current mem=1774.1M)
% Begin Save netlist data ... (date=11/14 16:50:46, mem=1774.1M)
Writing Binary DB to DBS/cts.encl.dat/restoring_division.v.bin in single-
threaded mode...
% End Save netlist data ... (date=11/14 16:50:46, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1774.8M, current mem=1774.8M)
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
setNanoRouteMode -droutePostRouteWidenWireRule
LEFDefaultRouteSpec_gdk090
setNanoRouteMode -extractThirdPartyCompatible false
setNanoRouteMode -routeBottomRoutingLayer 1
setNanoRouteMode -routeTopRoutingLayer 9
setNanoRouteMode -routeWithSiDriven false
setNanoRouteMode -routeWithTimingDriven false
setNanoRouteMode -timingEngine {}
setExtractRCMode -engine preRoute
setDelayCalMode -engine aae
setDelayCalMode -ignoreNetLoad false

/**INFO: multi-cut via swapping will not be performed after routing.
/**INFO: All auto set options tuned by routeDesign will be restored to
their original settings on command completion.
Begin checking placement ... (start mem=1931.0M, init mem=1931.0M)
*info: Placed = 156
*info: Unplaced = 0
Placement Density:69.54%(1512/2175)
Placement Density (including fixed std cells):69.54%(1512/2175)
Finished checkPlace (total: cpu=0:00:00.0, real=0:00:00.0; vio checks:
cpu=0:00:00.0, real=0:00:00.0; mem=1931.0M)

changeUseClockNetStatus Option : -noFixedNetWires
*** Changed status on (0) nets in Clock.
*** End changeUseClockNetStatus (cpu=0:00:00.0, real=0:00:00.0,
mem=1931.0M) ***

globalDetailRoute

#Start globalDetailRoute on Thu Nov 14 16:50:59 2024
#
#WARNING (NRIG-1303) The congestion map does not match the GCELL grid.
Clearing the map.
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
#num needed restored net=0
#need_extraction net=0 (total=180)
#WARNING (NRDB-2005) SPECIAL_NET vdd has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#WARNING (NRDB-2005) SPECIAL_NET vss has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Total number of trivial nets (e.g. < 2 pins) = 11 (skipped).
#Total number of routable nets = 169.
#Total number of nets in the design = 180.
#169 routable nets do not have any wires.
#169 nets will be global routed.
#Start routing data preparation on Thu Nov 14 16:50:59 2024
#
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.100.
#Voltage range [0.000 - 1.100] has 154 nets.
#Voltage range [0.000 - 0.000] has 25 nets.
#Voltage range [0.900 - 1.100] has 1 net.
#Build and mark too close pins for the same net.
#Rebuild pin access data for design.
#Initial pin access analysis.
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
Saving symbol-table file ...
Saving congestion map file
DBS/cts.encl.dat/restoring_division.route.congmap.gz ...
% Begin Save AAE data ... (date=11/14 16:50:46, mem=1775.3M)
Saving AAE Data ...
% End Save AAE data ... (date=11/14 16:50:46, total cpu=0:00:00.0,
real=0:00:01.0, peak res=1775.3M, current mem=1775.3M)
Saving preference file DBS/cts.encl.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=11/14 16:50:47, mem=1777.2M)
Saving floorplan file ...
% End Save floorplan data ... (date=11/14 16:50:47, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1777.2M, current mem=1777.2M)
Saving Drc markers ...
... No Drc file written since there is no markers found.
% Begin Save placement data ... (date=11/14 16:50:47, mem=1777.2M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=11/14 16:50:47, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1777.5M, current mem=1777.5M)
% Begin Save routing data ... (date=11/14 16:50:47, mem=1777.5M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1893.3M) ***
% End Save routing data ... (date=11/14 16:50:47, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1777.8M, current mem=1777.8M)
Saving property file DBS/cts.encl.dat/restoring_division.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1896.3M) ***
% Begin Save power constraints data ... (date=11/14 16:50:47,
mem=1779.0M)
% End Save power constraints data ... (date=11/14 16:50:47, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1779.0M, current mem=1779.0M)
Generated self-contained design cts.encl.dat
#%% End save design ... (date=11/14 16:50:47, total cpu=0:00:00.2,
real=0:00:01.0, peak res=1807.9M, current mem=1781.8M)
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 3> #WARNING (NRIF-91) Option setNanoRouteMode -
routeTopRoutingLayer is obsolete. It will continue to work for the
current release. To ensure compatibility with future releases, use option
setDesignMode -topRoutingLayer instead.
#WARNING (NRIF-90) Option setNanoRouteMode -routeBottomRoutingLayer is
obsolete. It will continue to work for the current release. To ensure
compatibility with future releases, use option setDesignMode -
bottomRoutingLayer instead.
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory =
1783.62 (MB), peak = 1807.89 (MB)
AAE_INFO: Pre Route call back at the beginning of routeDesign
###INFO: setDesignMode -flowEffort standard
###INFO: setDesignMode -powerEffort none
#WARNING (NRIG-96) Selected single pass global detail route "-"
globalDetail". Clock eco and post optimizations will not be run. See "man
NRIG-96" for more details.
#WARNING (NRIG-144) Cannot combine -viaOpt with -globalDetail option. The
-viaOpt will be ignored.
##INFO: User settings:
setNanoRouteMode -drouteEndIteration          1
setNanoRouteMode -droutePostRouteSpreadWire   1
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
#Detail pin access analysis.
# Metal1      H  Track-Pitch = 0.29000      Line-2-Via Pitch = 0.25500
# Metal2      V  Track-Pitch = 0.29000      Line-2-Via Pitch = 0.28500
# Metal3      H  Track-Pitch = 0.29000      Line-2-Via Pitch = 0.28500
# Metal4      V  Track-Pitch = 0.29000      Line-2-Via Pitch = 0.28500
# Metal5      H  Track-Pitch = 0.29000      Line-2-Via Pitch = 0.28500
# Metal6      V  Track-Pitch = 0.29000      Line-2-Via Pitch = 0.28500
# Metal7      H  Track-Pitch = 0.29000      Line-2-Via Pitch = 0.28500
# Metal8      V  Track-Pitch = 0.87000      Line-2-Via Pitch = 0.85000
# Metal9      H  Track-Pitch = 0.87000      Line-2-Via Pitch = 0.85000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1791.04 (MB),
peak = 1824.32 (MB)
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.29000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:01, elapsed time = 00:00:01, memory = 1795.52 (MB),
peak = 1824.32 (MB)
#
#Finished routing data preparation on Thu Nov 14 16:51:00 2024
#
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 10.55 (MB)
#Total memory = 1795.52 (MB)
#Peak memory = 1824.32 (MB)
#
#
#Start global routing on Thu Nov 14 16:51:00 2024
#
#
#Start global routing initialization on Thu Nov 14 16:51:00 2024
#
#Number of eco nets is 0
#
#Start global routing data preparation on Thu Nov 14 16:51:00 2024
#
#Start routing resource analysis on Thu Nov 14 16:51:00 2024
#
#Routing resource analysis is done on Thu Nov 14 16:51:00 2024
#
# Resource Analysis:
#
#          Routing #Avail      #Track      #Total      %Gcell
#  Layer    Direction Track     Blocked     Gcell     Blocked
# -----
#  Metal1      H        32       139       132      58.33%
#  Metal2      V       172       15       132      0.00%
#  Metal3      H       157       14       132      0.00%
#  Metal4      V       173       14       132      0.00%
#  Metal5      H       145       26       132      0.00%
#  Metal6      V        99       88       132      0.00%
#  Metal7      H       171        0       132      0.00%
#  Metal8      V        62        0       132      0.00%
#  Metal9      H        56        0       132      0.00%
# -----
#  Total           1067     18.55%      1188      6.48%
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

# Metal6      0(0.00%) (0.00%)
# Metal7      0(0.00%) (0.00%)
# Metal8      0(0.00%) (0.00%)
# Metal9      0(0.00%) (0.00%)
#
# -----
#     Total    0(0.00%) (0.00%)
#
# The worst congested Gcell overcon (routing demand over resource in
# number of tracks) = 1
# Overflow after GR: 0.00% H + 0.00% V
#
# Hotspot report including placement blocked areas
[hotspot] +-----+-----+-----+
[hotspot] |      layer      | max hotspot | total hotspot |
[hotspot bbox] |           |           |           |
[hotspot] +-----+-----+-----+
[hotspot] |      Metal1(H)   |           | 1.00 | 1.00 |
52.20 10.44 54.23 20.88 |
[hotspot] |      Metal2(V)   |           | 0.00 | 0.00 |
(none) |           |           |           |
[hotspot] |      Metal3(H)   |           | 0.00 | 0.00 |
(none) |           |           |           |
[hotspot] |      Metal4(V)   |           | 0.00 | 0.00 |
(none) |           |           |           |
[hotspot] |      Metal5(H)   |           | 0.00 | 0.00 |
(none) |           |           |           |
[hotspot] |      Metal6(V)   |           | 0.00 | 0.00 |
(none) |           |           |           |
[hotspot] |      Metal7(H)   |           | 0.00 | 0.00 |
(none) |           |           |           |
[hotspot] |      Metal8(V)   |           | 0.00 | 0.00 |
(none) |           |           |           |
[hotspot] |      Metal9(H)   |           | 0.00 | 0.00 |
(none) |           |           |           |
[hotspot] +-----+-----+-----+
[hotspot] |      worst      | (Metal1)   | 1.00 | (Metal1)   | 1.00 |
|
[hotspot] +-----+-----+-----+
[hotspot] |      all layers  |           | 0.00 | 0.00 |
|
[hotspot] +-----+-----+-----+
Local HotSpot Analysis (blockage included) (3d): normalized congestion
max/total hotspot area = 0.00/0.00 (area is in unit of 4 std-cell row
bins)
#Complete Global Routing.
#Total wire length = 2354 um.
#Total half perimeter of net bounding box = 2189 um.
#Total wire length on LAYER Metal1 = 0 um.
#Total wire length on LAYER Metal2 = 1293 um.
#Total wire length on LAYER Metal3 = 1013 um.
#Total wire length on LAYER Metal4 = 35 um.
#Total wire length on LAYER Metal5 = 13 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
#  
#  
#  
#  
#Global routing data preparation is done on Thu Nov 14 16:51:00 2024  
#  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1795.82 (MB),  
peak = 1824.32 (MB)  
#  
#  
#Global routing initialization is done on Thu Nov 14 16:51:00 2024  
#  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1795.82 (MB),  
peak = 1824.32 (MB)  
#  
#start global routing iteration 1...  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1797.27 (MB),  
peak = 1824.32 (MB)  
#  
#start global routing iteration 2...  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1797.27 (MB),  
peak = 1824.32 (MB)  
#  
#  
#Total number of trivial nets (e.g. < 2 pins) = 11 (skipped).  
#Total number of routable nets = 169.  
#Total number of nets in the design = 180.  
#  
#169 routable nets have routed wires.  
#  
#Routed nets constraints summary:  
#-----  
#      Rules    Unconstrained  
#-----  
#      Default        169  
#-----  
#      Total         169  
#-----  
#  
#Routing constraints summary of the whole design:  
#-----  
#      Rules    Unconstrained  
#-----  
#      Default        169  
#-----  
#      Total         169  
#-----  
#  
#  
# Congestion Analysis: (blocked Gcells are excluded)  
#  
#          OverCon  
#          #Gcell    %Gcell  
#      Layer        (1)    OverCon  
# -----  
#  Metal1        0 (0.00%)  (0.00%)  
#  Metal2        0 (0.00%)  (0.00%)  
#  Metal3        0 (0.00%)  (0.00%)  
#  Metal4        0 (0.00%)  (0.00%)  
#  Metal5        0 (0.00%)  (0.00%)
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 879
#Up-Via Summary (total 879):
#
#-----
# Metal1      574
# Metal2      296
# Metal3       7
# Metal4       2
#-----
#                      879
#
#Max overcon = 0 track.
#Total overcon = 0.00%.
#Worst layer Gcell overcon rate = 0.00%.
#
#Global routing statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 2.04 (MB)
#Total memory = 1797.57 (MB)
#Peak memory = 1824.32 (MB)
#
#Finished global routing on Thu Nov 14 16:51:00 2024
#
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1797.57 (MB),
peak = 1824.32 (MB)
#Start Track Assignment.
#Done with 201 horizontal wires in 1 hboxes and 260 vertical wires in 1
hboxes.
#Done with 39 horizontal wires in 1 hboxes and 61 vertical wires in 1
hboxes.
#Done with 1 horizontal wires in 1 hboxes and 1 vertical wires in 1
hboxes.
#
#Track assignment summary:
# layer      (wire length)      (overlap)      (long ovlp)      (with obs/pg/clk)
#-----
# Metal1      0.00    0.00%    0.00%    0.00%
# Metal2     1275.45   0.05%    0.00%    0.00%
# Metal3      971.42   0.13%    0.00%    0.00%
# Metal4      36.10    0.00%    0.00%    0.00%
# Metal5      13.34    0.00%    0.00%    0.00%
# Metal6      0.00    0.00%    0.00%    0.00%
# Metal7      0.00    0.00%    0.00%    0.00%
# Metal8      0.00    0.00%    0.00%    0.00%
# Metal9      0.00    0.00%    0.00%    0.00%
#-----
# All        2296.30   0.09%    0.00%    0.00%
#Complete Track Assignment.
#Total wire length = 2289 um.
#Total half perimeter of net bounding box = 2189 um.
#Total wire length on LAYER Metal1 = 0 um.
#Total wire length on LAYER Metal2 = 1271 um.
#Total wire length on LAYER Metal3 = 969 um.
#Total wire length on LAYER Metal4 = 36 um.
#Total wire length on LAYER Metal5 = 13 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
#  
#Start DRC checking..  
#   number of violations = 0  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1798.27 (MB),  
peak = 1828.92 (MB)  
#CELL_VIEW restoring_division,init has no DRC violation.  
#Total number of DRC violations = 0  
#Total number of process antenna violations = 0  
#Total number of net violated process antenna rule = 0  
#  
#Start data preparation for wire spreading...  
#  
#Data preparation is done on Thu Nov 14 16:51:00 2024  
#  
#  
#Start Post Route Wire Spread.  
#Done with 25 horizontal wires in 1 hboxes and 38 vertical wires in 1  
hboxes.  
#Complete Post Route Wire Spread.  
#  
#Total wire length = 2813 um.  
#Total half perimeter of net bounding box = 2189 um.  
#Total wire length on LAYER Metal1 = 177 um.  
#Total wire length on LAYER Metal2 = 1498 um.  
#Total wire length on LAYER Metal3 = 982 um.  
#Total wire length on LAYER Metal4 = 141 um.  
#Total wire length on LAYER Metal5 = 15 um.  
#Total wire length on LAYER Metal6 = 0 um.  
#Total wire length on LAYER Metal7 = 0 um.  
#Total wire length on LAYER Metal8 = 0 um.  
#Total wire length on LAYER Metal9 = 0 um.  
#Total number of vias = 1037  
#Up-Via Summary (total 1037):  
#-----  
# Metal1      634  
# Metal2      376  
# Metal3      25  
# Metal4      2  
#-----  
#                  1037  
#  
#  
#Start DRC checking..  
#   number of violations = 0  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1798.23 (MB),  
peak = 1828.92 (MB)  
#CELL_VIEW restoring_division,init has no DRC violation.  
#Total number of DRC violations = 0  
#Total number of process antenna violations = 0  
#Total number of net violated process antenna rule = 0  
#   number of violations = 0  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1798.23 (MB),  
peak = 1828.92 (MB)  
#CELL_VIEW restoring_division,init has no DRC violation.  
#Total number of DRC violations = 0  
#Total number of process antenna violations = 0  
#Total number of net violated process antenna rule = 0  
#Post Route wire spread is done.  
#Total wire length = 2813 um.
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 879
#Up-Via Summary (total 879):
#
#-----
# Metal1      574
# Metal2      296
# Metal3       7
# Metal4       2
#-----
#                   879
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1797.70 (MB),
peak = 1824.32 (MB)
#
#Routing data preparation, pin analysis, global routing and track
assignment statistics:
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 12.72 (MB)
#Total memory = 1797.70 (MB)
#Peak memory = 1824.32 (MB)
#
#Start Detail Routing..
#start initial detail routing ...
#   number of violations = 0
#cpu time = 00:00:01, elapsed time = 00:00:01, memory = 1798.13 (MB),
peak = 1828.92 (MB)
#Complete Detail Routing.
#Total wire length = 2783 um.
#Total half perimeter of net bounding box = 2189 um.
#Total wire length on LAYER Metal1 = 177 um.
#Total wire length on LAYER Metal2 = 1481 um.
#Total wire length on LAYER Metal3 = 968 um.
#Total wire length on LAYER Metal4 = 141 um.
#Total wire length on LAYER Metal5 = 15 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 1037
#Up-Via Summary (total 1037):
#
#-----
# Metal1      634
# Metal2      376
# Metal3       25
# Metal4       2
#-----
#                   1037
#
#Total number of DRC violations = 0
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 0.43 (MB)
#Total memory = 1798.13 (MB)
#Peak memory = 1828.92 (MB)
#
#Start Post Route wire spreading..
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
#Total half perimeter of net bounding box = 2189 um.
#Total wire length on LAYER Metal1 = 177 um.
#Total wire length on LAYER Metal2 = 1498 um.
#Total wire length on LAYER Metal3 = 982 um.
#Total wire length on LAYER Metal4 = 141 um.
#Total wire length on LAYER Metal5 = 15 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 1037
#Up-Via Summary (total 1037):
#
#-----
# Metall      634
# Metal2     376
# Metal3      25
# Metal4       2
#-----
#                  1037
#
#detailRoute Statistics:
#Cpu time = 00:00:01
#Elapsed time = 00:00:01
#Increased memory = 0.53 (MB)
#Total memory = 1798.23 (MB)
#Peak memory = 1828.92 (MB)
#    no debugging net set
#
#globalDetailRoute statistics:
#Cpu time = 00:00:02
#Elapsed time = 00:00:02
#Increased memory = 20.16 (MB)
#Total memory = 1804.20 (MB)
#Peak memory = 1828.92 (MB)
#Number of warnings = 3
#Total number of warnings = 7
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Thu Nov 14 16:51:00 2024
#
#Default setup view is reset to worst.

detailRoute

#Start detailRoute on Thu Nov 14 16:51:01 2024
#
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
#num needed restored net=0
#need_extraction net=0 (total=180)
#WARNING (NRDB-2005) SPECIAL_NET vdd has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#WARNING (NRDB-2005) SPECIAL_NET vss has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Start routing data preparation on Thu Nov 14 16:51:01 2024
#
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
#-----
#          1037
#
#      number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1812.75 (MB),
peak = 1828.92 (MB)
#CELL_VIEW restoring_division,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#Post Route wire spread is done.
#Total wire length = 2816 um.
#Total half perimeter of net bounding box = 2189 um.
#Total wire length on LAYER Metal1 = 177 um.
#Total wire length on LAYER Metal2 = 1500 um.
#Total wire length on LAYER Metal3 = 983 um.
#Total wire length on LAYER Metal4 = 141 um.
#Total wire length on LAYER Metal5 = 15 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 1037
#Up-Via Summary (total 1037):
#
#-----
# Metall1      634
# Metal2      376
# Metal3       25
# Metal4        2
#-----
#
#          1037
#
#      no debugging net set
#
#detailRoute statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 3.75 (MB)
#Total memory = 1808.12 (MB)
#Peak memory = 1828.92 (MB)
#Number of warnings = 2
#Total number of warnings = 9
#Number of fails = 0
#Total number of fails = 0
#Complete detailRoute on Thu Nov 14 16:51:01 2024
#
#Default setup view is reset to worst.
AAE_INFO: Post Route call back at the end of routeDesign
#routeDesign: cpu time = 00:00:02, elapsed time = 00:00:02, memory =
1808.17 (MB), peak = 1828.92 (MB)
*** Message Summary: 0 warning(s), 0 error(s)

innovus 3> **WARN: (IMPSP-5217): addFiller command is running on a
postRoute database. It is recommended to be followed by ecoRoute -target
command to make the DRC clean.
Type 'man IMPSP-5217' for more detail.
*INFO: Adding fillers to top-module.
*INFO: Added 2 filler insts (cell FILL64 / prefix FILLER).
*INFO: Added 2 filler insts (cell FILL32 / prefix FILLER).
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.100.
#Voltage range [0.000 - 1.100] has 154 nets.
#Voltage range [0.000 - 0.000] has 25 nets.
#Voltage range [0.900 - 1.100] has 1 net.
#Build and mark too close pins for the same net.
#Initial pin access analysis.
#Detail pin access analysis.
# Metal1      H  Track-Pitch = 0.29000   Line-2-Via Pitch = 0.25500
# Metal2      V  Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal3      H  Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal4      V  Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal5      H  Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal6      V  Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal7      H  Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal8      V  Track-Pitch = 0.87000   Line-2-Via Pitch = 0.85000
# Metal9      H  Track-Pitch = 0.87000   Line-2-Via Pitch = 0.85000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1808.95 (MB),
peak = 1828.92 (MB)
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.29000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1812.74 (MB),
peak = 1828.92 (MB)
#
#Start Post Route wire spreading..
#
#Start data preparation for wire spreading...
#
#Data preparation is done on Thu Nov 14 16:51:01 2024
#
#
#Start Post Route Wire Spread.
#Done with 6 horizontal wires in 1 hboxes and 12 vertical wires in 1
hboxes.
#Complete Post Route Wire Spread.
#
#Total wire length = 2816 um.
#Total half perimeter of net bounding box = 2189 um.
#Total wire length on LAYER Metal1 = 177 um.
#Total wire length on LAYER Metal2 = 1500 um.
#Total wire length on LAYER Metal3 = 983 um.
#Total wire length on LAYER Metal4 = 141 um.
#Total wire length on LAYER Metal5 = 15 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 1037
#Up-Via Summary (total 1037):
#
#-----
# Metal1      634
# Metal2      376
# Metal3      25
# Metal4      2
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```
*INFO: Added 13 filler insts (cell FILL16 / prefix FILLER).
*INFO: Added 28 filler insts (cell FILL8 / prefix FILLER).
*INFO: Added 37 filler insts (cell FILL4 / prefix FILLER).
*INFO: Added 32 filler insts (cell FILL2 / prefix FILLER).
*INFO: Added 39 filler insts (cell FILL1 / prefix FILLER).
*INFO: Total 153 filler insts added - prefix FILLER (CPU: 0:00:00.0).
For 153 new insts, innovus 3> Performing RC Extraction ...
Extraction called for design 'restoring_division' of instances=309 and
nets=180 using extraction engine 'preRoute' .
**WARN: (IMPEXT-3530): The process node is not set. Use the command
setDesignMode -process <process node> prior to extraction for maximum
accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design restoring_division.
RC Extraction called in multi-corner(1) mode.
RCMode: PreRoute
    RC Corner Indexes          0
Capacitance Scaling Factor   : 1.00000
Resistance Scaling Factor   : 1.00000
Clock Cap. Scaling Factor   : 1.00000
Clock Res. Scaling Factor   : 1.00000
Shrink Factor               : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0
MEM: 1982.289M)
innovus 3> Writing Netlist "restoring_division.v" ...
innovus 3> #% Begin save design ... (date=11/14 16:52:02, mem=1811.9M)
% Begin Save ccopt configuration ... (date=11/14 16:52:02, mem=1811.9M)
% End Save ccopt configuration ... (date=11/14 16:52:02, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1812.2M, current mem=1812.2M)
% Begin Save netlist data ... (date=11/14 16:52:02, mem=1812.2M)
Writing Binary DB to restoring_division.enc.dat/restoring_division.v.bin
in single-threaded mode...
% End Save netlist data ... (date=11/14 16:52:02, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1812.3M, current mem=1812.3M)
Saving symbol-table file ...
Saving congestion map file
restoring_division.enc.dat/restoring_division.route.congmap.gz ...
% Begin Save AAE data ... (date=11/14 16:52:02, mem=1812.3M)
Saving AAE Data ...
% End Save AAE data ... (date=11/14 16:52:02, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1812.3M, current mem=1812.3M)
Saving preference file restoring_division.enc.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=11/14 16:52:02, mem=1812.7M)
Saving floorplan file ...
% End Save floorplan data ... (date=11/14 16:52:02, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1812.7M, current mem=1812.7M)
Saving Drc markers ...
... No Drc file written since there is no markers found.
% Begin Save placement data ... (date=11/14 16:52:02, mem=1812.7M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=11/14 16:52:02, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1812.7M, current mem=1812.7M)
```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

132	Via6
131	Via6
130	Via6
129	Via6
128	Via6
127	Via6
122	Metal6
121	Metal6
120	Metal6
119	Metal6
118	Metal6
53	Metal3
52	Metal3
185	Metal9
48	Via2
29	Metal2
180	Metal9
47	Via2
182	Metal9
44	Via2
43	Via2
172	Via8
38	Metal2
95	Metal5
36	Metal2
93	Metal5
112	Via5
55	Metal3
113	Metal6
32	Metal2
54	Metal3
31	Metal2
107	Via5
30	Metal2
49	Via2
106	Via5
33	Metal2
109	Via5
10	Metal1
86	Via4
50	Metal3
69	Via3
143	Metal7
6	Cont
169	Via8
35	Metal2
8	Metal1
164	Metal8
27	Vial
141	Metal7
3	Cont
51	Metal3
70	Via3
7	Cont
64	Via3
173	Via8
34	Metal2
92	Metal5
111	Via5
11	Metal1

DA3 Logic synthesis & Physical design of restoring binary division algorithm

```

% Begin Save routing data ... (date=11/14 16:52:02, mem=1812.7M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1977.8M) ***
% End Save routing data ... (date=11/14 16:52:02, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1812.9M, current mem=1812.9M)
Saving property file restoring_division.enc.dat/restoring_division.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1980.8M) ***
#Saving pin access data to file
restoring_division.enc.dat/restoring_division.apa ...
#
% Begin Save power constraints data ... (date=11/14 16:52:02,
mem=1812.9M)
% End Save power constraints data ... (date=11/14 16:52:02, total
cpu=0:00:00.0, real=0:00:01.0, peak res=1812.9M, current mem=1812.9M)
Generated self-contained design restoring_division.enc.dat
#% End save design ... (date=11/14 16:52:03, total cpu=0:00:00.2,
real=0:00:01.0, peak res=1843.3M, current mem=1813.5M)
*** Message Summary: 0 warning(s), 0 error(s)

Parse flat map file...
Writing GDSII file ...
***** db unit per micron = 2000 *****
***** output gds2 file unit per micron = 2000 *****
***** unit scaling factor = 1 *****

Output for instance
Output for bump
Output for physical terminals
Output for logical terminals
Output for regular nets
Output for special nets and metal fills
Output for via structure generation total number 12
Statistics for GDS generated (version 3)
-----
Stream Out Layer Mapping Information:
GDS Layer Number          GDS Layer Name
-----
 191                      COMP
 192                      DIEAREA
 181                      Metal9
 179                      Metal9
 178                      Metal9
 177                      Metal9
 176                      Metal9
 175                      Via8
 174                      Via8
 170                      Via8
 160                      Metal8
 158                      Metal8
 157                      Metal8
 156                      Metal8
 155                      Metal8
 154                      Via7
 153                      Via7
 149                      Via7
 139                      Metal17
 137                      Metal17
 136                      Metal17
 135                      Metal17
 134                      Metal17
 133                      Via6

```

DA3 Logic synthesis & Physical design of restoring binary division algorithm

142	Metal7
4	Cont
9	Metal1
28	Vial
85	Via4
138	Metal7
5	Cont
12	Metal1
88	Via4
183	Metal9
45	Via2
22	Vial
152	Via7
13	Metal1
71	Metal4
90	Via4
184	Metal9
46	Via2
161	Metal8
23	Vial
171	Via8
37	Metal2
94	Metal5
148	Via7
14	Metal1
15	Metal1
72	Metal4
91	Via4
150	Via7
16	Metal1
73	Metal4
159	Metal8
26	Vial
151	Via7
17	Metal1
74	Metal4
1	Cont
162	Metal8
24	Vial
140	Metal7
2	Cont
163	Metal8
25	Vial
56	Metal3
57	Metal3
114	Metal6
58	Metal3
115	Metal6
59	Metal3
116	Metal6
65	Via3
66	Via3
67	Via3
68	Via3
75	Metal4
76	Metal4
77	Metal4
78	Metal4
79	Metal4
80	Metal4

DA3 Logic synthesis & Physical design of restoring binary division algorithm

87	Via4
89	Via4
96	Metal5
97	Metal5
98	Metal5
99	Metal5
100	Metal5
101	Metal5
108	Via5
110	Via5
117	Metal6
189	Metal9
188	Metal9
187	Metal9
186	Metal9
168	Metal8
167	Metal8
166	Metal8
165	Metal8
147	Metal7
146	Metal7
145	Metal7
144	Metal7
63	Metal3
62	Metal3
39	Metal2
105	Metal5
103	Metal5
123	Metal6
42	Metal2
41	Metal2
40	Metal2
20	Metal1
60	Metal3
18	Metal1
61	Metal3
102	Metal5
21	Metal1
19	Metal1
81	Metal4
104	Metal5
82	Metal4
83	Metal4
84	Metal4
124	Metal6
125	Metal6
126	Metal6

Stream Out Information Processed for GDS version 3:
Units: 2000 DBU

Object	Count
<hr/>	
Instances	309
<hr/>	
Ports/Pins	36
metal layer Metal2	16
metal layer Metal3	15
metal layer Metal4	3

DA3 Logic synthesis & Physical design of restoring binary division algorithm

metal layer Metal5	2
Nets	1585
metal layer Metal1	124
metal layer Metal2	1051
metal layer Metal3	392
metal layer Metal4	16
metal layer Metal5	2
Via Instances	1037
Special Nets	82
metal layer Metal1	54
metal layer Metal5	4
metal layer Metal6	24
Via Instances	228
Metal Fills	0
Via Instances	0
Metal FillOPCs	0
Via Instances	0
Metal FillDRCs	0
Via Instances	0
Text	207
metal layer Metal1	18
metal layer Metal2	127
metal layer Metal3	50
metal layer Metal4	7
metal layer Metal5	3
metal layer Metal6	2
Blockages	0
Custom Text	0
Custom Box	0
Trim Metal	0
#####Streamout is finished!	
innovus 3>	

Inference: A total of 152 leaf instance count is present in the gate level netlist with total area of 1514.4, total power of 33 uW.

Result: Hence a restoring binary division algorithm is verified and it was synthesized and the gate level netlist with timing,area and power report was generate successfully. Also the physical design was also built successfully.

