Course Code	Course Title	L	T	P	C
BECE407E	ASIC Design	2	0	2	3
Pre-requisite	BECE303L, BECE303P	Syllabus version			
	`	1.0			

Course Objectives

1. Explain the HDL coding guidelines, synthesizable HDL constructs and RTL synthesis Flow with respect to different cost functions.
2. Teach how to perform Static Timing Analysis for ASIC design.
3. Discuss the guidelines at each abstraction level in physical design
4. Provide detailed insight on importance of physical design verification

Course Outcomes

At the end of the course the student will be able to

1. Design a digital system by adhering to synthesizable HDL constructs.
2. Synthesize the given design by considering various constraints and to optimize the same.
3. Understand various timing parameters and perform Static Timing Analysis for ASIC design
4. Perform physical design by adhering to guidelines.
5. Apprehend the importance of physical design verification.
6. Design ASIC based systems using industry standard tools.

Module:1	**ASIC Design Methodology & Design Flow**	**3 hours**

Implementation Strategies for Digital ICs: Custom IC Design- Cell-based Design Methodology - Array based implementation approaches - Traditional and Physical Compiler based ASIC Flow.

Module:2	**Verilog HDL Coding Style for Synthesis**	**6 hours**

HDL Coding style – Guidelines and Recommendation - FSM Coding Guideline and Coding Style for Synthesis. Datapath and Control Logic Design.

Module:3	**RTL Synthesis**	**3 hours**

RTL synthesis Flow – Synthesis Design Environment & Constraints – Architecture of Logic Synthesizer - Technology Library Basics– Components of Technology Library –Synthesis Optimization- Technology independent and Technology dependent synthesis- Data path Synthesis – Low Power Synthesis - Formal Verification.

Module:4	**Basic Timing Analysis**	**4 hours**

Timing Parameter Definition – Setup Timing Check- Hold Timing Check- Multicycle Paths- Half-Cycle Paths- False Paths

Module:5	**Advanced Timing Analysis**	**5 hours**

Clock skew optimization – On-Chip Variations- AOCV-Time Borrowing- Setup and Hold Violation Fixing.

Module:6	**Physical Design**	**5 hours**

Detailed steps in Physical Design Flow- Guidelines for Floor plan, Placement, CTS and routing– ECO flow – Signal Integrity Issues.

Module:7	**Physical Design Verification**	**3 hours**

Timing Sign-off, Physical Verification – Signoff DRC and LVS, ERC, IR Drop Analysis, Electro-Migration Analysis and ESD Analysis.

Module:8	**Contemporary Issues**	**1 hours**

	Total Lecture hours:	**30 hours**
Text Book(s)		
1.	Vaibbhav Taraate, ASIC Design and Synthesis RTL Design Using Verilog, Springer, First Edition, 2021, Singapore.	
Reference Books		
1.	Khosrow Golshan, PHYSICAL DESIGN ESSENTIALS An ASIC Design Implementation Perspective, First Edition, 2010.	
2.	Michael John Sebastian Smith, Application-Specific Integrated Circuits, First Edition, 2002.	
3.	J. Bhasker and Rakesh Chadha, Static Timing Analysis for Nanometer Designs, Springer, First Edition, 2010, USA.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test		
Indicative Experiments		
1.	Design of Digital Architecture for given specification	**6 hours**
2.	Logical Synthesis of Digital Architecture	**6 hours**
3.	Netlist Optimization and Formal Verification	**6 hours**
4.	Physical Synthesis of Digital Architecture	**6 hours**
5.	Physical Verification of digital architecture	**6 hours**
	Total Laboratory Hours	**30 hours**
Mode of assessment: Continuous assessment and FAT		
Recommended by Board of Studies	28-02-2023	
Approved by Academic Council	No. 69	Date 16-03-2023