

## DA2: Logic synthesis and Functional Verification of a sequence detector for finding out the overlapping pattern “1001”.

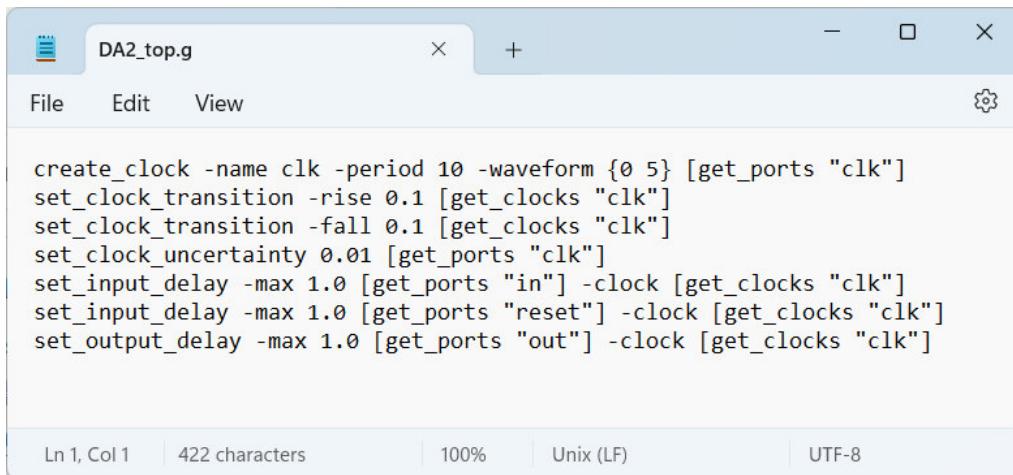
**Aim:** To synthesize a Mealy Overlapping FSM which detects the patter of 1001 and to get the gate level netlist with timing, area, and power reports.

**EDA Tools Used:** Cadence NC Launch, Genus (Logic synthesis tool) .

**Description:** A sequence detector for finding the overlapping pattern "1001" is a sequential circuit that identifies the specified binary sequence in a stream of data, even when the pattern overlaps. It operates using a finite state machine (FSM) with states representing partial progress in detecting the sequence. The circuit transitions through states based on the input bit stream, starting from an initial state and advancing upon recognizing parts of the pattern. When the entire sequence "1001" is detected, an output signal is asserted. For overlapping detection, the FSM does not reset entirely after a match but instead continues scanning for subsequent matches, ensuring overlapping sequences like in 1001001 are identified multiple times. The design typically includes flip-flops for state storage and combinational logic to determine transitions and outputs.

### **Procedure:**

1. Write the verilog file for the design and do the functional verification in NC Launch.
2. Copy the fast.lib and slow.lib files into the folder where (.v) files are located.
3. Create a Synopsys design constraint file (.SDC file) by entering the design constraints required for the synthesis.

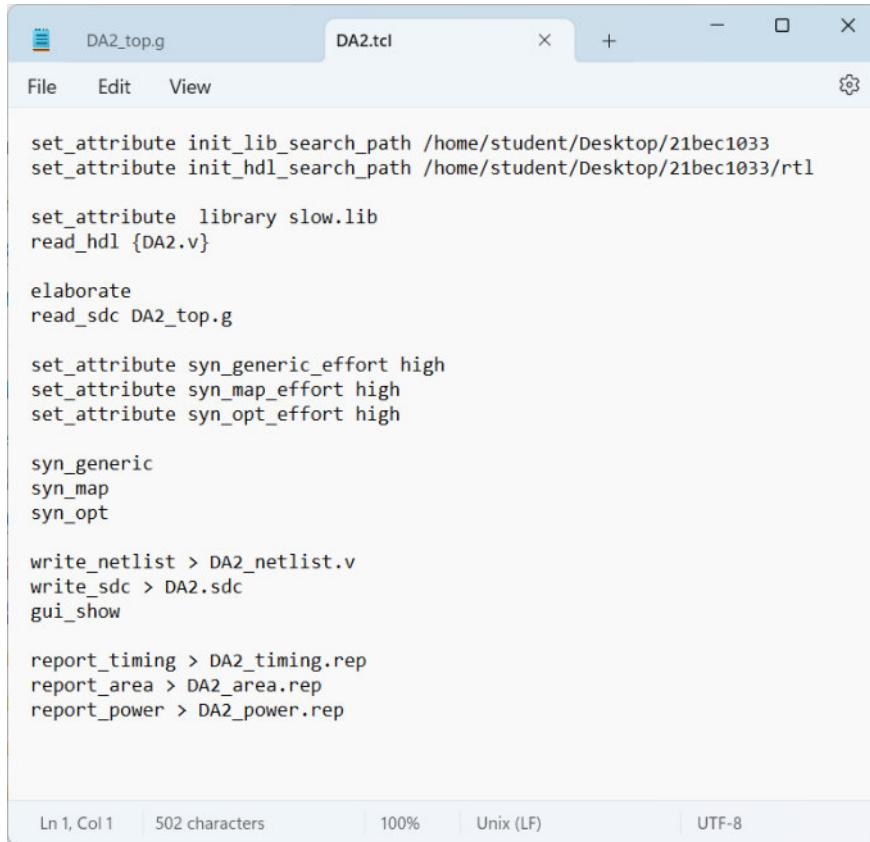


```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "in"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "reset"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "out"] -clock [get_clocks "clk"]
```

4. Create a (.tcl) file containing all the commands for performing the logic synthesis.

## DA2 Logic synthesis & Physical design of 1001 Mealy FSM

Synthesis effort can be medium or high.



```
DA2_top.g DA2.tcl
File Edit View
set_attribute init_lib_search_path /home/student/Desktop/21bec1033
set_attribute init_hdl_search_path /home/student/Desktop/21bec1033/rtl

set_attribute library slow.lib
read_hdl {DA2.v}

elaborate
read_sdc DA2_top.g

set_attribute syn_generic_effort high
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

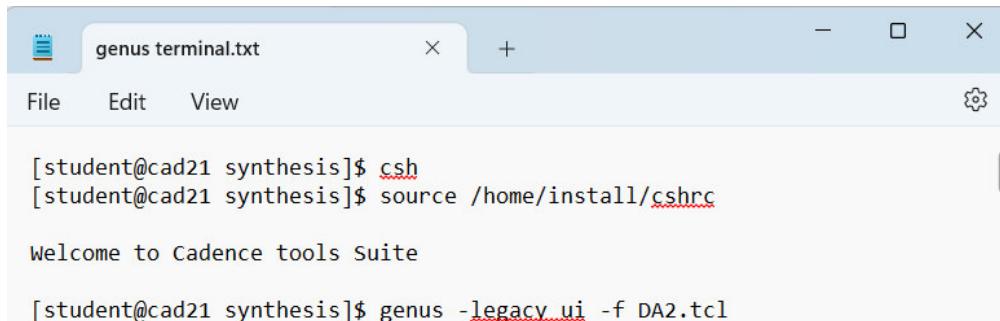
syn_generic
syn_map
syn_opt

write_netlist > DA2_netlist.v
write_sdc > DA2.sdc
gui_show

report_timing > DA2_timing.rep
report_area > DA2_area.rep
report_power > DA2_power.rep

Ln 1, Col 1 502 characters 100% Unix (LF) UTF-8
```

5. Invoke the C shell and launch the Genus tool by entering the below commands.



```
genus terminal.txt
File Edit View
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools suite

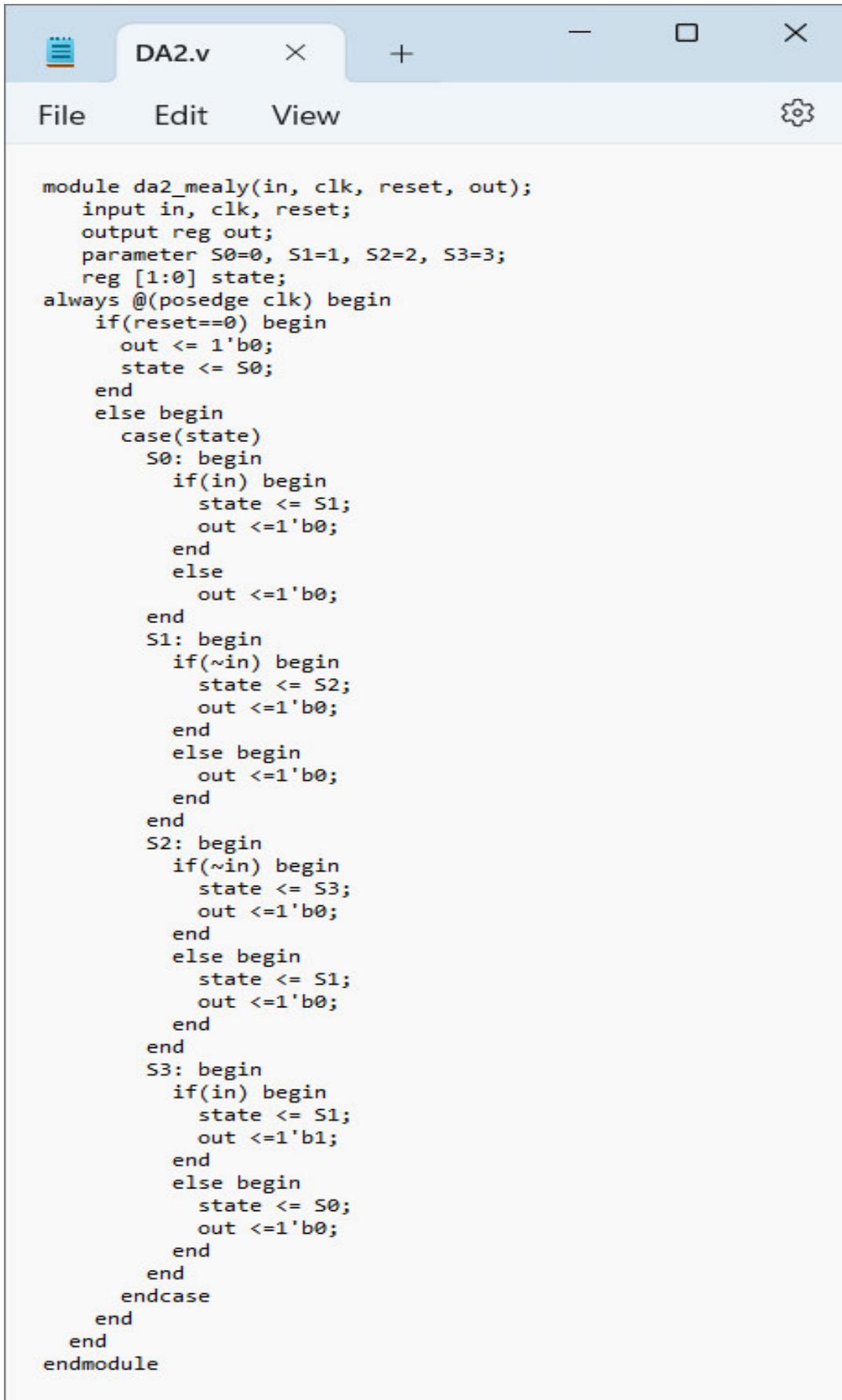
[student@cad21 synthesis]$ genus -legacy_ui -f DA2.tcl
```

6. Execute the commands in the (.tcl file) by entering **source DA2.tcl** command in the command line window.
7. Check for the area, timing and power reports generated in the respective folder.  
Also check the gate level netlist generated in the Genus synthesis solution window.
8. Now do the physical design using innovus.

---

Pre Synthesis Verilog Programs:

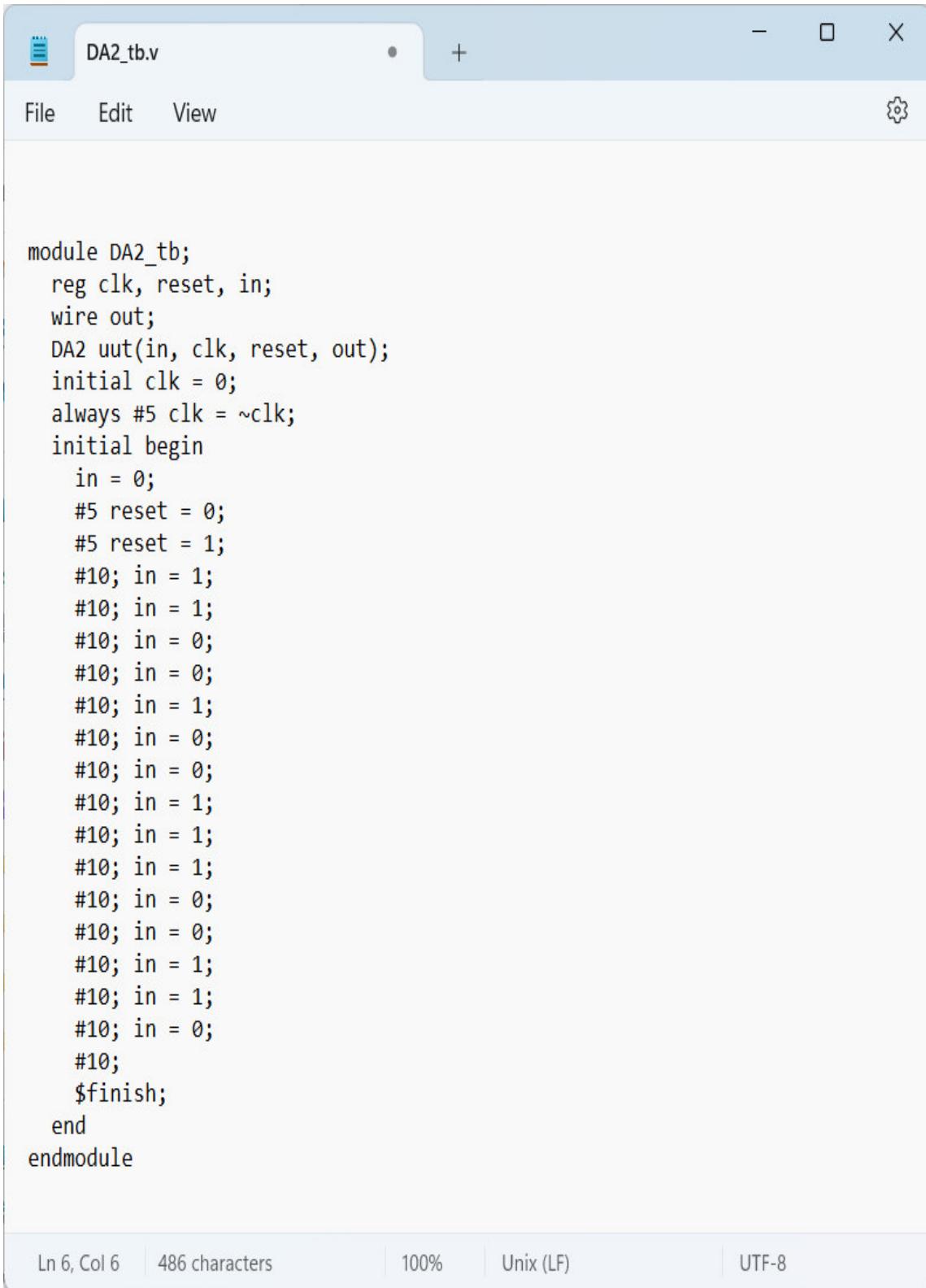
//Verilog Program of 1001 Mealy FSM



The screenshot shows a window titled "DA2.v" which is a Verilog code editor. The menu bar includes "File", "Edit", "View", and a settings gear icon. The code itself is a Verilog module named "da2\_mealy". It defines inputs "in", "clk", and "reset", and an output "reg out". Parameters S0=0, S1=1, S2=2, S3=3 are set. A "state" register is declared as a [1:0] type. An always block handles the logic: if reset is low, it initializes state to S0 and output to 0. Otherwise, it uses a case statement based on the current state. For state S0, if in is high, state becomes S1 and output is 0; otherwise, output is 0. For state S1, if in is low, state becomes S2 and output is 0; otherwise, output is 0. For state S2, if in is low, state becomes S3 and output is 0; otherwise, state becomes S1 and output is 0. For state S3, if in is high, state becomes S1 and output is 1; otherwise, state becomes S0 and output is 0. The case block ends with an endcase statement.

```
module da2_mealy(in, clk, reset, out);
    input in, clk, reset;
    output reg out;
    parameter S0=0, S1=1, S2=2, S3=3;
    reg [1:0] state;
    always @(posedge clk) begin
        if(reset==0) begin
            out <= 1'b0;
            state <= S0;
        end
        else begin
            case(state)
                S0: begin
                    if(in) begin
                        state <= S1;
                        out <=1'b0;
                    end
                    else
                        out <=1'b0;
                end
                S1: begin
                    if(~in) begin
                        state <= S2;
                        out <=1'b0;
                    end
                    else begin
                        out <=1'b0;
                    end
                end
                S2: begin
                    if(~in) begin
                        state <= S3;
                        out <=1'b0;
                    end
                    else begin
                        state <= S1;
                        out <=1'b0;
                    end
                end
                S3: begin
                    if(in) begin
                        state <= S1;
                        out <=1'b1;
                    end
                    else begin
                        state <= S0;
                        out <=1'b0;
                    end
                end
            endcase
        end
    end
endmodule
```

### //Verilog Program of the test bench



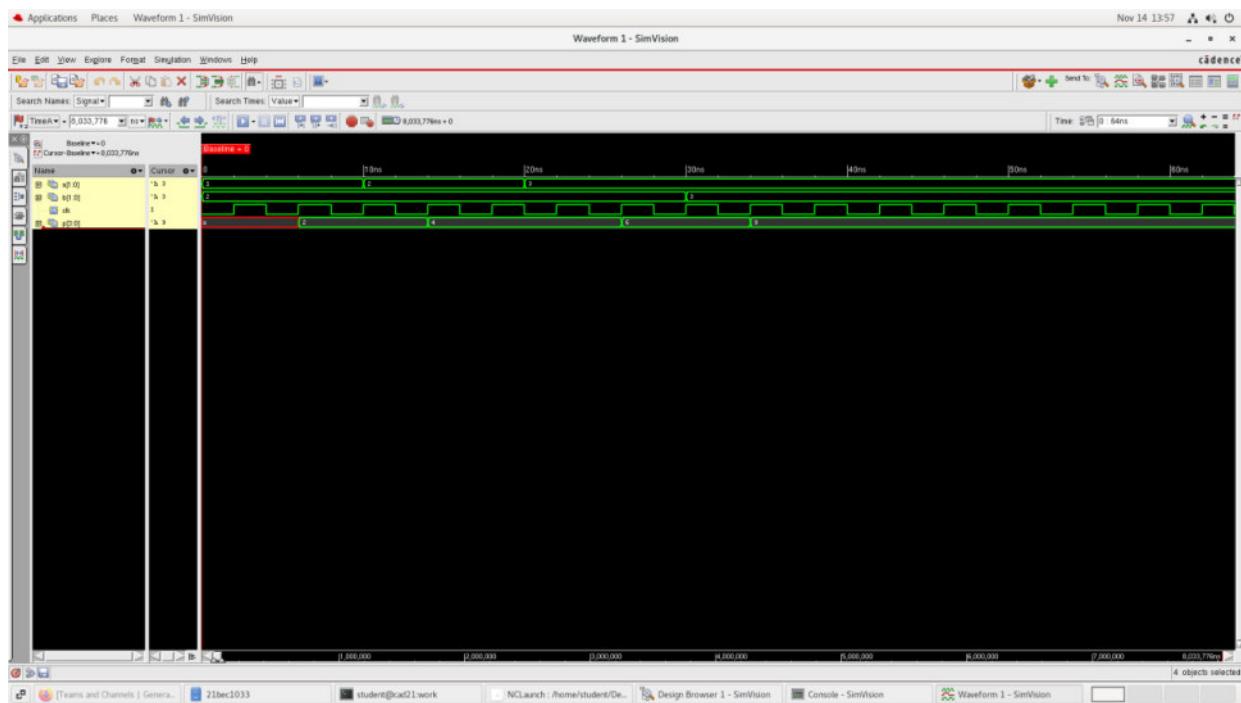
The screenshot shows a window titled "DA2\_tb.v" containing Verilog testbench code. The code defines a module DA2\_tb with inputs clk, reset, and in, and output out. It includes a DA2 component instantiation, initializations for clk and in, and a loop of 10-bit assignments for in. The code ends with a \$finish statement. The editor interface includes a toolbar with File, Edit, View, and a settings gear icon, and a status bar at the bottom.

```
module DA2_tb;
    reg clk, reset, in;
    wire out;
    DA2 uut(in, clk, reset, out);
    initial clk = 0;
    always #5 clk = ~clk;
    initial begin
        in = 0;
        #5 reset = 0;
        #5 reset = 1;
        #10; in = 1;
        #10; in = 1;
        #10; in = 0;
        #10; in = 0;
        #10; in = 1;
        #10; in = 0;
        #10; in = 1;
        #10; in = 1;
        #10; in = 1;
        #10; in = 0;
        #10; in = 0;
        #10; in = 1;
        #10; in = 1;
        #10; in = 0;
        #10; in = 0;
        $finish;
    end
endmodule
```

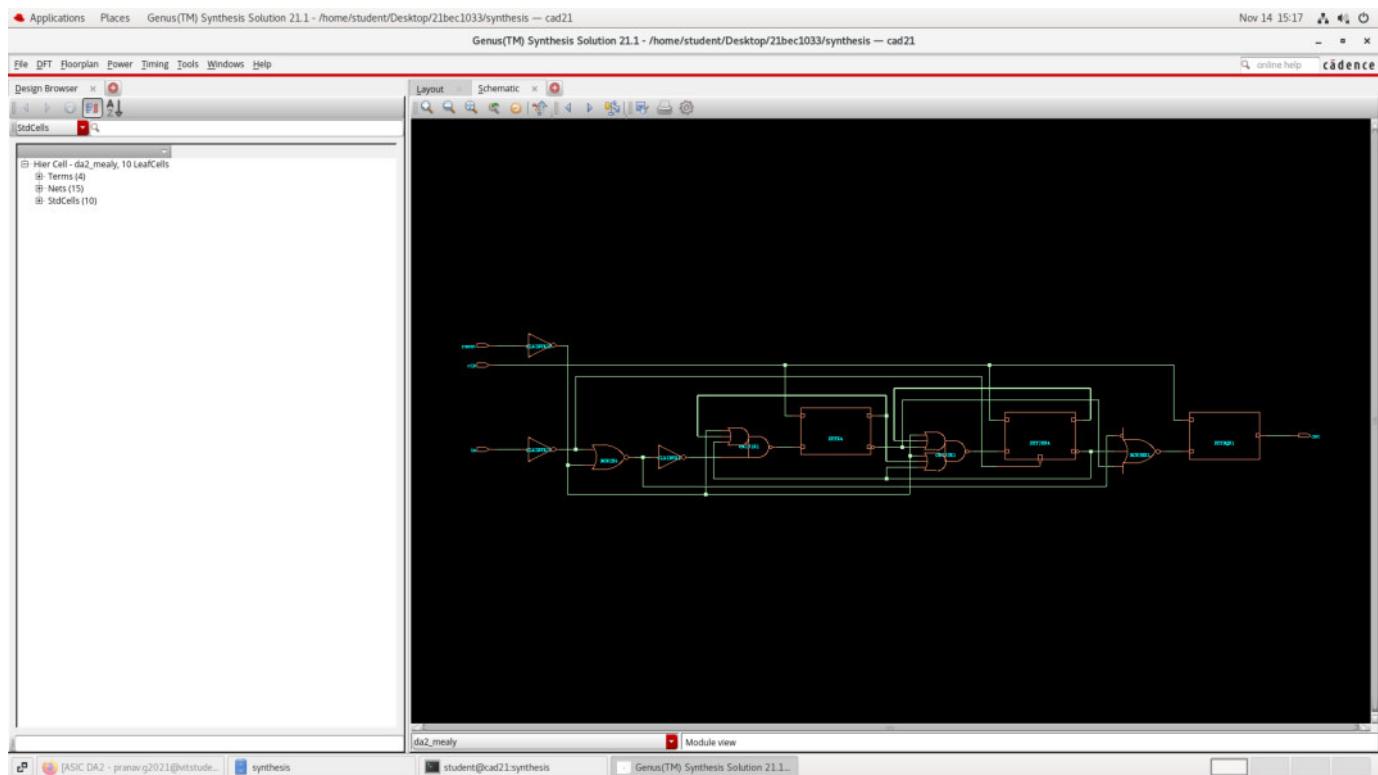
Ln 6, Col 6 | 486 characters | 100% | Unix (LF) | UTF-8

## DA2: Logic synthesis & Physical Design of 1001 Mealy FSM

### Pre Synthesis Verification:



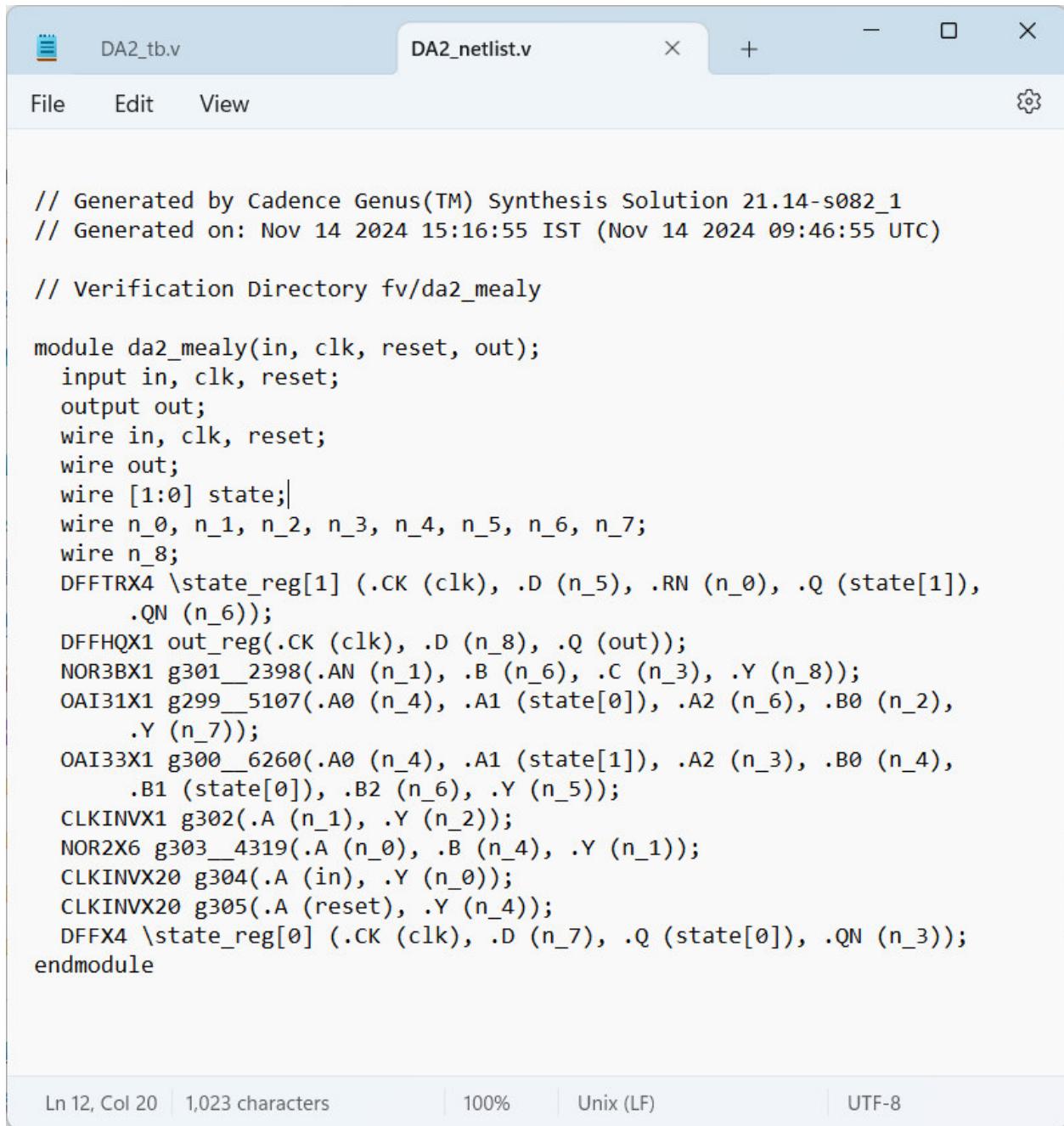
### Gate level Netlist:



## Observations:

Synthesis effort: High

- a) 1001 Mealy FSM Netlist :



The screenshot shows a software interface for Cadence Genus. The title bar indicates the file is 'DA2\_netlist.v'. The menu bar includes 'File', 'Edit', 'View', and a settings gear icon. The main code editor area displays the Verilog netlist for the 1001 Mealy FSM. The code is as follows:

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Nov 14 2024 15:16:55 IST (Nov 14 2024 09:46:55 UTC)

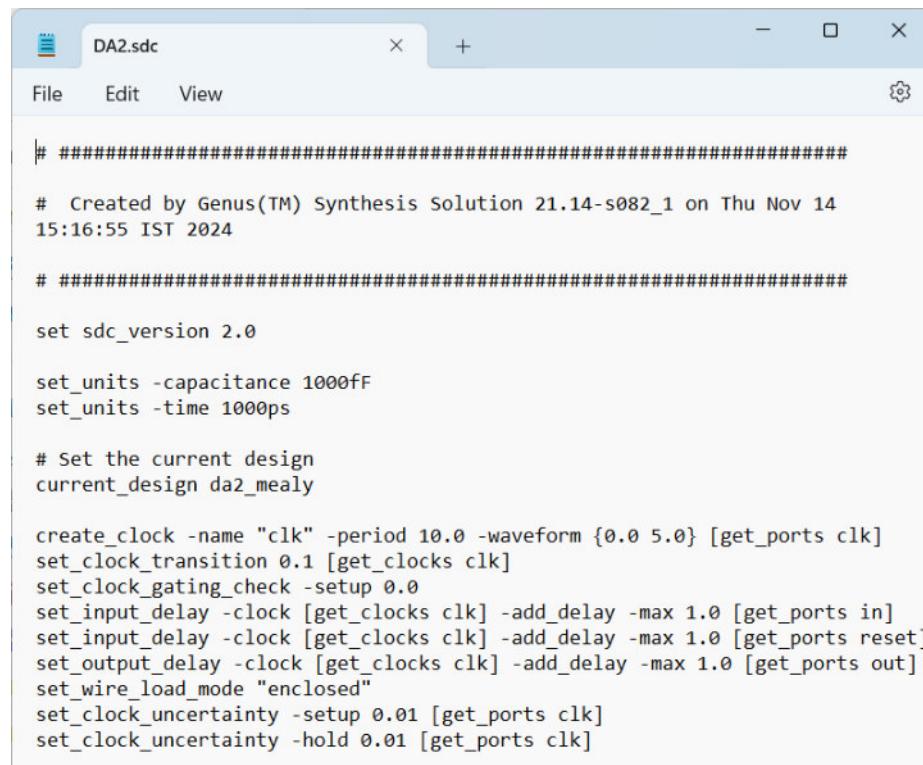
// Verification Directory fv/da2_mealy

module da2_mealy(in, clk, reset, out);
    input in, clk, reset;
    output out;
    wire in, clk, reset;
    wire out;
    wire [1:0] state;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8;
    DFFTRX4 \state_reg[1] (.CK (clk), .D (n_5), .RN (n_0), .Q (state[1]),
                           .QN (n_6));
    DFFHQX1 out_reg(.CK (clk), .D (n_8), .Q (out));
    NOR3BX1 g301_2398(.AN (n_1), .B (n_6), .C (n_3), .Y (n_8));
    OAI31X1 g299_5107(.A0 (n_4), .A1 (state[0]), .A2 (n_6), .B0 (n_2),
                        .Y (n_7));
    OAI33X1 g300_6260(.A0 (n_4), .A1 (state[1]), .A2 (n_3), .B0 (n_4),
                        .B1 (state[0]), .B2 (n_6), .Y (n_5));
    CLKINVX1 g302(.A (n_1), .Y (n_2));
    NOR2X6 g303_4319(.A (n_0), .B (n_4), .Y (n_1));
    CLKINVX20 g304(.A (in), .Y (n_0));
    CLKINVX20 g305(.A (reset), .Y (n_4));
    DFFX4 \state_reg[0] (.CK (clk), .D (n_7), .Q (state[0]), .QN (n_3));
endmodule
```

At the bottom of the code editor, status information is displayed: Ln 12, Col 20 | 1,023 characters | 100% | Unix (LF) | UTF-8.

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

### b) FSM\_Constraint\_created file



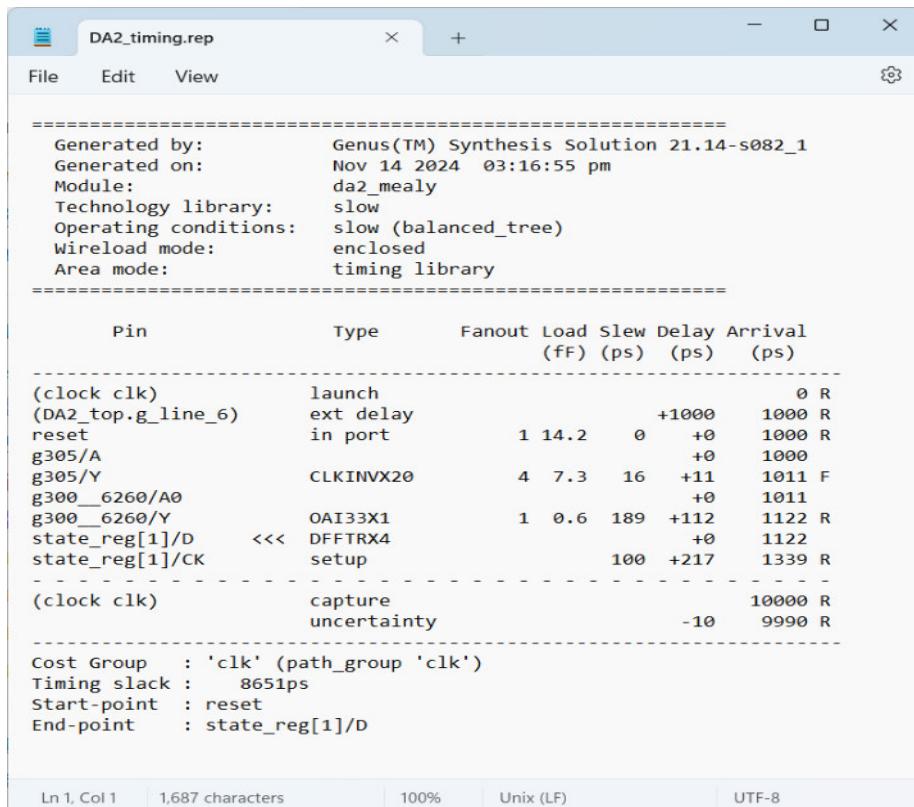
```
# #####
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Nov 14
# 15:16:55 IST 2024
#
# #####
set sdc_version 2.0

set_units -capacitance 1000ff
set_units -time 1000ps

# Set the current design
current_design da2_mealy

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports in]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports reset]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports out]
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.01 [get_ports clk]
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

### c) FSM\_timing\_timing\_report file



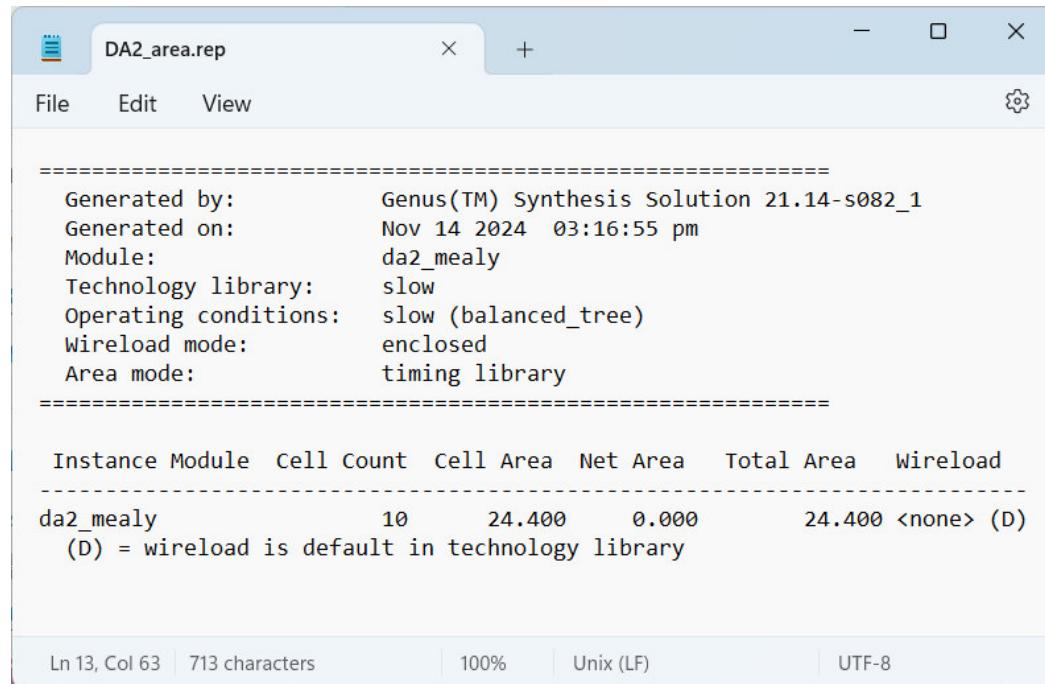
```
=====
Generated by:          Genus(TM) Synthesis Solution 21.14-s082_1
Generated on:         Nov 14 2024  03:16:55 pm
Module:               da2_mealy
Technology library:   slow
Operating conditions: slow (balanced_tree)
Wireload mode:        enclosed
Area mode:            timing library
=====

Pin           Type     Fanout Load Slew Delay Arrival
(fF) (ps)    (ps)   (ps)   (ps)
-----
(clock clk)  launch
(DA2_top.g_line_6) ext delay
reset        in port      1 14.2   0 +0  1000 R
g305/A
g305/Y       CLKINVX20    4  7.3   16 +11 1011 F
g300_6260/A0
g300_6260/Y  OAI33X1     1  0.6   189 +112 1122 R
state_reg[1]/D <<< DFFTRX4
state_reg[1]/CK setup
                     100 +217 1339 R
-----
(clock clk)  capture
                     uncertainty
                           10000 R
                           -10  9990 R
-----
Cost Group : 'clk' (path_group 'clk')
Timing slack : 8651ps
Start-point : reset
End-point   : state_reg[1]/D

Ln 1, Col 1 | 1,687 characters | 100% | Unix (LF) | UTF-8
```

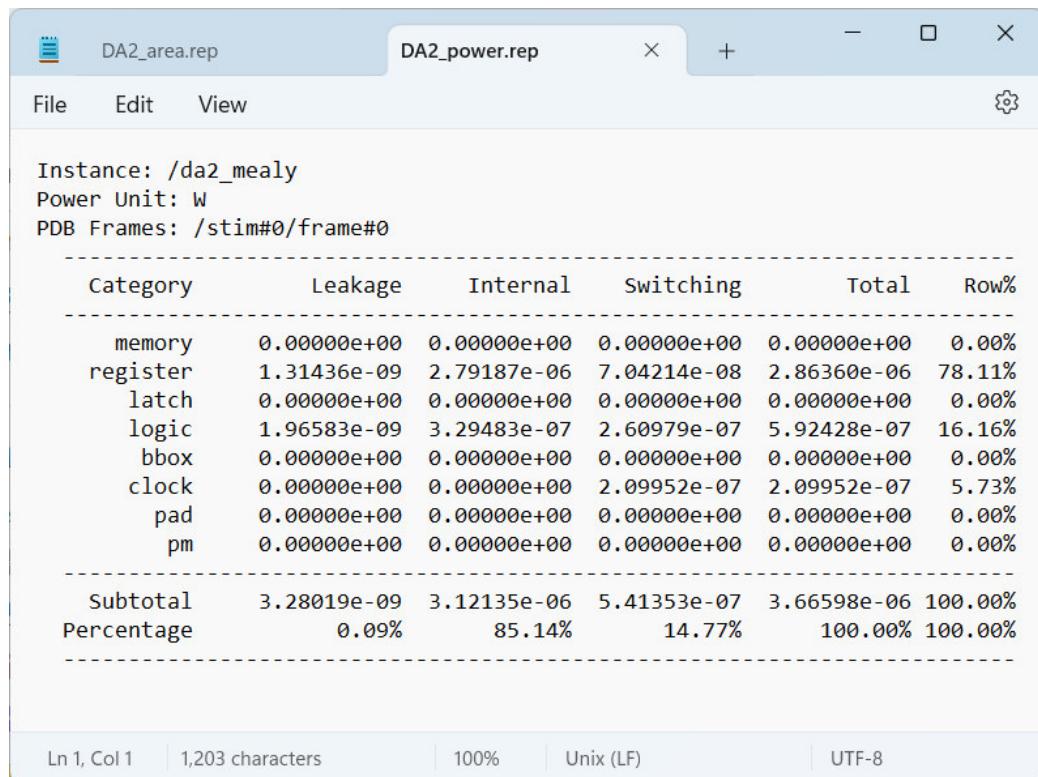
## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

### d) FSM\_area\_report file



```
DA2_area.rep
File Edit View
=====
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Nov 14 2024 03:16:55 pm
Module: da2_mealy
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====
Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----
da2_mealy 10 24.400 0.000 24.400 <none> (D)
(D) = wireload is default in technology library
Ln 13, Col 63 | 713 characters | 100% | Unix (LF) | UTF-8
```

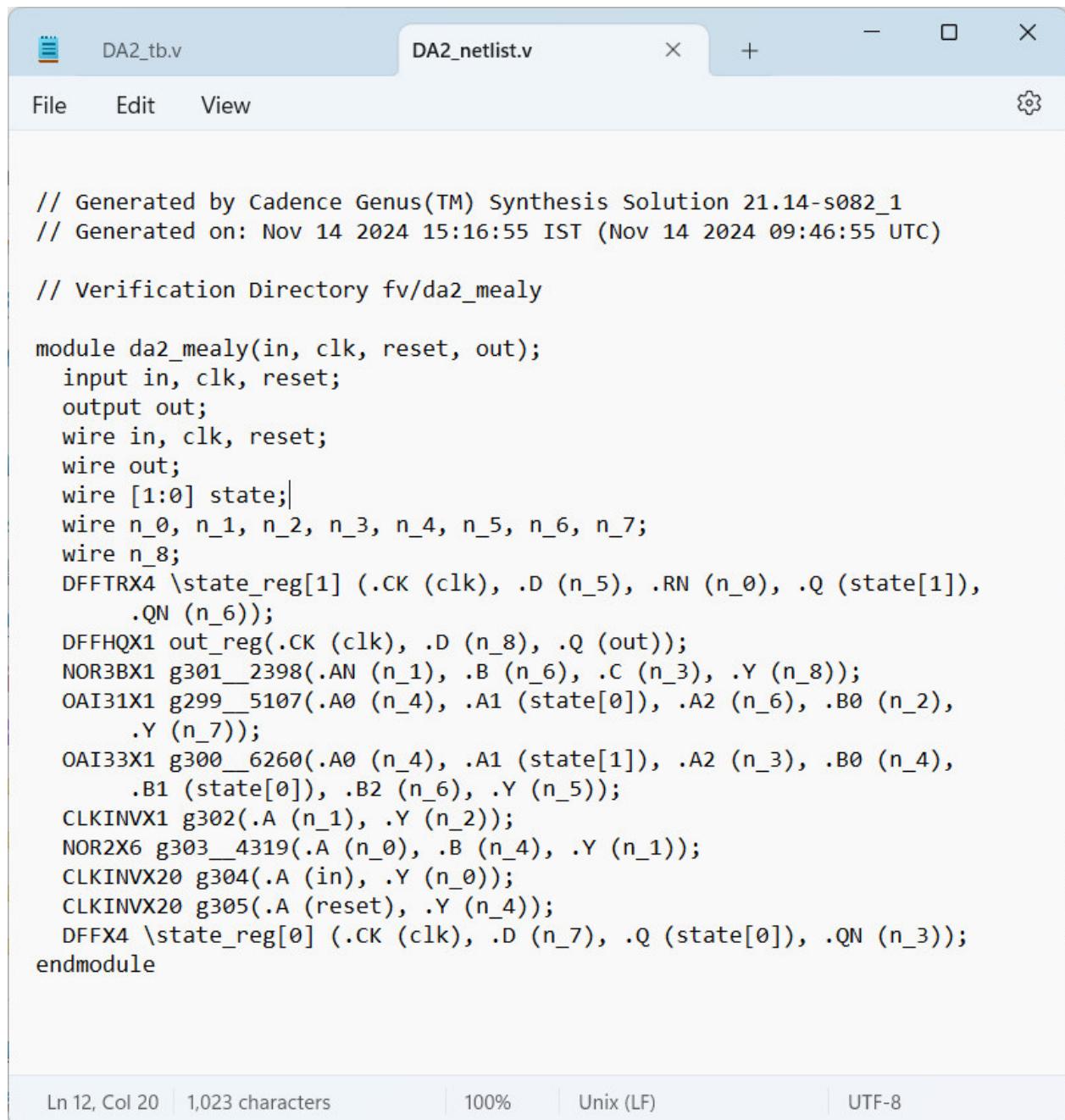
### e) FSM\_power\_report file



```
DA2_area.rep DA2_power.rep
File Edit View
=====
Instance: /da2_mealy
Power Unit: W
PDB Frames: /stim#0/frame#0
=====
Category Leakage Internal Switching Total Row%
-----
memory 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
register 1.31436e-09 2.79187e-06 7.04214e-08 2.86360e-06 78.11%
latch 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
logic 1.96583e-09 3.29483e-07 2.60979e-07 5.92428e-07 16.16%
bbox 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
clock 0.00000e+00 0.00000e+00 2.09952e-07 2.09952e-07 5.73%
pad 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
pm 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
=====
Subtotal 3.28019e-09 3.12135e-06 5.41353e-07 3.66598e-06 100.00%
Percentage 0.09% 85.14% 14.77% 100.00% 100.00%
Ln 1, Col 1 | 1,203 characters | 100% | Unix (LF) | UTF-8
```

## Post synthesis Verilog Programs:

### //Verilog Program of the FSM netlist



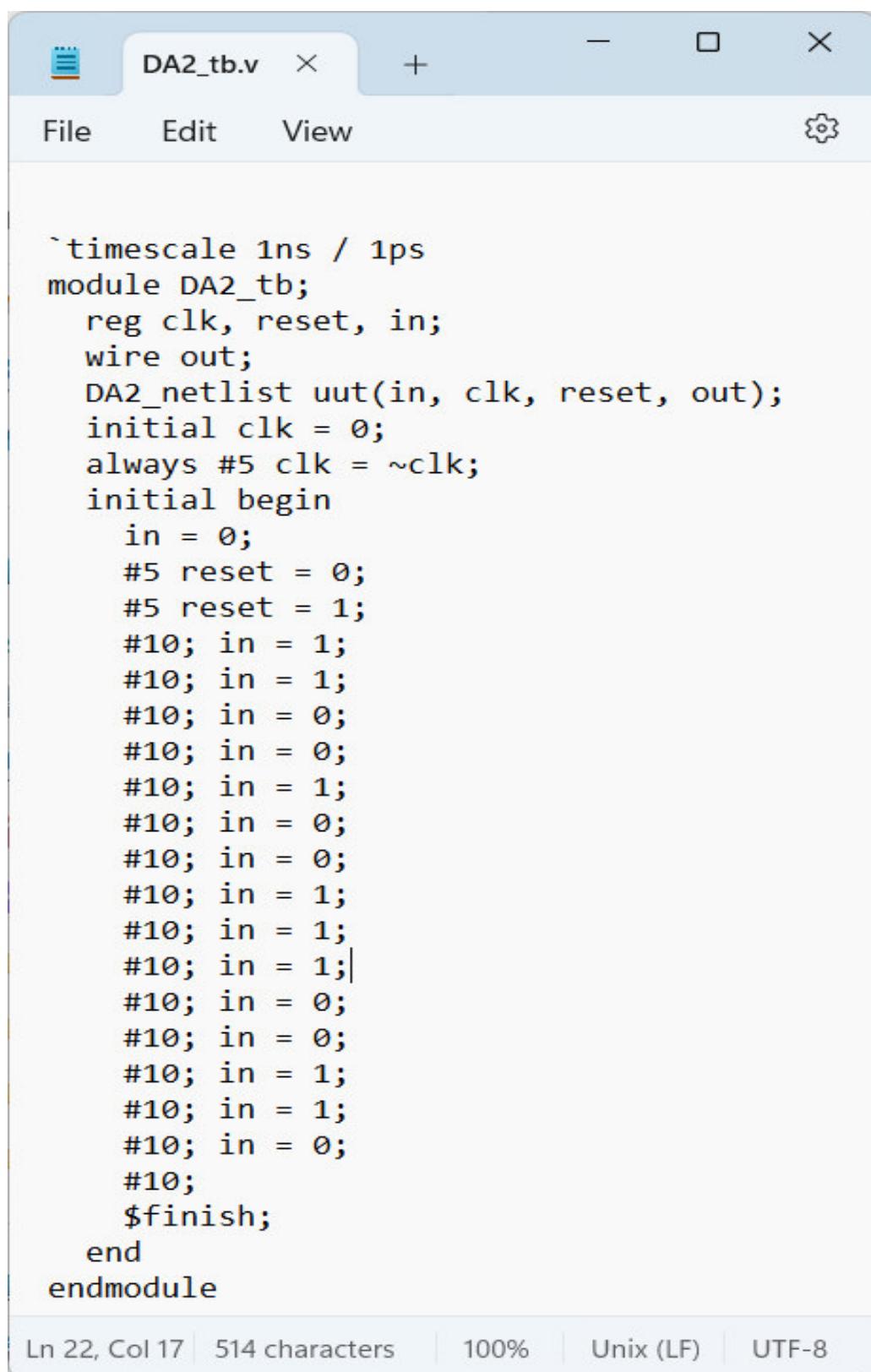
The screenshot shows a Cadence Genus IDE window with two tabs: "DA2\_tb.v" and "DA2\_netlist.v". The "DA2\_netlist.v" tab is active, displaying the generated Verilog code for the 1001 Overlapping Mealy FSM. The code includes comments indicating it was generated by Cadence Genus Synthesis Solution 21.14-s082\_1 on Nov 14 2024 at 15:16:55 IST. It defines a module "da2\_mealy" with inputs "in", "clk", and "reset", and output "out". The module uses various logic components like DFFTRX4, DFFHQX1, NOR3BX1, OAI31X1, OAI33X1, CLKINVX1, NOR2X6, CLKINVX20, and DFFX4 to implement the state transitions and output logic. The code ends with an "endmodule" statement. The status bar at the bottom shows "Ln 12, Col 20 | 1,023 characters | 100% | Unix (LF) | UTF-8".

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Nov 14 2024 15:16:55 IST (Nov 14 2024 09:46:55 UTC)

// Verification Directory fv/da2_mealy

module da2_mealy(in, clk, reset, out);
    input in, clk, reset;
    output out;
    wire in, clk, reset;
    wire out;
    wire [1:0] state;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8;
    DFFTRX4 \state_reg[1] (.CK (clk), .D (n_5), .RN (n_0), .Q (state[1]),
                           .QN (n_6));
    DFFHQX1 out_reg(.CK (clk), .D (n_8), .Q (out));
    NOR3BX1 g301_2398(.AN (n_1), .B (n_6), .C (n_3), .Y (n_8));
    OAI31X1 g299_5107(.A0 (n_4), .A1 (state[0]), .A2 (n_6), .B0 (n_2),
                        .Y (n_7));
    OAI33X1 g300_6260(.A0 (n_4), .A1 (state[1]), .A2 (n_3), .B0 (n_4),
                        .B1 (state[0]), .B2 (n_6), .Y (n_5));
    CLKINVX1 g302(.A (n_1), .Y (n_2));
    NOR2X6 g303_4319(.A (n_0), .B (n_4), .Y (n_1));
    CLKINVX20 g304(.A (in), .Y (n_0));
    CLKINVX20 g305(.A (reset), .Y (n_4));
    DFFX4 \state_reg[0] (.CK (clk), .D (n_7), .Q (state[0]), .QN (n_3));
endmodule
```

## //Verilog Program of the test bench



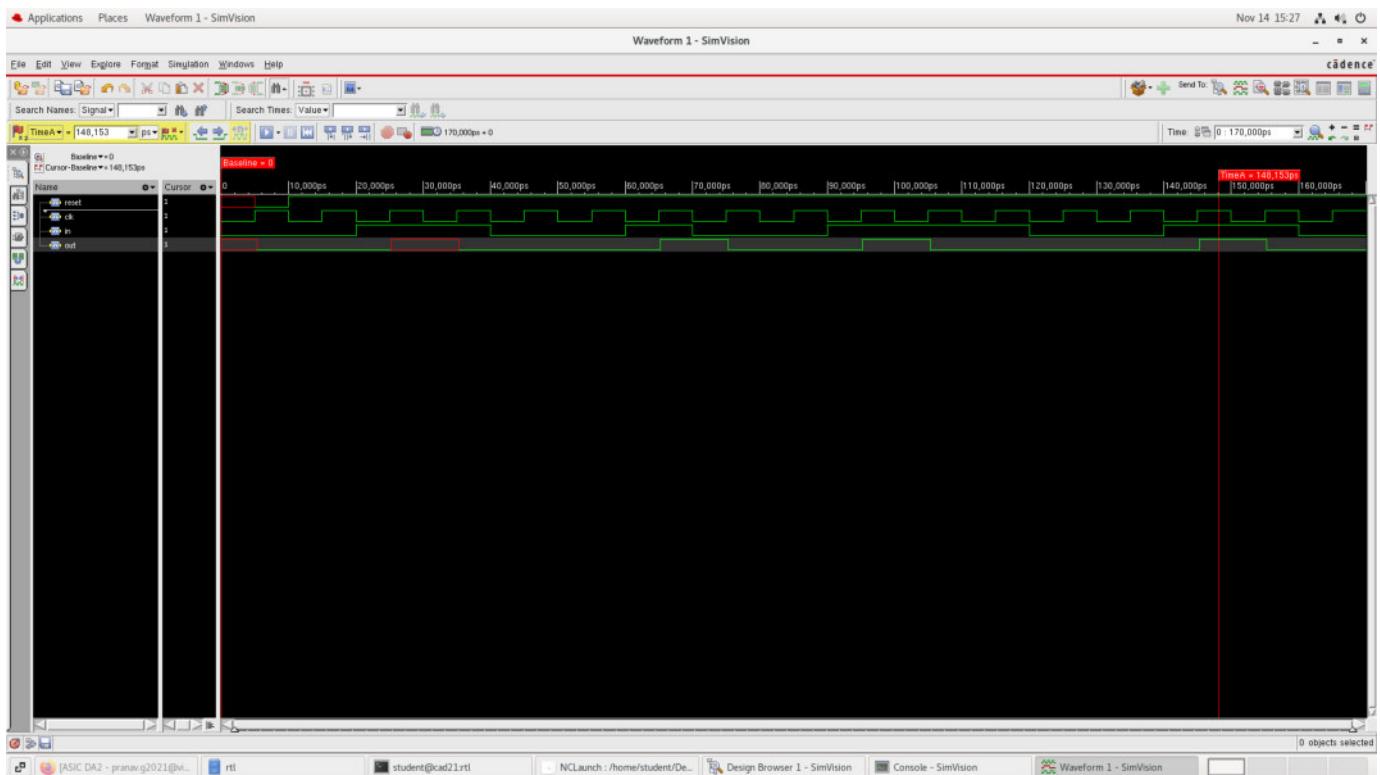
The screenshot shows a Verilog code editor window titled "DA2\_tb.v". The code is a test bench for a DA2 module. It includes a timescale declaration, a module definition with input (in), output (out), and control (clk, reset) ports. Inside the module, there's a self-timed clock generation block using an always block with a #5 period. The initial block sets the initial state of in to 0, then alternates it between 1 and 0 every 10 units of time. The simulation ends with a \$finish command. The code editor interface includes a toolbar at the top with icons for file operations, and a status bar at the bottom showing line 22, column 17, 514 characters, 100% zoom, Unix (LF) end-of-line, and UTF-8 encoding.

```
`timescale 1ns / 1ps
module DA2_tb;
    reg clk, reset, in;
    wire out;
    DA2_netlist uut(in, clk, reset, out);
    initial clk = 0;
    always #5 clk = ~clk;
    initial begin
        in = 0;
        #5 reset = 0;
        #5 reset = 1;
        #10; in = 1;
        #10; in = 1;
        #10; in = 0;
        #10; in = 0;
        #10; in = 1;
        #10; in = 0;
        #10; in = 0;
        #10; in = 1;
        #10; in = 1;
        #10; in = 1;
        #10; in = 0;
        #10; in = 0;
        #10; in = 1;
        #10; in = 1;
        #10; in = 0;
        #10;
        $finish;
    end
endmodule
```

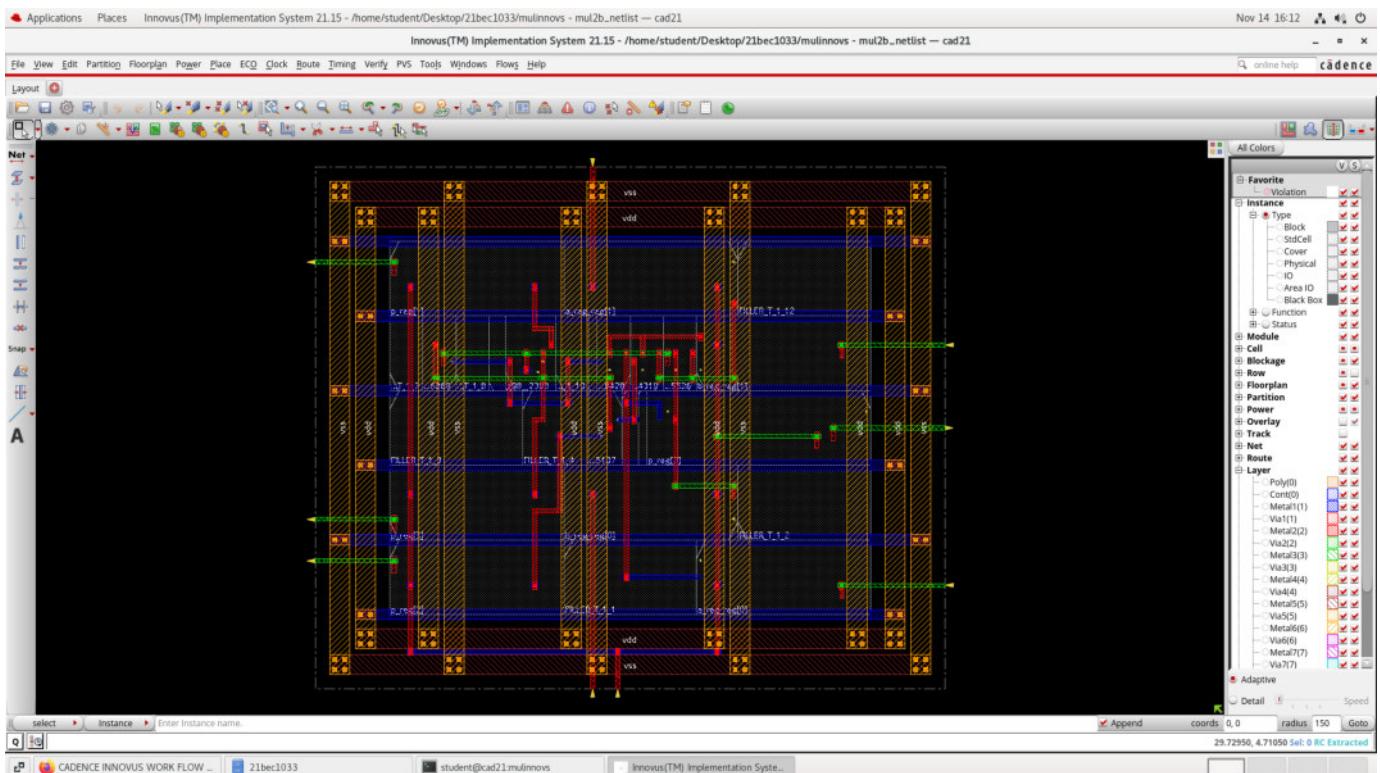
Ln 22, Col 17 | 514 characters | 100% | Unix (LF) | UTF-8

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

### Post Synthesis verification:



### Physical design of the Multiplier:



## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

### Genus Terminal:

```
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -legacy_ui -f DA2.tcl
2024/11/14 15:16:49 WARNING This OS does not appear to be a Cadence
supported Linux configuration.
2024/11/14 15:16:49 For more info, please run CheckSysConf in
<cdsRoot/tools.lnx86/bin/checkSysConf <productId>
TMPDIR is being set to /tmp/genus_temp_19286_cad21_student_oXtiZN
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved
worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a
trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[15:16:49.095697] Configured Lic search path (21.01-s002): 5280@cadence

Version: 21.14-s082_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files DA2.tcl
Date:    Thu Nov 14 15:16:49 2024
Host:    cad21 (x86_64 w/Linux 4.18.0-425.19.2.e18_7.x86_64)
(12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700
25600KB) (32402340KB)
PID:    19286
OS:     Red Hat Enterprise Linux release 8.8 (Ootpa)

[15:16:49.026595] Periodic Lic check successful
[15:16:49.026603] Feature usage summary:
[15:16:49.026603] Genus_Synthesis
Checking out license: Genus_Synthesis

*****
*****
```

Loading tool scripts...

Finished loading tool scripts (4 seconds elapsed).

```
#@ Processing -files option
@genus 1> source DA2.tcl
Setting attribute of root '/': 'init_lib_search_path' =
/home/student/Desktop/21bec1033
Setting attribute of root '/': 'init_hdl_search_path' =
/home/student/Desktop/21bec1033/rtl
```

Threads Configured:3

```
Message Summary for Library slow.lib:
*****
Missing a function attribute in the output pin definition. [LBR-518]: 1
Missing library level attribute. [LBR-516]: 1
*****
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
: Done elaborating 'da2_mealy'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_elab
-----
| Trick | Accepts | Rejects | Runtime (ms) |
|-----|
| ume_constant_bmux | 0 | 0 | 0.00 |
|-----|
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: da2_mealy, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: da2_mealy, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
-----
| Transform | Accepts | Rejects | Runtime (ms) |
|-----|
| hlo_clip_mux_input | 0 | 0 | 0.00 |
| hlo_clip | 0 | 0 | 0.00 |
|-----|
Statistics for commands executed by read_sdc:
"create_clock" - successful 1 , failed 0 (runtime 0.00)
"get_clocks" - successful 5 , failed 0 (runtime 0.00)
"get_ports" - successful 5 , failed 0 (runtime 0.00)
"set_clock_transition" - successful 2 , failed 0 (runtime 0.00)
"set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)
"set_input_delay" - successful 2 , failed 0 (runtime 0.00)
"set_output_delay" - successful 1 , failed 0 (runtime 0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
Setting attribute of root '/': 'syn_generic_effort' = high
Setting attribute of root '/': 'syn_map_effort' = high
Setting attribute of root '/': 'syn_opt_effort' = high

Stage: pre_early_cg
-----
| Transform | Accepts | Rejects | Runtime (ms) |
|-----|
##Generic Timing Info for library domain: _default_ typical gate delay: 108.0 ps std_slew: 19.0 ps std_load: 2.2 fF
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: da2_mealy, recur: true)
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Info      : Created nominal operating condition. [LBR-412]
            : Operating condition '_nominal_' was created for the PVT values
            (1.000000, 1.080000, 125.000000) in library 'slow.lib'.
            : The nominal operating condition is represented, either by the
            nominal PVT values specified in the library source (via
            nom_process,nom_voltage and nom_temperature respectively), or by the
            default PVT values (1.0,1.0,1.0).
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/ADDHX2'.
            : Specify a valid area value for the libcell.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/ADDHX4'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/ADDHXL'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/ADDFXL'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/ADDHX2'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/ADDHXL'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND2X4'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND2X6'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND2XL'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND3X1'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND3X8'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND3XL'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND4X1'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND4X4'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND4X8'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AND4XL'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AO21X1'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AO21X2'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AO21XL'.
Warning   : Libcell has no area attribute. Defaulting to 0 area. [LBR-43]
            : Assigning 0 area to library cell 'slow/AO22X1'.
Warning   : Maximum message print count reached. [MESG-11]
            : Maximum print count of '20' reached for message 'LBR-43'.
Setting attribute of root '/': 'library' = slow.lib
Library has 324 usable logic and 126 usable sequential lib-cells.
Info      : Elaborating Design. [ELAB-1]
            : Elaborating top-level block 'da2_mealy' from file
'/home/student/Desktop/21bec1033/rtl/DA2.v'.
Warning   : Using default parameter value for module elaboration. [CDFG-
818]
            : Elaborating block 'da2_mealy' with default parameters value.
Info      : Done Elaborating Design. [ELAB-3]
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_to_gen_setup
-----
| Transform | Accepts | Rejects | Runtime (ms) |
-----
| hlo_mux_reorder | 0 | 0 | 0.00 |
-----
Info : Deleting instances not driving any primary outputs. [GLO-34]
      : Deleting 1 hierarchical instance.
      : Optimizations such as constant propagation or redundancy removal could change the connections so a hierarchical instance does not drive any primary outputs anymore. To see the list of deleted hierarchical instances, set the 'information_level' attribute to 2 or above. If the message is truncated set the message attribute 'truncate' to false to see the complete list. To prevent this optimization, set the 'delete_unloaded_insts' root/subdesign attribute to 'false' or 'preserve' instance attribute to 'true'.
Info : Synthesizing. [SYNTH-1]
      : Synthesizing 'da2_mealy' to generic gates using 'high' effort.
PBS_Generic-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Start' being created for table 'pbs_debug'

      Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
      | Memory | Stage
-----+-----+-----+-----+
-----+-----+-----+-----+
 00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
TNS Restructuring config: no_value at stage: generic applied.
Info : Partition Based Synthesis execution skipped. [PHYS-752]
      : Design size is less than the partition size '100000' for distributed generic optimization to kick in.
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: da2_mealy, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_to_gen_setup
-----
| Transform | Accepts | Rejects | Runtime (ms) |
-----
| hlo_mux_reorder | 0 | 0 | 0.00 |
-----
Starting mux data reorder optimization [v1.0] (stage: post_to_gen_setup, startdef: da2_mealy, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_to_gen_setup
-----
| Transform | Accepts | Rejects | Runtime (ms) |
-----
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
| hlo_mux_reorder |      0 |      0 |      0.00 |
-----
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: pre_hlo_rtlopt
-----
| Trick | Accepts | Rejects | Runtime (ms) |
-----
Starting infer macro optimization [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed infer macro optimization (accepts: 0, rejects: 5, runtime: 0.000s)
Starting decode mux sandwich optimization [v2.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed decode mux sandwich optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting decode mux optimization [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed decode mux optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting chop wide muxes [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed chop wide muxes (accepts: 0, rejects: 0, runtime: 0.000s)
Starting common data mux cascade opt [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed common data mux cascade opt (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux input consolidation [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed mux input consolidation (accepts: 0, rejects: 0, runtime: 0.000s)
Starting constant-data mux optimization [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed constant-data mux optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting chain-to-tree inequality transform [v2.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed chain-to-tree inequality transform (accepts: 0, rejects: 0, runtime: 0.000s)
Starting reconvergence optimization [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed reconvergence optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting logic restructure optimization [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed logic restructure optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting common select mux optimization [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed common select mux optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting identity transform [v3.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed identity transform (accepts: 0, rejects: 0, runtime: 0.000s)
Starting reduce operator chain [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed reduce operator chain (accepts: 0, rejects: 0, runtime: 0.000s)
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Starting common data mux cascade opt [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed common data mux cascade opt (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux input consolidation [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed mux input consolidation (accepts: 0, rejects: 0, runtime: 0.000s)
Starting optimize datapath elements [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed optimize datapath elements (accepts: 0, rejects: 0, runtime: 0.000s)
Starting datapath recasting [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed datapath recasting (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip mux common data inputs [v1.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: pre_rtlopt, startdef: da2_mealy, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)
```

Stage: pre\_rtlopt

Transform	Accepts	Rejects	Runtime (ms)
hlo_infer_macro	0	5	0.00
hlo_decode_mux_sandwich	0	0	0.00
hlo_mux_decode	0	0	0.00
hlo_chop_mux	0	0	0.00
hlo_mux_cascade_opt	0	0	0.00
hlo_mux_consolidation	0	0	0.00
hlo_constant_mux_opt	0	0	0.00
hlo_inequality_transform	0	0	0.00
hlo_reconv_opt	0	0	0.00
hlo_restructure	0	0	0.00
hlo_common_select_muxopto	0	0	0.00
hlo_identity_transform	0	0	0.00
hlo_reduce_operator_chain	0	0	0.00
hlo_mux_cascade_opt	0	0	0.00
hlo_mux_consolidation	0	0	0.00
hlo_optimize_datapath	0	0	0.00
hlo_datapath_recast	0	0	0.00
hlo_clip_mux_input	0	0	0.00
hlo_clip	0	0	0.00

Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post\_hlo\_rtlopt

Trick	Accepts	Rejects	Runtime (ms)
ume_runtime	0	0	0.00

Number of big hc bmuxes before = 0
Info : Pre-processed datapath logic. [DPOPT-6]

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
: No pre-processing optimizations applied to datapath logic in
'da2_mealy'.
Info   : Skipping datapath optimization. [DPOPT-5]
        : There is no datapath logic in 'da2_mealy'.
Number of big hc bmuxes after = 0
Starting logic reduction [v1.0] (stage: post_rtlopt, startdef: da2_mealy,
recur: true)
Completed logic reduction (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux data reorder optimization [v1.0] (stage: post_rtlopt,
startdef: da2_mealy, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime:
0.000s)

Stage: post_rtlopt
-----
| Transform      | Accepts | Rejects | Runtime (ms) |
|-----|
| hlo_logic_reduction | 0 | 0 | 0.00 |
| hlo_mux_reordered | 0 | 0 | 0.00 |
|-----|
Starting mux speculation [v1.0] (stage: post_muxopt, startdef: da2_mealy,
recur: true)
Starting speculation optimization
Completed speculation optimization (accepts:0)
Completed mux speculation (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_muxopt
-----
| Transform      | Accepts | Rejects | Runtime (ms) |
|-----|
| hlo_speculation | 0 | 0 | 0.00 |
|-----|
=====
Stage : to_generic
=====
=====

Message Summary
=====

-----
| Id    | Sev   | Count | Message Text
|-----|
| CDFG-372 | Info   | 7 | Bitwidth mismatch in assignment.
|           |         |     | Review and make sure the mismatch is
|           |         |     | unintentional. Genus can possibly issue
bitwidth |           |     | mismatch warning for explicit assignments
|           |         |     | in RTL as-well-as for implicit assignments
present |           |     | inferred by the tool. For example, in case
of      |           |     | enum declaration without value, the tool
will    |           |     | implicitly assign value to the enum
variables. It |
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
|           |           |           | also issues the warning for any bitwidth  
mismatch |           |           | that appears in this implicit assignment.  
| CDFG-818 | Warning |   1 | Using default parameter value for module  
|           |           |           | elaboration.  
| CWD-19   | Info    |   1 | An implementation was inferred.  
| DPOPT-5  | Info    |   1 | Skipping datapath optimization.  
| DPOPT-6  | Info    |   1 | Pre-processed datapath logic.  
| ELAB-1   | Info    |   1 | Elaborating Design.  
| ELAB-3   | Info    |   1 | Done Elaborating Design.  
| GLO-34   | Info    |   1 | Deleting instances not driving any primary  
|           |           |           | outputs.  
|           |           |           | Optimizations such as constant propagation or  
|           |           |           | redundancy removal could change the  
connections |           |           | so a hierarchical instance does not drive  
any        |           |           | primary outputs anymore. To see the list of  
|           |           |           | deleted hierarchical instances, set the  
|           |           |           | 'information_level' attribute to 2 or above.  
If         |           |           | the message is truncated set the message  
|           |           |           | attribute 'truncate' to false to see the  
complete |           |           | list. To prevent this optimization, set the  
|           |           |           | 'delete_unloaded_insts' root/subdesign  
attribute |           |           | to 'false' or 'preserve' instance attribute  
to        |           |           | 'true'.  
| LBR-41   | Info    |   1 | An output library pin lacks a function  
attribute. |           |           | If the remainder of this library cell's  
semantic   |           |           | checks are successful, it will be considered  
as a      |           |           | timing-model  
|           |           | (because one of its outputs does not have a  
valid     |           |           | function.  
| LBR-43   | Warning |  485 | Libcell has no area attribute. Defaulting to  
0         |           |           |
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
|           |           | area.
|           |           |Specify a valid area value for the libcell.
| LBR-155  |Info    | 248 |Mismatch in unateness between 'timing_sense'
|           |           | attribute and the function.
|           |           |The 'timing_sense' attribute will be
respected. |
| LBR-161  |Info    | 1  |Setting the maximum print count of this
message to |
|           |           | 10 if information_level is less than 9.
|
| LBR-162  |Info    | 124 |Both 'pos_unate' and 'neg_unate' timing_sense
arcs |
|           |           | have been processed.
|
|           |           |Setting the 'timing_sense' to non_unate.
|
| LBR-170  |Info    | 64  |Ignoring specified timing sense.
|
|           |           |Timing sense should never be set with
|
|           |           | 'rising_edge' or 'falling_edge' timing type.
|
| LBR-412  |Info    | 1   |Created nominal operating condition.
|
|           |           |The nominal operating condition is
represented, |
|           |           | either by the nominal PVT values specified
in the |
|           |           | library source
|
|           |           | (via nom_process,nom_voltage and
nom_temperature |
|           |           | respectively)
|
|           |           | , or by the default PVT values
(1.0,1.0,1.0).
| LBR-516  |Info    | 1   |Missing library level attribute.
|
| LBR-518  |Info    | 1   |Missing a function attribute in the output
pin      |
|           |           | definition.
|
| PHYS-752 |Info    | 1   |Partition Based Synthesis execution skipped.
|
| SYNTH-1  |Info    | 1   |Synthesizing.
|
| TIM-1000 |Info    | 1   |Multimode clock gating check is disabled.
|
-----  
Mapper: Libraries have:  
    domain _default_: 324 combo usable cells and 126 sequential usable  
cells  
Multi-threaded constant propagation [1|0] ...  
Multi-threaded Virtual Mapping     (8 threads, 8 of 20 CPUs usable)
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Global mapping target info
=====
Cost Group 'clk' target slack: 268 ps
Target path end-point (Pin: state_reg[1]/d)

State Retention Synthesis Status
=====

Category                      Flops   Percentage
-----
Total instances                3       100.0
Excluded from State Retention 3       100.0
  - Will not convert          3       100.0
    - Preserved                0       0.0
    - Power intent excluded   3       100.0
  - Could not convert         0       0.0
    - Scan type                0       0.0
    - No suitable cell         0       0.0
State Retention instances      0       0.0
-----

PBS_Generic_Opt-Post - Elapsed_Time 1, CPU_Time 0.9955619999999996
stamp 'PBS_Generic_Opt-Post' being created for table 'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
  | Memory          | Stage           |
-----+-----+-----+-----+
  00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.0(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_Generic-Postgen HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Postgen HBO Optimizations' being created for table
'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
  | Memory          | Stage           |
-----+-----+-----+-----+
  00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.0(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
-----+-----+-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
##>===== Cadence Confidential (Generic-Logical)
=====
##>===== Cadence Confidential (Generic-Logical)
=====
##>Main Thread Summary:
##>-----
-----+-----+-----+-----+-----+
# ##>STEP
Area      Memory          Elapsed      WNS      TNS      Insts
# ##>-----
-----+-----+-----+-----+-----+
##>G:Initial           0          -        -       29
0      244
##>G:Setup              -          -        -       -
-      -
##>G:Launch ST          -          -        -       -
-      -
##>G:Design Partition   0          -        -       -
-      -
##>G>Create Partition Netlists 0          -        -       -
-      -
##>G:Init Power         0          -        -       -
-      -
##>G:Budgeting          0          -        -       -
-      -
##>G:Derenv-DB          0          -        -       -
-      -
##>G:Debug Outputs     0          -        -       -
-      -
##>G:ST loading         0          -        -       -
-      -
##>G:Distributed        0          -        -       -
-      -
##>G:Timer              0          -        -       -
-      -
##>G:Assembly           0          -        -       -
-      -
##>G:DFT                0          -        -       -
-      -
##>G:Const Prop         0          -        -       13
0      244
##>G:Misc               1
# ##>-----
-----+-----+-----+-----+-----+
# ##>Total Elapsed       1
# ##>=====
=====

Info      : Done synthesizing. [SYNTH-2]
            : Done synthesizing 'da2_mealy' to generic gates.
## Generic Timing Info for library domain: _default_ typical gate delay:
108.0 ps std_slew: 19.0 ps std_load: 2.2 fF
Info      : Mapping. [SYNTH-4]
            : Mapping 'da2_mealy' using 'high' effort.
Mapper: Libraries have:
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
domain _default_: 324 combo usable cells and 126 sequential usable
cells
Configuring mapper costing (none)
TNS Restructuring config: no_value at stage: map applied.
PBS_TechMap-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Start' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory | Stage
-----+-----+-----+
-----+-----+
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.0(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Start
-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Premap HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Premap HBO Optimizations' being created for table
'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory | Stage
-----+-----+-----+
-----+-----+
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.0(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Start
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
Info      : Partition Based Synthesis execution skipped. [PHYS-752]
      : Design size is less than the partition size '100000' for
distributed mapping optimization to kick in.
Mapper: Libraries have:
        domain _default_: 324 combo usable cells and 126 sequential usable
cells
Multi-threaded Virtual Mapping      (8 threads, 8 of 20 CPUs usable)

Global mapping target info
=====
Cost Group 'clk' target slack:  268 ps
Target path end-point (Pin: state_reg[1]/d)

Multi-threaded Virtual Mapping      (8 threads, 8 of 20 CPUs usable)
Multi-threaded Technology Mapping (8 threads, 8 of 20 CPUs usable)

Global mapping status
=====
                    Group
                    Tot Wrst
                    Total Weighted
Operation          Area   Slacks
global_map         0       0

Cost Group          Target    Slack    Diff.  Constr.
-----
clk                268      8650      10000

Global incremental target info
=====
Cost Group 'clk' target slack:  176 ps
Target path end-point (Pin: state_reg[1]/D (DFFTRX4/D))

=====
Stage : global_incr_map
=====

Message Summary
=====

|   Id   |Sev  |Count |           Message Text           |
|-----|
| PHYS-752 |Info |    1 |Partition Based Synthesis execution skipped. |
| SYNTH-2  |Info |    1 |Done synthesizing.                  |
| SYNTH-4  |Info |    1 |Mapping.                         |

=====

Global incremental optimization status
=====

                    Group
                    Tot Wrst
                    Total Weighted
Operation          Area   Slacks
global_incr        0       0

Cost Group          Target    Slack    Diff.  Constr.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
-----  
clk          176      8651      10000  
  
State Retention Synthesis Status  
=====  
  
Category           Flops   Percentage  
-----  
Total instances     3       100.0  
Excluded from State Retention    3       100.0  
  - Will not convert      3       100.0  
    - Preserved            0        0.0  
    - Power intent excluded 3       100.0  
  - Could not convert      0        0.0  
    - Scan type             0        0.0  
    - No suitable cell      0        0.0  
State Retention instances    0       0.0  
-----  
  
INFO: skipping constant propagation  
PBS_Techmap-Global Mapping - Elapsed_Time 0, CPU_Time -  
0.00861799999999348  
stamp 'PBS_Techmap-Global Mapping' being created for table 'pbs_debug'  
  
  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time  
| Memory | Stage  
+-----+-----+-----+-----+  
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53  
(Nov14) | 244.6 MB | PBS_Generic-Start  
+-----+-----+-----+-----+  
00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.9(100.0) | 15:16:54  
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post  
+-----+-----+-----+-----+  
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54  
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations  
+-----+-----+-----+-----+  
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54  
(Nov14) | 244.6 MB | PBS_TechMap-Start  
+-----+-----+-----+-----+  
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54  
(Nov14) | 244.6 MB | PBS_TechMap-Premap HBO Optimizations  
+-----+-----+-----+-----+  
00:00:04(00:00:03) | 00:00:00(00:00:00) | -0.9( 0.0) | 15:16:54  
(Nov14) | 244.6 MB | PBS_Techmap-Global Mapping  
+-----+-----+-----+-----+  
Number of threads: 8 * 1  (id: pbs_debug, time_info v1.57)  
Info: (*N*) indicates data that was populated from previously saved  
time_info database  
Info: CPU time includes time of parent + longest thread  
Warning : Command 'commit_power_intent' cannot proceed as there is no  
power intent loaded. [CPI-506]
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
: Command 'commit_power_intent' requires a valid power_intent to
be loaded.
Info   : Wrote formal verification information. [CFM-5]
      : Wrote 'fv/da2_mealy/fv_map.fv.json' for netlist
'fv/da2_mealy/fv_map.v.gz'.
Info   : Wrote dofile. [CFM-1]
      : Dofile is 'fv/da2_mealy/rtl_to_fv_map.do'.
      : Alias mapping flow is enabled.
PBS_TechMap-Datapath Postmap Operations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Datapath Postmap Operations' being created for table
'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
  | Memory | Stage
-----+-----+-----+-----+
-----+-----+
  00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+-----+
-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.9(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+-----+
-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Start
-----+-----+-----+
-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+-----+
-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:00) | -0.9( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Techmap-Global Mapping
-----+-----+-----+
-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Postmap HBO Optimizations - Elapsed_Time 0, CPU_Time -
3.900000000012227e-5
stamp 'PBS_TechMap-Postmap HBO Optimizations' being created for table
'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
  | Memory | Stage
-----+-----+-----+-----+
-----+-----+
  00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.9(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Start
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | -0.9( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Techmap-Global Mapping
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+
-----+-----+
00:00:04(00:00:03) | -01:59:57(00:00:00) | -0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap HBO Optimizations
-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
Doing ConstProp on /designs/da2_mealy ...

Time taken by ConstProp Step: 00:00:00
PBS_TechMap-Postmap Clock Gating - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Postmap Clock Gating' being created for table
'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory | Stage
-----+-----+-----+
-----+-----+
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.9(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Start
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```

-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | -0.9( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Techmap-Global Mapping
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | -01:59:57(00:00:00) | -0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap HBO Optimizations
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap Clock Gating
-----+-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
-----+-----+
-----+-----+
hi_fo_buf 0 0 0 0
-----+-----+
Trick Calls Accepts Attempts Time (secs)
-----+-----+
hi_fo_buf 0 ( 0 / 0 ) 0.00
-----+-----+
Incremental optimization status
=====
Group
Tot Wrst Total DRC Total
Operation Area Weighted Slack Neg Max
init_delay 0 0 0 0 0
-----+-----+
Trick Calls Accepts Attempts Time (secs)
-----+-----+
crit_upsz 0 ( 0 / 0 ) 0.00
plc_bal_star 0 ( 0 / 0 ) 0.00
drc_buftimb 0 ( 0 / 0 ) 0.00
plc_st 0 ( 0 / 0 ) 0.00
plc_st_fence 0 ( 0 / 0 ) 0.00
plc_star 0 ( 0 / 0 ) 0.00
plc_laf_st 0 ( 0 / 0 ) 0.00
plc_laf_st_fence 0 ( 0 / 0 ) 0.00
drc_buftims 0 ( 0 / 0 ) 0.00
fopt 0 ( 0 / 0 ) 0.00
plc_laf_lo_st 0 ( 0 / 0 ) 0.00
plc_lo_st 0 ( 0 / 0 ) 0.00
mb_split 0 ( 0 / 0 ) 0.00

```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```

Local TNS optimization status
=====
                                         Group
                                         Tot Wrst      Total DRC Total
                                         Area Slacks      Neg Max
Operation          Total Weighted      Slack Cap
init_tns           0       0          0       0

      Trick   Calls   Accepts   Attempts   Time (secs)
-----
plc_bal_star      0   (     0 /     0 )  0.00
drc_buftimb      0   (     0 /     0 )  0.00
drc_buftims      0   (     0 /     0 )  0.00
crit_upsz        0   (     0 /     0 )  0.00
plc_laf_lo_st    0   (     0 /     0 )  0.00
plc_lo_st        0   (     0 /     0 )  0.00
fopt              0   (     0 /     0 )  0.00
crit_dnsz         0   (     0 /     0 )  0.00
dup               0   (     0 /     0 )  0.00
setup_dn          0   (     0 /     0 )  0.00
mb_split          0   (     0 /     0 )  0.00

PBS_TechMap-Postmap Cleanup - Elapsed_Time 0, CPU_Time -3.200000000032e-5
stamp 'PBS_TechMap-Postmap Cleanup' being created for table 'pbs_debug'

      Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory   | Stage
-----+-----+-----+-----+
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.9(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Start
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | -0.9( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Techmap-Global Mapping
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+-----+
00:00:04(00:00:03) | -01:59:57(00:00:00) | -0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap HBO Optimizations

```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap Clock Gating
-----+-----+
-----+-----+
00:00:04(00:00:03) | -01:59:57(00:00:00) | -0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap Cleanup
-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_Techmap-Post_MBCI - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Techmap-Post_MBCI' being created for table 'pbs_debug'

      Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
      | Memory | Stage
-----+-----+-----+
-----+-----+
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:53
(Nov14) | 244.6 MB | PBS_Generic-Start
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:01) | 100.9(100.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic_Opt-Post
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Start
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | -0.9( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Techmap-Global Mapping
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+
-----+-----+
00:00:04(00:00:03) | -01:59:57(00:00:00) | -0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap Clock Gating
-----+-----+
-----+-----+
00:00:04(00:00:03) | -01:59:57(00:00:00) | -0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_TechMap-Postmap Cleanup
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```

-----+-----+-----+
-----+-----+
 00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:16:54
(Nov14) | 244.6 MB | PBS_Techmap-Post_MBCI
-----+-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
##>===== Cadence Confidential (Mapping-Logical)
======
##>Main Thread Summary:
##>-----

##>STEP
Area      Memory          Elapsed      WNS      TNS      Insts
##>-----
##>M:Initial          0           244        0         -         -         13
##>M:Pre Cleanup       0           244        0         -         -         13
##>M:Setup             -           -          0         -         -         -
##>M:Launch ST          -           -          0         -         -         -
##>M:Design Partition   -           -          0         -         -         -
##>M>Create Partition Netlists  -           -          0         -         -         -
##>M:Init Power          -           -          0         -         -         -
##>M:Budgeting           -           -          0         -         -         -
##>M:Derenv-DB           -           -          0         -         -         -
##>M:Debug Outputs        -           -          0         -         -         -
##>M:ST loading           -           -          0         -         -         -
##>M:Distributed          -           -          0         -         -         -
##>M:Timer               -           -          0         -         -         -
##>M:Assembly            -           -          0         -         -         -
##>M:DFT                 -           -          0         -         -         -
##>M:DP Operations        0           244        0         -         -         12
##>M:Const Prop           0           244        0         8651      0         12
##>M:Cleanup              0           244        0         8651      0         12
##>M:MBCI                0           244        0         -         -         12
##>M:Const Gate Removal    -           -          0         -         -         -
##>M:Misc                  -           -          0         -         -         -

```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```

##>-----
-----
##>Total Elapsed 0
##>=====
=====

Info : Done mapping. [SYNTH-5]
      : Done mapping 'da2_mealy'.
Info : Incrementally optimizing. [SYNTH-7]
      : Incrementally optimizing 'da2_mealy' using 'high' effort.

Incremental optimization status
=====

          Group
          Tot Wrst    Total DRC Total
          Total Weighted   Neg   Max
Operation     Area   Slacks   Slack   Cap
init_iopt      0       0        0       0

-----
const_prop      0       0        0       0

-----
hi_fo_buf       0       0        0       0

          Trick   Calls   Accepts   Attempts   Time (secs)
-----
hi_fo_buf      0 ( 0 / 0 ) 0.00

Incremental optimization status
=====

          Group
          Tot Wrst    Total DRC Total
          Total Weighted   Neg   Max
Operation     Area   Slacks   Slack   Cap
init_delay     0       0        0       0

          Trick   Calls   Accepts   Attempts   Time (secs)
-----
crit_msz       0 ( 0 / 0 ) 0.00
crit_upsz      0 ( 0 / 0 ) 0.00
crit_slew       0 ( 0 / 0 ) 0.00
setup_dn       0 ( 0 / 0 ) 0.00
plc_bal_star   0 ( 0 / 0 ) 0.00
drc_buftimb   0 ( 0 / 0 ) 0.00
plc_st         0 ( 0 / 0 ) 0.00
plc_st_fence   0 ( 0 / 0 ) 0.00
plc_star       0 ( 0 / 0 ) 0.00
plc_laf_st    0 ( 0 / 0 ) 0.00
plc_laf_st_fence 0 ( 0 / 0 ) 0.00
drc_buftims   0 ( 0 / 0 ) 0.00
plc_laf_lo_st 0 ( 0 / 0 ) 0.00
plc_lo_st     0 ( 0 / 0 ) 0.00
fopt           0 ( 0 / 0 ) 0.00
crit_swap      0 ( 0 / 0 ) 0.00
mux2_swap      0 ( 0 / 0 ) 0.00
crit_dnsz      0 ( 0 / 0 ) 0.00
load_swap      0 ( 0 / 0 ) 0.00
fopt           0 ( 0 / 0 ) 0.00
setup_dn       0 ( 0 / 0 ) 0.00

```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

load_isol	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
rem_hi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
rem_hi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
phase	0 (	0 /	0 )	0.00
in_phase	0 (	0 /	0 )	0.00
merge_bit	0 (	0 /	0 )	0.00
merge_idrvr	0 (	0 /	0 )	0.00
merge_iload	0 (	0 /	0 )	0.00
merge_idload	0 (	0 /	0 )	0.00
merge_drvr	0 (	0 /	0 )	0.00
merge_load	0 (	0 /	0 )	0.00
decomp	0 (	0 /	0 )	0.00
p_decomp	0 (	0 /	0 )	0.00
levelize	0 (	0 /	0 )	0.00
mb_split	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
mux_retime	0 (	0 /	0 )	0.00
buf2inv	0 (	0 /	0 )	0.00
exp	0 (	0 /	0 )	0.00
gate_deco	0 (	0 /	0 )	0.00
gcomp_tim	0 (	0 /	0 )	0.00
inv_pair_2_buf	0 (	0 /	0 )	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
<hr/>				
crr_220	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_200	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_300	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_400	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_111	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_210	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_110	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_101	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_201	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_211	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crit_msz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
crit_slew	0 (	0 /	0 )	0.00
setup_dn	0 (	0 /	0 )	0.00
plc_bal_star	0 (	0 /	0 )	0.00
drc_buftimb	0 (	0 /	0 )	0.00
plc_st	0 (	0 /	0 )	0.00
plc_st_fence	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

plc_laf_st	0 (	0 /	0 )	0.00
plc_laf_st_fence	0 (	0 /	0 )	0.00
drc_buftims	0 (	0 /	0 )	0.00
plc_lo_st	0 (	0 /	0 )	0.00
fopt	0 (	0 /	0 )	0.00
crit_swap	0 (	0 /	0 )	0.00
mux2_swap	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
load_swap	0 (	0 /	0 )	0.00
fopt	0 (	0 /	0 )	0.00
setup_dn	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
rem_bi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
rem_bi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
merge_bit	0 (	0 /	0 )	0.00
merge_idrvr	0 (	0 /	0 )	0.00
merge_iload	0 (	0 /	0 )	0.00
merge_idload	0 (	0 /	0 )	0.00
merge_drvr	0 (	0 /	0 )	0.00
merge_load	0 (	0 /	0 )	0.00
phase	0 (	0 /	0 )	0.00
decomp	0 (	0 /	0 )	0.00
p_decomp	0 (	0 /	0 )	0.00
levelize	0 (	0 /	0 )	0.00
mb_split	0 (	0 /	0 )	0.00
in_phase	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
mux_retime	0 (	0 /	0 )	0.00
buf2inv	0 (	0 /	0 )	0.00
exp	0 (	0 /	0 )	0.00
gate_deco	0 (	0 /	0 )	0.00
gcomp_tim	0 (	0 /	0 )	0.00
inv_pair_2_buf	0 (	0 /	0 )	0.00
init_drc	0	0	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
<hr/>				
plc_st	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
drc_bufs	0 (	0 /	0 )	0.00
drc_fopt	0 (	0 /	0 )	0.00
drc_bufb	0 (	0 /	0 )	0.00
simple_buf	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
crit_slew	0 (	0 /	0 )	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
<hr/>				
plc_st	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
drc_buf_sp	0 (	0 /	0 )	0.00
drc_bufs	0 (	0 /	0 )	0.00

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

drc_fopt	0 (	0 /	0 )	0.00
drc_bufb	0 (	0 /	0 )	0.00
simple_buf	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
drc_buf_sp	0 (	0 /	0 )	0.00
drc_bufs	0 (	0 /	0 )	0.00
drc_fopt	0 (	0 /	0 )	0.00
drc_bufb	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
init_tns		0	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
fopt	0 (	0 /	0 )	0.00
plc_bal_star	0 (	0 /	0 )	0.00
drc_buftimb	0 (	0 /	0 )	0.00
drc_buftims	0 (	0 /	0 )	0.00
crit_msz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
plc_laf_lo_st	0 (	0 /	0 )	0.00
plc_lo_st	0 (	0 /	0 )	0.00
crit_swap	0 (	0 /	0 )	0.00
mux2_swap	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
load_swap	0 (	0 /	0 )	0.00
fopt	0 (	0 /	0 )	0.00
setup_dn	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
rem_hi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
rem_hi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
merge_bit	0 (	0 /	0 )	0.00
merge_idrvr	0 (	0 /	0 )	0.00
merge_iload	0 (	0 /	0 )	0.00
merge_idload	0 (	0 /	0 )	0.00
merge_drvr	0 (	0 /	0 )	0.00
merge_load	0 (	0 /	0 )	0.00
phase	0 (	0 /	0 )	0.00
decomp	0 (	0 /	0 )	0.00
p_decomp	0 (	0 /	0 )	0.00
levelize	0 (	0 /	0 )	0.00
mb_split	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
mux_retime	0 (	0 /	0 )	0.00
crr_local	0 (	0 /	0 )	0.00

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

buf2inv	0 (	0 /	0 )	0.00
init_area	0 (	0	0	0
rem_inv_qb	0 (	0	0	0
Trick	Calls	Accepts	Attempts	Time (secs)
-----				
undup	0 (	0 /	0 )	0.00
rem_buf	0 (	0 /	0 )	0.00
rem_inv	0 (	0 /	0 )	0.00
merge.bi	0 (	0 /	0 )	0.00
rem_inv_qb	2 (	2 /	2 )	0.00
seq_res_area	3 (	0 /	0 )	0.02
io_phase	0 (	0 /	0 )	0.00
gate_comp	0 (	0 /	0 )	0.00
gcomp_mog	0 (	0 /	0 )	0.00
glob_area	5 (	0 /	5 )	0.00
area_down	0 (	0 /	0 )	0.00
size_n_buf	0 (	0 /	0 )	0.00
gate_deco_area	0 (	0 /	0 )	0.00
rem_buf	0 (	0 /	0 )	0.00
rem_inv	0 (	0 /	0 )	0.00
merge.bi	0 (	0 /	0 )	0.00
rem_inv_qb	0 (	0 /	0 )	0.00

Incremental optimization status

Operation	Group				
	Tot Wrst		Total DRC Total		
	Total	Weighted	Neg	Max	Cap
init_delay	0	0	0	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
-----				
crr_220	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_200	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_300	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_400	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_111	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_210	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_110	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_101	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_201	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crr_211	0 (	0 /	0 )	0.00
crr_glob	0 (	0 /	0 )	0.00
crit_msz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
crit_slew	0 (	0 /	0 )	0.00
setup_dn	0 (	0 /	0 )	0.00

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

plc_bal_star	0 (	0 /	0 )	0.00
drc_buftimb	0 (	0 /	0 )	0.00
plc_st	0 (	0 /	0 )	0.00
plc_st_fence	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
plc_laf_st	0 (	0 /	0 )	0.00
plc_laf_st_fence	0 (	0 /	0 )	0.00
drc_buftims	0 (	0 /	0 )	0.00
plc_lo_st	0 (	0 /	0 )	0.00
fopt	0 (	0 /	0 )	0.00
crit_swap	0 (	0 /	0 )	0.00
mux2_swap	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
load_swap	0 (	0 /	0 )	0.00
fopt	0 (	0 /	0 )	0.00
setup_dn	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
rem_bi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
rem_bi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
merge_bit	0 (	0 /	0 )	0.00
merge_idrvr	0 (	0 /	0 )	0.00
merge_iload	0 (	0 /	0 )	0.00
merge_idload	0 (	0 /	0 )	0.00
merge_drvr	0 (	0 /	0 )	0.00
merge_load	0 (	0 /	0 )	0.00
phase	0 (	0 /	0 )	0.00
decomp	0 (	0 /	0 )	0.00
p_decomp	0 (	0 /	0 )	0.00
levelize	0 (	0 /	0 )	0.00
mb_split	0 (	0 /	0 )	0.00
in_phase	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
mux_retime	0 (	0 /	0 )	0.00
buf2inv	0 (	0 /	0 )	0.00
exp	0 (	0 /	0 )	0.00
gate_deco	0 (	0 /	0 )	0.00
gcomp_tim	0 (	0 /	0 )	0.00
inv_pair_2_buf	0 (	0 /	0 )	0.00
init_drc	0	0	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
drc_bufs	0 (	0 /	0 )	0.00
drc_fopt	0 (	0 /	0 )	0.00
drc_bufb	0 (	0 /	0 )	0.00
simple_buf	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
crit_slew	0 (	0 /	0 )	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
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## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

plc_st	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
drc_bufs	0 (	0 /	0 )	0.00
drc_fopt	0 (	0 /	0 )	0.00
drc_bufb	0 (	0 /	0 )	0.00
simple_buf	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
init_tns	0	0	0	0
Trick	Calls	Accepts	Attempts	Time (secs)
fopt	0 (	0 /	0 )	0.00
plc_bal_star	0 (	0 /	0 )	0.00
drc_buftimb	0 (	0 /	0 )	0.00
drc_buftims	0 (	0 /	0 )	0.00
crit_msz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
plc_laf_lo_st	0 (	0 /	0 )	0.00
plc_lo_st	0 (	0 /	0 )	0.00
crit_swap	0 (	0 /	0 )	0.00
mux2_swap	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
load_swap	0 (	0 /	0 )	0.00
fopt	0 (	0 /	0 )	0.00
setup_dn	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
rem_hi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
rem_hi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
merge_bit	0 (	0 /	0 )	0.00
merge_idrvr	0 (	0 /	0 )	0.00
merge_iload	0 (	0 /	0 )	0.00
merge_idload	0 (	0 /	0 )	0.00
merge_drvr	0 (	0 /	0 )	0.00
merge_load	0 (	0 /	0 )	0.00
phase	0 (	0 /	0 )	0.00
decomp	0 (	0 /	0 )	0.00
p_decomp	0 (	0 /	0 )	0.00
levelize	0 (	0 /	0 )	0.00
mb_split	0 (	0 /	0 )	0.00

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

dup	0 (	0 /	0 )	0.00
mux_retime	0 (	0 /	0 )	0.00
crr_local	0 (	0 /	0 )	0.00
buf2inv	0 (	0 /	0 )	0.00
 init_area	 0	 0	 0	 0
Trick	Calls	Accepts	Attempts	Time (secs)
undup	0 (	0 /	0 )	0.00
rem_buf	0 (	0 /	0 )	0.00
rem_inv	0 (	0 /	0 )	0.00
merge_bi	0 (	0 /	0 )	0.00
rem_inv_qb	0 (	0 /	0 )	0.00
io_phase	0 (	0 /	0 )	0.00
gate_comp	0 (	0 /	0 )	0.00
gcomp_mog	0 (	0 /	0 )	0.00
glob_area	5 (	0 /	5 )	0.00
area_down	0 (	0 /	0 )	0.00
size_n_buf	0 (	0 /	0 )	0.00
gate_deco_area	0 (	0 /	0 )	0.00

### Incremental optimization status

Operation		Group		Total DRC Total	
		Area	Weighted Slacks		
init_delay		0	0	0 0	

Trick	Calls	Accepts	Attempts	Time (secs)
crit_msz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
crit_slew	0 (	0 /	0 )	0.00
setup_dn	0 (	0 /	0 )	0.00
plc_bal_star	0 (	0 /	0 )	0.00
drc_buftimb	0 (	0 /	0 )	0.00
plc_st	0 (	0 /	0 )	0.00
plc_st_fence	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
plc_laf_st	0 (	0 /	0 )	0.00
plc_laf_st_fence	0 (	0 /	0 )	0.00
drc_buftims	0 (	0 /	0 )	0.00
plc_laf_lo_st	0 (	0 /	0 )	0.00
plc_lo_st	0 (	0 /	0 )	0.00
fopt	0 (	0 /	0 )	0.00
crit_swap	0 (	0 /	0 )	0.00
mux2_swap	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
load_swap	0 (	0 /	0 )	0.00
fopt	0 (	0 /	0 )	0.00
setup_dn	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
load_isol	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
move_for	0 (	0 /	0 )	0.00
rem_bi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

rem_hi	0 (	0 /	0 )	0.00
offload	0 (	0 /	0 )	0.00
phase	0 (	0 /	0 )	0.00
in_phase	0 (	0 /	0 )	0.00
merge_bit	0 (	0 /	0 )	0.00
merge_idrvr	0 (	0 /	0 )	0.00
merge_iload	0 (	0 /	0 )	0.00
merge_idload	0 (	0 /	0 )	0.00
merge_drvr	0 (	0 /	0 )	0.00
merge_load	0 (	0 /	0 )	0.00
decomp	0 (	0 /	0 )	0.00
p_decomp	0 (	0 /	0 )	0.00
levelize	0 (	0 /	0 )	0.00
mb_split	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
mux_retime	0 (	0 /	0 )	0.00
buf2inv	0 (	0 /	0 )	0.00
exp	0 (	0 /	0 )	0.00
gate_deco	0 (	0 /	0 )	0.00
gcomp_tim	0 (	0 /	0 )	0.00
inv_pair_2_buf	0 (	0 /	0 )	0.00
init_drc	0	0	0	0
Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
drc_bufs	0 (	0 /	0 )	0.00
drc_fopt	0 (	0 /	0 )	0.00
drc_bufb	0 (	0 /	0 )	0.00
simple_buf	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
crit_slew	0 (	0 /	0 )	0.00
Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
drc_bufs	0 (	0 /	0 )	0.00
drc_fopt	0 (	0 /	0 )	0.00
drc_bufb	0 (	0 /	0 )	0.00
simple_buf	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00
crit_upsz	0 (	0 /	0 )	0.00
Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (	0 /	0 )	0.00
plc_star	0 (	0 /	0 )	0.00
drc_bufs	0 (	0 /	0 )	0.00
drc_fopt	0 (	0 /	0 )	0.00
drc_bufb	0 (	0 /	0 )	0.00
dup	0 (	0 /	0 )	0.00
crit_dnsz	0 (	0 /	0 )	0.00

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
crit_upsz          0 (      0 /      0 )  0.00
=====
Stage : incr_opt
=====
=====
Message Summary
=====

-----
| Id     | Sev   | Count |                         Message Text
|
-----

| CFM-1  | Info   | 1 |Wrote dofile.
|
| CFM-5  | Info   | 1 |Wrote formal verification information.
|
| CPI-506 | Warning | 1 |Command 'commit_power_intent' cannot proceed
as    |
|       |         |    | there is no power intent loaded.
|
| PA-7   | Info   | 4 |Resetting power analysis results.
|
|       |         |    |All computed switching activities are removed.
|
| SYNTH-5 | Info   | 1 |Done mapping.
|
| SYNTH-7 | Info   | 1 |Incrementally optimizing.
|
-----

Info   : Done incrementally optimizing. [SYNTH-8]
        : Done incrementally optimizing 'da2_mealy'.
Finished SDC export (command execution time mm:ss (real) = 00:00).
Info   : Joules engine is used. [RPT-16]
        : Joules engine is being used for the command report_power.
Info   : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0
netlist
        : da2_mealy
Info   : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info   : ACTP-0001 Activity propagation ended for stim#0
Info   : PWRA-0001 [PwrInfo] compute_power effective options
        : -mode : vectorless
        : -skip_propagation : 1
        : -frequency_scaling_factor : 1.0
        : -use_clock_freq : stim
        : -stim :/stim#0
        : -fromGenus : 1
Info   : ACTP-0001 Timing initialization started
Info   : ACTP-0001 Timing initialization ended
Info   : PWRA-0002 [PwrInfo] Skipping activity propagation due to -
skip_ap
        : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for
vectorless
        : flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with
vectorless mode
        : of power analysis, ignored this option.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Info    : PWRA-0002 Started 'vectorless' power computation.
Info    : PWRA-0002 Finished power computation.
Info    : PWRA-0007 [PwrInfo] Completed successfully.
          : Info=6, Warn=2, Error=0, Fatal=0
Output file: DA2_power.rep
WARNING: This version of the tool is 875 days old.
legacy_genus:/>
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

### Innovus Terminal:

```
[student@cad21 innovus]$ csh
[student@cad21 innovus]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 innovus]$ innovus

Cadence Innovus(TM) Implementation System.
Copyright 2021 Cadence Design Systems, Inc. All rights reserved
worldwide.

Version: v21.15-s110_1, built Fri Sep 23 13:08:12 PDT 2022
Options:
Date: Thu Nov 14 15:29:19 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64)
(12cores*20cpus*12th Gen Intel(R) Core(TM) i7-12700 25600KB)
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

License:
[15:29:19.095705] Configured Lic search path (21.01-s002):
5280@cadence

      invs Innovus Implementation System      21.1 checkout
succeeded
      8 CPU jobs allowed with the current license(s). Use
setMultiCpuUsage to set your required CPU count.
Create and set the environment variable TMPDIR to
/tmp/innovus_temp_21787_cad21_student_5P5DXT.

Change the soft stacksize limit to 0.2%RAM (63 mbytes). Set global
soft_stack_size_limit to change the value.

**INFO: MMMC transition support version v31-84

[INFO] Loading PVS 22.20 fill procedures
innovus 1> #% Begin Load MMMC data ... (date=11/14 15:32:32, mem=1026.6M)
#% End Load MMMC data ... (date=11/14 15:32:32, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1027.3M, current mem=1027.3M)

Loading LEF file
../../../../install/FOUNDRY/digital/180nm/dig/lef/all.lef ...
Set DBUPerIGU to M2 pitch 1320.
**WARN: (IMPLF-200): Pin 'A' in macro 'ANTENNA' has no ANTENNAGATEAREA
value defined. The library data is incomplete and some process antenna
rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-201): Pin 'Q[0]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[10]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[11]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
**WARN: (IMPLF-201): Pin 'Q[12]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[13]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[14]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[15]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[1]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[2]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[3]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[4]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[5]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[6]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[7]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[8]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[9]' in macro 'rom_512x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[0]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[10]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
**WARN: (IMPLF-201): Pin 'Q[11]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (IMPLF-201): Pin 'Q[12]' in macro 'ram_256x16A' has no
ANTENNADIFFAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-201' for more detail.
**WARN: (EMS-27): Message (IMPLF-201) has exceeded the current
message display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
**WARN: (IMPLF-200): Pin 'PAD' in macro 'PDB04DGZ' has no
ANTENNAGATEAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-200): Pin 'OEN' in macro 'PDB04DGZ' has no
ANTENNAGATEAREA value defined. The library data is incomplete and some
process antenna rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.
**WARN: (IMPLF-200): Pin 'I' in macro 'PDB04DGZ' has no ANTENNAGATEAREA
value defined. The library data is incomplete and some process antenna
rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.

## Check design process and node:
## Both design process and tech node are not set.

Loading view definition file from Default.view
Reading maxt timing library
'/home/install/FOUNDRY/digital/180nm/dig/lib/slow.lib' ...
**WARN: (TECHLIB-302): No function defined for cell 'HOLDX1'. The cell
will only be used for analysis. (File
/home/install/FOUNDRY/digital/180nm/dig/lib/slow.lib)
Read 462 cells in library 'tsmc18'
Reading mint timing library
'/home/install/FOUNDRY/digital/180nm/dig/lib/fast.lib' ...
**WARN: (TECHLIB-302): No function defined for cell 'HOLDX1'. The cell
will only be used for analysis. (File
/home/install/FOUNDRY/digital/180nm/dig/lib/fast.lib)
Read 470 cells in library 'tsmc18'
*** End library_loading (cpu=0.01min, real=0.02min, mem=31.9M,
fe_cpu=0.50min, fe_real=3.23min, fe_mem=1070.0M) ***
#% Begin Load netlist data ... (date=11/14 15:32:33, mem=1048.6M)
*** Begin netlist parsing (mem=1070.0M) ***
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR3X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR3X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR3X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (EMS-27): Message (IMPVL-159) has exceeded the current
message display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
Created 470 new cells from 2 timing libraries.
Reading netlist ...
Backslashed names will retain backslash and a trailing blank character.
Reading verilog netlist 'DA2_netlist.v'
**WARN: (IMPVL-346): Module 'NOR2X6' is instantiated in the netlist,
but is not defined in the LEF files. Since there is no real cell
definition for such a cell, it will be treated as an empty module.
Type 'man IMPVL-346' for more detail.

*** Memory Usage v#1 (Current mem = 1070.031M, initial mem = 483.863M)
***
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
*** End netlist parsing (cpu=0:00:00.0, real=0:00:00.0, mem=1070.0M) ***
#% End Load netlist data ... (date=11/14 15:32:33, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1063.1M, current mem=1063.1M)
Top level cell is da2_mealy.
Hooked 932 DB cells to tlib cells.
** Removed 8 unused lib cells.
**WARN: (IMPDB-2504): Unable to find netlist cell in the design data of
the library or LEF. The 'NOR2X6' cell is instantiated in the Verilog
netlist, but not defined in the library or design data. Its pin
directions might be derived incorrectly. Include the cell definition or
its pin information in the library or design data and reload the design
to avoid potential issues.
Type 'man IMPDB-2504' for more detail.
1 empty module found.
Starting recursive module instantiation check.
No recursion found.
Term dir updated for 0 vinsts of 1 cells.
Building hierarchical netlist for Cell da2_mealy ...
*** Netlist is unique.
** info: there are 952 modules.
** info: there are 9 stdCell insts.

*** Memory Usage v#1 (Current mem = 1124.445M, initial mem = 483.863M)
***
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
unless standard cell models of this type exist in the LEF/OA library.
Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 560 (derived)
Vertical Layer M2 offset = 660 (derived)
Start create_tracks
Generated pitch 0.99 in Metal6 is different from 1.32 defined in
technology file in preferred direction.
Generated pitch 0.56 in Metal5 is different from 1.12 defined in
technology file in preferred direction.
Extraction setup Started
Initializing multi-corner RC extraction with 1 active RC Corners ...
Reading Capacitance Table File
../../../../../install/FOUNDRY/digital/180nm/dig/captable/t018s6mlv.capTbl
...
Cap table was created using Encounter 10.10-s002_1.
Process name: t018s6mm.
Importing multi-corner RC tables ...
Summary of Active RC-Corners :

Analysis View: worst
  RC-Corner Name      : rc
  RC-Corner Index     : 0
  RC-Corner Temperature : 25 Celsius
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
RC-Corner Cap Table      :
'../../../../install/FOUNDRY/digital/180nm/dig/captable/t018s6mlv.capTbl'
  RC-Corner PreRoute Res Factor      : 1
  RC-Corner PreRoute Cap Factor     : 1
  RC-Corner PostRoute Res Factor    : 1 {1 1 1}
  RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
  RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
  RC-Corner PreRoute Clock Res Factor : 1      [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PreRoute Clock Cap Factor : 1      [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}  [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}  [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}

Analysis View: best
  RC-Corner Name      : rc
  RC-Corner Index     : 0
  RC-Corner Temperature : 25 Celsius
  RC-Corner Cap Table  :
'../../../../install/FOUNDRY/digital/180nm/dig/captable/t018s6mlv.capTbl'
  RC-Corner PreRoute Res Factor      : 1
  RC-Corner PreRoute Cap Factor     : 1
  RC-Corner PostRoute Res Factor    : 1 {1 1 1}
  RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
  RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
  RC-Corner PreRoute Clock Res Factor : 1      [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PreRoute Clock Cap Factor : 1      [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}  [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}  [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
*Info: initialize multi-corner CTS.
Reading timing constraints file 'DA2.sdc' ...
Current (total cpu=0:00:30.3, real=0:03:14, peak res=1355.9M, current
mem=1355.9M)
**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
DA2.sdc, Line 9).

**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
DA2.sdc, Line 10).

da2_mealy
INFO (CTE): Reading of timing constraints file DA2.sdc completed, with 2
WARNING
Ending "Constraint file reading stats" (total cpu=0:00:00.0,
real=0:00:00.0, peak res=1374.6M, current mem=1374.6M)
Current (total cpu=0:00:30.4, real=0:03:14, peak res=1374.6M, current
mem=1374.6M)
Total number of combinational cells: 266
Total number of sequential cells: 178
Total number of tristate cells: 18
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Total number of level shifter cells: 0
Total number of power gating cells: 0
Total number of isolation cells: 0
Total number of power switch cells: 0
Total number of pulse generator cells: 0
Total number of always on buffers: 0
Total number of retention cells: 0
List of usable buffers: BUFX2 BUFX1 BUFX12 BUFX16 BUFX20 BUFX3 BUFX4
BUFX8 BUFXL CLKBUFX2 CLKBUFX1 CLKBUFX12 CLKBUFX16 CLKBUFX20 CLKBUFX3
CLKBUFX4 CLKBUFX8 CLKBUFXL
Total number of usable buffers: 18
List of unusable buffers:
Total number of unusable buffers: 0
List of usable inverters: CLKINVX2 CLKINVX1 CLKINVX12 CLKINVX16 CLKINVX20
CLKINVX3 CLKINVX4 CLKINVX8 CLKINVXL INVX1 INVX2 INVX12 INVX16 INVX20
INVX3 INVXL INVX4 INVX8
Total number of usable inverters: 18
List of unusable inverters: RFRDX2 RFRDX1 RFRDX4
Total number of unusable inverters: 3
List of identified usable delay cells: DLY2X1 DLY1X1 DLY4X1 DLY3X1
Total number of identified usable delay cells: 4
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0

*** Summary of all messages that are not suppressed in this session:
Severity ID           Count Summary
WARNING IMPLF-200      4  Pin '%s' in macro '%s' has no
ANTENNAGAT...
WARNING IMPLF-201      50  Pin '%s' in macro '%s' has no
ANTENNADIF...
WARNING IMPFP-3961      2  The techSite '%s' has no related
standar...
WARNING IMPVL-346       1  Module '%s' is instantiated in the
netli...
WARNING IMPVL-159      924  Pin '%s' of cell '%s' is defined in LEF
...
WARNING IMPDB-2504      1  Unable to find netlist cell in the
desig...
WARNING TCLCMD-1461      2  Skipped unsupported command: %s
WARNING TECHLIB-302      2  No function defined for cell '%s'. The
c...
*** Message Summary: 986 warning(s), 0 error(s)

innovus 1> Adjusting coreMargin left    to finFet grid (PlacementGrid) :
after adjusting :2.64
Adjusting coreMargin bottom   to finFet grid (PlacementGrid) : after
adjusting :2.8
Adjusting coreMargin right    to finFet grid (PlacementGrid) : after
adjusting :2.64
Adjusting coreMargin top     to finFet grid (PlacementGrid) : after
adjusting :2.8
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
unless standard cell models of this type exist in the LEF/OA library.  
Ignore this warning if the SITE is not used by the library.  
Alternatively, remove the SITE definition for the LEF/OA library to avoid  
this message.  
Type 'man IMPFP-3961' for more detail.  
Horizontal Layer M1 offset = 560 (derived)  
Vertical Layer M2 offset = 660 (derived)  
Start create_tracks  
Generated pitch 0.99 in Metal6 is different from 1.32 defined in  
technology file in preferred direction.  
Generated pitch 0.56 in Metal5 is different from 1.12 defined in  
technology file in preferred direction.  
innovus 1> **WARN: (IMPFP-3961): The techSite 'corner' has no related  
standard cells in the LEF/OA library. The calculations for this site type  
cannot be made unless standard cell models of this type exist in the  
LEF/OA library. Ignore this warning if the SITE is not used by the  
library. Alternatively, remove the SITE definition for the LEF/OA library  
to avoid this message.  
Type 'man IMPFP-3961' for more detail.  
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells  
in the LEF/OA library. The calculations for this site type cannot be made  
unless standard cell models of this type exist in the LEF/OA library.  
Ignore this warning if the SITE is not used by the library.  
Alternatively, remove the SITE definition for the LEF/OA library to avoid  
this message.  
Type 'man IMPFP-3961' for more detail.  
Horizontal Layer M1 offset = 560 (derived)  
Vertical Layer M2 offset = 660 (derived)  
Start create_tracks  
Generated pitch 0.99 in Metal6 is different from 1.32 defined in  
technology file in preferred direction.  
Generated pitch 0.56 in Metal5 is different from 1.12 defined in  
technology file in preferred direction.  
innovus 1> The ring targets are set to core/block ring wires.  
addRing command will consider rows while creating rings.  
addRing command will disallow rings to go over rows.  
addRing command will ignore shorts while creating rings.
```

```
viaInitial starts at Thu Nov 14 15:35:53 2024  
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is  
obsolete and is being ignored. Remove this statement from the technology  
file: VIARULE TURNM1 GENERATE.  
Type 'man IMPPP-557' for more detail.  
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is  
obsolete and is being ignored. Remove this statement from the technology  
file: VIARULE TURNM2 GENERATE.  
Type 'man IMPPP-557' for more detail.  
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is  
obsolete and is being ignored. Remove this statement from the technology  
file: VIARULE TURNM3 GENERATE.  
Type 'man IMPPP-557' for more detail.  
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is  
obsolete and is being ignored. Remove this statement from the technology  
file: VIARULE TURNM4 GENERATE.  
Type 'man IMPPP-557' for more detail.  
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is  
obsolete and is being ignored. Remove this statement from the technology  
file: VIARULE TURNM5 GENERATE.  
Type 'man IMPPP-557' for more detail.
```

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```
**WARN: (IMPPP-557): A single-layer VIARULE GENERATE for turn-vias is
obsolete and is being ignored. Remove this statement from the technology
file: VIARULE TURNM6 GENERATE.
Type 'man IMPPP-557' for more detail.
viaInitial ends at Thu Nov 14 15:35:53 2024
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1439.1M)
**WARN: (IMPPP-136): The currently specified top spacing 0.200000 is
less than the required spacing 0.280000 for widths specified as 0.700000
and 0.700000.
**WARN: (IMPPP-136): The currently specified bottom spacing 0.200000
is less than the required spacing 0.280000 for widths specified as
0.700000 and 0.700000.
**WARN: (IMPPP-136): The currently specified left spacing 0.200000 is
less than the required spacing 0.460000 for widths specified as 0.700000
and 0.700000.
**WARN: (IMPPP-136): The currently specified right spacing 0.200000 is
less than the required spacing 0.460000 for widths specified as 0.700000
and 0.700000.
Ring generation is complete.
vias are now being generated.
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 1.68) (2.14, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 28.50) (2.14,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.86, 1.68) (31.30,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.86, 28.50) (31.30,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 1.68) (2.14, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.86, 1.68) (31.30,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 28.50) (2.14,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.86, 28.50) (31.30,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 0.70) (0.98, 1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 29.66) (1.24,
30.10).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (32.02, 0.70) (32.46,
1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (32.02, 29.40) (32.46,
30.10).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 0.70) (0.98, 1.40).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (32.02, 0.70) (32.46,
1.40).
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (0.54, 29.66) (1.24,
30.10).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (32.02, 29.40) (32.46,
30.10).
addRing created 8 wires.
ViaGen created 0 via, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+-----+
| Metal5 |         4        |       NA      |
| Metal6 |         4        |       NA      |
+-----+-----+-----+
innovus 1> addStripe will allow jog to connect padcore ring and block
ring.

Stripes will stop at the boundary of the specified area.
When breaking rings, the power planner will consider the existence of
blocks.
Stripes will not extend to closest target.
The power planner will set stripe antenna targets to none (no trimming
allowed).
Stripes will not be created over regions without power planning wires.
The entire stripe set will break at the domain if one of the nets is not
in the domain.
addStripe will break automatically at non-default domains when generating
global stripes over the core area or default domain.
Offset for stripe breaking is set to 0.

Initialize fgc environment(mem: 1439.1M) ... fail and won't use fgc to
check drc(cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1439.1M)
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1439.1M)
Loading wires (cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1439.1M)
Loading via instances (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1439.1M)
**WARN: (IMPPP-136): The currently specified spacing 0.200000 in -
spacing option is less than the required spacing 0.460000 for widths
specified as 0.700000 and 0.700000.
Starting stripe generation ...
Non-Default Mode Option Settings :
    NONE
Stripe generation is complete.
vias are now being generated.
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (3.64, 1.68) (4.08, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (3.64, 28.50) (4.08,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (8.64, 1.68) (9.08, 2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (8.64, 28.50) (9.08,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (13.64, 1.68) (14.08,
2.30).
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (13.64, 28.50) (14.08,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (18.64, 1.68) (19.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (18.64, 28.50) (19.08,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (23.64, 1.68) (24.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (23.64, 28.50) (24.08,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (28.64, 1.68) (29.08,
2.30).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (28.64, 28.50) (29.08,
29.12).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (4.80, 0.70) (5.24, 1.32).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (4.80, 29.48) (5.24,
30.10).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (9.80, 0.70) (10.24, 1.32).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (9.80, 29.48) (10.24,
30.10).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (14.80, 0.70) (15.24,
1.32).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (14.80, 29.48) (15.24,
30.10).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (19.80, 0.70) (20.24,
1.32).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (19.80, 29.48) (20.24,
30.10).
**WARN: (EMS-27): Message (IMPPP-531) has exceeded the current
message display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
addStripe created 12 wires.
ViaGen created 0 via, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+-----+
| Metal16 |      12       |      NA       |
+-----+-----+-----+
innovus 1> **WARN: (IMPSR-4058): Sroute option: blockPinTarget should be
used in conjunction with option: -connect blockPin.
*** Begin SPECIAL ROUTE on Thu Nov 14 15:36:42 2024 ***
SPECIAL ROUTE ran on directory: /home/student/Desktop/21bec1033/innovus
SPECIAL ROUTE ran on machine: cad21 (Linux 4.18.0-425.19.2.el8_7.x86_64
x86_64 2.10Ghz)
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Begin option processing ...
srouteConnectPowerBump set to false
routeSelectNet set to "vdd vss"
routeSpecial set to true
srouteBottomLayerLimit set to 1
srouteBottomTargetLayerLimit set to 1
srouteConnectBlockPin set to false
srouteConnectConverterPin set to false
srouteConnectPadPin set to false
srouteConnectStripe set to false
srouteCrossoverViaBottomLayer set to 1
srouteCrossoverViaTopLayer set to 6
srouteFollowCorePinEnd set to 3
srouteFollowPadPin set to false
srouteJogControl set to "preferWithChanges differentLayer"
srouteNoViaOnWireShape set to "padring ring stripe blockring blockpin
coverpin blockwire corewire followpin iowire"
sroutePadPinAllPorts set to true
sroutePreserveExistingRoutes set to true
srouteRoutePowerBarPortOnBothDir set to true
srouteStopBlockPin set to "nearestTarget"
srouteTopLayerLimit set to 6
srouteTopTargetLayerLimit set to 6
End option processing: cpu: 0:00:00, real: 0:00:00, peak: 2944.00 megs.

Reading DB technology information...
Finished reading DB technology information.
Reading floorplan and netlist information...
Finished reading floorplan and netlist information.
Read in 12 layers, 6 routing layers, 1 overlap layer
Read in 471 macros, 10 used
Read in 8 components
  8 core components: 8 unplaced, 0 placed, 0 fixed
Read in 4 logical pins
Read in 4 nets
Read in 2 special nets, 2 routed
2 nets selected.

Begin power routing ...
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the vdd net.
Run the globalNetConnect command or change the CPF file to ensure that
the netlist reflects the correct power ground connections. The standard
cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
connection.
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the vss net.
Run the globalNetConnect command or change the CPF file to ensure that
the netlist reflects the correct power ground connections. The standard
cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
connection.
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net vdd.  
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".  
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net vss.  
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".  
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net vss.  
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".  
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net vdd.  
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".  
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net vss.  
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".  
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net vdd.  
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".  
CPU time for vdd FollowPin 0 seconds  
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net vss.  
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".  
CPU time for vss FollowPin 0 seconds  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation, viaGen fail to generate via on layer Via56 at (30.86, 22.56) (31.30, 23.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation, viaGen fail to generate via on layer Via56 at (30.86, 22.56) (31.30, 23.36).  
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation, viaGen fail to generate via on layer Via56 at (30.86, 22.56) (31.30, 23.36).
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.89, 22.56) (31.30,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (31.16, 22.56) (31.30,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.86, 12.48) (31.30,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.86, 12.48) (31.30,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.86, 12.48) (31.30,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.89, 12.48) (31.30,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (31.16, 12.48) (31.30,
13.28).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (30.86, 2.58) (31.30,
3.20).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 22.56) (2.14,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 22.56) (2.14,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 22.56) (2.14,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 22.56) (2.14,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 22.56) (2.14,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 22.56) (2.14,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.77, 22.56) (2.14,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 22.56) (2.14,
23.36).
**WARN: (IMPPP-531): ViaGen Warning: Due to SPACING rule violation,
viaGen fail to generate via on layer Via56 at (1.70, 12.48) (2.14,
13.28).
**WARN: (EMS-27): Message (IMPPP-531) has exceeded the current
message display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
Number of Core ports routed: 11 open: 1
Number of Followpin connections: 6
End power routing: cpu: 0:00:00, real: 0:00:00, peak: 2952.00 megs.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Begin updating DB with routing results ...
Updating DB with 5 via definition ...Extracting standard cell pins and
blockage .....
Pin and blockage extraction finished

sroute post-processing starts at Thu Nov 14 15:36:42 2024
The viaGen is rebuilding shadow vias for net vdd.
sroute post-processing ends at Thu Nov 14 15:36:42 2024
sroute created 29 wires.
ViaGen created 1 via, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+-----+
| Metal1 |         17      |        NA     |
| Via12  |          1       |         0     |
| Metal2 |          1       |        NA     |
| Metal6 |         11      |        NA     |
+-----+-----+-----+
*** placeDesign #1 [begin] : totSession cpu/real = 0:00:51.0/0:07:47.8
(0.1), mem = 1444.0M
Extracting standard cell pins and blockage .....
Pin and blockage extraction finished
*** Starting placeDesign default flow ***
*** Start deleteBufferTree ***
Info: Detect buffers to remove automatically.
Analyzing netlist ...
Updating netlist

*summary: 0 instances (buffers/inverters) removed
*** Finish deleteBufferTree (0:00:00.1) ***
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
Set Default Input Pin Transition as 1 ps.
**INFO: Analyzing IO path groups for slack adjustment
Effort level <high> specified for reg2reg_tmp.21787 path_group
AAE_INFO: opIsDesignInPostRouteState() is 0
AAE_DB initialization (MEM=1564.27 CPU=0:00:00.0 REAL=0:00:00.0)
#####
# Design Stage: PreRoute
# Design Name: da2_mealy
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=1567.27)
Total number of fetched objects 14
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
End delay calculation. (MEM=1716.09 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1716.09 CPU=0:00:00.0
REAL=0:00:00.0)
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Input Pin Transition as 0.1 ps.
Set Default Net Load as 0.5 pF.
**INFO: Pre-place timing setting for timing analysis already disabled
Deleted 0 physical inst (cell - / prefix -).
INFO: #ExclusiveGroups=0
INFO: There are no Exclusive Groups.
*** Starting "NanoPlace(TM) placement v#6 (mem=1690.4M)" ...
*** Build Buffered Sizing Timing Model
(cpu=0:00:00.9 mem=1698.4M) ***
*** Build Virtual Sizing Timing Model
(cpu=0:00:01.0 mem=1698.4M) ***
No user-set net weight.
Net fanout histogram:
2          : 10 (66.7%) nets
3          : 2 (13.3%) nets
4      -    14    : 3 (20.0%) nets
15     -    39    : 0 (0.0%) nets
40     -    79    : 0 (0.0%) nets
80     -   159    : 0 (0.0%) nets
160    -   319    : 0 (0.0%) nets
320    -   639    : 0 (0.0%) nets
640    -  1279    : 0 (0.0%) nets
1280   -  2559    : 0 (0.0%) nets
2560   -  5119    : 0 (0.0%) nets
5120+   : 0 (0.0%) nets
Options: timingDriven clkGateAware ignoreScan pinGuide congEffort=auto
gpeffort=medium
**WARN: (IMPSP-9042): Scan chains were not defined, -
place_global_ignore_scan option will be ignored.
Define the scan chains before using this option.
Type 'man IMPSP-9042' for more detail.
#std cell=9 (0 fixed + 9 movable) #buf cell=0 #inv cell=3 #block=0 (0
floating + 0 preplaced)
#ioInst=0 #net=15 #term=38 #term/net=2.53, #fixedIo=0, #floatIo=0,
#fixedPin=0, #floatPin=4
stdCell: 9 single + 0 double + 0 multi
Total standard cell length = 0.0970 (mm), area = 0.0005 (mm^2)
Average module density = 0.700.
Density for the design = 0.700.
= stdcell_area 147 sites (489 um^2) / alloc_area 210 sites (699
um^2).
Pin Density = 0.1810.
= total # of pins 38 / total area 210.
== lastAutoLevel = 4
Clock gating cells determined by native netlist tracing.
Iteration 1: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
             Est. stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
             cpu = 0:00:00.0 real = 0:00:00.0 mem = 1743.9M
Iteration 2: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
             Est. stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
             cpu = 0:00:00.0 real = 0:00:00.0 mem = 1743.9M
Iteration 3: Total net bbox = 5.285e-01 (3.00e-01 2.29e-01)
             Est. stn bbox = 5.305e-01 (3.01e-01 2.30e-01)
             cpu = 0:00:00.0 real = 0:00:00.0 mem = 1745.4M
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Active setup views:
worst
Iteration 4: Total net bbox = 1.419e+02 (7.59e+01 6.60e+01)
             Est. stn bbox = 1.431e+02 (7.66e+01 6.65e+01)
             cpu = 0:00:00.0 real = 0:00:00.0 mem = 1745.4M
Iteration 5: Total net bbox = 1.867e+02 (1.04e+02 8.26e+01)
             Est. stn bbox = 1.885e+02 (1.05e+02 8.33e+01)
             cpu = 0:00:00.0 real = 0:00:00.0 mem = 1745.4M
Iteration 6: Total net bbox = 2.281e+02 (1.31e+02 9.71e+01)
             Est. stn bbox = 2.326e+02 (1.34e+02 9.90e+01)
             cpu = 0:00:00.1 real = 0:00:01.0 mem = 1745.4M
*** cost = 2.281e+02 (1.31e+02 9.71e+01) (cpu for global=0:00:00.1)
real=0:00:01.0***
Info: 0 clock gating cells identified, 0 (on average) moved 0/1
Solver runtime cpu: 0:00:00.0 real: 0:00:00.0
Core Placement runtime cpu: 0:00:00.0 real: 0:00:01.0
**WARN: (IMPSP-9025): No scan chain specified/traced.
Type 'man IMPSP-9025' for more detail.
*** Starting refinePlace (0:00:53.0 mem=1737.4M) ***
Total net bbox length = 2.474e+02 (1.402e+02 1.072e+02) (ext = 3.796e+01)
Move report: Detail placement moves 9 insts, mean move: 1.12 um, max
move: 2.84 um
     Max move on inst (g301_2398): (24.75, 15.39) --> (25.08, 12.88)
     Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 1761.4MB
Summary Report:
Instances move: 9 (out of 9 movable)
Instances flipped: 0
Mean displacement: 1.12 um
Max displacement: 2.84 um (Instance: g301_2398) (24.75, 15.3945) ->
(25.08, 12.88)
Length: 6 sites, height: 1 rows, site name: tsm3site, cell type:
NOR3BX1
Total net bbox length = 2.287e+02 (1.204e+02 1.084e+02) (ext = 2.689e+01)
Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 1761.4MB
*** Finished refinePlace (0:00:53.1 mem=1761.4M) ***
*** End of Placement (cpu=0:00:01.2, real=0:00:02.0, mem=1761.4M) ***
default core: bins with density > 0.750 = 0.00 % ( 0 / 1 )
Density distribution unevenness ratio = 0.000%
*** Free Virtual Timing Model ... (mem=1761.4M)
Starting IO pin assignment...
The design is not routed. Using placement based method for pin
assignment.
Completed IO pin assignment.
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
**INFO: Analyzing IO path groups for slack adjustment
Effort level <high> specified for reg2reg_tmp.21787 path_group
AAE_INFO: opIsDesignInPostRouteState() is 0
#####
# Design Stage: PreRoute
# Design Name: da2_mealy
# Design Mode: 90nm
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
#####
Start delay calculation (fullDC) (1 T). (MEM=1742.62)
Total number of fetched objects 14
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1794.05 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1794.05 CPU=0:00:00.0
REAL=0:00:00.0)
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Info: Disable timing driven in postCTS congRepair.

Starting congRepair ...
[NR-eGR] Num Prerouted Nets = 0  Num Prerouted Wires = 0
[NR-eGR] Read 15 nets ( ignored 0 )
[NR-eGR] There are 1 clock nets ( 0 with NDR ).
[NR-eGR] Layer group 1: route 15 net(s) in layer range [2, 6]
[NR-eGR] Early Global Route overflow of layer group 1: 0.00% H + 0.00% V.
EstWL: 2.217600e+02um
[NR-eGR] Overflow after Early Global Route 0.00% H + 0.00% V
Early Global Route congestion estimation runtime: 0.00 seconds, mem =
1784.3M
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00,
normalized total congestion hotspot area = 0.00 (area is in unit of 4
std-cell row bins)
Skipped repairing congestion.
[NR-eGR]          Length (um)  Vias
[NR-eGR] -----
[NR-eGR]   Metall1  (1H)          0    34
[NR-eGR]   Metal2  (2V)         130    40
[NR-eGR]   Metal3  (3H)         116    0
[NR-eGR]   Metal4  (4V)          0    0
[NR-eGR]   Metal5  (5H)          0    0
[NR-eGR]   Metal6  (6V)          0    0
[NR-eGR] -----
[NR-eGR]           Total        245    74
[NR-eGR] -----
[NR-eGR] Total half perimeter of net bounding box: 232um
[NR-eGR] Total length: 245um, number of vias: 74
[NR-eGR] -----
[NR-eGR] Total eGR-routed clock nets wire length: 46um, number of vias: 9
[NR-eGR] -----
Early Global Route wiring runtime: 0.00 seconds, mem = 1722.3M
Tdgp not successfully initied but do clear! skip clearing
End of congRepair (cpu=0:00:00.0, real=0:00:00.0)
*** Finishing placeDesign default flow ***
***** Total cpu 0:0:2
***** Total real time 0:0:3
**placeDesign ... cpu = 0: 0: 2, real = 0: 0: 3, mem = 1722.3M **
Tdgp not successfully initied but do clear! skip clearing
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPDC-1629      2 The default delay limit was set to %d.
T...
WARNING IMPSP-9025      1 No scan chain specified/traced.
WARNING IMPSP-9042      1 Scan chains were not defined, -
place_glo...
*** Message Summary: 4 warning(s), 0 error(s)

*** placeDesign #1 [finish] : cpu/real = 0:00:02.2/0:00:03.2 (0.7),
totSession cpu/real = 0:00:53.3/0:07:51.1 (0.1), mem = 1722.3M
innovus 1>
innovus 1> source ccopt.spec
Extracting original clock gating for clk...
    clock_tree clk contains 3 sinks and 0 clock gates.
Extracting original clock gating for clk done.
The skew group clk/cont was created. It contains 3 sinks and 1 sources.
Checking clock tree convergence...
Checking clock tree convergence done.
innovus 2> ccopt_design -cts
#% Begin ccopt_design (date=11/14 15:37:56, mem=1623.2M)
*** ccopt_design #1 [begin] : totSession cpu/real = 0:00:56.6/0:08:36.3
(0.1), mem = 1722.6M
Runtime...
**INFO: User's settings:
setNanoRouteMode -droutePostRouteSpreadWire           1
setNanoRouteMode -extractThirdPartyCompatible        false
setNanoRouteMode -timingEngine                      {}
setExtractRCMode -engine                           preRoute
setDelayCalMode -engine                          aae
setDelayCalMode -ignoreNetLoad                   false
setPlaceMode -place_design_floorplan_mode       false
setPlaceMode -place_detail_check_route         false
setPlaceMode -place_detail_preserve_routing     true
setPlaceMode -place_detail_remove_affected_routing false
setPlaceMode -place_detail_swap_eeq_cells       false
setPlaceMode -place_global_clock_gate_aware     true
setPlaceMode -place_global_cong_effort          auto
setPlaceMode -place_global_ignore_scan         true
setPlaceMode -place_global_ignore_spare        false
setPlaceMode -place_global_module_aware_spare   false
setPlaceMode -place_global_place_io_pins        true
setPlaceMode -place_global_reorder_scan        true
setPlaceMode -powerDriven                      false
setPlaceMode -timingDriven                     true
setRouteMode -earlyGlobalHonorMsvRouteConstraint false
setRouteMode -earlyGlobalRoutePartitionPinGuide  true

(ccopt_design): CTS Engine: auto. Used Spec: pre-existing CCOPT spec.
Placement constraints of type 'region' or 'fence' will not be downgraded
to 'guide' because the property change_fences_to_guides has been set to
false.
CCOpt::Phase::Initialization...
Check Prerequisites...
Leaving CCOpt scope - CheckPlace...
Begin checking placement ... (start mem=1722.6M, init mem=1722.6M)
*info: Placed = 9
*info: Unplaced = 0
Placement Density:70.00%(489/699)
Placement Density (including fixed std cells):70.00%(489/699)
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Finished checkPlace (total: cpu=0:00:00.0, real=0:00:00.0; vio checks:  
cpu=0:00:00.0, real=0:00:00.0; mem=1722.6M)  
Leaving CCOpt scope - CheckPlace done. (took cpu=0:00:00.0  
real=0:00:00.0)  
Innovus will update I/O latencies  
Found 0 ideal nets, 0 pins with transition annotations, 0 instances with  
delay annotations, 0 nets with delay annotations, refer to logv for  
details.  
  
Check Prerequisites done. (took cpu=0:00:00.0 real=0:00:00.0)  
CCOpt::Phase::Initialization done. (took cpu=0:00:00.0 real=0:00:00.0)  
Executing ccopt post-processing.  
Synthesizing clock trees with CCOpt...  
*** CTS #1 [begin] (ccopt_design #1) : totSession cpu/real =  
0:00:56.6/0:08:36.3 (0.1), mem = 1722.6M  
CCOpt::Phase::PreparingToBalance...  
Leaving CCOpt scope - Initializing power interface...  
Leaving CCOpt scope - Initializing power interface done. (took  
cpu=0:00:00.0 real=0:00:00.0)  
Found 0 advancing pin insertion delay (0.000% of 3 clock tree sinks)  
Found 0 delaying pin insertion delay (0.000% of 3 clock tree sinks)  
Leaving CCOpt scope - optDesignGlobalRouteStep...  
Updating RC grid for preRoute extraction ...  
Initializing multi-corner capacitance tables ...  
Initializing multi-corner resistance tables ...  
[NR-eGR] Started Early Global Route kernel ( Curr Mem: 1722.63 MB )  
[NR-eGR] Num Prerouted Nets = 0 Num Prerouted Wires = 0  
[NR-eGR] Read 15 nets ( ignored 0 )  
[NR-eGR] There are 1 clock nets ( 0 with NDR ).  
[NR-eGR] Layer group 1: route 15 net(s) in layer range [2, 6]  
[NR-eGR] Early Global Route overflow of layer group 1: 0.00% H + 0.00% V.  
EstWL: 2.217600e+02um  
[NR-eGR] Overflow after Early Global Route 0.00% H + 0.00% V  
[NR-eGR] Length (um) Vias  
[NR-eGR] -----  
[NR-eGR] Metal1 (1H) 0 34  
[NR-eGR] Metal2 (2V) 130 40  
[NR-eGR] Metal3 (3H) 116 0  
[NR-eGR] Metal4 (4V) 0 0  
[NR-eGR] Metal5 (5H) 0 0  
[NR-eGR] Metal6 (6V) 0 0  
[NR-eGR] -----  
[NR-eGR] Total 245 74  
[NR-eGR] -----  
-----  
[NR-eGR] Total half perimeter of net bounding box: 232um  
[NR-eGR] Total length: 245um, number of vias: 74  
[NR-eGR] -----  
-----  
[NR-eGR] Total eGR-routed clock nets wire length: 46um, number of vias: 9  
[NR-eGR] -----  
-----  
[NR-eGR] Finished Early Global Route kernel ( CPU: 0.01 sec, Real: 0.01  
sec, Curr Mem: 1722.63 MB )  
Leaving CCOpt scope - optDesignGlobalRouteStep done. (took cpu=0:00:00.0  
real=0:00:00.0)  
Legalization setup...  
Using cell based legalization.  
Initializing placement interface...  
Use check_library -place or consult logv if problems occur.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Leaving CCOpt scope - Initializing placement interface...
Leaving CCOpt scope - Initializing placement interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
Initializing placement interface done.
Leaving CCOpt scope - Cleaning up placement interface...
Leaving CCOpt scope - Cleaning up placement interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
Leaving CCOpt scope - Initializing placement interface...
Leaving CCOpt scope - Initializing placement interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
Legalization setup done. (took cpu=0:00:00.0 real=0:00:00.0)
Validating CTS configuration...
Checking module port directions...
Checking module port directions done. (took cpu=0:00:00.0 real=0:00:00.0)
Non-default CCOpt properties:
    Public non-default CCOpt properties:
        route_type is set for at least one object
        target_max_trans_sdc is set for at least one object
    No private non-default CCOpt properties
Route type trimming info:
    No route type modifications were made.
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
**WARN: (IMPCCOPT-1182): The clock_gating_cells property has no usable
full-cycle clock gates for power domain auto-default. Gating limited for
clock tree clk. You may be able to solve this problem by specifying a
list of lib_cells to use with the clock_gating_cells property.
Library trimming inverters in power domain auto-default and half-corner
maxd:setup.late removed 4 of 8 cells
Original list had 8 cells:
CLKINVX20 CLKINVX16 CLKINVX12 CLKINVX8 CLKINVX4 CLKINVX3 CLKINVX2
CLKINVX1
New trimmed list has 4 cells:
CLKINVX8 CLKINVX4 CLKINVX3 CLKINVX1
Clock tree balancer configuration for clock_tree clk:
Non-default CCOpt properties:
    Public non-default CCOpt properties:
        route_type (leaf): default_route_type_leaf (default: default)
        route_type (top): default_route_type_nonleaf (default: default)
        route_type (trunk): default_route_type_nonleaf (default: default)
    No private non-default CCOpt properties
For power domain auto-default:
    Buffers: {CLKBUFX20 CLKBUFX16 CLKBUFX12 CLKBUFX8 CLKBUFX4 CLKBUFX3
CLKBUFX1}
    Inverters: {CLKINVX8 CLKINVX4 CLKINVX3 CLKINVX1}
    Unblocked area available for placement of any clock cells in
power_domain auto-default: 698.544um^2
Top Routing info:
    Route-type name: default_route_type_nonleaf; Top/bottom preferred layer
name: Metal4/Metal3;
    Unshielded; Mask Constraint: 0; Source: route_type.
Trunk Routing info:
    Route-type name: default_route_type_nonleaf; Top/bottom preferred layer
name: Metal4/Metal3;
    Unshielded; Preferred extra space: 1; Mask Constraint: 0; Source:
route_type.
Leaf Routing info:
    Route-type name: default_route_type_leaf; Top/bottom preferred layer
name: Metal4/Metal3;
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Unshielded; Preferred extra space: 1; Mask Constraint: 0; Source:  
route_type.  
For timing_corner maxd:setup, late and power domain auto-default:  
    Slew time target (leaf): 0.100ns (Too low; min: 0.215ns)  
    Slew time target (trunk): 0.100ns (Too low; min: 0.215ns)  
    Slew time target (top): 0.100ns (Note: no nets are considered top  
nets in this clock tree)  
    Buffer unit delay: 0.125ns  
    Buffer max distance: 629.524um  
Fastest wire driving cells and distances:  
    Buffer : {lib_cell:CLKBUFX20,  
fastest_considered_half_corner=maxd:setup.late,  
optimalDrivingDistance=629.524um, saturatedSlew=0.094ns, speed=3893.160um  
per ns, cellArea=126.816um^2 per 1000um}  
    Inverter : {lib_cell:CLKINVX8,  
fastest_considered_half_corner=maxd:setup.late,  
optimalDrivingDistance=149.615um, saturatedSlew=0.094ns, speed=2028.678um  
per ns, cellArea=133.398um^2 per 1000um}  
  
**ERROR: (IMPCCOPT-1013): The target_max_trans time is too low for at  
least one clock tree, net type and timing corner. Search the log for the  
string 'Too low;' to find the minimum acceptable targets for each  
combination. CTS will now terminate.  
Type 'man IMPCCOPT-1013' for more detail.
```

Logic Sizing Table:

Cell	Instance count	Source	Eligible library cells
(empty table)			

```
Clock tree balancer configuration for skew_group clk/cont:  
Sources: pin clk  
Total number of sinks: 3  
Delay constrained sinks: 3  
Constrains: default  
Non-leaf sinks: 0  
Ignore pins: 0  
Timing corner maxd:setup.late:  
    Skew target: 0.000ns  
Primary reporting skew groups are:  
skew_group clk/cont with 3 clock sinks  
  
Clock DAG stats initial state:  
    cell counts : b=0, i=0, icg=0, dcg=0, l=0, total=0  
    sink counts : regular=3, enable_latch=0, load_capacitance=0,  
antenna=0, node_sink=0, total=3  
    misc counts : r=1, pp=0  
    cell areas : b=0.000um^2, i=0.000um^2, icg=0.000um^2,  
dcg=0.000um^2, l=0.000um^2, total=0.000um^2  
    hp wire lengths : top=0.000um, trunk=0.000um, leaf=0.000um,  
total=0.000um  
No ideal or dont_touch nets found in the clock tree  
No dont_touch hnets found in the clock tree  
No dont_touch hpins found in the clock network.  
Checking for illegal sizes of clock logic instances...
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
Checking for illegal sizes of clock logic instances done. (took
cpu=0:00:00.0 real=0:00:00.0)
Validating CTS configuration done. (took cpu=0:00:00.1 real=0:00:00.1)

CCOpt configuration status: cannot run ccopt_design.
Check the log for details of problem(s) found:

-----
Design configuration problems
-----
One or more clock trees have configuration problems
-----

Clock tree configuration problems:

-----
Clock tree      Problem
-----
clk            The maximum transition target is too low
-----


CCOpt::Phase::PreparingToBalance done. (took cpu=0:00:00.2
real=0:00:00.2)
Runtime done. (took cpu=0:00:00.2 real=0:00:00.2)
Runtime Summary
-----
Clock Runtime: (88%) Core CTS          0.15 (Init 0.15, Construction
0.00, Implementation 0.00, eGRPC 0.00, PostConditioning 0.00, Other 0.00)
Clock Runtime: (0%) CTS services       0.00 (RefinePlace 0.00,
EarlyGlobalClock 0.00, NanoRoute 0.00, ExtractRC 0.00, TimingAnalysis
0.00)
Clock Runtime: (11%) Other CTS         0.02 (Init 0.02, CongRepair/EGR-
DP 0.00, TimingUpdate 0.00, Other 0.00)
Clock Runtime: (100%) Total           0.17

Leaving CCOpt scope - Cleaning up placement interface...
Leaving CCOpt scope - Cleaning up placement interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
**ERROR: 3
*** CTS #1 [finish] (ccopt_design #1) : cpu/real = 0:00:00.2/0:00:00.2
(1.0), totSession cpu/real = 0:00:56.7/0:08:36.5 (0.1), mem = 1727.4M
**ERROR: (IMPCCOPT-2196): Cannot run ccopt_design because the command
prerequisites were not met. Review the previous error messages for more
details about the failure.

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count  Summary
ERROR    IMPCCOPT-2196   1  Cannot run ccopt_design because the
comm...
WARNING  IMPCCOPT-1182   1  The clock_gating_cells property has no
u...
ERROR    IMPCCOPT-1013   1  The target_max_trans time is too low
for...
*** Message Summary: 1 warning(s), 2 error(s)

*** ccopt_design #1 [finish] : cpu/real = 0:00:00.2/0:00:00.2 (0.9),
totSession cpu/real = 0:00:56.7/0:08:36.5 (0.1), mem = 1727.4M
#% End ccopt_design (date=11/14 15:37:56, total cpu=0:00:00.2,
real=0:00:00.0, peak res=1638.2M, current mem=1638.2M)
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
innovus 3> saveDesign DBS/cts.encl
% Begin save design ... (date=11/14 15:38:25, mem=1641.6M)
% Begin Save ccopt configuration ... (date=11/14 15:38:25, mem=1641.6M)
% End Save ccopt configuration ... (date=11/14 15:38:25, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1641.6M, current mem=1641.5M)
% Begin Save netlist data ... (date=11/14 15:38:25, mem=1641.5M)
Writing Binary DB to DBS/cts.encl.dat/da2_mealy.v.bin in single-threaded
mode...
% End Save netlist data ... (date=11/14 15:38:25, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1641.6M, current mem=1641.6M)
Saving symbol-table file ...
Saving congestion map file DBS/cts.encl.dat/da2_mealy.route.congmap.gz
...
% Begin Save AAE data ... (date=11/14 15:38:25, mem=1641.6M)
Saving AAE Data ...
% End Save AAE data ... (date=11/14 15:38:25, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1641.6M, current mem=1641.6M)
Saving preference file DBS/cts.encl.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=11/14 15:38:25, mem=1643.5M)
Saving floorplan file ...
% End Save floorplan data ... (date=11/14 15:38:25, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1643.6M, current mem=1643.6M)
Saving Drc markers ...
... 11 markers are saved ...
... 0 geometry drc markers are saved ...
... 0 antenna drc markers are saved ...
% Begin Save placement data ... (date=11/14 15:38:25, mem=1643.6M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=11/14 15:38:25, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1643.9M, current mem=1643.9M)
% Begin Save routing data ... (date=11/14 15:38:25, mem=1643.9M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1730.2M) ***
% End Save routing data ... (date=11/14 15:38:25, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1644.0M, current mem=1644.0M)
Saving property file DBS/cts.encl.dat/da2_mealy.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1733.2M) ***
% Begin Save power constraints data ... (date=11/14 15:38:25,
mem=1645.2M)
% End Save power constraints data ... (date=11/14 15:38:25, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1645.2M, current mem=1645.2M)
Generated self-contained design cts.encl.dat
#%% End save design ... (date=11/14 15:38:25, total cpu=0:00:00.2,
real=0:00:00.0, peak res=1674.1M, current mem=1648.5M)
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 4> #WARNING (NRIF-91) Option setNanoRouteMode -
routeTopRoutingLayer is obsolete. It will continue to work for the
current release. To ensure compatibility with future releases, use option
setDesignMode -topRoutingLayer instead.
#WARNING (NRIF-90) Option setNanoRouteMode -routeBottomRoutingLayer is
obsolete. It will continue to work for the current release. To ensure
compatibility with future releases, use option setDesignMode -
bottomRoutingLayer instead.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory =
1650.02 (MB), peak = 1674.07 (MB)
AAE_INFO: Pre Route call back at the beginning of routeDesign
***INFO: setDesignMode -flowEffort standard
***INFO: setDesignMode -powerEffort none
#WARNING (NRIG-96) Selected single pass global detail route "-globalDetail". Clock eco and post optimizations will not be run. See "man NRIG-96" for more details.
#WARNING (NRIG-144) Cannot combine -viaOpt with -globalDetail option. The -viaOpt will be ignored.
**INFO: User settings:
setNanoRouteMode -drouteEndIteration          1
setNanoRouteMode -droutePostRouteSpreadWire    1
setNanoRouteMode -extractThirdPartyCompatible   false
setNanoRouteMode -drouteBottomRoutingLayer      1
setNanoRouteMode -drouteTopRoutingLayer         6
setNanoRouteMode -drouteWithSiDriven           false
setNanoRouteMode -drouteWithTimingDriven        false
setNanoRouteMode -timingEngine                 {}
setExtractRCMode -engine                      preRoute
setDelayCalMode -engine                      aae
setDelayCalMode -ignoreNetLoad                false

***INFO: multi-cut via swapping will not be performed after routing.
***INFO: All auto set options tuned by routeDesign will be restored to their original settings on command completion.
Begin checking placement ... (start mem=1769.9M, init mem=1769.9M)
*info: Placed = 9
*info: Unplaced = 0
Placement Density:70.00%(489/699)
Placement Density (including fixed std cells):70.00%(489/699)
Finished checkPlace (total: cpu=0:00:00.0, real=0:00:00.0; vio checks:
cpu=0:00:00.0, real=0:00:00.0; mem=1769.9M)

changeUseClockNetStatus Option : -noFixedNetWires
*** Changed status on (0) nets in Clock.
*** End changeUseClockNetStatus (cpu=0:00:00.0, real=0:00:00.0,
mem=1769.9M) ***

globalDetailRoute

#Start globalDetailRoute on Thu Nov 14 15:38:42 2024
#
#WARNING (NRIG-1303) The congestion map does not match the GCELL grid.
Clearing the map.
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
#num needed restored net=0
#need_extraction net=0 (total=17)
#WARNING (NRDB-2005) SPECIAL_NET vdd has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.
#WARNING (NRDB-2005) SPECIAL_NET vss has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Total number of trivial nets (e.g. < 2 pins) = 2 (skipped).
#Total number of routable nets = 15.
#Total number of nets in the design = 17.
#15 routable nets do not have any wires.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
#15 nets will be global routed.
#Start routing data preparation on Thu Nov 14 15:38:42 2024
#
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.980.
#Voltage range [0.000 - 1.980] has 15 nets.
#Voltage range [1.620 - 1.980] has 1 net.
#Voltage range [0.000 - 0.000] has 1 net.
#Build and mark too close pins for the same net.
#Rebuild pin access data for design.
#Initial pin access analysis.
#Detail pin access analysis.
# Metal1      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.48500
# Metal2      V  Track-Pitch = 0.66000   Line-2-Via Pitch = 0.56000
# Metal3      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.56000
# Metal4      V  Track-Pitch = 0.66000   Line-2-Via Pitch = 0.56000
# Metal5      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.56000
# Metal6      V  Track-Pitch = 0.99000   Line-2-Via Pitch = 0.95000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1657.68 (MB),
peak = 1691.11 (MB)
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.56000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1660.48 (MB),
peak = 1691.11 (MB)
#
#Finished routing data preparation on Thu Nov 14 15:38:42 2024
#
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 8.88 (MB)
#Total memory = 1660.48 (MB)
#Peak memory = 1691.11 (MB)
#
#
#Start global routing on Thu Nov 14 15:38:42 2024
#
#
#Start global routing initialization on Thu Nov 14 15:38:42 2024
#
#Number of eco nets is 0
#
#Start global routing data preparation on Thu Nov 14 15:38:42 2024
#
#Start routing resource analysis on Thu Nov 14 15:38:42 2024
#
#Routing resource analysis is done on Thu Nov 14 15:38:42 2024
#
# Resource Analysis:
#
#          Routing #Avail      #Track      #Total      %Gcell
#  Layer     Direction  Track    Blocked    Gcell    Blocked
#  -----  -----
#  Metal1      H        15        40         16      18.75%
#  Metal2      V        48         2         16      0.00%
#  Metal3      H        55         0         16      0.00%
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
# Metal4      V      50      0      16      0.00%
# Metal5      H      47      8      16      0.00%
# Metal6      V     11     22      16      0.00%
#
# -----
# Total          226    26.32%      96      3.12%
#
#
#
#
#Global routing data preparation is done on Thu Nov 14 15:38:42 2024
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1660.48 (MB),
peak = 1691.11 (MB)
#
#
#Global routing initialization is done on Thu Nov 14 15:38:42 2024
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1660.48 (MB),
peak = 1691.11 (MB)
#
#start global routing iteration 1...
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1662.25 (MB),
peak = 1691.11 (MB)
#
#start global routing iteration 2...
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1662.25 (MB),
peak = 1691.11 (MB)
#
#
#Total number of trivial nets (e.g. < 2 pins) = 2 (skipped).
#Total number of routable nets = 15.
#Total number of nets in the design = 17.
#
#15 routable nets have routed wires.
#
#Routed nets constraints summary:
#-----
#      Rules   Unconstrained
#-----
#      Default      15
#-----
#      Total      15
#-----
#
#Routing constraints summary of the whole design:
#-----
#      Rules   Unconstrained
#-----
#      Default      15
#-----
#      Total      15
#-----
#
#
# Congestion Analysis: (blocked Gcells are excluded)
#
#          OverCon
#          #Gcell  %Gcell
#      Layer      (1)  OverCon
# -----
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```

#  Metall1      0(0.00%)  (0.00%)
#  Metal2      0(0.00%)  (0.00%)
#  Metal3      0(0.00%)  (0.00%)
#  Metal4      0(0.00%)  (0.00%)
#  Metal5      0(0.00%)  (0.00%)
#  Metal6      0(0.00%)  (0.00%)
#
# -----
#      Total      0(0.00%)  (0.00%)
#
# The worst congested Gcell overcon (routing demand over resource in
# number of tracks) = 1
# Overflow after GR: 0.00% H + 0.00% V
#
#Hotspot report including placement blocked areas
[hotspot] +-----+-----+-----+
-----+
[hotspot] |      layer      | max hotspot | total hotspot |
hotspot bbox           |
[hotspot] +-----+-----+-----+
-----+
[hotspot] |    Metall1(H)   |       0.00 |       0.00 |
(none)                   |
[hotspot] |    Metal2(V)   |       0.00 |       0.00 |
(none)                   |
[hotspot] |    Metal3(H)   |       0.00 |       0.00 |
(none)                   |
[hotspot] |    Metal4(V)   |       0.00 |       0.00 |
(none)                   |
[hotspot] |    Metal5(H)   |       0.00 |       0.00 |
(none)                   |
[hotspot] |    Metal6(V)   |       0.00 |       0.00 |
(none)                   |
[hotspot] +-----+-----+-----+
-----+
[hotspot] |      worst      |       0.00 |       0.00 |
|
[hotspot] +-----+-----+-----+
-----+
[hotspot] |    all layers   |       0.00 |       0.00 |
|
[hotspot] +-----+-----+-----+
-----+
Local HotSpot Analysis (blockage included) (3d): normalized congestion
max/total hotspot area = 0.00/0.00 (area is in unit of 4 std-cell row
bins)
#Complete Global Routing.
#Total wire length = 228 um.
#Total half perimeter of net bounding box = 285 um.
#Total wire length on LAYER Metall1 = 0 um.
#Total wire length on LAYER Metal2 = 104 um.
#Total wire length on LAYER Metal3 = 125 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 51
#Up-Via Summary (total 51):
#
#-----
# Metall1      31
# Metal2      20

```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
#-----
#          51
#
#Max overcon = 0 track.
#Total overcon = 0.00%.
#Worst layer Gcell overcon rate = 0.00%.
#
#Global routing statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.89 (MB)
#Total memory = 1662.38 (MB)
#Peak memory = 1691.11 (MB)
#
#Finished global routing on Thu Nov 14 15:38:42 2024
#
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1662.38 (MB),
peak = 1691.11 (MB)
#Start Track Assignment.
#Done with 13 horizontal wires in 1 hboxes and 12 vertical wires in 1
hboxes.
#Done with 2 horizontal wires in 1 hboxes and 0 vertical wires in 1
hboxes.
#Done with 1 horizontal wires in 1 hboxes and 1 vertical wires in 1
hboxes.
#
#Track assignment summary:
# layer      (wire length)    (overlap)    (long ovlp)    (with obs/pg/clk)
#-----
# Metall      0.00    0.00%    0.00%    0.00%
# Metal2     98.02    0.00%    0.00%    0.00%
# Metal3     121.25    0.00%    0.00%    0.00%
# Metal4      0.00    0.00%    0.00%    0.00%
# Metal5      0.00    0.00%    0.00%    0.00%
# Metal6      0.00    0.00%    0.00%    0.00%
#-----
# All        219.27    0.00%    0.00%    0.00%
#Complete Track Assignment.
#Total wire length = 213 um.
#Total half perimeter of net bounding box = 285 um.
#Total wire length on LAYER Metall = 0 um.
#Total wire length on LAYER Metal2 = 95 um.
#Total wire length on LAYER Metal3 = 118 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 51
#Up-Via Summary (total 51):
#
#-----
# Metall      31
# Metal2     20
#-----
#          51
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1662.50 (MB),
peak = 1691.11 (MB)
#
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
#Routing data preparation, pin analysis, global routing and track
assignment statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 10.89 (MB)
#Total memory = 1662.50 (MB)
#Peak memory = 1691.11 (MB)
#
#Start Detail Routing..
#start initial detail routing ...
#   number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1663.93 (MB),
peak = 1691.11 (MB)
#Complete Detail Routing.
#Total wire length = 239 um.
#Total half perimeter of net bounding box = 285 um.
#Total wire length on LAYER Metal1 = 33 um.
#Total wire length on LAYER Metal2 = 122 um.
#Total wire length on LAYER Metal3 = 84 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 51
#Up-Via Summary (total 51):
#
#-----
# Metall      37
# Metal2     14
#-----
#                  51
#
#Total number of DRC violations = 0
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.43 (MB)
#Total memory = 1663.93 (MB)
#Peak memory = 1691.11 (MB)
#
#Start Post Route wire spreading..
#
#Start DRC checking..
#   number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1664.29 (MB),
peak = 1691.11 (MB)
#CELL_VIEW da2_mealy,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#
#Start data preparation for wire spreading...
#
#Data preparation is done on Thu Nov 14 15:38:42 2024
#
#
#Start Post Route Wire Spread.
#Done with 3 horizontal wires in 1 hboxes and 0 vertical wires in 1
hboxes.
#Complete Post Route Wire Spread.
#
#Total wire length = 241 um.
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
#Total half perimeter of net bounding box = 285 um.
#Total wire length on LAYER Metal1 = 33 um.
#Total wire length on LAYER Metal2 = 122 um.
#Total wire length on LAYER Metal3 = 86 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 51
#Up-Via Summary (total 51):
#
#-----
# Metall      37
# Metal2      14
#-----
#                  51
#
#
#Start DRC checking..
#   number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1664.05 (MB),
peak = 1691.11 (MB)
#CELL_VIEW da2_mealy,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#   number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1664.05 (MB),
peak = 1691.11 (MB)
#CELL_VIEW da2_mealy,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#Post Route wire spread is done.
#Total wire length = 241 um.
#Total half perimeter of net bounding box = 285 um.
#Total wire length on LAYER Metal1 = 33 um.
#Total wire length on LAYER Metal2 = 122 um.
#Total wire length on LAYER Metal3 = 86 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total number of vias = 51
#Up-Via Summary (total 51):
#
#-----
# Metall      37
# Metal2      14
#-----
#                  51
#
#
#detailRoute Statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.55 (MB)
#Total memory = 1664.05 (MB)
#Peak memory = 1691.11 (MB)
#   no debugging net set
#
#globalDetailRoute statistics:
#Cpu time = 00:00:00
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
#Elapsed time = 00:00:00
#Increased memory = 22.14 (MB)
#Total memory = 1672.44 (MB)
#Peak memory = 1691.11 (MB)
#Number of warnings = 3
#Total number of warnings = 7
#Number of fails = 0
#Total number of fails = 0
#Complete globalDetailRoute on Thu Nov 14 15:38:42 2024
#
#Default setup view is reset to worst.

detailRoute

#Start detailRoute on Thu Nov 14 15:38:42 2024
#
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
#num needed restored net=0
#need_extraction net=0 (total=17)
#WARNING (NRDB-2005) SPECIAL_NET vdd has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#WARNING (NRDB-2005) SPECIAL_NET vss has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Start routing data preparation on Thu Nov 14 15:38:42 2024
#
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.980.
#Voltage range [0.000 - 1.980] has 15 nets.
#Voltage range [1.620 - 1.980] has 1 net.
#Voltage range [0.000 - 0.000] has 1 net.
#Build and mark too close pins for the same net.
#Initial pin access analysis.
#Detail pin access analysis.
# Metal1      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.48500
# Metal2      V  Track-Pitch = 0.66000   Line-2-Via Pitch = 0.56000
# Metal3      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.56000
# Metal4      V  Track-Pitch = 0.66000   Line-2-Via Pitch = 0.56000
# Metal5      H  Track-Pitch = 0.56000   Line-2-Via Pitch = 0.56000
# Metal6      V  Track-Pitch = 0.99000   Line-2-Via Pitch = 0.95000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1670.39 (MB),
peak = 1691.11 (MB)
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.56000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1672.96 (MB),
peak = 1691.11 (MB)
#
#Start Post Route wire spreading..
#
#Start data preparation for wire spreading...
#
#Data preparation is done on Thu Nov 14 15:38:42 2024
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
#  
#  
#Start Post Route Wire Spread.  
#Done with 1 horizontal wires in 1 hboxes and 0 vertical wires in 1  
hboxes.  
#Complete Post Route Wire Spread.  
#  
#Total wire length = 241 um.  
#Total half perimeter of net bounding box = 285 um.  
#Total wire length on LAYER Metal1 = 33 um.  
#Total wire length on LAYER Metal2 = 122 um.  
#Total wire length on LAYER Metal3 = 86 um.  
#Total wire length on LAYER Metal4 = 0 um.  
#Total wire length on LAYER Metal5 = 0 um.  
#Total wire length on LAYER Metal6 = 0 um.  
#Total number of vias = 51  
#Up-Via Summary (total 51):  
#  
#-----  
# Metal1      37  
# Metal2      14  
#-----  
#          51  
#  
#    number of violations = 0  
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1673.05 (MB),  
peak = 1691.11 (MB)  
#CELL_VIEW da2_mealy,init has no DRC violation.  
#Total number of DRC violations = 0  
#Total number of process antenna violations = 0  
#Total number of net violated process antenna rule = 0  
#Post Route wire spread is done.  
#Total wire length = 241 um.  
#Total half perimeter of net bounding box = 285 um.  
#Total wire length on LAYER Metal1 = 33 um.  
#Total wire length on LAYER Metal2 = 122 um.  
#Total wire length on LAYER Metal3 = 86 um.  
#Total wire length on LAYER Metal4 = 0 um.  
#Total wire length on LAYER Metal5 = 0 um.  
#Total wire length on LAYER Metal6 = 0 um.  
#Total number of vias = 51  
#Up-Via Summary (total 51):  
#  
#-----  
# Metal1      37  
# Metal2      14  
#-----  
#          51  
#  
#    no debugging net set  
#  
#detailRoute statistics:  
#Cpu time = 00:00:00  
#Elapsed time = 00:00:00  
#Increased memory = 1.59 (MB)  
#Total memory = 1669.90 (MB)  
#Peak memory = 1691.11 (MB)  
#Number of warnings = 2  
#Total number of warnings = 9  
#Number of fails = 0
```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```
#Total number of fails = 0
#Complete detailRoute on Thu Nov 14 15:38:42 2024
#
#Default setup view is reset to worst.
AAE_INFO: Post Route call back at the end of routeDesign
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory =
1669.90 (MB), peak = 1691.11 (MB)
*** Message Summary: 0 warning(s), 0 error(s)

innovus 4> **WARN: (IMPSP-5217): addFiller command is running on a
postRoute database. It is recommended to be followed by ecoRoute -target
command to make the DRC clean.
Type 'man IMPSP-5217' for more detail.
*INFO: Adding fillers to top-module.
*INFO: Added 0 filler inst (cell FILL64 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILL32 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILL16 / prefix FILLER).
*INFO: Added 4 filler insts (cell FILL8 / prefix FILLER).
*INFO: Added 3 filler insts (cell FILL4 / prefix FILLER).
*INFO: Added 6 filler insts (cell FILL2 / prefix FILLER).
*INFO: Added 7 filler insts (cell FILL1 / prefix FILLER).
*INFO: Total 20 filler insts added - prefix FILLER (CPU: 0:00:00.0).
For 20 new insts, innovus 4> Performing RC Extraction ...
Extraction called for design 'da2_mealy' of instances=29 and nets=17
using extraction engine 'preRoute'.
**WARN: (IMPEXT-3530): The process node is not set. Use the command
setDesignMode -process <process node> prior to extraction for maximum
accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design da2_mealy.
RC Extraction called in multi-corner(1) mode.
RCMode: PreRoute
    RC Corner Indexes          0
    Capacitance Scaling Factor : 1.00000
    Resistance Scaling Factor : 1.00000
    Clock Cap. Scaling Factor : 1.00000
    Clock Res. Scaling Factor : 1.00000
    Shrink Factor             : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0
MEM: 1784.180M)
innovus 4> Writing Netlist "da2_mealy.v" ...
innovus 4> #% Begin save design ... (date=11/14 15:39:46, mem=1673.1M)
% Begin Save ccopt configuration ... (date=11/14 15:39:46, mem=1673.1M)
% End Save ccopt configuration ... (date=11/14 15:39:46, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1673.1M, current mem=1673.1M)
% Begin Save netlist data ... (date=11/14 15:39:46, mem=1673.1M)
Writing Binary DB to da2_mealy.enc.dat/da2_mealy.v.bin in single-threaded
mode...
% End Save netlist data ... (date=11/14 15:39:46, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1673.3M, current mem=1673.3M)
Saving symbol-table file ...
Saving congestion map file da2_mealy.enc.dat/da2_mealy.route.congmap.gz
...
% Begin Save AAE data ... (date=11/14 15:39:46, mem=1673.3M)
Saving AAE Data ...
```

DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

```

AAE DB initialization (MEM=1789.72 CPU=0:00:00.0 REAL=0:00:00.0)
% End Save AAE data ... (date=11/14 15:39:46, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1673.9M, current mem=1673.9M)
Saving preference file da2_mealy.enc.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=11/14 15:39:46, mem=1674.5M)
Saving floorplan file ...
% End Save floorplan data ... (date=11/14 15:39:46, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1674.5M, current mem=1674.5M)
Saving Drc markers ...
... 11 markers are saved ...
... 0 geometry drc markers are saved ...
... 0 antenna drc markers are saved ...
% Begin Save placement data ... (date=11/14 15:39:46, mem=1674.5M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=11/14 15:39:46, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1674.5M, current mem=1674.5M)
% Begin Save routing data ... (date=11/14 15:39:46, mem=1674.5M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1790.2M) ***
% End Save routing data ... (date=11/14 15:39:46, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1674.5M, current mem=1674.5M)
Saving property file da2_mealy.enc.dat/da2_mealy.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1793.2M) ***
#Saving pin access data to file da2_mealy.enc.dat/da2_mealy.apa ...
#
% Begin Save power constraints data ... (date=11/14 15:39:46,
mem=1674.5M)
% End Save power constraints data ... (date=11/14 15:39:46, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1674.5M, current mem=1674.5M)
Generated self-contained design da2_mealy.enc.dat
#% End save design ... (date=11/14 15:39:47, total cpu=0:00:00.2,
real=0:00:01.0, peak res=1705.1M, current mem=1675.2M)
*** Message Summary: 0 warning(s), 0 error(s)

Parse flat map file...
Writing GDSII file ...
***** db unit per micron = 2000 *****
***** output gds2 file unit per micron = 2000 *****
***** unit scaling factor = 1 *****

Output for instance
Output for bump
Output for physical terminals
Output for logical terminals
Output for regular nets
Output for special nets and metal fills
Output for via structure generation total number 5
Statistics for GDS generated (version 3)
-----
Stream Out Layer Mapping Information:
GDS Layer Number          GDS Layer Name
-----
121                         COMP
122                         DIEAREA
58                          Via34
57                          Via34
50                          Metal3
107                         Metal6

```

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

46	Metal3
45	Metal3
44	Metal3
63	Via34
43	Metal3
62	Via34
41	Via23
22	Metal2
40	Via23
37	Via23
59	Via34
36	Via23
31	Metal2
88	Metal5
29	Metal2
86	Metal5
105	Via56
9	Metal1
66	Metal4
42	Via23
23	Metal2
99	Via56
19	Via12
8	Metal1
65	Metal4
84	Via45
30	Metal2
87	Metal5
7	Metal1
6	Metal1
64	Metal4
83	Via45
39	Via23
16	Via12
52	Metal3
109	Metal6
2	Metal1
21	Via12
78	Via45
10	Metal1
67	Metal4
51	Metal3
108	Metal6
28	Metal2
1	Metal1
20	Via12
38	Via23
15	Via12
5	Metal1
81	Via45
17	Via12
49	Metal3
18	Via12
47	Metal3
24	Metal2
100	Via56
48	Metal3
106	Metal6
25	Metal2
3	Metal1

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

79	Via45
26	Metal2
102	Via56
4	Metal1
27	Metal2
85	Metal5
104	Via56
60	Via34
61	Via34
68	Metal4
69	Metal4
70	Metal4
71	Metal4
72	Metal4
73	Metal4
80	Via45
82	Via45
90	Metal5
91	Metal5
92	Metal5
93	Metal5
94	Metal5
101	Via56
103	Via56
111	Metal6
112	Metal6
113	Metal6
114	Metal6
115	Metal6
110	Metal6
89	Metal5
117	Metal6
56	Metal3
55	Metal3
54	Metal3
53	Metal3
32	Metal2
98	Metal5
96	Metal5
76	Metal4
33	Metal2
75	Metal4
97	Metal5
74	Metal4
119	Metal6
12	Metal1
77	Metal4
118	Metal6
11	Metal1
34	Metal2
116	Metal6
35	Metal2
13	Metal1
14	Metal1
95	Metal5

Stream Out Information Processed for GDS version 3:  
Units: 2000 DBU

## DA2: Logic synthesis & Physical Design of a 1001 Overlapping Mealy FSM

Object	Count
<hr/>	
Instances	29
Ports/Pins	4
metal layer Metal2	4
Nets	63
metal layer Metal1	17
metal layer Metal2	31
metal layer Metal3	15
Via Instances	51
Special Nets	49
metal layer Metal1	17
metal layer Metal2	1
metal layer Metal5	4
metal layer Metal6	27
Via Instances	1
Metal Fills	0
Via Instances	0
Metal FillOPCs	0
Via Instances	0
Metal FillDRCs	0
Via Instances	0
Text	21
metal layer Metal1	2
metal layer Metal2	14
metal layer Metal3	3
metal layer Metal6	2
Blockages	0
Custom Text	0
Custom Box	0
Trim Metal	0
#####Streamout is finished!	
innovus 4>	

**Inference:** A total of 10 leaf instance count is present in the gate level netlist with total area of 24.4, total power of 3.6 uW.

**Result:** Hence a 1001 Overlapping Mealy FSM is verified before the synthesis and after the synthesis and it was synthesized and the gate level netlist with timing,area and power report was generate successfully. Also the physical design of the FSM was built successfully.

