

Lab-6: Logic synthesis and Physical Desgin of a 2bit Multiplier

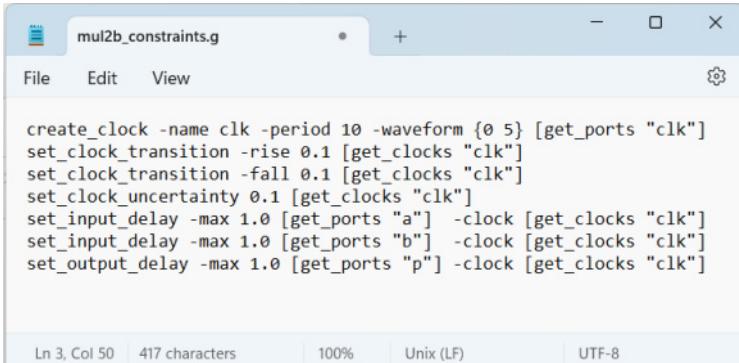
Aim: To synthesize a 2 bit multiplier and to get the gate level netlist with timing, area, and power reports. And also to do pre synthesis verification and post synthesis verification using NCLaunch.

EDA Tools Used: Cadence NC Launch, Genus (Logic synthesis tool) and Innovus

Description: An essential combinational circuit which is a 2-bit multiplier is explained as a circuit that helps in the process of binary multiplication of two 2 bit numbers that will give a 4 bit output. This is achieved by first creating the partial products from the input bits and then summing them to arrive at the final output. In this case, the circuit is usually constructed using AND gates to produce the partial products and adders i.e. half-adders and full-adders, to interconnect the partial products. A 2-bit multiplier is easy to look at, however, it contains some useful concepts of digital designs such as combination of Boolean logic, circuit design, and minimization. It forms the basis of more advanced designing in arithmetic logic units boasted of their multipliers, prospective digital signal processors and many more computation devices. In hardware synthesis, 2-bit multiplier design seeks to take the logic and representation it at the gate level which is the one that can be found on the silicon chip. The emphasis here is on how the structure is synthesized to come up with an improved gate level netlist where the timing figures are managed, the area cut down, and the power consumption improved. There is a process, which is verification, which is very important. There is a simulation pre synthesis where the high level design is checked for errors and after synthesis or post synthesis simulation, the logic is tested in terms of how it works and its speed.

Procedure:

1. Write the verilog file for the design and do the functional verification in NC Launch.
2. Copy the fast.lib and slow.lib files into the folder where (.v) files are located.
3. Create a Synopsys design constraint file (.SDC file) by entering the design constraints required for the synthesis.

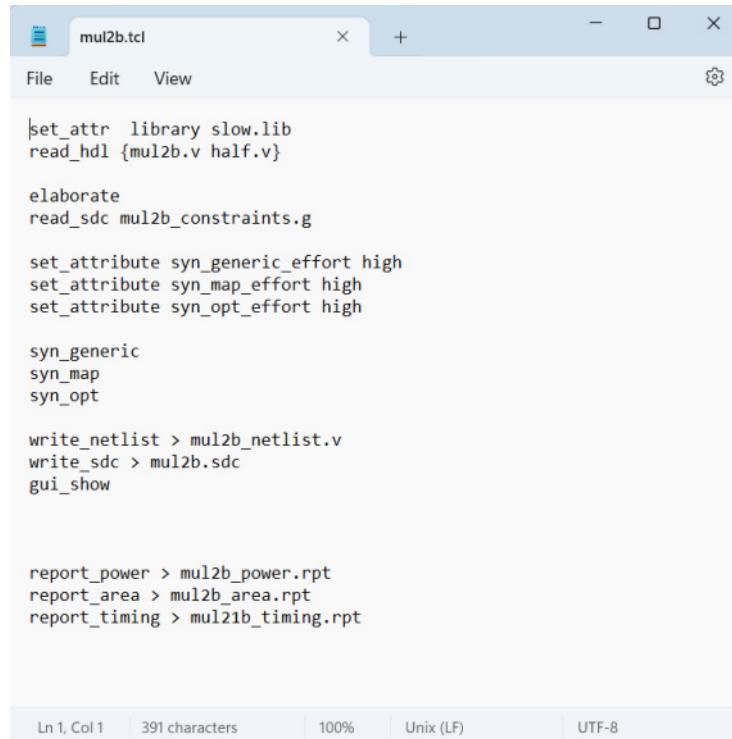


```
mul2b_constraints.sdc
File Edit View
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.1 [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "p"] -clock [get_clocks "clk"]

Ln 3, Col 50 417 characters 100% Unix (LF) UTF-8
```

Lab-6: Logic synthesis of an 2bit Multiplier

4. Create a (.tcl) file containing all the commands for performing the logic synthesis.
Synthesis effort can be medium or high.



```
mul2b.tcl

File Edit View

set_attr library slow.lib
read_hdl {mul2b.v half.v}

elaborate
read_sdc mul2b_constraints.sdc

set_attribute syn_generic_effort high
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

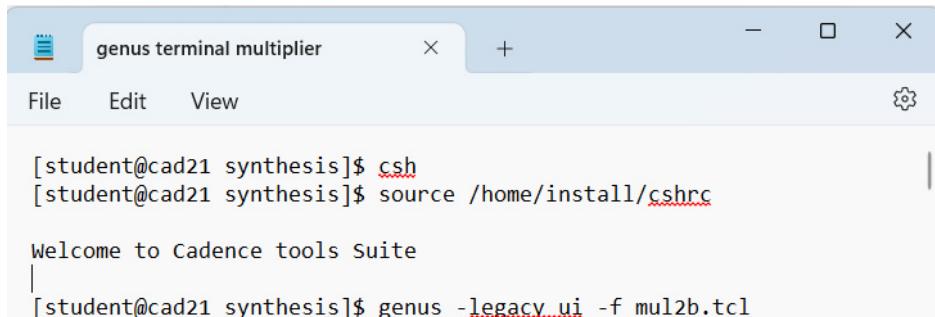
syn_generic
syn_map
syn_opt

write_netlist > mul2b_netlist.v
write_sdc > mul2b.sdc
gui_show

report_power > mul2b_power.rpt
report_area > mul2b_area.rpt
report_timing > mul2b_timing.rpt

Ln 1, Col 1 391 characters 100% Unix (LF) UTF-8
```

5. Invoke the C shell and launch the Genus tool by entering the below commands.



```
genus terminal multiplier

File Edit View

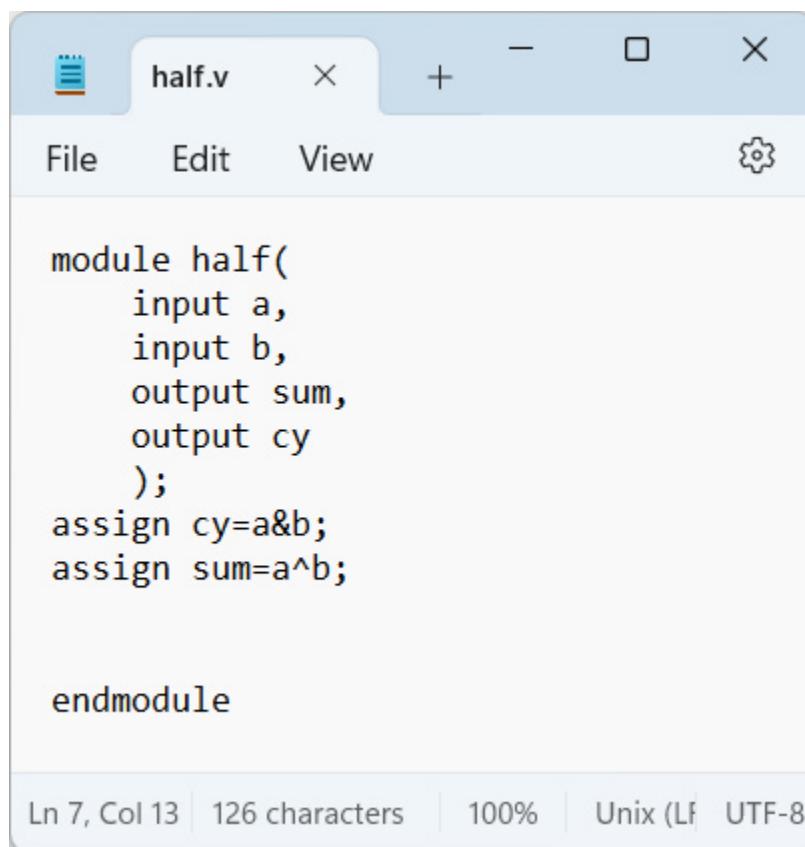
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite
|
[student@cad21 synthesis]$ genus -legacy_ui -f mul2b.tcl
```

6. Execute the commands in the (.tcl file) by entering **source mul2b.tcl** command in the command line window.
7. Check for the area, timing and power reports generated in the respective adding CPU folder. Also check the gate level netlist generated in the Genus synthesis solution window.
8. Now do the post synthesis verification with the netlist verilog file with the same testbench in nc launch.
9. After the post synthesis verification do the physical design using innovus.

Pre synthesis Verilog Programs:

//Verilog Program of half adder



The screenshot shows a Verilog code editor window titled "half.v". The code defines a module named "half" with two inputs ("a" and "b") and two outputs ("sum" and "cy"). The logic is implemented using a bitwise AND operation for the carry output and a bitwise XOR operation for the sum output. The code is as follows:

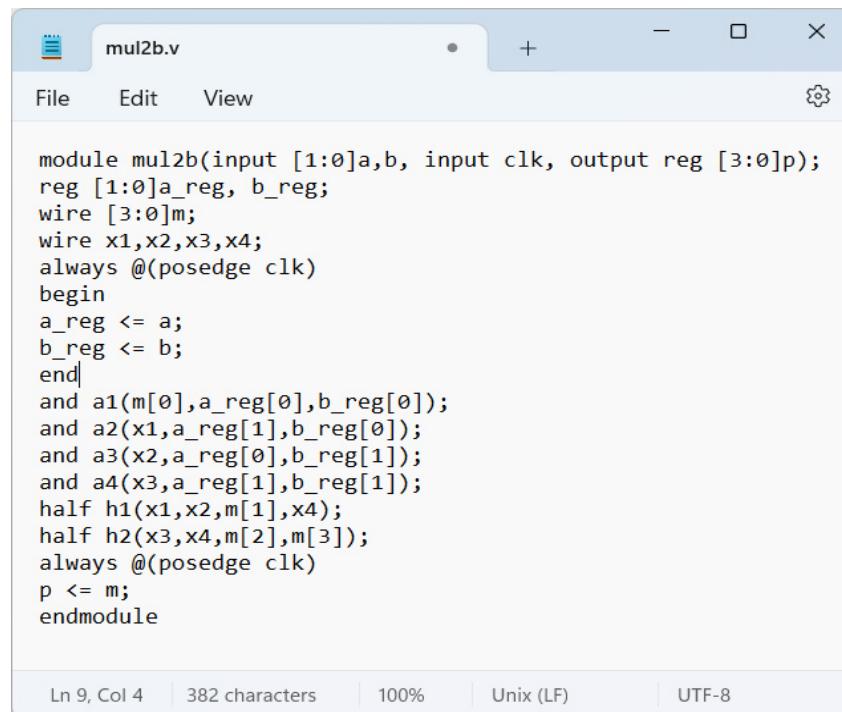
```
module half(
    input a,
    input b,
    output sum,
    output cy
);
    assign cy=a&b;
    assign sum=a^b;

endmodule
```

At the bottom of the editor, status information is displayed: "Ln 7, Col 13 | 126 characters | 100% | Unix (LF) | UTF-8".

Lab-6: Logic synthesis & Physical design of an 2bit multiplier

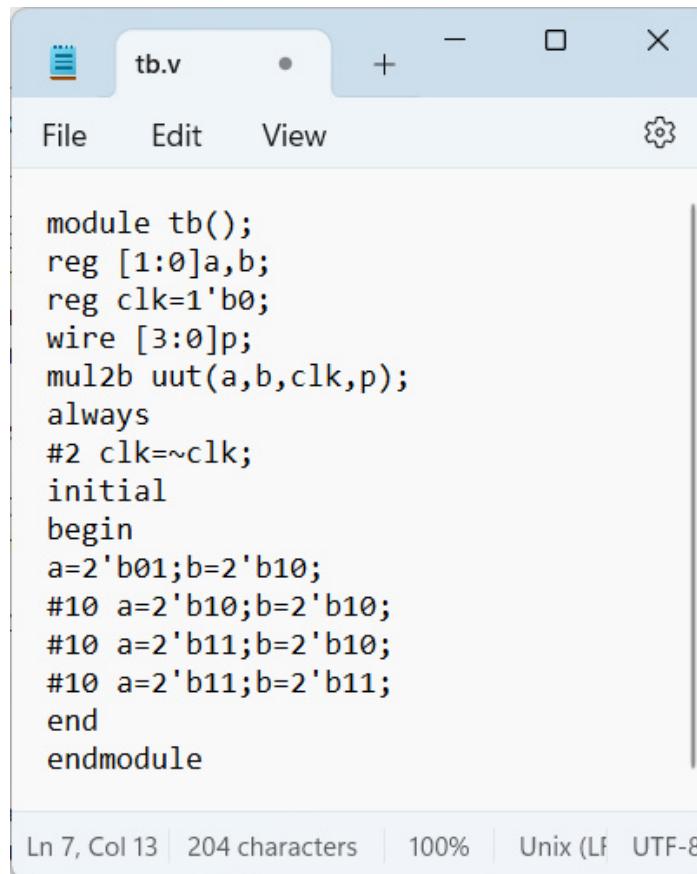
//Verilog Program of the multiplier



```
mul2b.v
File Edit View
module mul2b(input [1:0]a,b, input clk, output reg [3:0]p);
reg [1:0]a_reg, b_reg;
wire [3:0]m;
wire x1,x2,x3,x4;
always @(posedge clk)
begin
a_reg <= a;
b_reg <= b;
end
and a1(m[0],a_reg[0],b_reg[0]);
and a2(x1,a_reg[1],b_reg[0]);
and a3(x2,a_reg[0],b_reg[1]);
and a4(x3,a_reg[1],b_reg[1]);
half h1(x1,x2,m[1],x4);
half h2(x3,x4,m[2],m[3]);
always @(posedge clk)
p <= m;
endmodule

Ln 9, Col 4 | 382 characters | 100% | Unix (LF) | UTF-8
```

//Verilog Program of the test bench

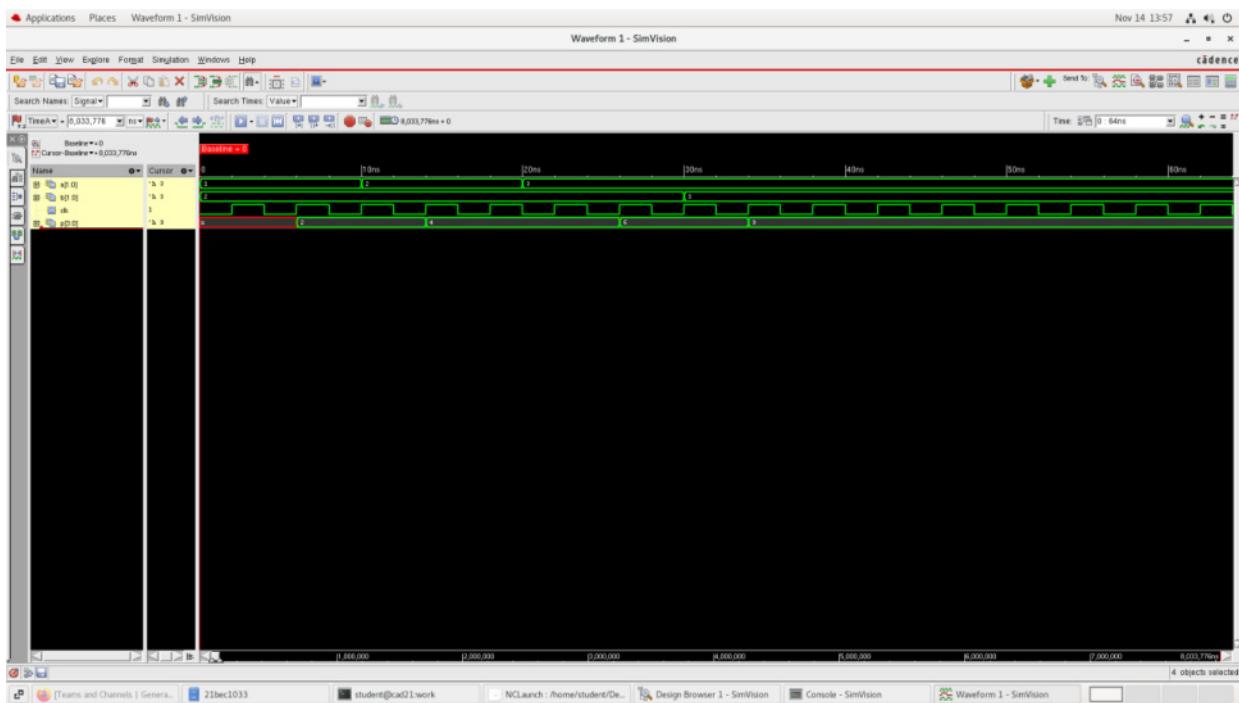


```
tb.v
File Edit View
module tb();
reg [1:0]a,b;
reg clk=1'b0;
wire [3:0]p;
mul2b uut(a,b,clk,p);
always
#2 clk=~clk;
initial
begin
a=2'b01;b=2'b10;
#10 a=2'b10;b=2'b10;
#10 a=2'b11;b=2'b10;
#10 a=2'b11;b=2'b11;
end
endmodule

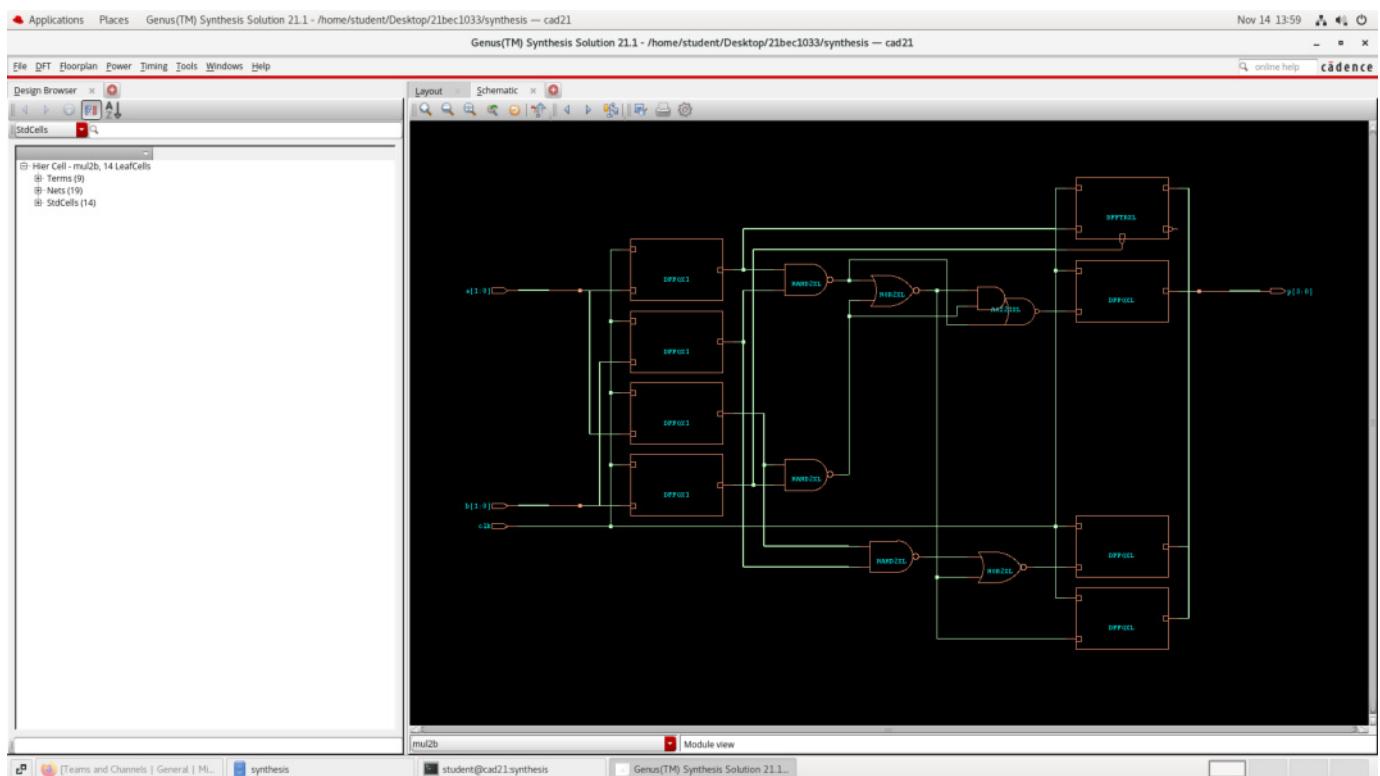
Ln 7, Col 13 | 204 characters | 100% | Unix (LF) | UTF-8
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

Pre Synthesis verification:



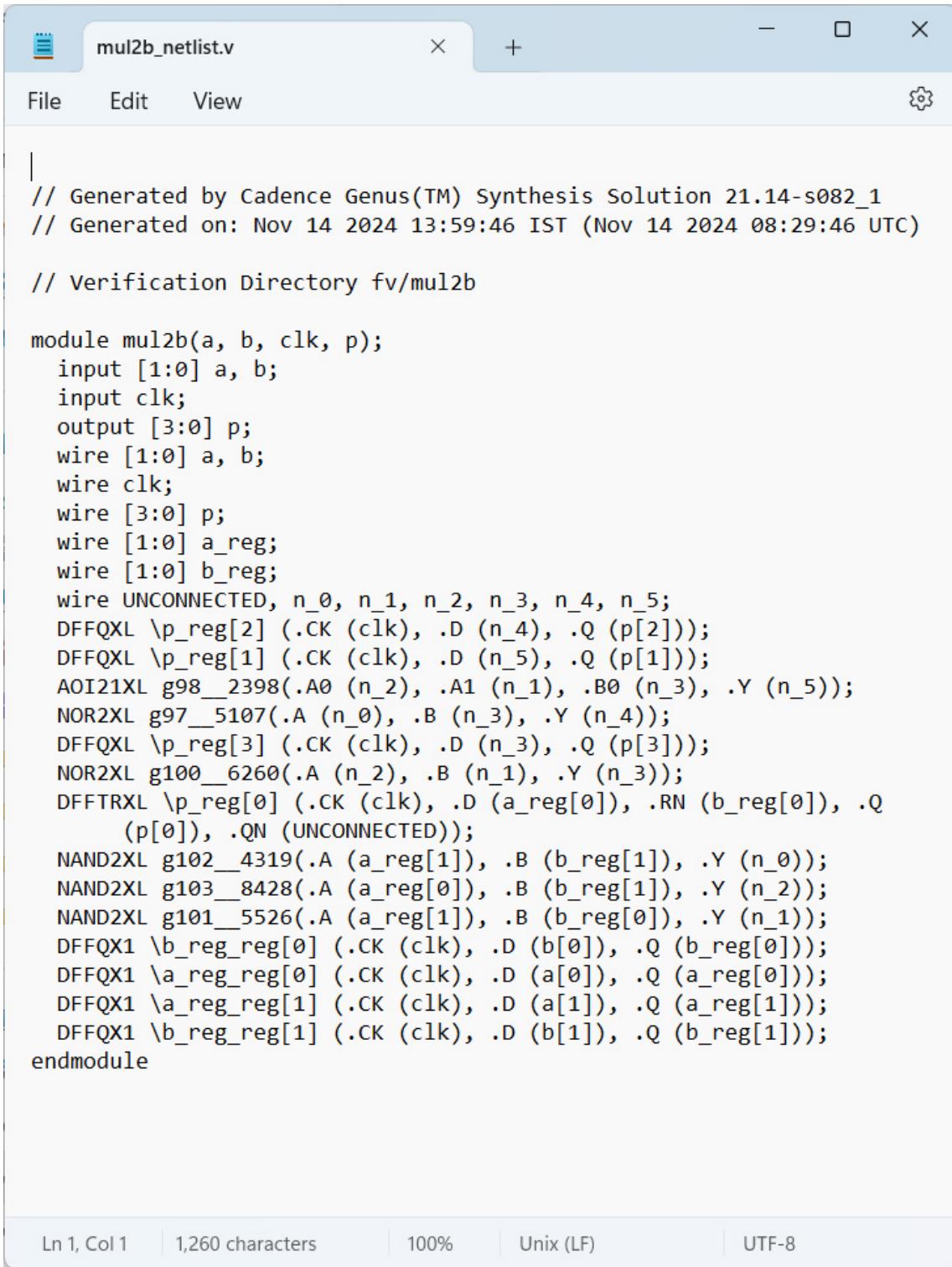
Gate level Netlist:



Observations:

Synthesis effort: High

a) Multiplier Netlist :



The screenshot shows a Cadence Genus IDE window titled "mul2b_netlist.v". The code is a Verilog netlist for a 2-bit multiplier. It includes comments indicating it was generated by Cadence Genus Synthesis Solution 21.14-s082_1 on Nov 14 2024 at 13:59:46 IST. The module "mul2b" takes inputs a[1:0], b[1:0], and clk, and produces output p[3:0]. The implementation uses various logic components like DFFQXL, AOI21XL, NOR2XL, DFFQXL, NOR2XL, DFFTRXL, NAND2XL, and DFFQX1 to perform the multiplication.

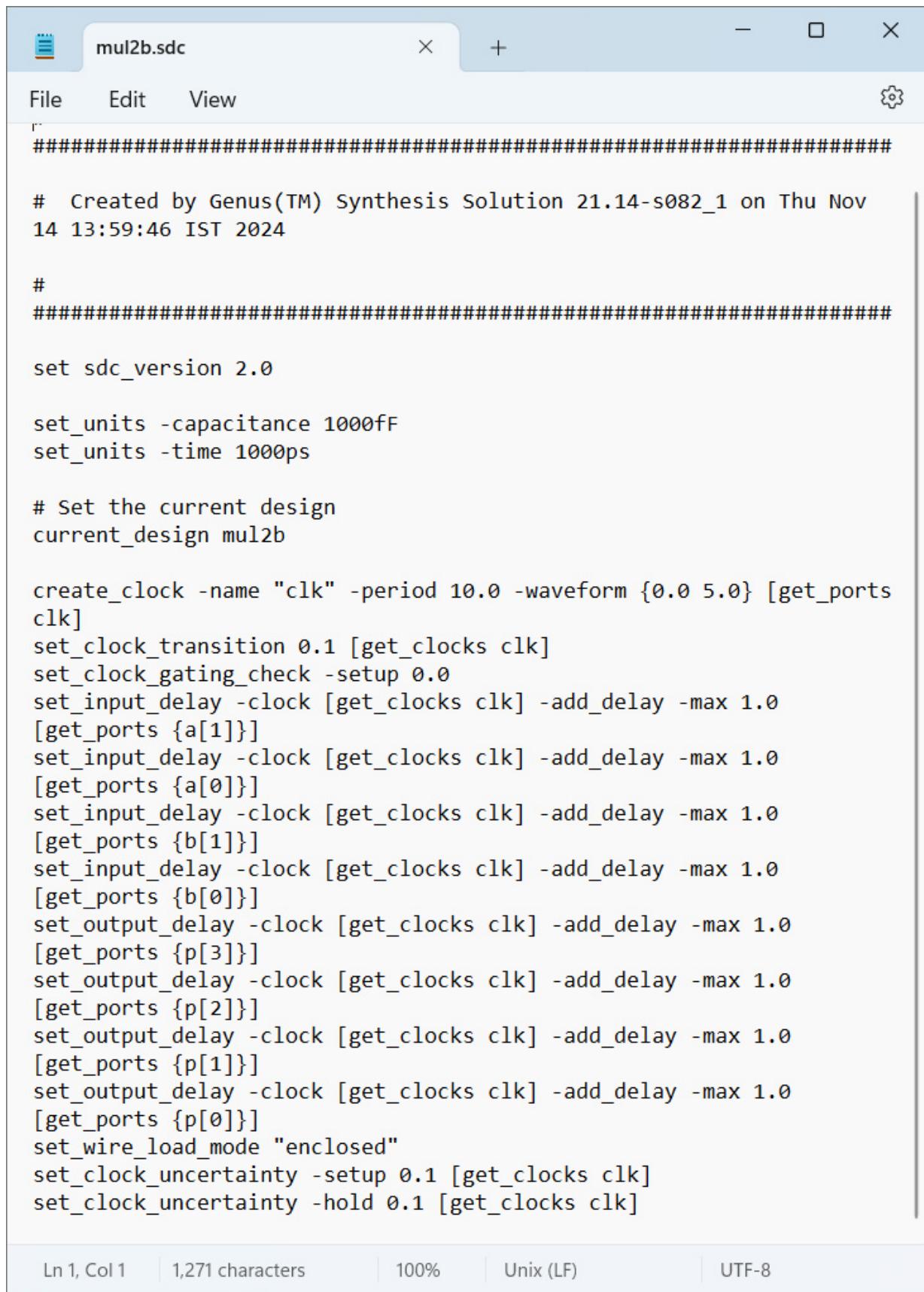
```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Nov 14 2024 13:59:46 IST (Nov 14 2024 08:29:46 UTC)

// Verification Directory fv/mul2b

module mul2b(a, b, clk, p);
    input [1:0] a, b;
    input clk;
    output [3:0] p;
    wire [1:0] a, b;
    wire clk;
    wire [3:0] p;
    wire [1:0] a_reg;
    wire [1:0] b_reg;
    wire UNCONNECTED, n_0, n_1, n_2, n_3, n_4, n_5;
    DFFQXL \p_reg[2] (.CK (clk), .D (n_4), .Q (p[2]));
    DFFQXL \p_reg[1] (.CK (clk), .D (n_5), .Q (p[1]));
    AOI21XL g98_2398(.A0 (n_2), .A1 (n_1), .B0 (n_3), .Y (n_5));
    NOR2XL g97_5107(.A (n_0), .B (n_3), .Y (n_4));
    DFFQXL \p_reg[3] (.CK (clk), .D (n_3), .Q (p[3]));
    NOR2XL g100_6260(.A (n_2), .B (n_1), .Y (n_3));
    DFFTRXL \p_reg[0] (.CK (clk), .D (a_reg[0]), .RN (b_reg[0]), .Q
        (p[0]), .QN (UNCONNECTED));
    NAND2XL g102_4319(.A (a_reg[1]), .B (b_reg[1]), .Y (n_0));
    NAND2XL g103_8428(.A (a_reg[0]), .B (b_reg[1]), .Y (n_2));
    NAND2XL g101_5526(.A (a_reg[1]), .B (b_reg[0]), .Y (n_1));
    DFFQX1 \b_reg_reg[0] (.CK (clk), .D (b[0]), .Q (b_reg[0]));
    DFFQX1 \a_reg_reg[0] (.CK (clk), .D (a[0]), .Q (a_reg[0]));
    DFFQX1 \a_reg_reg[1] (.CK (clk), .D (a[1]), .Q (a_reg[1]));
    DFFQX1 \b_reg_reg[1] (.CK (clk), .D (b[1]), .Q (b_reg[1]));
endmodule
```

Ln 1, Col 1 | 1,260 characters | 100% | Unix (LF) | UTF-8

b) Mul2b_Constraint_created file



The screenshot shows a text editor window titled "mul2b.sdc". The menu bar includes "File", "Edit", "View", and a settings gear icon. The main content area contains a script in SDC (System Design Constraints) language. The script starts with a header indicating it was created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Nov 14 13:59:46 IST 2024. It then sets the SDC version to 2.0 and specifies capacitance and time units. It defines a current design named "mul2b" and creates a clock named "clk" with a period of 10.0. The script then performs various timing constraints on ports "a[1]", "a[0]", "b[1]", "b[0]", and "p[3..0]" relative to the "clk" clock. Finally, it sets wire load mode to "enclosed" and specifies clock uncertainty setup and hold times.

```
mul2b.sdc
-----
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Nov
14 13:59:46 IST 2024

#
#####

set sdc_version 2.0

set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design mul2b

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports
clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0
[get_ports {a[1]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0
[get_ports {a[0]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0
[get_ports {b[1]}]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0
[get_ports {b[0]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0
[get_ports {p[3]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0
[get_ports {p[2]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0
[get_ports {p[1]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0
[get_ports {p[0]}]
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.1 [get_clocks clk]
set_clock_uncertainty -hold 0.1 [get_clocks clk]

Ln 1, Col 1 | 1,271 characters | 100% | Unix (LF) | UTF-8
```

Lab-5: Logic synthesis & Physical Design of an adding CPU

c) Mul2b_timing_created file

```
mul2b_timing.rpt x + File Edit View ⚙
=====
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Nov 14 2024 01:59:46 pm
Module: mul2b
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====

Pin Type Fanout Load Slew Delay Arrival
      (fF) (ps) (ps) (ps)
=====
(clock clk) launch
p_reg[0]/CK          100    +0    0 R
p_reg[0]/Q           1  0.0   30  +306  306 F
p[0]                 <<< interconnect
                     out port
                     +0    306 F
(mul2b_constraints.g_line_15_3_1) ext delay
                     +1000 1306 F
-----
(clock clk) capture
                     uncertainty
                     -100  9900 R
-----
Cost Group : 'clk' (path_group 'clk')
Timing slack : 8594ps
Start-point : p_reg[0]/CK
End-point   : p[0]

Ln 1, Col 1 1,674 characters | 100% | Unix (LF) | UTF-8
```

d) addingCPU_area_created file

```
mul2b_area.rpt x + File Edit View ⚙
=====
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Nov 14 2024 01:59:46 pm
Module: mul2b
Technology library: slow
Operating conditions: slow (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====

Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----
mul2b          14    151.380    0.000    151.380 <none> (D)
(D) = wireload is default in technology library

Ln 1, Col 1 704 characters | 100% | Unix (LF) | UTF-8
```

Lab-6: Logic synthesis & Physical design of an 2bit multiplier

e) mul2b_power_created file

The screenshot shows a software interface for viewing a power report. The title bar says "mul2b_power.rpt". The menu bar includes "File", "Edit", "View", and a settings gear icon. The main content area displays power consumption details:

```
Instance: /mul2b
Power Unit: W
PDB Frames: /stim#0/frame#0

Category      Leakage    Internal    Switching    Total    Row%
memory        0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
register     7.92494e-07  1.28993e-05  1.58760e-07  1.38505e-05  89.93%
latch         0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
logic          6.47855e-08  2.84746e-07  1.15830e-07  4.65362e-07  3.02%
bbox           0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
clock          0.00000e+00  0.00000e+00  1.08540e-06  1.08540e-06  7.05%
pad            0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%
pm             0.00000e+00  0.00000e+00  0.00000e+00  0.00000e+00  0.00%

Subtotal      8.57280e-07  1.31840e-05  1.35999e-06  1.54013e-05  100.00%
Percentage    5.57%       85.60%       8.83%       100.00%      100.00%
```

At the bottom, it shows "Ln 2, Col 14" and "1,199 characters" on the left, "100%" in the center, "Unix (LF)" and "UTF-8" on the right.

Post synthesis Verilog Programs:

//Verilog Program of half adder

The screenshot shows a software interface for writing Verilog code. The title bar has tabs for "tb.v" and "half.v", with "half.v" currently active. The menu bar includes "File", "Edit", "View", and a settings gear icon. The main content area contains the Verilog code for a half adder:

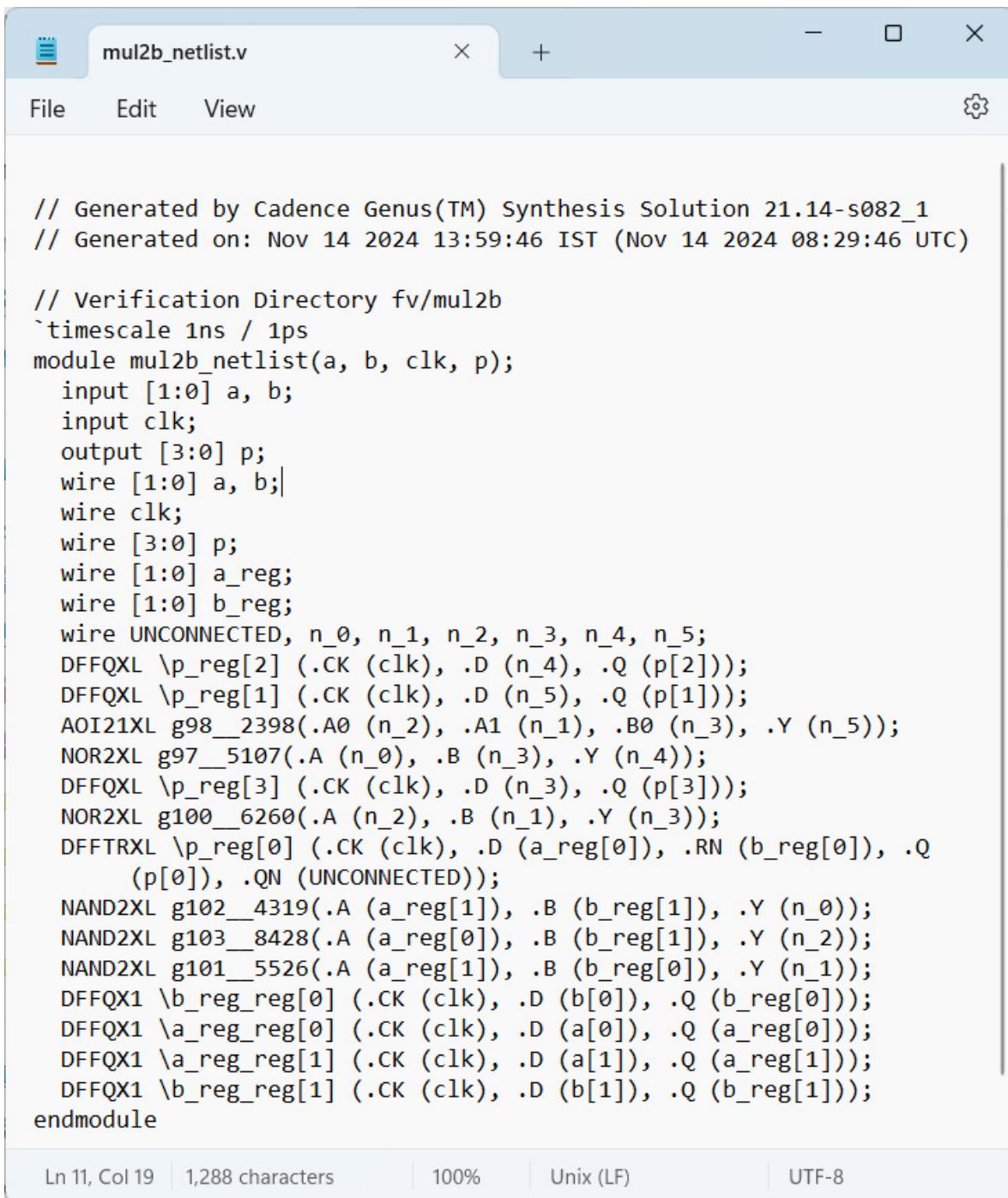
```
`timescale 1ns / 1ps

module half(
    input a,
    input b,
    output sum,
    output cy
);
    assign cy=a&b;
    assign sum=a^b;

endmodule
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

//Verilog Program of the multiplier netlist



The screenshot shows a Cadence Genus IDE window titled "mul2b_netlist.v". The code is a Verilog netlist for a 2-bit multiplier. It includes comments indicating it was generated by Cadence Genus Synthesis Solution 21.14-s082_1 on Nov 14 2024 at 13:59:46 IST. The code defines a module "mul2b_netlist" with inputs "a" [1:0], "clk", and "b"; output "p" [3:0]; and internal wires for registers "a_reg" and "b_reg", and various logic components like DFFQXL, AOI21XL, NOR2XL, and DFFTRXL.

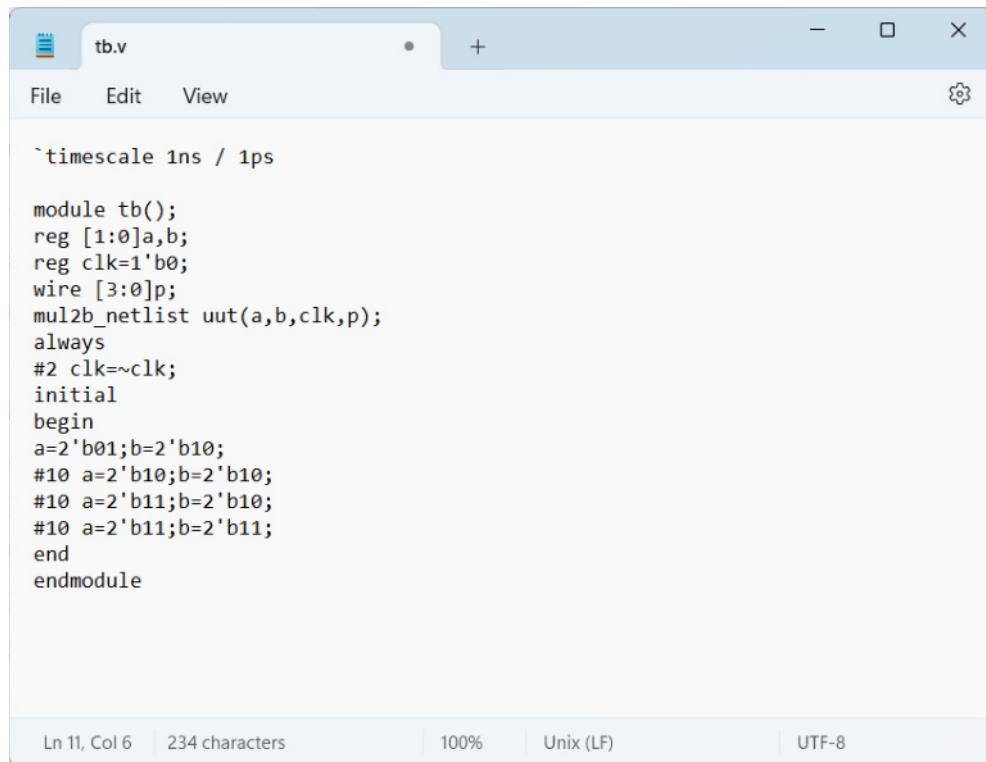
```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Nov 14 2024 13:59:46 IST (Nov 14 2024 08:29:46 UTC)

// Verification Directory fv/mul2b
`timescale 1ns / 1ps
module mul2b_netlist(a, b, clk, p);
    input [1:0] a, b;
    input clk;
    output [3:0] p;
    wire [1:0] a, b;
    wire clk;
    wire [3:0] p;
    wire [1:0] a_reg;
    wire [1:0] b_reg;
    wire UNCONNECTED, n_0, n_1, n_2, n_3, n_4, n_5;
    DFFQXL \p_reg[2] (.CK (clk), .D (n_4), .Q (p[2]));
    DFFQXL \p_reg[1] (.CK (clk), .D (n_5), .Q (p[1]));
    AOI21XL g98_2398(.A0 (n_2), .A1 (n_1), .B0 (n_3), .Y (n_5));
    NOR2XL g97_5107(.A (n_0), .B (n_3), .Y (n_4));
    DFFQXL \p_reg[3] (.CK (clk), .D (n_3), .Q (p[3]));
    NOR2XL g100_6260(.A (n_2), .B (n_1), .Y (n_3));
    DFFTRXL \p_reg[0] (.CK (clk), .D (a_reg[0]), .RN (b_reg[0]), .Q
        (p[0]), .QN (UNCONNECTED));
    NAND2XL g102_4319(.A (a_reg[1]), .B (b_reg[1]), .Y (n_0));
    NAND2XL g103_8428(.A (a_reg[0]), .B (b_reg[1]), .Y (n_2));
    NAND2XL g101_5526(.A (a_reg[1]), .B (b_reg[0]), .Y (n_1));
    DFFQX1 \b_reg_reg[0] (.CK (clk), .D (b[0]), .Q (b_reg[0]));
    DFFQX1 \a_reg_reg[0] (.CK (clk), .D (a[0]), .Q (a_reg[0]));
    DFFQX1 \a_reg_reg[1] (.CK (clk), .D (a[1]), .Q (a_reg[1]));
    DFFQX1 \b_reg_reg[1] (.CK (clk), .D (b[1]), .Q (b_reg[1]));
endmodule
```

Ln 11, Col 19 | 1,288 characters | 100% | Unix (LF) | UTF-8

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

//Verilog Program of the test bench



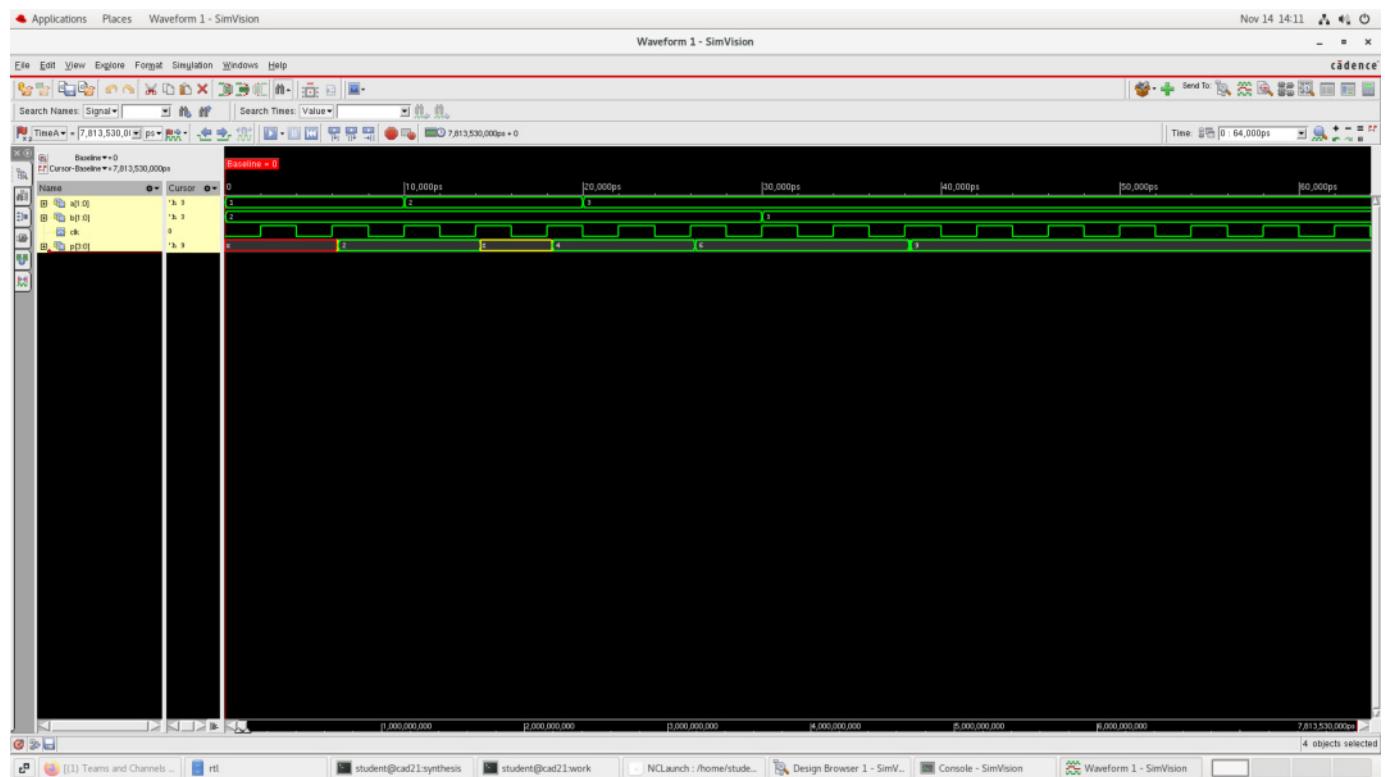
The screenshot shows a Verilog code editor window titled "tb.v". The code defines a test bench module "tb" with a clock input "clk" and two 2-bit inputs "a" and "b". It uses a "mul2b_netlist" component to perform the multiplication. The simulation script includes several stimulus cases: a=2'b01, b=2'b10; a=2'b10, b=2'b10; a=2'b11, b=2'b10; and a=2'b11, b=2'b11.

```
tb.v
`timescale 1ns / 1ps

module tb();
reg [1:0]a,b;
reg clk=1'b0;
wire [3:0]p;
mul2b_netlist uut(a,b,clk,p);
always
#2 clk=~clk;
initial
begin
a=2'b01;b=2'b10;
#10 a=2'b10;b=2'b10;
#10 a=2'b11;b=2'b10;
#10 a=2'b11;b=2'b11;
end
endmodule
```

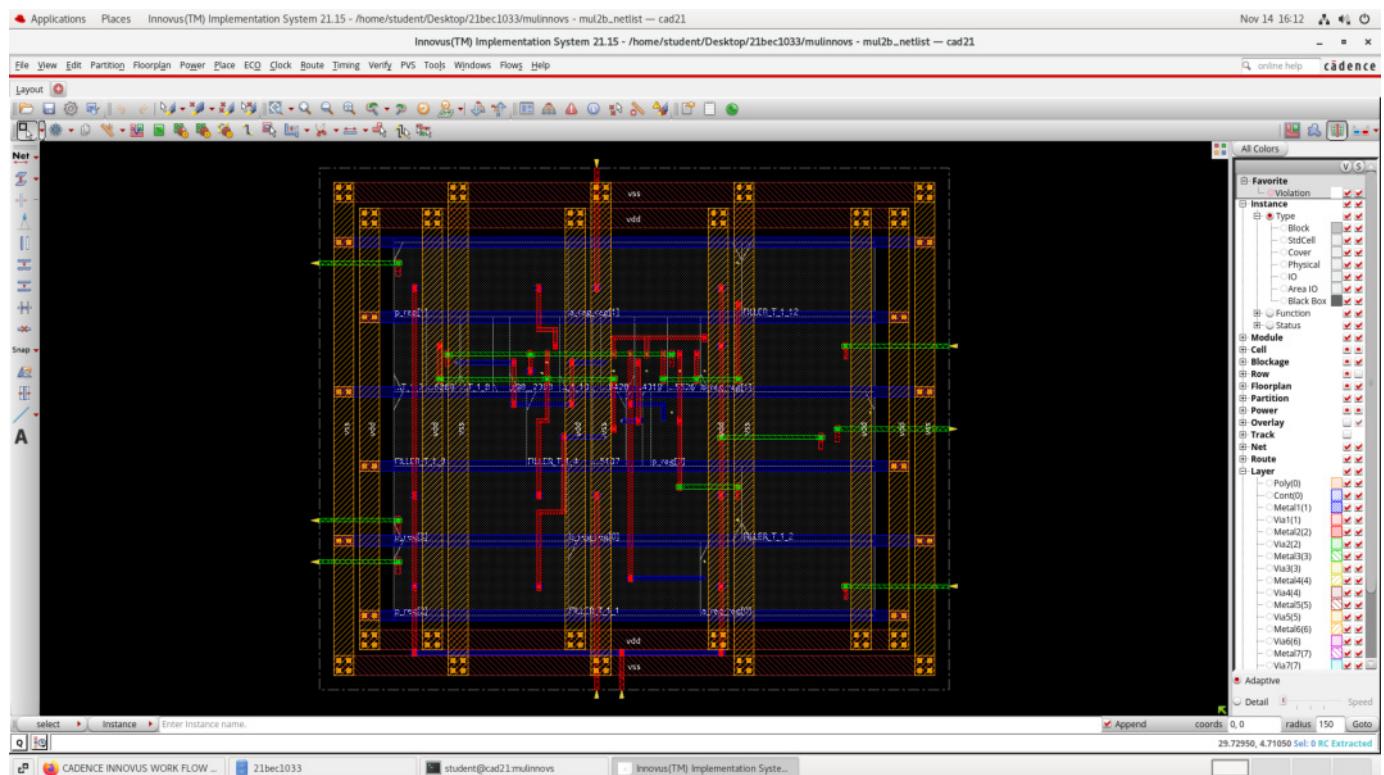
Ln 11, Col 6 | 234 characters | 100% | Unix (LF) | UTF-8

Post Synthesis verification:



Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Physical design of the Multiplier:



Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Genus Terminal:

```
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -legacy_ui -f mul2b.tcl
2024/11/14 13:59:34 WARNING This OS does not appear to be a Cadence
supported Linux configuration.
2024/11/14 13:59:34 For more info, please run CheckSysConf in
<cdsRoot/tools.lnx86/bin/checkSysConf <productId>
TMPDIR is being set to /tmp/genus_temp_6041_cad21_student_Zv8Eh3
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved
worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a
trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[13:59:38.095721] Configured Lic search path (21.01-s002): 5280@cadence

Version: 21.14-s082_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files mul2b.tcl
Date:    Thu Nov 14 13:59:38 2024
Host:    cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64)
(12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700
25600KB) (32402340KB)
PID:     6041
OS:      Red Hat Enterprise Linux release 8.8 (Ootpa)

[13:59:38.067337] Periodic Lic check successful
[13:59:38.067337] Feature usage summary:
[13:59:38.067337] Genus_Synthesis
Checking out license: Genus_Synthesis

*****
***** Loading tool scripts...
***** Finished loading tool scripts (6 seconds elapsed).

#@ Processing -files option
@genus 1> source mul2b.tcl

Threads Configured:3

Message Summary for Library slow.lib:
*****
Missing a function attribute in the output pin definition. [LBR-518]: 1
Missing library level attribute. [LBR-516]: 1
*****


Info    : Created nominal operating condition. [LBR-412]
          : Operating condition '_nominal_' was created for the PVT values
(1.000000, 0.900000, 125.000000) in library 'slow.lib'.
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
: The nominal operating condition is represented, either by the
nominal PVT values specified in the library source (via
nom_process, nom_voltage and nom_temperature respectively), or by the
default PVT values (1.0,1.0,1.0).
Setting attribute of root '/': 'library' = slow.lib
Library has 324 usable logic and 128 usable sequential lib-cells.
Info    : Elaborating Design. [ELAB-1]
          : Elaborating top-level block 'mul2b' from file 'mul2b.v'.
Info    : Done Elaborating Design. [ELAB-3]
          : Done elaborating 'mul2b'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_elab
-----
| Trick           | Accepts | Rejects | Runtime (ms) |
|-----|
| ume_constant_bmux |      0 |      0 |      0.00 |
|-----|
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef:
mul2b, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime:
0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab,
startdef: mul2b, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime:
0.000s)

Stage: post_elab
-----
| Transform        | Accepts | Rejects | Runtime (ms) |
|-----|
| hlo_clip_mux_input |      0 |      0 |      0.00 |
| hlo_clip          |      0 |      0 |      0.00 |
|-----|
Statistics for commands executed by read_sdc:
  "create_clock"           - successful     1 , failed      0 (runtime
0.00)
  "get_clocks"            - successful     6 , failed      0 (runtime
0.00)
  "get_ports"             - successful     4 , failed      0 (runtime
0.00)
  "set_clock_transition" - successful     2 , failed      0 (runtime
0.00)
  "set_clock_uncertainty" - successful     1 , failed      0 (runtime
0.00)
  "set_input_delay"       - successful     2 , failed      0 (runtime
0.00)
  "set_output_delay"      - successful     1 , failed      0 (runtime
0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
  Setting attribute of root '/': 'syn_generic_effort' = high
  Setting attribute of root '/': 'syn_map_effort' = high
  Setting attribute of root '/': 'syn_opt_effort' = high

Stage: pre_early_cg
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
| Transform | Accepts | Rejects | Runtime (ms) |
-----+-----+-----+-----+-----+
##Generic Timing Info for library domain: _default_ typical gate delay:
127.0 ps std_slew: 15.5 ps std_load: 7.0 fF
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup,
startdef: mul2b, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime:
0.000s)

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
-----+-----+-----+-----+-----+
| hlo_mux_reorder | 0 | 0 | 0.00 |
-----+
Info      : Synthesizing. [SYNTH-1]
            : Synthesizing 'mul2b' to generic gates using 'high' effort.
PBS_Generic-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Start' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory | Stage
-----+-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
TNS Restructuring config: no_value at stage: generic applied.
Info      : Partition Based Synthesis execution skipped. [PHYS-752]
            : Design size is less than the partition size '100000' for
distributed generic optimization to kick in.
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup,
startdef: mul2b, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime:
0.000s)

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
-----+-----+-----+-----+-----+
| hlo_mux_reorder | 0 | 0 | 0.00 |
-----+
Starting mux data reorder optimization [v1.0] (stage: post_to_gen_setup,
startdef: mul2b, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime:
0.000s)

Stage: post_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
-----+-----+-----+-----+-----+
| hlo_mux_reorder | 0 | 0 | 0.00 |
-----+
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: pre_hlo_rtlopt
-----
| Trick | Accepts | Rejects | Runtime (ms) |
-----
Starting infer macro optimization [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed infer macro optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting decode mux sandwich optimization [v2.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed decode mux sandwich optimization (accepts: 0, rejects: 0, runtime: 0.001s)
Starting decode mux optimization [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed decode mux optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting chop wide muxes [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed chop wide muxes (accepts: 0, rejects: 0, runtime: 0.000s)
Starting common data mux cascade opt [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed common data mux cascade opt (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux input consolidation [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed mux input consolidation (accepts: 0, rejects: 0, runtime: 0.000s)
Starting constant-data mux optimization [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed constant-data mux optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting chain-to-tree inequality transform [v2.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed chain-to-tree inequality transform (accepts: 0, rejects: 0, runtime: 0.000s)
Starting reconvergence optimization [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed reconvergence optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting logic restructure optimization [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed logic restructure optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting common select mux optimization [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed common select mux optimization (accepts: 0, rejects: 0, runtime: 0.000s)
Starting identity transform [v3.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed identity transform (accepts: 0, rejects: 0, runtime: 0.000s)
Starting reduce operator chain [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed reduce operator chain (accepts: 0, rejects: 0, runtime: 0.000s)
Starting common data mux cascade opt [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Completed common data mux cascade opt (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux input consolidation [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed mux input consolidation (accepts: 0, rejects: 0, runtime: 0.000s)
Starting optimize datapath elements [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed optimize datapath elements (accepts: 0, rejects: 0, runtime: 0.000s)
Starting datapath recasting [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed datapath recasting (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip mux common data inputs [v1.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: pre_rtlopt, startdef: mul2b, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)
```

Stage: pre_rtlopt

Transform	Accepts	Rejects	Runtime (ms)
hlo_infer_macro	0	0	0.00
hlo_decode_mux_sandwich	0	0	1.00
hlo_mux_decode	0	0	0.00
hlo_chop_mux	0	0	0.00
hlo_mux_cascade_opt	0	0	0.00
hlo_mux_consolidation	0	0	0.00
hlo_constant_mux_opt	0	0	0.00
hlo_inequality_transform	0	0	0.00
hlo_reconv_opt	0	0	0.00
hlo_restructure	0	0	0.00
hlo_common_select_muxopto	0	0	0.00
hlo_identity_transform	0	0	0.00
hlo_reduce_operator_chain	0	0	0.00
hlo_mux_cascade_opt	0	0	0.00
hlo_mux_consolidation	0	0	0.00
hlo_optimize_datapath	0	0	0.00
hlo_datapath_recast	0	0	0.00
hlo_clip_mux_input	0	0	0.00
hlo_clip	0	0	0.00

Running Unified Mux Engine Tricks...

Completed Unified Mux Engine Tricks

Stage: post_hlo_rtlopt

Trick	Accepts	Rejects	Runtime (ms)
ume_runtime	0	0	0.00

Number of big hc bmuxes before = 0

Info : Pre-processed datapath logic. [DPOPT-6]
: No pre-processing optimizations applied to datapath logic in 'mul2b'.
Info : Skipping datapath optimization. [DPOPT-5]

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
: There is no datapath logic in 'mul2b'.
Number of big hc bmxes after = 0
Starting logic reduction [v1.0] (stage: post_rtlopt, startdef: mul2b,
recur: true)
Completed logic reduction (accepts: 0, rejects: 0, runtime: 0.000s)
Starting mux data reorder optimization [v1.0] (stage: post_rtlopt,
startdef: mul2b, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime:
0.000s)

Stage: post_rtlopt
-----
| Transform | Accepts | Rejects | Runtime (ms) |
|-----|
| hlo_logic_reduction | 0 | 0 | 0.00 |
| hlo_mux_reorder | 0 | 0 | 0.00 |
|-----|
Starting mux speculation [v1.0] (stage: post_muxopt, startdef: mul2b,
recur: true)
Starting speculation optimization
Completed speculation optimization (accepts:0)
Completed mux speculation (accepts: 0, rejects: 0, runtime: 0.002s)

Stage: post_muxopt
-----
| Transform | Accepts | Rejects | Runtime (ms) |
|-----|
| hlo_speculation | 0 | 0 | 2.00 |
|-----|
=====
Stage : to_generic
=====
=====
Message Summary
=====
-----
| Id | Sev | Count | Message Text
|-----|
| DPOPT-5 | Info | 1 | Skipping datapath optimization.
| DPOPT-6 | Info | 1 | Pre-processed datapath logic.
| ELAB-1 | Info | 1 | Elaborating Design.
| ELAB-2 | Info | 1 | Elaborating Subdesign.
| ELAB-3 | Info | 1 | Done Elaborating Design.
| LBR-41 | Info | 1 | An output library pin lacks a function
attribute. |
| | | | If the remainder of this library cell's semantic
| | | | checks are successful, it will be considered as
a | | | timing-model
| | | |
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
|           |       | (because one of its outputs does not have a  
valid fu |       | nction.  
| LBR-155  |Info  | 372 |Mismatch in unateness between 'timing_sense'  
|           |       | attribute and the function.  
|           |       |The 'timing_sense' attribute will be respected.  
| LBR-161  |Info  | 1  |Setting the maximum print count of this message  
to 10 |           | if information_level is less than 9.  
| LBR-162  |Info  | 124 |Both 'pos_unate' and 'neg_unate' timing_sense  
arcs    |           | have been processed.  
|           |       |Setting the 'timing_sense' to non_unate.  
| LBR-170  |Info  | 32  |Ignoring specified timing sense.  
|           |       |Timing sense should never be set with  
'rising_edge' |           | or 'falling_edge' timing type.  
| LBR-412  |Info  | 1  |Created nominal operating condition.  
|           |       |The nominal operating condition is represented,  
|           |       | either by the nominal PVT values specified in  
the     |           | library source  
|           |       | (via nom_process,nom_voltage and  
nom_temperature res |           | pectively)  
|           |       | , or by the default PVT values (1.0,1.0,1.0).  
| LBR-516  |Info  | 1  |Missing library level attribute.  
| LBR-518  |Info  | 1  |Missing a function attribute in the output pin  
|           |       | definition.  
| PHYS-752 |Info  | 1  |Partition Based Synthesis execution skipped.  
| SYNTH-1  |Info  | 1  |Synthesizing.  
| TIM-1000 |Info  | 1  |Multimode clock gating check is disabled.  
|-----  
-----  
Mapper: Libraries have:  
    domain _default_: 324 combo usable cells and 128 sequential usable  
cells  
Multi-threaded constant propagation [1|0] ...  
Multi-threaded Virtual Mapping (8 threads, 8 of 20 CPUs usable)  
=====
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Stage : first_condense
=====
=====
Message Summary
=====

-----
| Id    | Sev   | Count |                                Message Text
|       |
|-----|
| GLO-51 | Info  |      2 | Hierarchical instance automatically ungrouped.
|       |       |       | Hierarchical instances can be automatically
ungrouped   |       |       | to allow for better area or timing optimization.
To       |       |       | prevent this ungroup, set the root-level
attribute |       |       | 'auto_ungroup' to 'none'. You can also prevent
           |       |       | individual ungroup with setting the attribute
           |       |       | 'ungroup_ok' of instances or modules to 'false'.
|       |
|-----|
Global mapping target info
=====
Cost Group 'clk' target slack:  267 ps
Target path end-point (Port: mul2b/p[0])

State Retention Synthesis Status
=====
Category                      Flops Percentage
-----
Total instances                8      100.0
Excluded from State Retention 8      100.0
  - Will not convert          8      100.0
    - Preserved               0      0.0
    - Power intent excluded  8      100.0
  - Could not convert         0      0.0
    - Scan type               0      0.0
    - No suitable cell        0      0.0
State Retention instances     0      0.0
-----
PBS_Generic_Opt-Post - Elapsed_Time 1, CPU_Time 0.9913040000000004
stamp 'PBS_Generic_Opt-Post' being created for table 'pbs_debug'

  Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
  | Memory   | Stage
  -----+-----+-----+-----+
  00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```

-----+-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 100.0(100.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_Generic-Postgen HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Generic-Postgen HBO Optimizations' being created for table
'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory | Stage
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
-----+-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 100.0(100.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
##>===== Cadence Confidential (Generic-Logical)
=====
##>===== Cadence Confidential (Generic-Logical)
=====
##>Main Thread Summary:
##>-----
-----+-----+-----+-----+-----+
# ##>STEP Elapsed WNS TNS Insts
Area Memory
##>-
-----+-----+-----+-----+-----+
##>G:Initial 0 - - 18
282 460
##>G:Setup 0 - - - -
-----+-----+-----+-----+-----+
##>G:Launch ST 0 - - - -
-----+-----+-----+-----+-----+
##>G:Design Partition 0 - - - -
-----+-----+-----+-----+-----+
##>G>Create Partition Netlists 0 - - - -
-----+-----+-----+-----+-----+
##>G:Init Power 0 - - - -
-----+-----+-----+-----+-----+
##>G:Budgeting 0 - - - -
-----+-----+-----+-----+-----+

```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
##>G:Derenv-DB          0      -      -      -
-      -
##>G:Debug Outputs      0      -      -      -
-      -
##>G:ST loading          0      -      -      -
-      -
##>G:Distributed          0      -      -      -
-      -
##>G:Timer                0      -      -      -
-      -
##>G:Assembly              0      -      -      -
-      -
##>G:DFT                  0      -      -      -
-      -
##>G:Const Prop          0      -      -      18
286     460
##>G:Misc                  1
##>-----
-----+
##>Total Elapsed           1
##>=====
=====+
Info      : Done synthesizing. [SYNTH-2]
          : Done synthesizing 'mul2b' to generic gates.
##Generic Timing Info for library domain: _default_ typical gate delay:
127.0 ps std_slew: 15.5 ps std_load: 7.0 ff
Info      : Mapping. [SYNTH-4]
          : Mapping 'mul2b' using 'high' effort.
Mapper: Libraries have:
          domain _default_: 324 combo usable cells and 128 sequential usable
cells
Configuring mapper costing (none)
TNS Restructuring config: no_value at stage: map applied.
PBS_TechMap-Start - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Start' being created for table 'pbs_debug'

      Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
      | Memory   | Stage
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 100.0(100.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Start
-----+-----+-----+
Number of threads: 8 * 1  (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
PBS_TechMap-Premap HBO Optimizations - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Premap HBO Optimizations' being created for table
'pbs_debug'

      Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
      | Memory | Stage
-----+-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 100.0(100.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Start
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
Info : Partition Based Synthesis execution skipped. [PHYS-752]
      : Design size is less than the partition size '100000' for
distributed mapping optimization to kick in.
Mapper: Libraries have:
      domain _default_: 324 combo usable cells and 128 sequential usable
cells
Multi-threaded Virtual Mapping (8 threads, 8 of 20 CPUs usable)

Global mapping target info
=====
Cost Group 'clk' target slack: 267 ps
Target path end-point (Port: mul2b/p[0])

Multi-threaded Virtual Mapping (8 threads, 8 of 20 CPUs usable)
Multi-threaded Technology Mapping (8 threads, 8 of 20 CPUs usable)

Global mapping status
=====
                    Group
                    Tot Wrst
                    Total Weighted
Operation          Area   Slacks
global_map         151    0

Cost Group          Target     Slack     Diff. Constr.
-----
clk                267       8594      10000
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Global incremental target info
=====
Cost Group 'clk' target slack: 178 ps
Target path end-point (Port: mul2b/p[0])

=====
Stage : global_incr_map
=====

=====
Message Summary
=====

-----
|   Id    |Sev  |Count |           Message Text          |
|-----|
| PHYS-752 |Info |     1 |Partition Based Synthesis execution skipped. |
| SYNTH-2  |Info |     1 |Done synthesizing.                |
| SYNTH-4  |Info |     1 |Mapping.                         |
-----


Global incremental optimization status
=====
                               Group
                               Tot Wrst
                           Total  Weighted
Operation             Area    Slacks
global_incr          151      0

Cost Group          Target   Slack   Diff.  Constr.
-----
clk                 178     8594    10000

State Retention Synthesis Status
=====

Category              Flops  Percentage
-----
Total instances        8      100.0
Excluded from State Retention  8      100.0
  - Will not convert    8      100.0
    - Preserved         0      0.0
    - Power intent excluded  8      100.0
  - Could not convert    0      0.0
    - Scan type          0      0.0
    - No suitable cell   0      0.0
State Retention instances  0      0.0
-----


INFO: skipping constant propagation
PBS_Techmap-Global Mapping - Elapsed_Time 0, CPU_Time -
0.01803700000000525
stamp 'PBS_Techmap-Global Mapping' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory | Stage
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
-----+-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 101.9(100.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Start
-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | -1.9( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Techmap-Global Mapping
-----+-----+
-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
Warning : Command 'commit_power_intent' cannot proceed as there is no
power intent loaded. [CPI-506]
      : Command 'commit_power_intent' requires a valid power_intent to
be loaded.
Info   : Wrote formal verification information. [CFM-5]
      : Wrote 'fv/mul2b/fv_map.fv.json' for netlist
'fv/mul2b/fv_map.v.gz'.
Info   : Wrote dofile. [CFM-1]
      : Dofile is 'fv/mul2b/rtl_to_fv_map.do'.
      : Alias mapping flow is enabled.
PBS_TechMap-Datapath Postmap Operations - Elapsed_Time 1, CPU_Time 0.0
stamp 'PBS_TechMap-Datapath Postmap Operations' being created for table
'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory | Stage
-----+-----+-----+
-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 101.9( 50.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+
-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Start
-----+-----+
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Premap HBO Optimizations
-----
+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | -1.9( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Techmap-Global Mapping
-----
+-----+
00:00:04(00:00:05) | 00:00:00(00:00:01) | 0.0( 50.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Datapath Postmap Operations
-----
+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_TechMap-Postmap HBO Optimizations - Elapsed_Time 0, CPU_Time -
0.0001319999999979894
stamp 'PBS_TechMap-Postmap HBO Optimizations' being created for table
'pbs_debug'

      Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
      | Memory | Stage
-----
+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
-----
+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 101.9( 50.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----
+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----
+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Start
-----
+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Premap HBO Optimizations
-----
+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | -1.9( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Techmap-Global Mapping
-----
+-----+
00:00:04(00:00:05) | 00:00:00(00:00:01) | 0.0( 50.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Datapath Postmap Operations
-----
+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | -0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap HBO Optimizations
-----
+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Info: CPU time includes time of parent + longest thread
Doing ConstProp on /designs/mul2b ...

Time taken by ConstProp Step: 00:00:00
PBS_TechMap-Postmap Clock Gating - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_TechMap-Postmap Clock Gating' being created for table
'pbs_debug'

      Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
      | Memory   | Stage
-----+-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 101.9( 50.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Start
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | -1.9( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Techmap-Global Mapping
-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:01) | 0.0( 50.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | -0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap HBO Optimizations
-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap Clock Gating
-----+-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
-----
hi_fo_buf           151       0       0       0
      Trick    Calls   Accepts  Attempts   Time (secs)
-----
hi_fo_buf          0 (      0 /      0 )  0.00
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Incremental optimization status

Operation		Group				
		Total Area	Wrst Slacks	Total	DRC	Total
				Neg Slack	Max Cap	
init_delay		151	0	0	0	0
<hr/>						
Trick	Calls	Accepts	Attempts	Time (secs)		
crit_upsz	0 (0 /	0)	0.00		
plc_bal_star	0 (0 /	0)	0.00		
drc_buftimb	0 (0 /	0)	0.00		
plc_st	0 (0 /	0)	0.00		
plc_st_fence	0 (0 /	0)	0.00		
plc_star	0 (0 /	0)	0.00		
plc_laf_st	0 (0 /	0)	0.00		
plc_laf_st_fence	0 (0 /	0)	0.00		
drc_buftims	0 (0 /	0)	0.00		
fopt	0 (0 /	0)	0.00		
plc_laf_lo_st	0 (0 /	0)	0.00		
plc_lo_st	0 (0 /	0)	0.00		
mb_split	0 (0 /	0)	0.00		

Local TNS optimization status

Operation	Group				
	Total Area	Wrst Slacks	Total	DRC	Total
			Neg Slack	Max Cap	
init_tns	151	0	0	0	0
<hr/>					
Trick	Calls	Accepts	Attempts	Time (secs)	
plc_bal_star	0 (0 /	0)	0.00	
drc_buftimb	0 (0 /	0)	0.00	
drc_buftims	0 (0 /	0)	0.00	
crit_upsz	0 (0 /	0)	0.00	
plc_laf_lo_st	0 (0 /	0)	0.00	
plc_lo_st	0 (0 /	0)	0.00	
fopt	0 (0 /	0)	0.00	
crit_dnsz	0 (0 /	0)	0.00	
dup	0 (0 /	0)	0.00	
setup_dn	0 (0 /	0)	0.00	
mb_split	0 (0 /	0)	0.00	

PBS_TechMap-Postmap Cleanup - Elapsed_Time 0, CPU_Time - 0.0003039999999985994

stamp 'PBS_TechMap-Postmap Cleanup' being created for table 'pbs_debug'

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time
Memory	Stage		
<hr/>			
00:00:04(00:00:03)	00:00:00(00:00:00)	0.0(0.0)	13:59:44
<hr/>			
(Nov14)	460.7 MB	PBS_Generic-Start	
<hr/>			

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
00:00:04(00:00:04) | 00:00:00(00:00:01) | 101.9( 50.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Start
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Premap HBO Optimizations
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | -1.9( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Techmap-Global Mapping
-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:01) | 0.0( 50.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Datapath Postmap Operations
-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | -0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap HBO Optimizations
-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap Clock Gating
-----+-----+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | -0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap Cleanup
-----+-----+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
PBS_Techmap-Post_MBCI - Elapsed_Time 0, CPU_Time 0.0
stamp 'PBS_Techmap-Post_MBCI' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time
| Memory | Stage
-----+-----+-----+
00:00:04(00:00:03) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:44
(Nov14) | 460.7 MB | PBS_Generic-Start
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:01) | 101.9( 50.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic_Opt-Post
-----+-----+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Generic-Postgen HBO Optimizations
-----+-----+-----+
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```

00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Start
-----
+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_TechMap-Premap HBO Optimizations
-----
+-----+
00:00:04(00:00:04) | 00:00:00(00:00:00) | -1.9( 0.0) | 13:59:45
(Nov14) | 460.7 MB | PBS_Techmap-Global Mapping
-----
+-----+
00:00:04(00:00:05) | 00:00:00(00:00:01) | 0.0( 50.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Datapath Postmap Operations
-----
+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | -0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap HBO Optimizations
-----
+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap Clock Gating
-----
+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | -0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_TechMap-Postmap Cleanup
-----
+-----+
00:00:04(00:00:05) | 00:00:00(00:00:00) | 0.0( 0.0) | 13:59:46
(Nov14) | 460.7 MB | PBS_Techmap-Post_MBCI
-----
+-----+
Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*N*) indicates data that was populated from previously saved
time_info database
Info: CPU time includes time of parent + longest thread
##>===== Cadence Confidential (Mapping-Logical)
=====
##>Main Thread Summary:
##>-
-----
#>STEP                               Elapsed      WNS      TNS      Insts
Area     Memory
#>-
-----
##>M:Initial                           0          -        -       18
286      460
##>M:Pre Cleanup                       0          -        -       18
286      460
##>M:Setup                            0          -        -       -
-      -
##>M:Launch ST                         0          -        -       -
-      -
##>M:Design Partition                  0          -        -       -
-      -
##>M>Create Partition Netlists         0          -        -       -
-      -
##>M:Init Power                        0          -        -       -
-      -

```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```

##>M:Budgeting          0      -      -      -
##>M:Derenv-DB          0      -      -      -
##>M:Debug Outputs       0      -      -      -
##>M:ST loading           0      -      -      -
##>M:Distributed          0      -      -      -
##>M:Timer                0      -      -      -
##>M:Assembly              0      -      -      -
##>M:DFT                  0      -      -      -
##>M:DP Operations         1      -      -      14
151      460
##>M:Const Prop            0     8594    0     14
151      460
##>M:Cleanup               0     8594    0     14
151      460
##>M:MBCI                 0      -      -      14
151      460
##>M:Const Gate Removal     0      -      -      -
##>M:Misc                  0
##>-----
##>Total Elapsed           1
##>=====
=====

Info      : Done mapping. [SYNTH-5]
          : Done mapping 'mul2b'.
Info      : Incrementally optimizing. [SYNTH-7]
          : Incrementally optimizing 'mul2b' using 'high' effort.

Incremental optimization status
=====
                    Group
                    Tot Wrst      Total DRC Total
                    Total Weighted    Neg      Max
Operation          Area   Slacks      Slack    Cap
init_iopt          151      0          0        0
-----
const_prop          151      0          0        0
-----
hi_fo_buf          151      0          0        0
Trick      Calls      Accepts      Attempts      Time (secs)
-----
hi_fo_buf          0 ( 0 / 0 ) 0.00

```

```

Incremental optimization status
=====
                    Group
                    Tot Wrst      Total DRC Total

```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Operation	Total	Weighted	Neg	Max
	Area	Slacks	Slack	Cap
init_delay	151	0	0	0
Trick	Calls	Accepts	Attempts	Time (secs)
crit_msz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
crit_slew	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
plc_bal_star	0 (0 /	0)	0.00
drc_buftimb	0 (0 /	0)	0.00
plc_st	0 (0 /	0)	0.00
plc_st_fence	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
plc_laf_st	0 (0 /	0)	0.00
plc_laf_st_fence	0 (0 /	0)	0.00
drc_buftims	0 (0 /	0)	0.00
plc_laf_lo_st	0 (0 /	0)	0.00
plc_lo_st	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
crit_swap	0 (0 /	0)	0.00
mux2_swap	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
load_swap	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
phase	0 (0 /	0)	0.00
in_phase	0 (0 /	0)	0.00
merge_bit	0 (0 /	0)	0.00
merge_idrvr	0 (0 /	0)	0.00
merge_iload	0 (0 /	0)	0.00
merge_idload	0 (0 /	0)	0.00
merge_drvr	0 (0 /	0)	0.00
merge_load	0 (0 /	0)	0.00
decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
exp	0 (0 /	0)	0.00
gate_deco	0 (0 /	0)	0.00
gcomp_tim	0 (0 /	0)	0.00
inv_pair_2_buf	0 (0 /	0)	0.00
Trick	Calls	Accepts	Attempts	Time (secs)
crr_220	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

crr_200	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_300	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_400	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_111	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_210	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_110	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_101	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_201	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crr_211	0 (0 /	0)	0.00
crr_glob	0 (0 /	0)	0.00
crit_msz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
crit_slew	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
plc_bal_star	0 (0 /	0)	0.00
drc_buftimb	0 (0 /	0)	0.00
plc_st	0 (0 /	0)	0.00
plc_st_fence	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
plc_laf_st	0 (0 /	0)	0.00
plc_laf_st_fence	0 (0 /	0)	0.00
drc_buftims	0 (0 /	0)	0.00
plc_lo_st	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
crit_swap	0 (0 /	0)	0.00
mux2_swap	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
load_swap	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
rem_hi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
rem_hi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
merge_bit	0 (0 /	0)	0.00
merge_idrvr	0 (0 /	0)	0.00
merge_iload	0 (0 /	0)	0.00
merge_idload	0 (0 /	0)	0.00
merge_drvr	0 (0 /	0)	0.00
merge_load	0 (0 /	0)	0.00
phase	0 (0 /	0)	0.00
decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
in_phase	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

buf2inv	0 (0 /	0)	0.00
exp	0 (0 /	0)	0.00
gate_deco	0 (0 /	0)	0.00
gcomp_tim	0 (0 /	0)	0.00
inv_pair_2_buf	0 (0 /	0)	0.00
init_drc		151	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
crit_slew	0 (0 /	0)	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_buf_sp	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_buf_sp	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00

init_tns		151	0	0	0
----------	--	-----	---	---	---

Trick	Calls	Accepts	Attempts	Time (secs)
fopt	0 (0 /	0)	0.00
plc_bal_star	0 (0 /	0)	0.00
drc_buftimb	0 (0 /	0)	0.00
drc_buftims	0 (0 /	0)	0.00
crit_msz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
plc_laf_lo_st	0 (0 /	0)	0.00
plc_lo_st	0 (0 /	0)	0.00
crit_swap	0 (0 /	0)	0.00

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
load_swap	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
merge_bit	0 (0 /	0)	0.00
merge_idrvr	0 (0 /	0)	0.00
merge_iload	0 (0 /	0)	0.00
merge_idload	0 (0 /	0)	0.00
merge_drvr	0 (0 /	0)	0.00
merge_load	0 (0 /	0)	0.00
phase	0 (0 /	0)	0.00
decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00
crr_local	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
 init_area	 151	 0	 0	 0
 Trick	 Calls	 Accepts	 Attempts	 Time (secs)
undup	0 (0 /	0)	0.00
rem_buf	0 (0 /	0)	0.00
rem_inv	0 (0 /	0)	0.00
merge_bi	0 (0 /	0)	0.00
rem_inv_qb	0 (0 /	0)	0.00
seq_res_area	3 (0 /	0)	0.04
io_phase	0 (0 /	0)	0.00
gate_comp	0 (0 /	0)	0.00
gcomp_mog	0 (0 /	0)	0.00
glob_area	4 (0 /	4)	0.00
area_down	0 (0 /	0)	0.00
size_n_buf	0 (0 /	0)	0.00
gate_deco_area	0 (0 /	0)	0.00
rem_buf	0 (0 /	0)	0.00
rem_inv	0 (0 /	0)	0.00
merge_bi	0 (0 /	0)	0.00
rem_inv_qb	0 (0 /	0)	0.00

Incremental optimization status

=====

Operation	Group			Total DRC Total	
	Total Area	Weighted Slacks	Slack Cap		
init_delay	151	0	0	0	

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Trick	Calls	Accepts	Attempts	Time (secs)
crit_msz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00
crit_slew	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
plc_bal_star	0 (0 /	0)	0.00
drc_buftimb	0 (0 /	0)	0.00
plc_st	0 (0 /	0)	0.00
plc_st_fence	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
plc_laf_st	0 (0 /	0)	0.00
plc_laf_st_fence	0 (0 /	0)	0.00
drc_buftims	0 (0 /	0)	0.00
plc_laf_lo_st	0 (0 /	0)	0.00
plc_lo_st	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
crit_swap	0 (0 /	0)	0.00
mux2_swap	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
load_swap	0 (0 /	0)	0.00
fopt	0 (0 /	0)	0.00
setup_dn	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
load_isol	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
move_for	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
rem_bi	0 (0 /	0)	0.00
offload	0 (0 /	0)	0.00
phase	0 (0 /	0)	0.00
in_phase	0 (0 /	0)	0.00
merge_bit	0 (0 /	0)	0.00
merge_idrvr	0 (0 /	0)	0.00
merge_iload	0 (0 /	0)	0.00
merge_idload	0 (0 /	0)	0.00
merge_drvr	0 (0 /	0)	0.00
merge_load	0 (0 /	0)	0.00
decomp	0 (0 /	0)	0.00
p_decomp	0 (0 /	0)	0.00
levelize	0 (0 /	0)	0.00
mb_split	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
mux_retime	0 (0 /	0)	0.00
buf2inv	0 (0 /	0)	0.00
exp	0 (0 /	0)	0.00
gate_deco	0 (0 /	0)	0.00
gcomp_tim	0 (0 /	0)	0.00
inv_pair_2_buf	0 (0 /	0)	0.00
init_drc	151	0	0	0

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```

simple_buf      0 (      0 /      0 )  0.00
    dup        0 (      0 /      0 )  0.00
crit_dnsz     0 (      0 /      0 )  0.00
crit_upsz     0 (      0 /      0 )  0.00
crit_slew     0 (      0 /      0 )  0.00

```

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
simple_buf	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00

Trick	Calls	Accepts	Attempts	Time (secs)
plc_st	0 (0 /	0)	0.00
plc_star	0 (0 /	0)	0.00
drc_bufs	0 (0 /	0)	0.00
drc_fopt	0 (0 /	0)	0.00
drc_bufb	0 (0 /	0)	0.00
dup	0 (0 /	0)	0.00
crit_dnsz	0 (0 /	0)	0.00
crit_upsz	0 (0 /	0)	0.00

=====

Stage : incr_opt

=====

=====

Message Summary

=====

Id	Sev	Count	Message Text
<hr/>			
CFM-1 Info 1 Wrote dofile.			
CFM-5 Info 1 Wrote formal verification information.			
CPI-506 Warning 1 Command 'commit_power_intent' cannot proceed as there is no power intent loaded.			
PA-7 Info 4 Resetting power analysis results.			
All computed switching activities are removed.			
SYNTH-5 Info 1 Done mapping.			
SYNTH-7 Info 1 Incrementally optimizing.			

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
-----
Info      : Done incrementally optimizing. [SYNTH-8]
            : Done incrementally optimizing 'mul2b'.
Finished SDC export (command execution time mm:ss (real) = 00:00).
Info      : Joules engine is used. [RPT-16]
            : Joules engine is being used for the command report_power.
Info      : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0
netlist
            : mul2b
Info      : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info      : ACTP-0001 Activity propagation ended for stim#0
Info      : PWRA-0001 [PwrInfo] compute_power effective options
            : -mode : vectorless
            : -skip_propagation : 1
            : -frequency_scaling_factor : 1.0
            : -use_clock_freq : stim
            : -stim :/stim#0
            : -fromGenus : 1
Info      : ACTP-0001 Timing initialization started
Info      : ACTP-0001 Timing initialization ended
Info      : PWRA-0002 [PwrInfo] Skipping activity propagation due to -
skip_ap
            : option....
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for
vectorless
            : flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with
vectorless mode
            : of power analysis, ignored this option.
Info      : PWRA-0002 Started 'vectorless' power computation.
Info      : PWRA-0002 Finished power computation.
Info      : PWRA-0007 [PwrInfo] Completed successfully.
            : Info=6, Warn=2, Error=0, Fatal=0
Output file: mul2b_power.rpt
WARNING: This version of the tool is 874 days old.
legacy_genus:/>
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Innovus Terminal:

```
[student@cad21 mulinnovs]$ csh
[student@cad21 mulinnovs]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 mulinnovs]$ innovus

Cadence Innovus(TM) Implementation System.
Copyright 2021 Cadence Design Systems, Inc. All rights reserved
worldwide.

Version: v21.15-s110_1, built Fri Sep 23 13:08:12 PDT 2022
Options:
Date: Thu Nov 14 16:01:00 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.e18_7.x86_64)
(12cores*20cpus*12th Gen Intel(R) Core(TM) i7-12700 25600KB)
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

License:
[16:01:00.095553] Configured Lic search path (21.01-s002):
5280@cadence

      invs  Innovus Implementation System      21.1  checkout
succeeded
      8 CPU jobs allowed with the current license(s). Use
setMultiCpuUsage to set your required CPU count.
Create and set the environment variable TMPDIR to
/tmp/innovus_temp_29042_cad21_student_7MxDwd.

Change the soft stacksize limit to 0.2%RAM (63 mbytes). Set global
soft_stack_size_limit to change the value.

**INFO: MMMC transition support version v31-84

[INFO] Loading PVS 22.20 fill procedures
innovus 1> #% Begin Load MMMC data ... (date=11/14 16:03:57, mem=1027.2M)
#% End Load MMMC data ... (date=11/14 16:03:57, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1027.9M, current mem=1027.9M)

Loading LEF file
../../../../install/FOUNDRY/digital/90nm/dig/lef/gsclib090_translated.lef
...
**WARN: (IMPLF-105): The layer 'Oxide' specified in SAMENET spacing
rule is neither a routing layer nor a cut layer. The rule is ignored.
**WARN: (IMPLF-105): The layer 'Poly' specified in SAMENET spacing
rule is neither a routing layer nor a cut layer. The rule is ignored.
Set DBUPerIGU to M2 pitch 580.
**WARN: (IMPLF-200): Pin 'A' in macro 'ANTENNA' has no ANTENNAGATEAREA
value defined. The library data is incomplete and some process antenna
rules will not be checked correctly.
Type 'man IMPLF-200' for more detail.

## Check design process and node:
## Both design process and tech node are not set.

Loading view definition file from Default.view
Reading maxt timing library
'/home/install/FOUNDRY/digital/90nm/dig/lib/slow.lib' ...
Read 479 cells in library 'slow'
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Reading mint timing library
'/home/install/FOUNDRY/digital/90nm/dig/lib/fast.lib' ...
Read 479 cells in library 'fast'
*** End library_loading (cpu=0.01min, real=0.00min, mem=31.0M,
fe_cpu=0.51min, fe_real=2.97min, fe_mem=1062.0M) ***
#% Begin Load netlist data ... (date=11/14 16:03:58, mem=1049.8M)
*** Begin netlist parsing (mem=1062.0M) ***
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR3X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR3X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XOR2X2' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XOR2X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR3X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR3X1' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR2XL' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR2XL' is defined in LEF but
not in the timing library.
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VSS' of cell 'XNOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (IMPVL-159): Pin 'VDD' of cell 'XNOR2X4' is defined in LEF but
not in the timing library.
Type 'man IMPVL-159' for more detail.
**WARN: (EMS-27): Message (IMPVL-159) has exceeded the current
message display limit of 20.
To increase the message display limit, refer to the product command
reference manual.
Created 479 new cells from 2 timing libraries.
Reading netlist ...
Backslashed names will retain backslash and a trailing blank character.
Reading verilog netlist 'mul2b_netlist.v'

*** Memory Usage v#1 (Current mem = 1061.953M, initial mem = 483.863M)
 ***
*** End netlist parsing (cpu=0:00:00.0, real=0:00:00.0, mem=1062.0M) ***
#% End Load netlist data ... (date=11/14 16:03:58, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1063.9M, current mem=1063.9M)
Top level cell is mul2b_netlist.
Hooked 958 DB cells to tlib cells.
Starting recursive module instantiation check.
No recursion found.
Building hierarchical netlist for Cell mul2b_netlist ...
*** Netlist is unique.
** info: there are 967 modules.
** info: there are 14 stdCell insts.

*** Memory Usage v#1 (Current mem = 1118.367M, initial mem = 483.863M)
 ***
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
unless standard cell models of this type exist in the LEF/OA library.
Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 290 (derived)
Vertical Layer M2 offset = 290 (derived)
Start create_tracks
Generated pitch 0.29 in Metal8 is different from 0.87 defined in
technology file in unpreferred direction.
Extraction setup Started
Initializing multi-corner RC extraction with 1 active RC Corners ...
Reading Capacitance Table File
../../../../install/FOUNDRY/digital/90nm/dig/captable/gpdk090.lef.extende
d.CapTbl ...
Cap table was created using Encounter 05.20-s112_1.
Process name: gpdk090_91.
Importing multi-corner RC tables ...
Summary of Active RC-Corners :
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Analysis View: worst
  RC-Corner Name      : rc
  RC-Corner Index     : 0
  RC-Corner Temperature : 25 Celsius
  RC-Corner Cap Table  :
'.../.../.../install/FOUNDRY/digital/90nm/dig/captable/gpdk090.lef.extend
ed.CapTbl'
  RC-Corner PreRoute Res Factor      : 1
  RC-Corner PreRoute Cap Factor     : 1
  RC-Corner PostRoute Res Factor    : 1 {1 1 1}
  RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
  RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
  RC-Corner PreRoute Clock Res Factor : 1      [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PreRoute Clock Cap Factor : 1      [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}  [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}  [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}

Analysis View: best
  RC-Corner Name      : rc
  RC-Corner Index     : 0
  RC-Corner Temperature : 25 Celsius
  RC-Corner Cap Table  :
'.../.../.../install/FOUNDRY/digital/90nm/dig/captable/gpdk090.lef.extend
ed.CapTbl'
  RC-Corner PreRoute Res Factor      : 1
  RC-Corner PreRoute Cap Factor     : 1
  RC-Corner PostRoute Res Factor    : 1 {1 1 1}
  RC-Corner PostRoute Cap Factor   : 1 {1 1 1}
  RC-Corner PostRoute XCap Factor  : 1 {1 1 1}
  RC-Corner PreRoute Clock Res Factor : 1      [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PreRoute Clock Cap Factor : 1      [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Cap Factor : 1 {1 1 1}  [Derived from
postRoute_cap (effortLevel low)]
  RC-Corner PostRoute Clock Res Factor : 1 {1 1 1}  [Derived from
postRoute_res (effortLevel low)]
  RC-Corner PostRoute Clock coupling capacitance Factor : 1 {1 1 1}

Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
*Info: initialize multi-corner CTS.
Reading timing constraints file 'mul2b.sdc' ...
Current (total cpu=0:00:30.6, real=0:02:58, peak res=1364.9M, current
mem=1364.9M)
**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
mul2b.sdc, Line 9).

**WARN: (TCLCMD-1461): Skipped unsupported command: set_units (File
mul2b.sdc, Line 10).

**WARN: (TCLCMD-513): The software could not find a matching object of
the specified type for the pattern 'mul2b' (File mul2b.sdc, Line 13).
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
**ERROR: (TCLCMD-917): Cannot find 'designs' that match 'mul2b' (File mul2b.sdc, Line 13).

INFO (CTE): Reading of timing constraints file mul2b.sdc completed, with 3 Warnings and 1 Errors.
Ending "Constraint file reading stats" (total cpu=0:00:00.0, real=0:00:00.0, peak res=1385.3M, current mem=1385.3M)
Current (total cpu=0:00:30.6, real=0:02:58, peak res=1385.3M, current mem=1385.3M)
Total number of combinational cells: 317
Total number of sequential cells: 152
Total number of tristate cells: 10
Total number of level shifter cells: 0
Total number of power gating cells: 0
Total number of isolation cells: 0
Total number of power switch cells: 0
Total number of pulse generator cells: 0
Total number of always on buffers: 0
Total number of retention cells: 0
List of usable buffers: BUFX2 BUFX12 BUFX16 BUFX20 CLKBUFX2 BUFX3 BUFX4
BUFX6 BUFX8 CLKBUFX12 CLKBUFX16 CLKBUFX20 CLKBUFX3 CLKBUFX4 CLKBUFX6
CLKBUFX8
Total number of usable buffers: 16
List of unusable buffers:
Total number of unusable buffers: 0
List of usable inverters: CLKINVX1 CLKINVX2 CLKINVX12 CLKINVX16 CLKINVX20
CLKINVX3 CLKINVX4 CLKINVX6 CLKINVX8 INVX1 INVX2 INVX12 INVX16 INVX20
INVXL INVX3 INVX4 INVX6 INVX8
Total number of usable inverters: 19
List of unusable inverters:
Total number of unusable inverters: 0
List of identified usable delay cells: DLY1X1 DLY1X4 DLY2X1 DLY2X4 DLY3X1
DLY3X4 DLY4X1 DLY4X4
Total number of identified usable delay cells: 8
List of identified unusable delay cells:
Total number of identified unusable delay cells: 0

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPLF-200      1 Pin '%s' in macro '%s' has no
ANTENNAGAT...
WARNING IMPLF-105      2 The layer '%s' specified in SAMENET
spac...
WARNING IMPFP-3961     2 The techSite '%s' has no related
standar...
WARNING IMPVL-159      958 Pin '%s' of cell '%s' is defined in LEF
...
WARNING TCLCMD-513      1 The software could not find a matching
o....
ERROR   TCLCMD-917      1 Cannot find '%s' that match '%s'
WARNING TCLCMD-1461     2 Skipped unsupported command: %s
*** Message Summary: 966 warning(s), 1 error(s)

innovus 1> Adjusting coreMargin left    to finFet grid (PlacementGrid) :
after adjusting :2.61
Adjusting coreMargin bottom  to finFet grid (PlacementGrid) : after
adjusting :2.61
Adjusting coreMargin right   to finFet grid (PlacementGrid) : after
adjusting :2.61
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Adjusting coreMargin top      to finFet grid (PlacementGrid) : after
adjusting :2.61
Adjusting core size to PlacementGrid : width :16.82 height : 13.05
**WARN: (IMPFP-3961): The techSite 'pad' has no related standard cells
in the LEF/OA library. The calculations for this site type cannot be made
unless standard cell models of this type exist in the LEF/OA library.
Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 290 (derived)
Vertical Layer M2 offset = 290 (derived)
Start create_tracks
Generated pitch 0.29 in Metal8 is different from 0.87 defined in
technology file in unpreferred direction.
innovus 1> **WARN: (IMPFP-3961): The techSite 'pad' has no related
standard cells in the LEF/OA library. The calculations for this site type
cannot be made unless standard cell models of this type exist in the
LEF/OA library. Ignore this warning if the SITE is not used by the
library. Alternatively, remove the SITE definition for the LEF/OA library
to avoid this message.
Type 'man IMPFP-3961' for more detail.
**WARN: (IMPFP-3961): The techSite 'corner' has no related standard
cells in the LEF/OA library. The calculations for this site type cannot
be made unless standard cell models of this type exist in the LEF/OA
library. Ignore this warning if the SITE is not used by the library.
Alternatively, remove the SITE definition for the LEF/OA library to avoid
this message.
Type 'man IMPFP-3961' for more detail.
Horizontal Layer M1 offset = 290 (derived)
Vertical Layer M2 offset = 290 (derived)
Start create_tracks
Generated pitch 0.29 in Metal8 is different from 0.87 defined in
technology file in unpreferred direction.
innovus 1> The ring targets are set to core/block ring wires.
addRing command will consider rows while creating rings.
addRing command will disallow rings to go over rows.
addRing command will ignore shorts while creating rings.

viaInitial starts at Thu Nov 14 16:06:21 2024
viaInitial ends at Thu Nov 14 16:06:21 2024
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1467.7M)
Ring generation is complete.
vias are now being generated.
addRing created 8 wires.
ViaGen created 8 vias, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created    |     Deleted   |
+-----+-----+-----+
| Metal5 |         4        |       NA      |
| Via5   |         8        |         0      |
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
| Metal6 |      4      |      NA      |
+-----+-----+-----+
innovus 1> addStripe will allow jog to connect padcore ring and block
ring.

Stripes will stop at the boundary of the specified area.
When breaking rings, the power planner will consider the existence of
blocks.
Stripes will not extend to closest target.
The power planner will set stripe antenna targets to none (no trimming
allowed).
Stripes will not be created over regions without power planning wires.
The entire stripe set will break at the domain if one of the nets is not
in the domain.
addStripe will break automatically at non-default domains when generating
global stripes over the core area or default domain.
Offset for stripe breaking is set to 0.

Initialize fgc environment(mem: 1472.8M) ... fail and won't use fgc to
check drc(cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1472.8M)
Loading cell geometries (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1472.8M)
Loading wires (cpu: 0:00:00.0, real: 0:00:00.0, peak mem: 1472.8M)
Loading via instances (cpu: 0:00:00.0, real: 0:00:00.0, peak mem:
1472.8M)
Starting stripe generation ...
Non-Default Mode Option Settings :
    NONE
Stripe generation is complete.
vias are now being generated.
addStripe created 7 wires.
ViaGen created 14 vias, deleted 0 via to avoid violation.
+-----+-----+-----+
|   Layer  |     Created    |     Deleted    |
+-----+-----+-----+
|   Via5   |       14        |         0        |
|   Metal6  |        7         |       NA        |
+-----+-----+-----+
innovus 1> **WARN: (IMPSR-4058): Sroute option: blockPinTarget should be
used in conjunction with option: -connect blockPin.
*** Begin SPECIAL ROUTE on Thu Nov 14 16:07:31 2024 ***
SPECIAL ROUTE ran on directory: /home/student/Desktop/21bec1033/mulinnovs
SPECIAL ROUTE ran on machine: cad21 (Linux 4.18.0-425.19.2.el8_7.x86_64
x86_64 2.10Ghz)

Begin option processing ...
srouteConnectPowerBump set to false
routeSelectNet set to "vdd vss"
routeSpecial set to true
srouteBottomLayerLimit set to 1
srouteBottomTargetLayerLimit set to 1
srouteConnectBlockPin set to false
srouteConnectConverterPin set to false
srouteConnectPadPin set to false
srouteConnectStripe set to false
srouteCrossoverViaBottomLayer set to 1
srouteCrossoverViaTopLayer set to 9
srouteFollowCorePinEnd set to 3
srouteFollowPadPin set to false
srouteJogControl set to "preferWithChanges differentLayer"
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
srouteNoViaOnWireShape set to "padring ring stripe blockring blockpin
coverpin blockwire corewire followpin iowire"
sroutePadPinAllPorts set to true
sroutePreserveExistingRoutes set to true
srouteRoutePowerBarPortOnBothDir set to true
srouteStopBlockPin set to "nearestTarget"
srouteTopLayerLimit set to 9
srouteTopTargetLayerLimit set to 9
End option processing: cpu: 0:00:00, real: 0:00:00, peak: 2965.00 megs.

Reading DB technology information...
Finished reading DB technology information.
Reading floorplan and netlist information...
Finished reading floorplan and netlist information.
Read in 19 layers, 9 routing layers, 1 overlap layer
Read in 2 nondefault rules, 0 used
Read in 487 macros, 7 used
Read in 6 components
    6 core components: 6 unplaced, 0 placed, 0 fixed
Read in 9 logical pins
Read in 9 nets
Read in 2 special nets, 2 routed
2 nets selected.

Begin power routing ...
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the vdd net.
Run the globalNetConnect command or change the CPF file to ensure that
the netlist reflects the correct power ground connections. The standard
cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
connection.
**WARN: (IMPSR-1253): Unable to find any standard cell pin connected to
the vss net.
Run the globalNetConnect command or change the CPF file to ensure that
the netlist reflects the correct power ground connections. The standard
cell pins must be defined as 'USE POWER' or 'USE GROUND' for the
connection.
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vss.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vss.
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vss.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vdd.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
CPU time for vdd FollowPin 0 seconds
**WARN: (IMPSR-468): Cannot find any standard cell pin connected to net
vss.
Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a
reference macro for followpin connection, or run globalNetConnect command
or change CPF file to make sure that the netlist reflects the correct
power ground connections. The standard cell pins must be defined as "USE
POWER" or "USE GROUND".
CPU time for vss FollowPin 0 seconds
    Number of Core ports routed: 12
    Number of Followpin connections: 6
End power routing: cpu: 0:00:00, real: 0:00:00, peak: 2971.00 megs.
```

```
Begin updating DB with routing results ...
Updating DB with 0 via definition ...Extracting standard cell pins and
blockage .....
Pin and blockage extraction finished

sroute created 18 wires.
ViaGen created 60 vias, deleted 0 via to avoid violation.
+-----+-----+-----+
| Layer |     Created   |     Deleted   |
+-----+-----+-----+
| Metall |        18      |       NA      |
| Vial   |        12      |        0      |
| Via2   |        12      |        0      |
| Via3   |        12      |        0      |
| Via4   |        12      |        0      |
| Via5   |        12      |        0      |
+-----+-----+-----+
*** placeDesign #1 [begin] : totSession cpu/real = 0:00:58.1/0:08:57.3
(0.1), mem = 1463.3M
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Extracting standard cell pins and blockage .....
Pin and blockage extraction finished
*** Starting placeDesign default flow ***
*** Start deleteBufferTree ***
Info: Detect buffers to remove automatically.
Analyzing netlist ...
Updating netlist

*summary: 0 instances (buffers/inverters) removed
*** Finish deleteBufferTree (0:00:00.1) ***
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
Set Default Input Pin Transition as 1 ps.
**INFO: Analyzing IO path groups for slack adjustment
Effort level <high> specified for reg2reg_tmp.29042 path_group
AAE_INFO: opIsDesignInPostRouteState() is 0
AAE_DB initialization (MEM=1577.35 CPU=0:00:00.0 REAL=0:00:00.0)
#####
# Design Stage: PreRoute
# Design Name: mul2b_netlist
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=1580.36)
*** Calculating scaling factor for maxt libraries using the default
operating condition of each library.
Total number of fetched objects 20
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1729.18 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1729.18 CPU=0:00:00.1
REAL=0:00:00.0)
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Input Pin Transition as 0.1 ps.
Set Default Net Load as 0.5 pF.
**INFO: Pre-place timing setting for timing analysis already disabled
Deleted 0 physical inst (cell - / prefix -).
INFO: #ExclusiveGroups=0
INFO: There are no Exclusive Groups.
*** Starting "NanoPlace(TM) placement v#6 (mem=1703.5M)" ...
*** Build Buffered Sizing Timing Model
(cpu=0:00:00.8 mem=1711.5M) ***
*** Build Virtual Sizing Timing Model
(cpu=0:00:00.9 mem=1711.5M) ***
No user-set net weight.
Net fanout histogram:
2 : 11 (57.9%) nets
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
3          : 6 (31.6%) nets
4      -    14    : 2 (10.5%) nets
15     -    39    : 0 (0.0%) nets
40     -    79    : 0 (0.0%) nets
80     -   159    : 0 (0.0%) nets
160    -   319    : 0 (0.0%) nets
320    -   639    : 0 (0.0%) nets
640    -  1279    : 0 (0.0%) nets
1280   -  2559    : 0 (0.0%) nets
2560   -  5119    : 0 (0.0%) nets
5120+    : 0 (0.0%) nets
Options: timingDriven clkGateAware ignoreScan pinGuide congEffort=auto
gpeffort=medium
**WARN: (IMPSP-9042): Scan chains were not defined, -
place_global_ignore_scan option will be ignored.
Define the scan chains before using this option.
Type 'man IMPSP-9042' for more detail.
#std cell=14 (0 fixed + 14 movable) #buf cell=0 #inv cell=0 #block=0 (0
floating + 0 preplaced)
#ioInst=0 #net=19 #term=53 #term/net=2.79, #fixedIo=0, #floatIo=0,
#fixedPin=0, #floatPin=9
stdCell: 14 single + 0 double + 0 multi
Total standard cell length = 0.0580 (mm), area = 0.0002 (mm^2)
Average module density = 0.690.
Density for the design = 0.690.
    = stdcell_area 200 sites (151 um^2) / alloc_area 290 sites (220
um^2).
Pin Density = 0.1828.
    = total # of pins 53 / total area 290.
==== lastAutoLevel = 4
Clock gating cells determined by native netlist tracing.
Iteration 1: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
            Est. stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
            cpu = 0:00:00.0 real = 0:00:00.0 mem = 1753.8M
Iteration 2: Total net bbox = 0.000e+00 (0.00e+00 0.00e+00)
            Est. stn bbox = 0.000e+00 (0.00e+00 0.00e+00)
            cpu = 0:00:00.0 real = 0:00:00.0 mem = 1753.8M
Iteration 3: Total net bbox = 6.145e-01 (2.50e-01 3.64e-01)
            Est. stn bbox = 6.494e-01 (2.58e-01 3.92e-01)
            cpu = 0:00:00.0 real = 0:00:00.0 mem = 1755.2M
Active setup views:
    worst
Iteration 4: Total net bbox = 7.418e+01 (4.03e+01 3.39e+01)
            Est. stn bbox = 7.873e+01 (4.27e+01 3.60e+01)
            cpu = 0:00:00.0 real = 0:00:00.0 mem = 1755.2M
Iteration 5: Total net bbox = 1.007e+02 (5.87e+01 4.19e+01)
            Est. stn bbox = 1.062e+02 (6.17e+01 4.45e+01)
            cpu = 0:00:00.0 real = 0:00:00.0 mem = 1755.2M
Iteration 6: Total net bbox = 1.502e+02 (9.05e+01 5.97e+01)
            Est. stn bbox = 1.577e+02 (9.50e+01 6.27e+01)
            cpu = 0:00:00.1 real = 0:00:02.0 mem = 1755.2M
*** cost = 1.502e+02 (9.05e+01 5.97e+01) (cpu for global=0:00:00.1)
real=0:00:02.0***
Info: 0 clock gating cells identified, 0 (on average) moved 0/1
Solver runtime cpu: 0:00:00.0 real: 0:00:00.0
Core Placement runtime cpu: 0:00:00.0 real: 0:00:01.0
**WARN: (IMPSP-9025): No scan chain specified/traced.
Type 'man IMPSP-9025' for more detail.
*** Starting refinePlace (0:00:59.9 mem=1747.2M) ***
Total net bbox length = 1.771e+02 (1.015e+02 7.552e+01) (ext = 6.304e+01)
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Move report: Detail placement moves 14 insts, mean move: 2.24 um, max
move: 7.38 um
    Max move on inst (g103_8428): (16.13, 9.33) --> (9.86, 10.44)
    Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 1771.2MB
Summary Report:
Instances move: 14 (out of 14 movable)
Instances flipped: 0
Mean displacement: 2.24 um
Max displacement: 7.38 um (Instance: g103_8428) (16.1325, 9.331) ->
(9.86, 10.44)
    Length: 4 sites, height: 1 rows, site name: gsclib090site, cell
type: NAND2XL
Total net bbox length = 1.569e+02 (7.587e+01 8.101e+01) (ext = 7.038e+01)
Runtime: CPU: 0:00:00.0 REAL: 0:00:00.0 MEM: 1771.2MB
*** Finished refinePlace (0:01:00.0 mem=1771.2M) ***
*** End of Placement (cpu=0:00:01.2, real=0:00:03.0, mem=1771.2M) ***
default core: bins with density > 0.750 = 0.00 % ( 0 / 1 )
Density distribution unevenness ratio = 0.000%
*** Free Virtual Timing Model ...(mem=1771.2M)
Starting IO pin assignment...
The design is not routed. Using placement based method for pin
assignment.
Completed IO pin assignment.
**INFO: Enable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 101.
**WARN: (IMPDC-1629): The default delay limit was set to 101. This is
less than the default of 1000 and may result in inaccurate delay
calculation for nets with a fanout higher than the setting. If needed,
the default delay limit may be adjusted by running the command 'set
delaycal_use_default_delay_limit'.
Set Default Net Delay as 0 ps.
Set Default Net Load as 0 pF.
**INFO: Analyzing IO path groups for slack adjustment
Effort level <high> specified for reg2reg_tmp.29042 path_group
AAE_INFO: opIsDesignInPostRouteState() is 0
#####
# Design Stage: PreRoute
# Design Name: mul2b_netlist
# Design Mode: 90nm
# Analysis Mode: MMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
Start delay calculation (fullDC) (1 T). (MEM=1754.22)
Total number of fetched objects 20
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1805.64 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1805.64 CPU=0:00:00.0
REAL=0:00:00.0)
**INFO: Disable pre-place timing setting for timing analysis
Set Using Default Delay Limit as 1000.
Set Default Net Delay as 1000 ps.
Set Default Net Load as 0.5 pF.
Info: Disable timing driven in postCTS congRepair.

Starting congRepair ...
[NR-eGR] Num Prerouted Nets = 0  Num Prerouted Wires = 0
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
[NR-eGR] Read 19 nets ( ignored 0 )
[NR-eGR] There are 1 clock nets ( 0 with NDR ).
[NR-eGR] Layer group 1: route 19 net(s) in layer range [2, 9]
[NR-eGR] Early Global Route overflow of layer group 1: 0.00% H + 0.00% V.
EstWL: 1.305000e+02um
[NR-eGR] Overflow after Early Global Route 0.00% H + 0.00% V
Early Global Route congestion estimation runtime: 0.01 seconds, mem =
1795.9M
Local HotSpot Analysis: normalized max congestion hotspot area = 0.00,
normalized total congestion hotspot area = 0.00 (area is in unit of 4
std-cell row bins)
Skipped repairing congestion.
[NR-eGR]           Length (um)   Vias
[NR-eGR] -----
[NR-eGR]   Metal1    (1H)        0     44
[NR-eGR]   Metal2    (2V)       70     47
[NR-eGR]   Metal3    (3H)       71     0
[NR-eGR]   Metal4    (4V)        0     0
[NR-eGR]   Metal5    (5H)        0     0
[NR-eGR]   Metal6    (6V)        0     0
[NR-eGR]   Metal7    (7H)        0     0
[NR-eGR]   Metal8    (8V)        0     0
[NR-eGR]   Metal9    (9H)        0     0
[NR-eGR] -----
[NR-eGR]           Total      141     91
[NR-eGR] -----
[NR-eGR] Total half perimeter of net bounding box: 125um
[NR-eGR] Total length: 141um, number of vias: 91
[NR-eGR] -----
[NR-eGR] Total eGR-routed clock nets wire length: 40um, number of vias:
18
[NR-eGR] -----
Early Global Route wiring runtime: 0.00 seconds, mem = 1730.9M
Tdg not successfully initied but do clear! skip clearing
End of congRepair (cpu=0:00:00.0, real=0:00:00.0)
*** Finishing placeDesign default flow ***
***** Total cpu 0:0:2
***** Total real time 0:0:3
**placeDesign ... cpu = 0: 0: 2, real = 0: 0: 3, mem = 1730.9M **
Tdg not successfully initied but do clear! skip clearing

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count Summary
WARNING IMPDC-1629      2 The default delay limit was set to %d.
T...
WARNING IMPSP-9025      1 No scan chain specified/traced.
WARNING IMPSP-9042      1 Scan chains were not defined, -
place_glo...
*** Message Summary: 4 warning(s), 0 error(s)

*** placeDesign #1 [finish] : cpu/real = 0:00:02.1/0:00:03.1 (0.7),
totSession cpu/real = 0:01:00.2/0:09:00.4 (0.1), mem = 1730.9M
innovus 1>
innovus 1> source ccopt.spec
Extracting original clock gating for clk...
clock_tree clk contains 8 sinks and 0 clock gates.
Extracting original clock gating for clk done.
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
The skew group clk/cont was created. It contains 8 sinks and 1 sources.
Checking clock tree convergence...
Checking clock tree convergence done.
innovus 2> ccopt_design -cts
#% Begin ccopt_design (date=11/14 16:10:46, mem=1635.8M)
*** ccopt_design #1 [begin] : totSession cpu/real = 0:01:03.5/0:09:45.2
(0.1), mem = 1731.2M
Runtime...
**INFO: User's settings:
setNanoRouteMode -droutePostRouteSpreadWire           1
setNanoRouteMode -droutePostRouteWidenWireRule
LEFDefaultRouteSpec_gpdk090
setNanoRouteMode -extractThirdPartyCompatible        false
setNanoRouteMode -timingEngine                      {}
setExtractRCMode -engine                           preRoute
setDelayCalMode -engine                          aae
setDelayCalMode -ignoreNetLoad                   false
setPlaceMode -place_design_floorplan_mode       false
setPlaceMode -place_detail_check_route          false
setPlaceMode -place_detail_preserve_routing     true
setPlaceMode -place_detail_remove_affected_routing false
setPlaceMode -place_detail_swap_eeq_cells       false
setPlaceMode -place_global_clock_gate_aware     true
setPlaceMode -place_global_cong_effort          auto
setPlaceMode -place_global_ignore_scan          true
setPlaceMode -place_global_ignore_spare         false
setPlaceMode -place_global_module_aware_spare   false
setPlaceMode -place_global_place_io_pins        true
setPlaceMode -place_global_reorder_scan         true
setPlaceMode -powerDriven                       false
setPlaceMode -timingDriven                      true
setRouteMode -earlyGlobalHonorMsvRouteConstraint false
setRouteMode -earlyGlobalRoutePartitionPinGuide  true

(ccopt_design): CTS Engine: auto. Used Spec: pre-existing CCOPT spec.
Placement constraints of type 'region' or 'fence' will not be downgraded
to 'guide' because the property change_fences_to_guides has been set to
false.
CCOpt::Phase::Initialization...
Check Prerequisites...
Leaving CCOpt scope - CheckPlace...
Begin checking placement ... (start mem=1731.2M, init mem=1731.2M)
*info: Placed = 14
*info: Unplaced = 0
Placement Density:68.97%(151/220)
Placement Density (including fixed std cells):68.97%(151/220)
Finished checkPlace (total: cpu=0:00:00.0, real=0:00:00.0; vio checks:
cpu=0:00:00.0, real=0:00:00.0; mem=1731.2M)
Leaving CCOpt scope - CheckPlace done. (took cpu=0:00:00.0
real=0:00:00.0)
Innovus will update I/O latencies
Found 0 ideal nets, 0 pins with transition annotations, 0 instances with
delay annotations, 0 nets with delay annotations, refer to logv for
details.

Check Prerequisites done. (took cpu=0:00:00.0 real=0:00:00.0)
CCOpt::Phase::Initialization done. (took cpu=0:00:00.0 real=0:00:00.0)
Executing ccopt post-processing.
Synthesizing clock trees with CCOpt...
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
*** CTS #1 [begin] (ccopt_design #1) : totSession cpu/real =
0:01:03.5/0:09:45.3 (0.1), mem = 1731.2M
CCOpt::Phase::PreparingToBalance...
Leaving CCOpt scope - Initializing power interface...
Leaving CCOpt scope - Initializing power interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
Found 0 advancing pin insertion delay (0.000% of 8 clock tree sinks)
Found 0 delaying pin insertion delay (0.000% of 8 clock tree sinks)
Leaving CCOpt scope - optDesignGlobalRouteStep...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
[NR-eGR] Started Early Global Route kernel ( Curr Mem: 1731.22 MB )
[NR-eGR] Num Prerouted Nets = 0  Num Prerouted Wires = 0
[NR-eGR] Read 19 nets ( ignored 0 )
[NR-eGR] There are 1 clock nets ( 0 with NDR ).
[NR-eGR] Layer group 1: route 19 net(s) in layer range [2, 9]
[NR-eGR] Early Global Route overflow of layer group 1: 0.00% H + 0.00% V.
EstWL: 1.305000e+02um
[NR-eGR] Overflow after Early Global Route 0.00% H + 0.00% V
[NR-eGR]           Length (um)   Vias
[NR-eGR] -----
[NR-eGR]   Metal1  (1H)          0    44
[NR-eGR]   Metal2  (2V)         70    47
[NR-eGR]   Metal3  (3H)         71    0
[NR-eGR]   Metal4  (4V)          0    0
[NR-eGR]   Metal5  (5H)          0    0
[NR-eGR]   Metal6  (6V)          0    0
[NR-eGR]   Metal7  (7H)          0    0
[NR-eGR]   Metal8  (8V)          0    0
[NR-eGR]   Metal9  (9H)          0    0
[NR-eGR] -----
[NR-eGR]   Total            141    91
[NR-eGR] -----
[NR-eGR] Total half perimeter of net bounding box: 125um
[NR-eGR] Total length: 141um, number of vias: 91
[NR-eGR] -----
[NR-eGR] Total eGR-routed clock nets wire length: 40um, number of vias:
18
[NR-eGR] -----
[NR-eGR] Finished Early Global Route kernel ( CPU: 0.01 sec, Real: 0.01
sec, Curr Mem: 1731.22 MB )
Leaving CCOpt scope - optDesignGlobalRouteStep done. (took cpu=0:00:00.0
real=0:00:00.0)
Legalization setup...
Using cell based legalization.
Initializing placement interface...
  Use check_library -place or consult logv if problems occur.
  Leaving CCOpt scope - Initializing placement interface...
  Leaving CCOpt scope - Initializing placement interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
Initializing placement interface done.
Leaving CCOpt scope - Cleaning up placement interface...
Leaving CCOpt scope - Cleaning up placement interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
Leaving CCOpt scope - Initializing placement interface...
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Leaving CCOpt scope - Initializing placement interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
Legalization setup done. (took cpu=0:00:00.0 real=0:00:00.0)
Validating CTS configuration...
Checking module port directions...
Checking module port directions done. (took cpu=0:00:00.0 real=0:00:00.0)
Non-default CCOpt properties:
  Public non-default CCOpt properties:
    route_type is set for at least one object
    target_max_trans_sdc is set for at least one object
  No private non-default CCOpt properties
Route type trimming info:
  No route type modifications were made.
**WARN: (IMPCCOPT-1183): The library has no usable balanced buffers
for power domain auto-default, while balancing clock_tree clk. If this is
not intended behavior, you can specify a list of lib_cells to use with
the buffer_cells property.
**WARN: (IMPCCOPT-1184): The library has no usable balanced inverters
for power domain auto-default, while balancing clock_tree clk. If this is
not intended behavior, you can specify a list of lib_cells to use with
the inverter_cells property.
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
**ERROR: (IMPCCOPT-1135): CTS found neither inverters nor buffers while
balancing clock_tree clk. CTS cannot continue.
Type 'man IMPCCOPT-1135' for more detail.
Clock tree balancer configuration for clock_tree clk:
Non-default CCOpt properties:
  Public non-default CCOpt properties:
    route_type (leaf): default_route_type_leaf (default: default)
    route_type (top): default_route_type_nonleaf (default: default)
    route_type (trunk): default_route_type_nonleaf (default: default)
  No private non-default CCOpt properties
```

Logic Sizing Table:

Cell	Instance count	Source	Eligible library cells
(empty table)			

```
Clock tree balancer configuration for skew_group clk/cont:
  Sources:                  pin clk
  Total number of sinks:     8
  Delay constrained sinks:  8
  Constrains:               default
  Non-leaf sinks:           0
  Ignore pins:              0
  Timing corner maxd:setup.late:
    Skew target:             0.000ns
  Primary reporting skew groups are:
    skew_group clk/cont with 8 clock sinks

Clock DAG stats initial state:
  cell counts      : b=0, i=0, icg=0, dcg=0, l=0, total=0
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
sink counts      : regular=8, enable_latch=0, load_capacitance=0,
antenna=0, node_sink=0, total=8
misc counts      : r=1, pp=0
cell areas       : b=0.000um^2, i=0.000um^2, icg=0.000um^2,
dcg=0.000um^2, l=0.000um^2, total=0.000um^2
hp wire lengths : top=0.000um, trunk=0.000um, leaf=0.000um,
total=0.000um
No ideal or dont_touch nets found in the clock tree
No dont_touch hnets found in the clock tree
No dont_touch hpins found in the clock network.
Checking for illegal sizes of clock logic instances...
Checking for illegal sizes of clock logic instances done. (took
cpu=0:00:00.0 real=0:00:00.0)
Validating CTS configuration done. (took cpu=0:00:00.0 real=0:00:00.0)

CCOpt configuration status: cannot run ccopt_design.
Check the log for details of problem(s) found:

-----
Design configuration problems
-----
One or more clock trees have configuration problems
-----

Clock tree configuration problems:

-----
Clock tree    Problem
-----
clk          Could not determine drivers to use
-----


CCOpt::Phase::PreparingToBalance done. (took cpu=0:00:00.1
real=0:00:00.1)
Runtime done. (took cpu=0:00:00.1 real=0:00:00.1)
Runtime Summary
=====
Clock Runtime: (63%) Core CTS           0.06 (Init 0.06, Construction
0.00, Implementation 0.00, eGRPC 0.00, PostConditioning 0.00, Other 0.00)
Clock Runtime: (0%) CTS services        0.00 (RefinePlace 0.00,
EarlyGlobalClock 0.00, NanoRoute 0.00, ExtractRC 0.00, TimingAnalysis
0.00)
Clock Runtime: (36%) Other CTS          0.03 (Init 0.03, CongRepair/EGR-
DP 0.00, TimingUpdate 0.00, Other 0.00)
Clock Runtime: (100%) Total             0.09

Leaving CCOpt scope - Cleaning up placement interface...
Leaving CCOpt scope - Cleaning up placement interface done. (took
cpu=0:00:00.0 real=0:00:00.0)
**ERROR: 3
*** CTS #1 [finish] (ccopt_design #1) : cpu/real = 0:00:00.1/0:00:00.1
(1.0), totSession cpu/real = 0:01:03.6/0:09:45.4 (0.1), mem = 1731.3M
**ERROR: (IMPCCOPT-2196): Cannot run ccopt_design because the command
prerequisites were not met. Review the previous error messages for more
details about the failure.

*** Summary of all messages that are not suppressed in this session:
Severity ID          Count   Summary
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
ERROR      IMPCCOPT-1135          1  CTS found neither inverters nor buffers
...
ERROR      IMPCCOPT-2196          1  Cannot run ccopt_design because the
comm...
WARNING    IMPCCOPT-1183          1  The library has no usable balanced %ss
f...
WARNING    IMPCCOPT-1184          1  The library has no usable balanced %ss
f...
*** Message Summary: 2 warning(s), 2 error(s)

*** ccopt_design #1 [finish] : cpu/real = 0:00:00.1/0:00:00.1 (1.0),
totSession cpu/real = 0:01:03.6/0:09:45.4 (0.1), mem = 1731.3M
#% End ccopt_design (date=11/14 16:10:46, total cpu=0:00:00.1,
real=0:00:00.0, peak res=1644.2M, current mem=1644.2M)

innovus 3> saveDesign DBS/cts.encl
#% Begin save design ... (date=11/14 16:11:11, mem=1647.5M)
% Begin Save ccopt configuration ... (date=11/14 16:11:11, mem=1647.5M)
% End Save ccopt configuration ... (date=11/14 16:11:11, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1648.1M, current mem=1648.1M)
% Begin Save netlist data ... (date=11/14 16:11:11, mem=1648.1M)
Writing Binary DB to DBS/cts.encl.dat/mul2b_netlist.v.bin in single-
threaded mode...
% End Save netlist data ... (date=11/14 16:11:11, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1648.2M, current mem=1648.2M)
Saving symbol-table file ...
Saving congestion map file
DBS/cts.encl.dat/mul2b_netlist.route.congmap.gz ...
% Begin Save AAE data ... (date=11/14 16:11:11, mem=1648.2M)
Saving AAE Data ...
% End Save AAE data ... (date=11/14 16:11:11, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1648.2M, current mem=1648.2M)
Saving preference file DBS/cts.encl.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=11/14 16:11:11, mem=1650.2M)
Saving floorplan file ...
% End Save floorplan data ... (date=11/14 16:11:11, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1650.3M, current mem=1650.3M)
Saving Drc markers ...
... No Drc file written since there is no markers found.
% Begin Save placement data ... (date=11/14 16:11:11, mem=1650.3M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=11/14 16:11:11, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1650.6M, current mem=1650.6M)
% Begin Save routing data ... (date=11/14 16:11:11, mem=1650.6M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1734.0M) ***
% End Save routing data ... (date=11/14 16:11:11, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1650.8M, current mem=1650.8M)
Saving property file DBS/cts.encl.dat/mul2b_netlist.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1737.0M) ***
% Begin Save power constraints data ... (date=11/14 16:11:11,
mem=1652.1M)
% End Save power constraints data ... (date=11/14 16:11:11, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1652.1M, current mem=1652.1M)
Generated self-contained design cts.encl.dat
#% End save design ... (date=11/14 16:11:12, total cpu=0:00:00.2,
real=0:00:01.0, peak res=1681.0M, current mem=1654.6M)
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
*** Message Summary: 0 warning(s), 0 error(s)

0
innovus 4> #WARNING (NRIF-91) Option setNanoRouteMode -
routeTopRoutingLayer is obsolete. It will continue to work for the
current release. To ensure compatibility with future releases, use option
setDesignMode -topRoutingLayer instead.
#WARNING (NRIF-90) Option setNanoRouteMode -routeBottomRoutingLayer is
obsolete. It will continue to work for the current release. To ensure
compatibility with future releases, use option setDesignMode -
bottomRoutingLayer instead.
#routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory =
1656.41 (MB), peak = 1680.97 (MB)
AAE_INFO: Pre Route call back at the beginning of routeDesign
#**INFO: setDesignMode -flowEffort standard
#**INFO: setDesignMode -powerEffort none
#WARNING (NRIG-96) Selected single pass global detail route "-
globalDetail". Clock eco and post optimizations will not be run. See "man
NRIG-96" for more details.
#WARNING (NRIG-144) Cannot combine -viaOpt with -globalDetail option. The
-viaOpt will be ignored.
**INFO: User settings:
setNanoRouteMode -drouteEndIteration           1
setNanoRouteMode -droutePostRouteSpreadWire     1
setNanoRouteMode -droutePostRouteWidenWireRule
LEFDefaultRouteSpec_gpdk090
setNanoRouteMode -extractThirdPartyCompatible   false
setNanoRouteMode -routeBottomRoutingLayer        1
setNanoRouteMode -routeTopRoutingLayer          9
setNanoRouteMode -routeWithSiDriven            false
setNanoRouteMode -routeWithTimingDriven        false
setNanoRouteMode -timingEngine                 {}
setExtractRCMode -engine                      preRoute
setDelayCalMode -engine                      aae
setDelayCalMode -ignoreNetLoad                false

#**INFO: multi-cut via swapping will not be performed after routing.
#**INFO: All auto set options tuned by routeDesign will be restored to
their original settings on command completion.
Begin checking placement ... (start mem=1771.5M, init mem=1771.5M)
*info: Placed = 14
*info: Unplaced = 0
Placement Density:68.97%(151/220)
Placement Density (including fixed std cells):68.97%(151/220)
Finished checkPlace (total: cpu=0:00:00.0, real=0:00:00.0; vio checks:
cpu=0:00:00.0, real=0:00:00.0; mem=1771.5M)

changeUseClockNetStatus Option : -noFixedNetWires
*** Changed status on (0) nets in Clock.
*** End changeUseClockNetStatus (cpu=0:00:00.0, real=0:00:00.0,
mem=1771.5M) ***

globalDetailRoute

#Start globalDetailRoute on Thu Nov 14 16:11:24 2024
#
#WARNING (NRIG-1303) The congestion map does not match the GCELL grid.
Clearing the map.
#Invoke dbWirePreImport deleteTR=1 convert_unrouted=0 selected_only=0
(nr_selected_net=0)
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
#num needed restored net=0
#need_extraction net=0 (total=22)
#WARNING (NRDB-2005) SPECIAL_NET vdd has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#WARNING (NRDB-2005) SPECIAL_NET vss has special wires but no definitions
for instance pins or top level pins. This will cause routability problems
later.
#NanoRoute Version 21.15-s110_1 NR220912-2004/21_15-UB
#Total number of trivial nets (e.g. < 2 pins) = 3 (skipped).
#Total number of routable nets = 19.
#Total number of nets in the design = 22.
#19 routable nets do not have any wires.
#19 nets will be global routed.
#Start routing data preparation on Thu Nov 14 16:11:24 2024
#
#Minimum voltage of a net in the design = 0.000.
#Maximum voltage of a net in the design = 1.100.
#Voltage range [0.000 - 1.100] has 20 nets.
#Voltage range [0.900 - 1.100] has 1 net.
#Voltage range [0.000 - 0.000] has 1 net.
#Build and mark too close pins for the same net.
#Rebuild pin access data for design.
#Initial pin access analysis.
#Detail pin access analysis.
# Metal1      H Track-Pitch = 0.29000   Line-2-Via Pitch = 0.25500
# Metal2      V Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal3      H Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal4      V Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal5      H Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal6      V Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal7      H Track-Pitch = 0.29000   Line-2-Via Pitch = 0.28500
# Metal8      V Track-Pitch = 0.87000   Line-2-Via Pitch = 0.85000
# Metal9      H Track-Pitch = 0.87000   Line-2-Via Pitch = 0.85000
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1663.12 (MB),
peak = 1696.09 (MB)
#Regenerating Ggrids automatically.
#Auto generating G-grids with size=15 tracks, using layer Metal3's pitch
= 0.29000.
#Using automatically generated G-grids.
#(check_and_prepare_match_target_file) no match_target_file in
constraint. quit
#Done routing data preparation.
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1667.15 (MB),
peak = 1696.09 (MB)
#
#Finished routing data preparation on Thu Nov 14 16:11:25 2024
#
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 9.92 (MB)
#Total memory = 1667.15 (MB)
#Peak memory = 1696.09 (MB)
#
#
#Start global routing on Thu Nov 14 16:11:25 2024
#
#
#Start global routing initialization on Thu Nov 14 16:11:25 2024
#
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
#Number of eco nets is 0
#
#Start global routing data preparation on Thu Nov 14 16:11:25 2024
#
#Start routing resource analysis on Thu Nov 14 16:11:25 2024
#
#Routing resource analysis is done on Thu Nov 14 16:11:25 2024
#
# Resource Analysis:
#
#          Routing  #Avail      #Track      #Total      %Gcell
#  Layer     Direction   Track   Blocked   Gcell   Blocked
# -----
#  Metal1      H        23       40         20    20.00%
#  Metal2      V        62       14         20    0.00%
#  Metal3      H        52       11         20    0.00%
#  Metal4      V        63       13         20    0.00%
#  Metal5      H        40       23         20    0.00%
#  Metal6      V        36       40         20    0.00%
#  Metal7      H        63        0         20    0.00%
#  Metal8      V        24        0         20    0.00%
#  Metal9      H        20        0         20    0.00%
# -----
#  Total           384      22.70%      180    2.22%
#
#
#
#
#Global routing data preparation is done on Thu Nov 14 16:11:25 2024
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1667.15 (MB),
peak = 1696.09 (MB)
#
#
#Global routing initialization is done on Thu Nov 14 16:11:25 2024
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1667.15 (MB),
peak = 1696.09 (MB)
#
#start global routing iteration 1...
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1669.29 (MB),
peak = 1696.09 (MB)
#
#start global routing iteration 2...
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1669.29 (MB),
peak = 1696.09 (MB)
#
#
#Total number of trivial nets (e.g. < 2 pins) = 3 (skipped).
#Total number of routable nets = 19.
#Total number of nets in the design = 22.
#
#19 routable nets have routed wires.
#
#Routed nets constraints summary:
#-----
#      Rules    Unconstrained
#-----
#      Default      19
#-----
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```

#          Total          19
#-----
#
# Routing constraints summary of the whole design:
#-----
#          Rules    Unconstrained
#-----
#          Default          19
#-----
#          Total          19
#-----
#
#
# Congestion Analysis: (blocked Gcells are excluded)
#
#          OverCon
#          #Gcell  %Gcell
# Layer      (1)  OverCon
# -----
#  Metal1      0(0.00%) (0.00%)
#  Metal2      0(0.00%) (0.00%)
#  Metal3      0(0.00%) (0.00%)
#  Metal4      0(0.00%) (0.00%)
#  Metal5      0(0.00%) (0.00%)
#  Metal6      0(0.00%) (0.00%)
#  Metal7      0(0.00%) (0.00%)
#  Metal8      0(0.00%) (0.00%)
#  Metal9      0(0.00%) (0.00%)
# -----
#  Total       0(0.00%) (0.00%)
#
# The worst congested Gcell overcon (routing demand over resource in
# number of tracks) = 1
# Overflow after GR: 0.00% H + 0.00% V
#
# Hotspot report including placement blocked areas
[hotspot] +-----+-----+-----+
-----+
[hotspot] |     layer     | max hotspot | total hotspot |
hotspot bbox           |
[hotspot] +-----+-----+-----+
-----+
[hotspot] |  Metal1(H)  |           | 0.00 | 0.00 |
(none)                   |           |           |
[hotspot] |  Metal2(V)  |           | 0.00 | 0.00 |
(none)                   |           |           |
[hotspot] |  Metal3(H)  |           | 0.00 | 0.00 |
(none)                   |           |           |
[hotspot] |  Metal4(V)  |           | 0.00 | 0.00 |
(none)                   |           |           |
[hotspot] |  Metal5(H)  |           | 0.00 | 0.00 |
(none)                   |           |           |
[hotspot] |  Metal6(V)  |           | 0.00 | 0.00 |
(none)                   |           |           |
[hotspot] |  Metal7(H)  |           | 0.00 | 0.00 |
(none)                   |           |           |
[hotspot] |  Metal8(V)  |           | 0.00 | 0.00 |
(none)                   |           |           |
[hotspot] |  Metal9(H)  |           | 0.00 | 0.00 |
(none)                   |           |           |

```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
[hotspot] +-----+-----+-----+-----+
-----+-----+-----+-----+
[hotspot] |      worst      |          0.00 |          0.00 |
|
[hotspot] +-----+-----+-----+-----+
-----+-----+
[hotspot] |    all layers    |          0.00 |          0.00 |
|
[hotspot] +-----+-----+-----+-----+
-----+
Local HotSpot Analysis (blockage included) (3d): normalized congestion
max/total hotspot area = 0.00/0.00 (area is in unit of 4 std-cell row
bins)
#Complete Global Routing.
#Total wire length = 119 um.
#Total half perimeter of net bounding box = 144 um.
#Total wire length on LAYER Metal1 = 0 um.
#Total wire length on LAYER Metal2 = 63 um.
#Total wire length on LAYER Metal3 = 57 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 71
#Up-Via Summary (total 71):
#
#-----
# Metall      43
# Metal2     28
#-----
#                  71
#
#Max overcon = 0 track.
#Total overcon = 0.00%.
#Worst layer Gcell overcon rate = 0.00%.
#
#Global routing statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 2.43 (MB)
#Total memory = 1669.58 (MB)
#Peak memory = 1696.09 (MB)
#
#Finished global routing on Thu Nov 14 16:11:25 2024
#
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1669.58 (MB),
peak = 1696.09 (MB)
#Start Track Assignment.
#Done with 13 horizontal wires in 1 hboxes and 12 vertical wires in 1
hboxes.
#Done with 0 horizontal wires in 1 hboxes and 1 vertical wires in 1
hboxes.
#Done with 1 horizontal wires in 1 hboxes and 1 vertical wires in 1
hboxes.
#
#Track assignment summary:
# layer   (wire length)   (overlap)   (long ovlp)   (with obs/pg/clk)
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
#-----
# Metall1      0.00  0.00%   0.00%   0.00%
# Metall2      57.95 0.00%   0.00%   0.00%
# Metall3      52.00 0.00%   0.00%   0.00%
# Metall4      0.00  0.00%   0.00%   0.00%
# Metall5      0.00  0.00%   0.00%   0.00%
# Metall6      0.00  0.00%   0.00%   0.00%
# Metall7      0.00  0.00%   0.00%   0.00%
# Metall8      0.00  0.00%   0.00%   0.00%
# Metall9      0.00  0.00%   0.00%   0.00%
#-----
# All          109.95 0.00%   0.00%   0.00%
#Complete Track Assignment.
#Total wire length = 109 um.
#Total half perimeter of net bounding box = 144 um.
#Total wire length on LAYER Metall1 = 0 um.
#Total wire length on LAYER Metal2 = 56 um.
#Total wire length on LAYER Metal3 = 53 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 71
#Up-Via Summary (total 71):
#
#-----
# Metall1      43
# Metall2      28
#-----
#                      71
#
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1669.69 (MB),
peak = 1696.09 (MB)
#
#Routing data preparation, pin analysis, global routing and track
assignment statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 12.46 (MB)
#Total memory = 1669.69 (MB)
#Peak memory = 1696.09 (MB)
#
#Start Detail Routing..
#start initial detail routing ...
#    number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1671.00 (MB),
peak = 1696.09 (MB)
#Complete Detail Routing.
#Total wire length = 141 um.
#Total half perimeter of net bounding box = 144 um.
#Total wire length on LAYER Metall1 = 22 um.
#Total wire length on LAYER Metal2 = 80 um.
#Total wire length on LAYER Metal3 = 39 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 67
#Up-Via Summary (total 67):
#
#-----
# Metall          48
# Metal2         19
#-----
#                  67
#
#Total number of DRC violations = 0
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 1.31 (MB)
#Total memory = 1671.00 (MB)
#Peak memory = 1696.09 (MB)
#
#Start Post Route wire spreading..
#
#Start DRC checking..
#   number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1671.08 (MB),
peak = 1696.09 (MB)
#CELL VIEW mul2b_netlist,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#
#Start data preparation for wire spreading...
#
#Data preparation is done on Thu Nov 14 16:11:25 2024
#
#
#Start Post Route Wire Spread.
#Done with 0 horizontal wires in 1 hboxes and 0 vertical wires in 1
hboxes.
#Complete Post Route Wire Spread.
#
#Total wire length = 141 um.
#Total half perimeter of net bounding box = 144 um.
#Total wire length on LAYER Metal1 = 22 um.
#Total wire length on LAYER Metal2 = 80 um.
#Total wire length on LAYER Metal3 = 39 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 67
#Up-Via Summary (total 67):
#
#-----
# Metall          48
# Metal2         19
#-----
#                  67
#
#Start DRC checking..
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 67
#Up-Via Summary (total 67):
#
#-----
# Metall          48
# Metal2         19
#-----
#                  67
#
#      number of violations = 0
#cpu time = 00:00:00, elapsed time = 00:00:00, memory = 1679.65 (MB),
peak = 1696.09 (MB)
#CELL_VIEW mul2b_netlist,init has no DRC violation.
#Total number of DRC violations = 0
#Total number of process antenna violations = 0
#Total number of net violated process antenna rule = 0
#Post Route wire spread is done.
#Total wire length = 141 um.
#Total half perimeter of net bounding box = 144 um.
#Total wire length on LAYER Metal1 = 22 um.
#Total wire length on LAYER Metal2 = 80 um.
#Total wire length on LAYER Metal3 = 39 um.
#Total wire length on LAYER Metal4 = 0 um.
#Total wire length on LAYER Metal5 = 0 um.
#Total wire length on LAYER Metal6 = 0 um.
#Total wire length on LAYER Metal7 = 0 um.
#Total wire length on LAYER Metal8 = 0 um.
#Total wire length on LAYER Metal9 = 0 um.
#Total number of vias = 67
#Up-Via Summary (total 67):
#
#-----
# Metall          48
# Metal2         19
#-----
#                  67
#
#      no debugging net set
#
#detailRoute statistics:
#Cpu time = 00:00:00
#Elapsed time = 00:00:00
#Increased memory = 2.80 (MB)
#Total memory = 1675.36 (MB)
#Peak memory = 1696.09 (MB)
#Number of warnings = 2
#Total number of warnings = 9
#Number of fails = 0
#Total number of fails = 0
#Complete detailRoute on Thu Nov 14 16:11:25 2024
#
#Default setup view is reset to worst.
AAE_INFO: Post Route call back at the end of routeDesign
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
#routeDesign: cpu time = 00:00:01, elapsed time = 00:00:01, memory =
1675.36 (MB), peak = 1696.09 (MB)
*** Message Summary: 0 warning(s), 0 error(s)

innovus 4> **WARN: (IMPSP-5217): addFiller command is running on a
postRoute database. It is recommended to be followed by ecoRoute -target
command to make the DRC clean.
Type 'man IMPSP-5217' for more detail.
*INFO: Adding fillers to top-module.
*INFO: Added 0 filler inst (cell FILL64 / prefix FILLER).
*INFO: Added 0 filler inst (cell FILL32 / prefix FILLER).
*INFO: Added 4 filler insts (cell FILL16 / prefix FILLER).
*INFO: Added 1 filler inst (cell FILL8 / prefix FILLER).
*INFO: Added 3 filler insts (cell FILL4 / prefix FILLER).
*INFO: Added 2 filler insts (cell FILL2 / prefix FILLER).
*INFO: Added 2 filler insts (cell FILL1 / prefix FILLER).
*INFO: Total 12 filler insts added - prefix FILLER (CPU: 0:00:00.0).
For 12 new insts, innovus 4> AAE DB initialization (MEM=1802.62
CPU=0:00:00.0 REAL=0:00:00.0)
*** timeDesign #1 [begin] : totSession cpu/real = 0:01:09.7/0:10:51.4
(0.1), mem = 1802.6M
Setting timing_disable_library_data_to_data_checks to 'true'.
Setting timing_disable_user_data_to_data_checks to 'true'.
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1791.6M)
Extraction called for design 'mul2b_netlist' of instances=26 and nets=22
using extraction engine 'preRoute'.
**WARN: (IMPEXT-3530): The process node is not set. Use the command
setDesignMode -process <process node> prior to extraction for maximum
accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design mul2b_netlist.
RC Extraction called in multi-corner(1) mode.
RCMode: PreRoute
    RC Corner Indexes          0
    Capacitance Scaling Factor : 1.00000
    Resistance Scaling Factor : 1.00000
    Clock Cap. Scaling Factor : 1.00000
    Clock Res. Scaling Factor : 1.00000
    Shrink Factor             : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0
MEM: 1791.625M)
Starting delay calculation for Setup views
AAE_INFO: opIsDesignInPostRouteState() is 1
AAE_INFO: deleting AAE DB due to opIsDesignInPostRouteState() is changed
...
AAE DB initialization (MEM=1806.45 CPU=0:00:00.0 REAL=0:00:00.0)
#####
# Design Stage: PostRoute
# Design Name: mul2b_netlist
# Design Mode: 90nm
# Analysis Mode: MMMC OCV
# Parasitics Mode: No SPEF/RCDB
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
# Signoff Settings: SI Off
#####
##### Start delay calculation (fullDC) (1 T). (MEM=1806.45)
Total number of fetched objects 20
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1878.49 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1878.49 CPU=0:00:00.0
REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0
totSessionCpu=0:01:10 mem=1878.5M)

-----
          timeDesign Summary
-----

Setup views included:
worst

+-----+-----+-----+
|      Setup mode     |    all    | reg2reg | default |
+-----+-----+-----+
|          WNS (ns):|  8.587  |  9.083  |  8.587  |
|          TNS (ns):|  0.000  |  0.000  |  0.000  |
| Violating Paths:|    0    |    0    |    0    |
|      All Paths:  |   13   |    5   |    8   |
+-----+-----+-----+

+-----+-----+-----+
|           |          Real          |          Total          | |
|      DRVs       |          |          |          |
|           |  Nr nets(terms)  | Worst Vio | Nr nets(terms) |
+-----+-----+-----+
|  max_cap     |  0 (0)    |  0.000   |  0 (0)   |
|  max_tran    |  0 (0)    |  0.000   |  0 (0)   |
|  max_fanout  |  0 (0)    |    0     |  0 (0)   |
|  max_length  |  0 (0)    |    0     |  0 (0)   |
+-----+-----+-----+

Density: 68.966%
(100.000% with Fillers)
Routing Overflow: 0.00% H and 0.00% V

-----
Reported timing to dir timingReports
Total CPU time: 0.25 sec
Total Real time: 1.0 sec
Total Memory Usage: 1844.910156 Mbytes
*** timeDesign #1 [finish] : cpu/real = 0:00:00.3/0:00:00.8 (0.3),
totSession cpu/real = 0:01:10.0/0:10:52.2 (0.1), mem = 1844.9M
innovus 4> *** timeDesign #2 [begin] : totSession cpu/real =
0:01:10.4/0:10:57.2 (0.1), mem = 1855.1M
Start to check current routing status for nets...
All nets are already routed correctly.
End to check current routing status for nets (mem=1810.4M)
Starting delay calculation for Hold views
AAE_INFO: opIsDesignInPostRouteState() is 1
#####
## Design Stage: PostRoute
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
# Design Name: mul2b_netlist
# Design Mode: 90nm
# Analysis Mode: MMC OCV
# Parasitics Mode: No SPEF/RCDB
# Signoff Settings: SI Off
#####
#####
Start delay calculation (fullDC) (1 T). (MEM=1823.45)
*** Calculating scaling factor for mint libraries using the default
operating condition of each library.
Total number of fetched objects 20
AAE_INFO: Total number of nets for which stage creation was skipped for
all views 0
End delay calculation. (MEM=1875.61 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=1875.61 CPU=0:00:00.0
REAL=0:00:00.0)
Turning on fast DC mode.
*** Done Building Timing Graph (cpu=0:00:00.1 real=0:00:00.0
totSessionCpu=0:01:11 mem=1883.6M)

-----
          timeDesign Summary
-----

Hold views included:
  best

+-----+-----+-----+
| Hold mode | all | reg2reg | default |
+-----+-----+-----+
|           WNS (ns):| -0.085 | -0.085 | 0.000 |
|           TNS (ns):| -0.197 | -0.197 | 0.000 |
| Violating Paths:| 4 | 4 | 0 |
| All Paths:| 5 | 5 | 0 |
+-----+-----+-----+

Density: 68.966%
(100.000% with Fillers)
Routing Overflow: 0.00% H and 0.00% V

-----
Reported timing to dir timingReports
Total CPU time: 0.23 sec
Total Real time: 0.0 sec
Total Memory Usage: 1797.882812 Mbytes
*** timeDesign #2 [finish] : cpu/real = 0:00:00.2/0:00:00.2 (1.0),
totSession cpu/real = 0:01:10.6/0:10:57.4 (0.1), mem = 1797.9M
innovus 4> Performing RC Extraction ...
Extraction called for design 'mul2b_netlist' of instances=26 and nets=22
using extraction engine 'preRoute'.
**WARN: (IMPEXT-3530): The process node is not set. Use the command
setDesignMode -process <process node> prior to extraction for maximum
accuracy and optimal automatic threshold setting.
Type 'man IMPEXT-3530' for more detail.
PreRoute RC Extraction called for design mul2b_netlist.
RC Extraction called in multi-corner(1) mode.
RCMode: PreRoute
      RC Corner Indexes          0
Capacitance Scaling Factor    : 1.00000
Resistance Scaling Factor     : 1.00000
Clock Cap. Scaling Factor     : 1.00000
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
Clock Res. Scaling Factor      : 1.00000
Shrink Factor                 : 1.00000
PreRoute extraction is honoring NDR/Shielding/ExtraSpace for clock nets.
Using capacitance table file ...
Updating RC grid for preRoute extraction ...
Initializing multi-corner capacitance tables ...
Initializing multi-corner resistance tables ...
PreRoute RC Extraction DONE (CPU Time: 0:00:00.0  Real Time: 0:00:00.0
MEM: 1806.188M)
innovus 4> Writing Netlist "mul2b_netlist.v" ...
innovus 4> #% Begin save design ... (date=11/14 16:12:12, mem=1694.1M)
% Begin Save ccopt configuration ... (date=11/14 16:12:12, mem=1694.1M)
% End Save ccopt configuration ... (date=11/14 16:12:12, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1694.4M, current mem=1694.4M)
% Begin Save netlist data ... (date=11/14 16:12:12, mem=1694.4M)
Writing Binary DB to mul2b_netlist.dat/mul2b_netlist.v.bin in single-
threaded mode...
% End Save netlist data ... (date=11/14 16:12:13, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1694.6M, current mem=1694.6M)
Saving symbol-table file ...
Saving congestion map file
mul2b_netlist.dat/mul2b_netlist.route.congmap.gz ...
% Begin Save AAE data ... (date=11/14 16:12:13, mem=1694.8M)
Saving AAE Data ...
% End Save AAE data ... (date=11/14 16:12:13, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1694.8M, current mem=1694.8M)
Saving preference file mul2b_netlist.dat/gui.pref.tcl ...
Saving mode setting ...
Saving global file ...
% Begin Save floorplan data ... (date=11/14 16:12:13, mem=1695.3M)
Saving floorplan file ...
% End Save floorplan data ... (date=11/14 16:12:13, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1695.3M, current mem=1695.3M)
Saving Drc markers ...
... No Drc file written since there is no markers found.
% Begin Save placement data ... (date=11/14 16:12:13, mem=1695.3M)
** Saving stdCellPlacement_binary (version# 2) ...
Save Adaptive View Pruning View Names to Binary file
% End Save placement data ... (date=11/14 16:12:13, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1695.3M, current mem=1695.3M)
% Begin Save routing data ... (date=11/14 16:12:13, mem=1695.3M)
Saving route file ...
*** Completed saveRoute (cpu=0:00:00.0 real=0:00:00.0 mem=1806.9M) ***
% End Save routing data ... (date=11/14 16:12:13, total cpu=0:00:00.0,
real=0:00:00.0, peak res=1695.4M, current mem=1695.4M)
Saving property file mul2b_netlist.dat/mul2b_netlist.prop
*** Completed saveProperty (cpu=0:00:00.0 real=0:00:00.0 mem=1809.9M) ***
#Saving pin access data to file mul2b_netlist.dat/mul2b_netlist.apa ...
#
% Begin Save power constraints data ... (date=11/14 16:12:13,
mem=1695.4M)
% End Save power constraints data ... (date=11/14 16:12:13, total
cpu=0:00:00.0, real=0:00:00.0, peak res=1695.4M, current mem=1695.4M)
Generated self-contained design mul2b_netlist.dat
#% End save design ... (date=11/14 16:12:13, total cpu=0:00:00.2,
real=0:00:01.0, peak res=1696.3M, current mem=1696.3M)
*** Message Summary: 0 warning(s), 0 error(s)

Parse flat map file...
Writing GDSII file ...
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

```
***** db unit per micron = 2000 *****
***** output gds2 file unit per micron = 2000 *****
***** unit scaling factor = 1 *****

Output for instance
Output for bump
Output for physical terminals
Output for logical terminals
Output for regular nets
Output for special nets and metal fills
Output for via structure generation total number 10
Statistics for GDS generated (version 3)

-----
Stream Out Layer Mapping Information:
GDS Layer Number      GDS Layer Name
-----
191                  COMP
192                  DIEAREA
181                  Metal9
179                  Metal9
178                  Metal9
177                  Metal9
176                  Metal9
175                  Via8
174                  Via8
170                  Via8
160                  Metal8
158                  Metal8
157                  Metal8
156                  Metal8
155                  Metal8
154                  Via7
153                  Via7
149                  Via7
139                  Metal7
137                  Metal7
136                  Metal7
135                  Metal7
134                  Metal7
133                  Via6
132                  Via6
131                  Via6
130                  Via6
129                  Via6
128                  Via6
127                  Via6
122                  Metal6
121                  Metal6
120                  Metal6
119                  Metal6
118                  Metal6
53                   Metal3
52                   Metal3
185                  Metal9
48                   Via2
29                   Metal2
180                  Metal9
47                   Via2
182                  Metal9
44                   Via2
43                   Via2
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

172	Via8
38	Metal2
95	Metal5
36	Metal2
93	Metal5
112	Via5
55	Metal3
113	Metal6
32	Metal2
54	Metal3
31	Metal2
107	Via5
30	Metal2
49	Via2
106	Via5
33	Metal2
109	Via5
10	Metal1
86	Via4
50	Metal3
69	Via3
143	Metal7
6	Cont
169	Via8
35	Metal2
8	Metal1
164	Metal8
27	Vial
141	Metal7
3	Cont
51	Metal3
70	Via3
7	Cont
64	Via3
173	Via8
34	Metal2
92	Metal5
111	Via5
11	Metal1
142	Metal7
4	Cont
9	Metal1
28	Vial
85	Via4
138	Metal7
5	Cont
12	Metal1
88	Via4
183	Metal9
45	Via2
22	Vial
152	Via7
13	Metal1
71	Metal4
90	Via4
184	Metal9
46	Via2
161	Metal8
23	Vial
171	Via8

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

37	Metal2
94	Metal5
148	Via7
14	Metal1
15	Metal1
72	Metal4
91	Via4
150	Via7
16	Metal1
73	Metal4
159	Metal8
26	Vial
151	Via7
17	Metal1
74	Metal4
1	Cont
162	Metal8
24	Vial
140	Metal7
2	Cont
163	Metal8
25	Vial
56	Metal3
57	Metal3
114	Metal6
58	Metal3
115	Metal6
59	Metal3
116	Metal6
65	Via3
66	Via3
67	Via3
68	Via3
75	Metal4
76	Metal4
77	Metal4
78	Metal4
79	Metal4
80	Metal4
87	Via4
89	Via4
96	Metal5
97	Metal5
98	Metal5
99	Metal5
100	Metal5
101	Metal5
108	Via5
110	Via5
117	Metal6
189	Metal9
188	Metal9
187	Metal9
186	Metal8
168	Metal8
167	Metal8
166	Metal8
165	Metal8
147	Metal7
146	Metal7

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

145	Metal7
144	Metal7
63	Metal3
62	Metal3
39	Metal2
105	Metal5
103	Metal5
123	Metal6
42	Metal2
41	Metal2
40	Metal2
20	Metal1
60	Metal3
18	Metal1
61	Metal3
102	Metal5
21	Metal1
19	Metal1
81	Metal4
104	Metal5
82	Metal4
83	Metal4
84	Metal4
124	Metal6
125	Metal6
126	Metal6

Stream Out Information Processed for GDS version 3:
Units: 2000 DBU

Object	Count
<hr/>	
Instances	26
<hr/>	
Ports/Pins	9
metal layer Metal2	3
metal layer Metal3	6
<hr/>	
Nets	72
metal layer Metal1	10
metal layer Metal2	48
metal layer Metal3	14
<hr/>	
Via Instances	67
<hr/>	
Special Nets	33
metal layer Metal1	18
metal layer Metal5	4
metal layer Metal6	11
<hr/>	
Via Instances	82
<hr/>	
Metal Fills	0
<hr/>	
Via Instances	0
<hr/>	
Metal FillOPCs	0
<hr/>	
Via Instances	0

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Metal FillDRCs	0
Via Instances	0
Text	30
metal layer Metal1	2
metal layer Metal2	15
metal layer Metal3	11
metal layer Metal6	2
Blockages	0
Custom Text	0
Custom Box	0
Trim Metal	0

```
#####Streamout is finished!
innovus 4>
```

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Timing Reports:

Lab-6: Logic synthesis & Physical Design of a 2 bit multiplier

Inference: A total of 14 leaf instance count is present in the gate level netlist with total area of 151.380, total power of 15.4 uW.

Result: Hence an 2 bit multiplier is verified before the synthesis and after and synthesis and it is synthesized and the gate level netlist with timing,area and power report was generate successfully. Also the physical design of the multiplier was built successfully.