BECE407E ASIC DESIGN

Timing Analysis

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Interconnect & Delay Calculations

- Interconnects
- Interconnect Models
- Wire Load Models
- Parasitic Formats
- Delay Calculation

Net

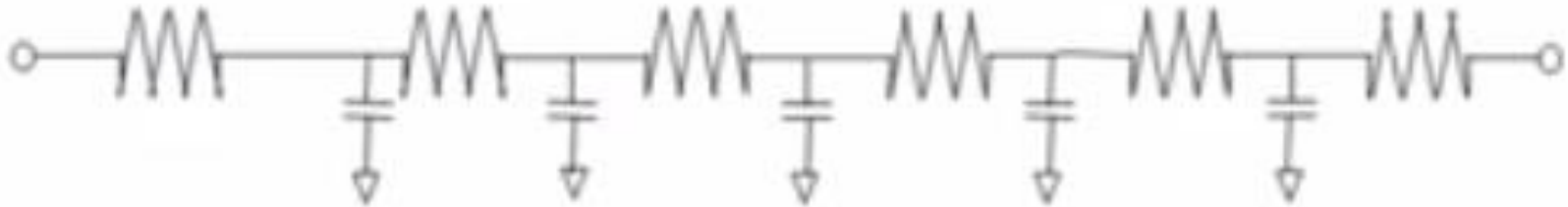
- Is a wire connecting pins of standard cells and blocks
- Has only one driver
- Can drive a number of fanout cells or blocks
- Can travel on multiple metal layers of the chip
- Can be broken up into segments for equivalent electrical representation

RLC for interconnect

- Interconnect resistance - resistance between the output pin of a cell and the input pins of the fanout cells
- Interconnect capacitance - is comprised of grounded and between neighboring signal routes capacitances
- Interconnect inductance - arises due to current loops; effect of inductance can be ignored

RC Interconnect

(a) Trace of length L



(b) Distributed RC tree

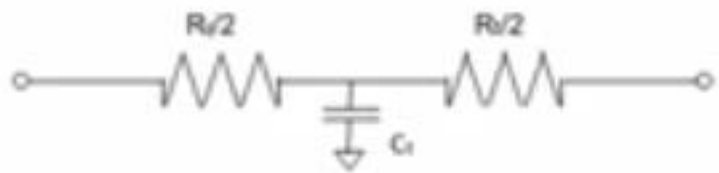
- R_t and C_t - total resistance and capacitance of RC tree

$$R_t = R_p * L$$

$$C_t = C_p * L$$

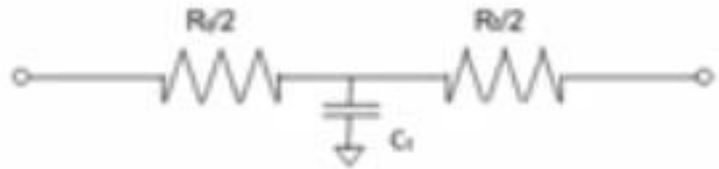
- R_p, C_p - per unit length values
- L - trace length

T - model



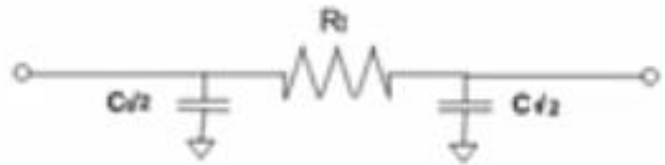
- C_t (total capacitance) is modeled as connected halfway in the resistive tree
- R_t (total resistance) is broken in two sections (each being R_t / 2)

T - model



- C_t (total capacitance) is modeled as connected halfway in the resistive tree
- R_t (total resistance) is broken in two sections (each being R_t / 2)

P_i - model

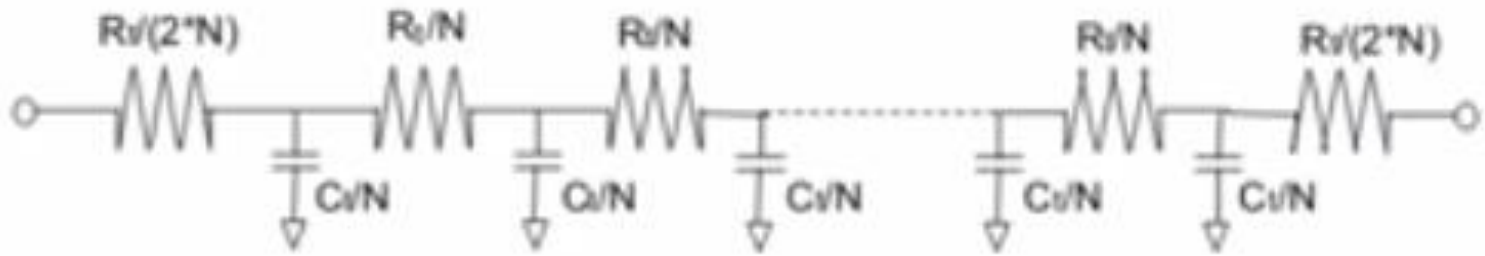


- C_t is broken into two sections (C_t / 2) and connected on either side of the resistance
- R_t (total resistance) is broken in two sections (each being R_t / 2)

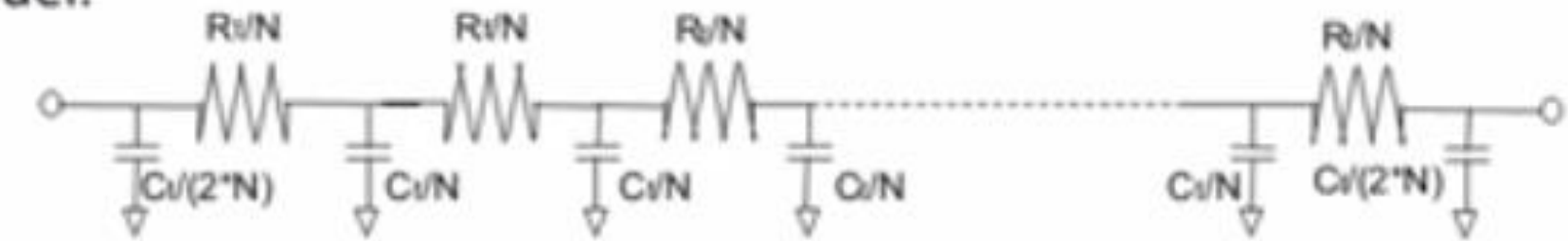
N Section Representation

- More accurate representations of the distributed RC tree are obtained by breaking R_t and C_t into multiple sections.

T model:



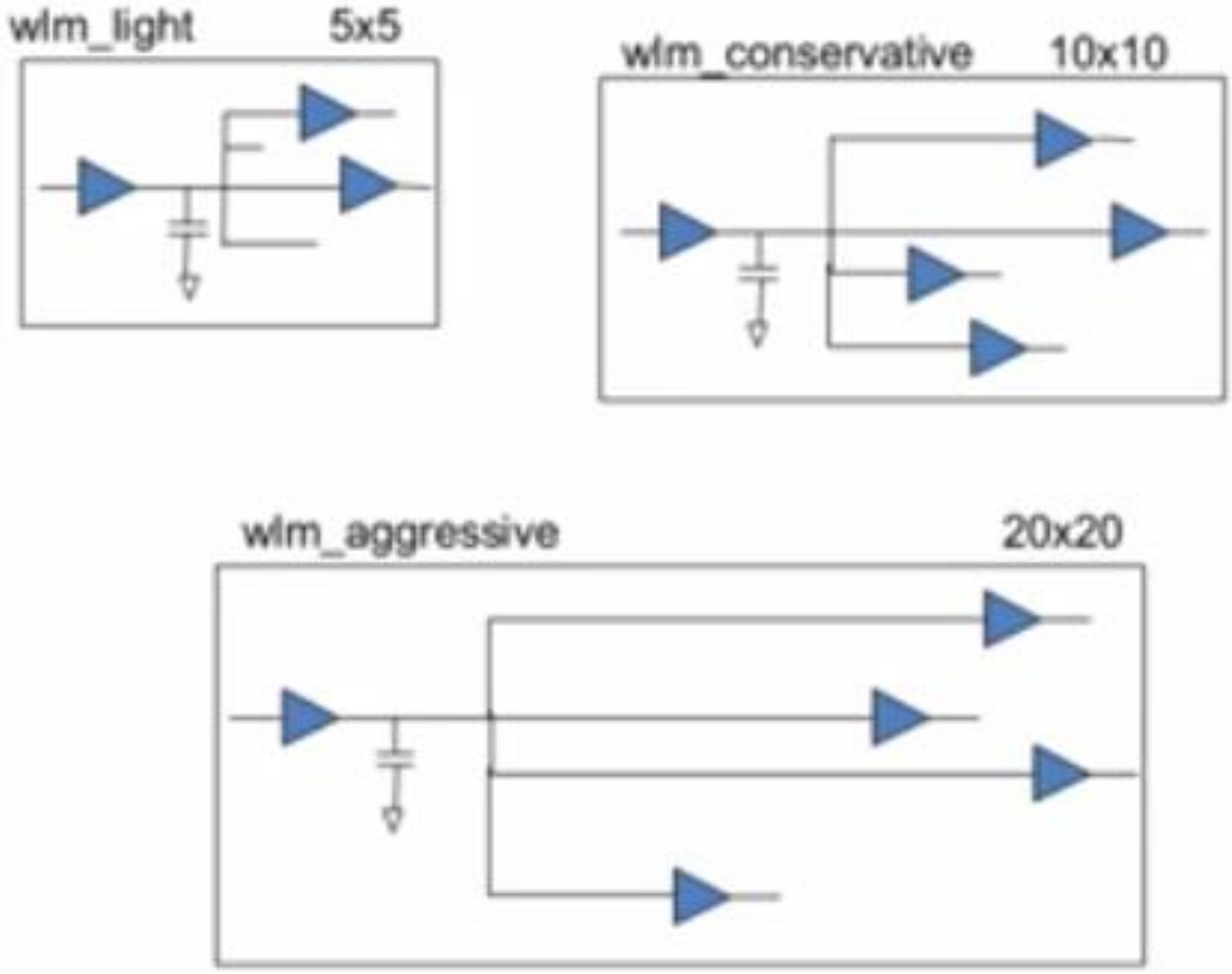
Pi model:



Wireload Models

- Used to estimate:
  - Capacitance
  - Resistance
  - The area overhead due to interconnect
  - The length of a net based upon the number of its fanouts

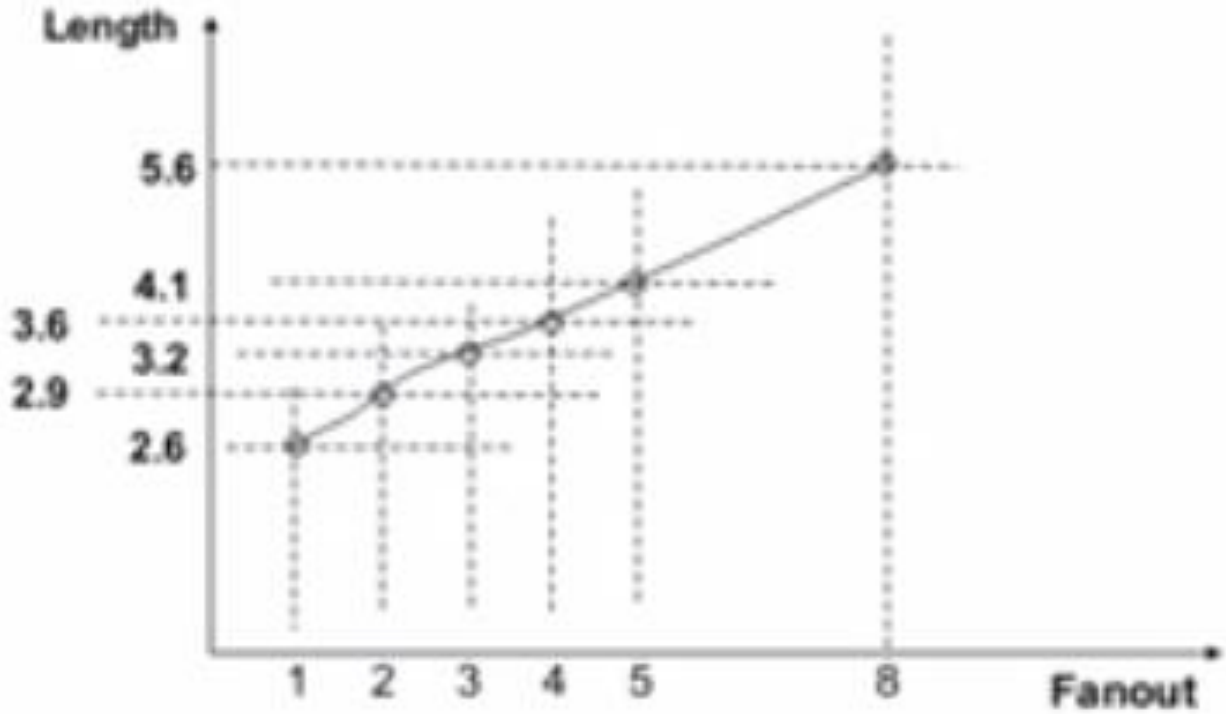
Different Wireload Models



Example of Wireload Model

```
wire_load ("wlm_conservative") {
resistance : 5.0;
capacitance : 1.1;
area : 0.05;
slope : 0.5;
fanout_length (1, 2.6);
fanout_length (2, 2.9);
fanout_length (3, 3.2);
fanout_length (4, 3.6);
fanout_length (5, 4.1);                    }
```

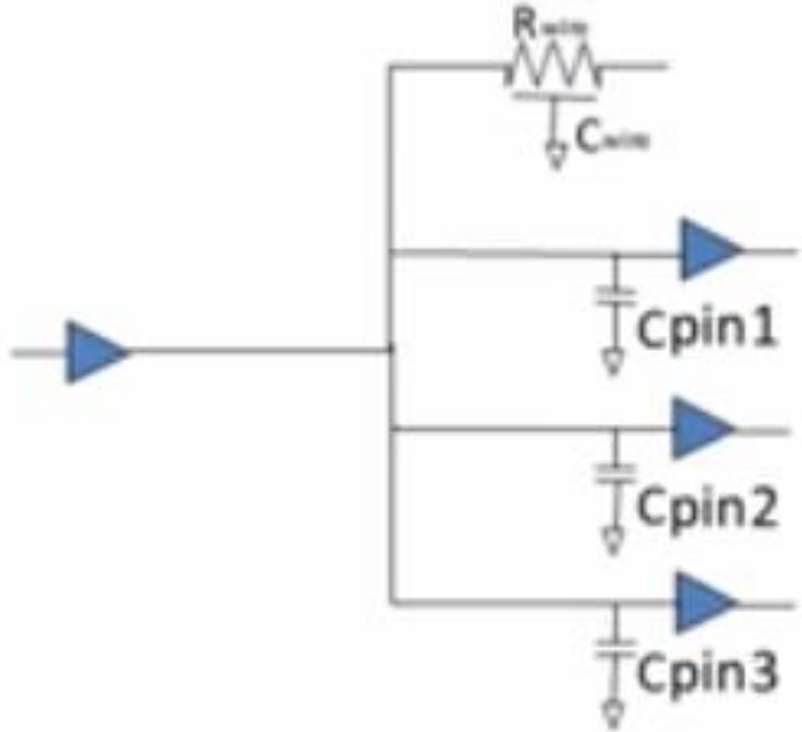
Calculating by Wireload Model



- Length = 4.1 + (8 - 5) * 0.5 = 5.6 units
- Capacitance = Length * cap_coeff(1.1) = 6.16 units
- Resistance = Length * res_coeff(5.0) = 28.0 units
- Area overhead due to interconnect = Length * area_coeff(0.05) = 0.28 area units

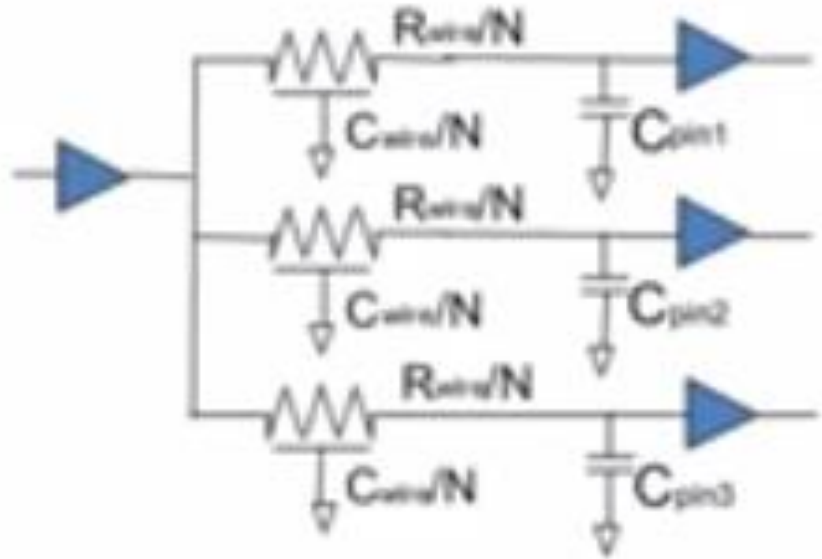
Interconnect Trees: Best-case Tree

- In the best-case tree, it is assumed that the destination (load) pin is physically adjacent to the driver. Thus, none of the wire resistance is in the path to the destination pin. All of the wire capacitance and the pin capacitances from other fanout pins still act as load on the driver pin.



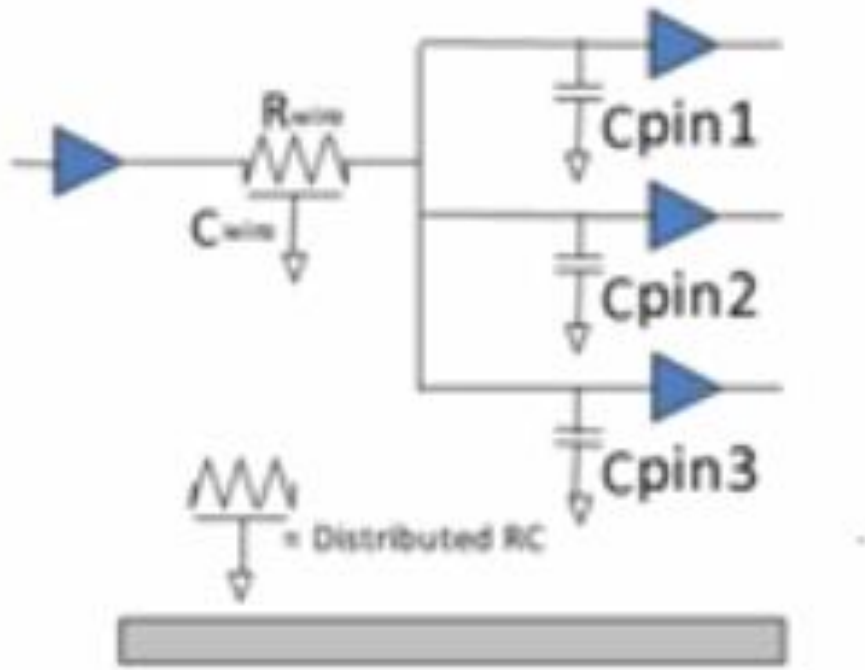
Interconnect Trees: Balanced Tree

- In this scenario, it is assumed that each destination pin is on a separate portion of the interconnect wire. Each path to the destination sees an equal portion of the total wire resistance and capacitance.



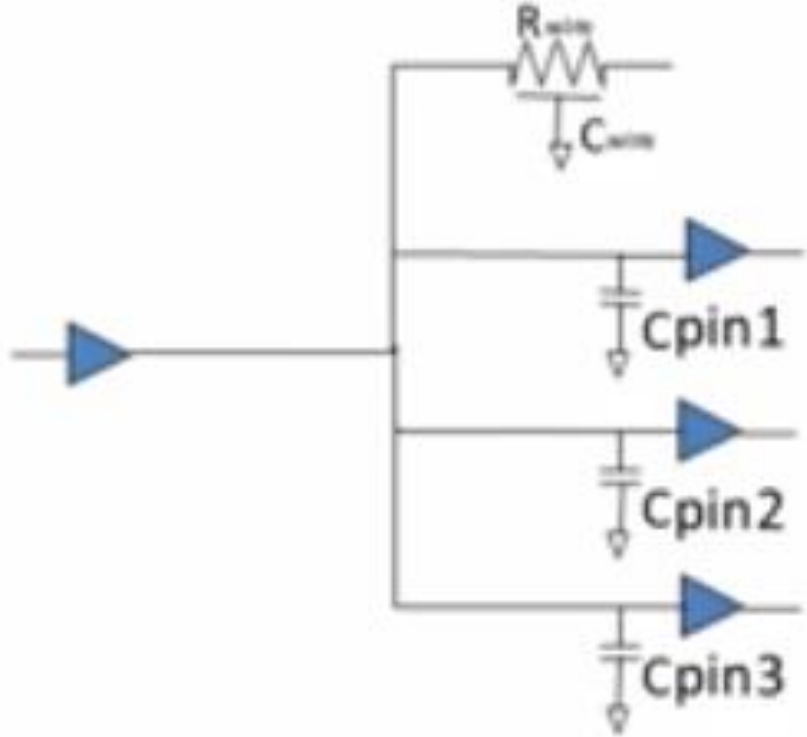
Interconnect Trees: Worst-case Tree

- In this scenario, it is assumed that all the destination pins are together at the far end of the wire. Thus each destination pin sees the total wire resistance and the total wire capacitance.



Interconnect Trees: Best-case Tree

- In the best-case tree, it is assumed that the destination (load) pin is physically adjacent to the driver. Thus, none of the wire resistance is in the path to the destination pin. All of the wire capacitance and the pin capacitances from other fanout pins still act as load on the driver pin.



Specifying Wireload Models

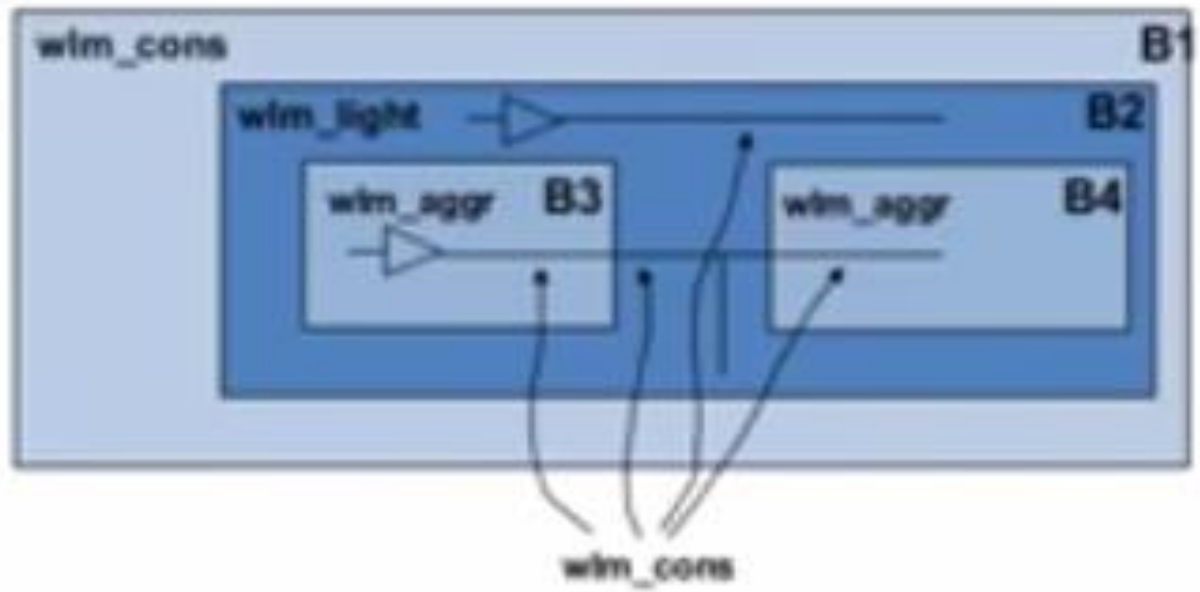
- set_wire_load_model “wlm_cons” -library “lib_stdcell”
- # Says to use the wireload model wlm_cons present in the
- # cell library lib_stdcell

Wireload Modes

- Used to define different wireload models in different hierarchical boundaries
- Command: set_wire_load_mode
- Types:
  - Top
  - Enclosed
  - Segmented

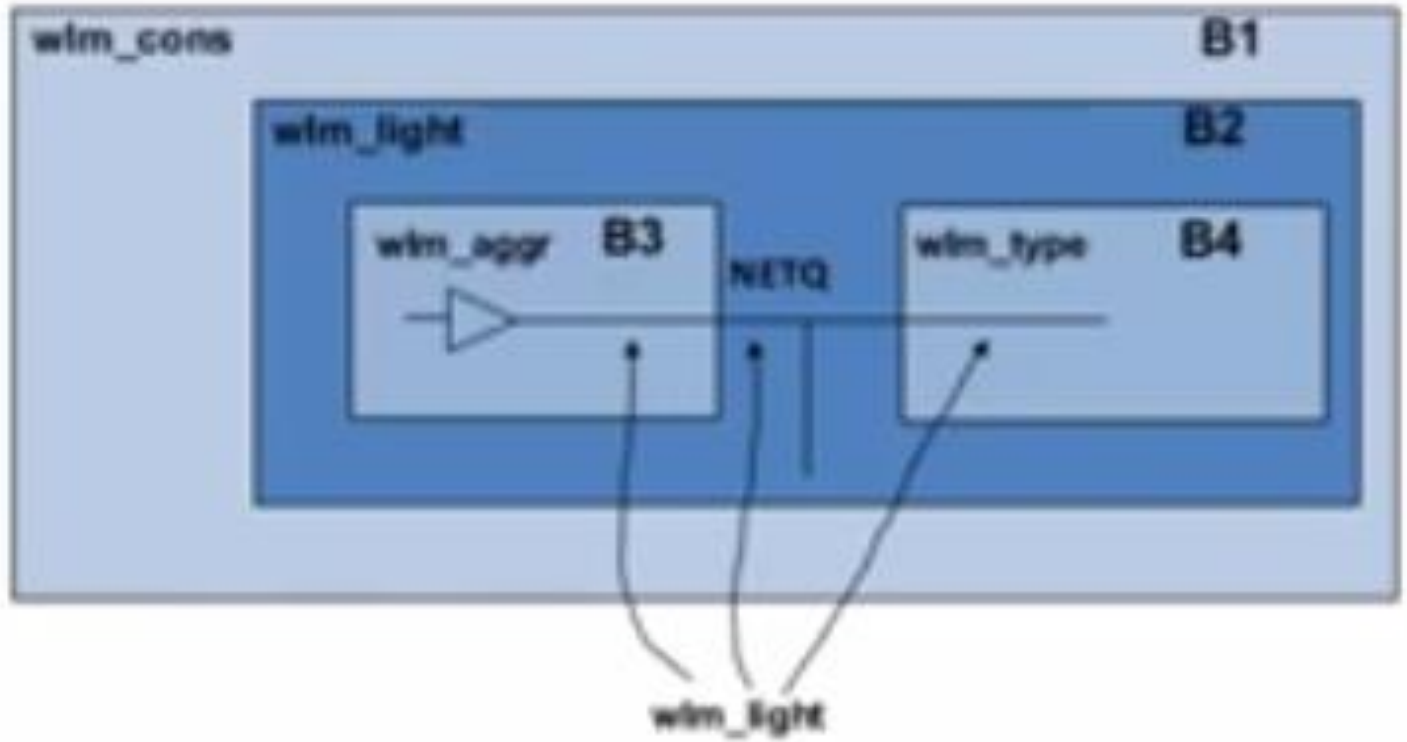
Top Wireload Mode

- All nets within the hierarchy inherit the wireload model of the top-level (any wireload models specified in lower-level blocks are ignored)



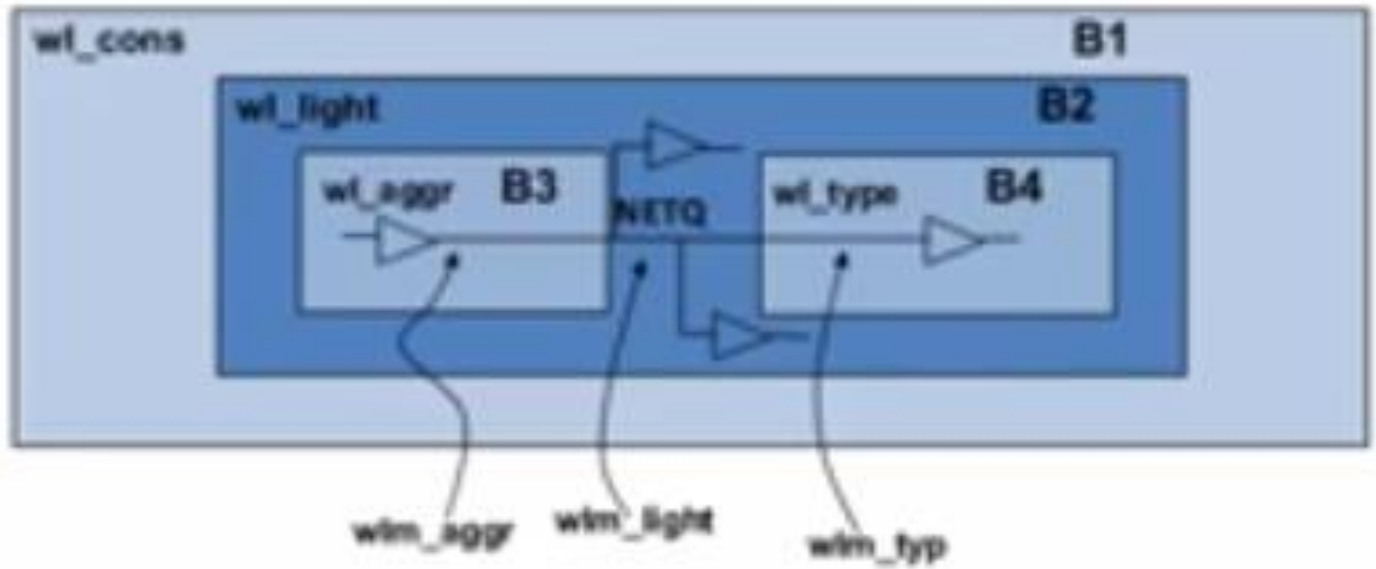
Enclosed Wireload Mode

- Fully encompasses the net is used for the entire net



Segmented Wireload Mode

- Each segment of the net gets its wireload model from the block that encompasses the net segment
- Each portion of the net uses the appropriate wireload model within that level



Wireload Model in Cell Library

- A default wireload model may optionally be specified in the cell library as:

```
default_wire_load: "wlm_light";
```

- wire_load_selection - wireload selection group, which selects a wireload model based upon area:

```
wire_load_selection (WireAreaSelGrp){
wire_load_from_area(0, 50000, "wlm_light");
wire_load_from_area(50000, 100000, "wlm_cons");
wire_load_from_area(100000, 200000, "wlm_typ");
wire_load_from_area(200000, 500000, "wlm_aggr");
}
```

Extracted Parasitics Formats

- Parasitics extracted from a layout can be described in three formats:
  - Detailed Standard Parasitic Format (DSPF)
  - Reduced Standard Parasitic Format (RSPF)
  - Standard Parasitic Extraction Format (SPEF)

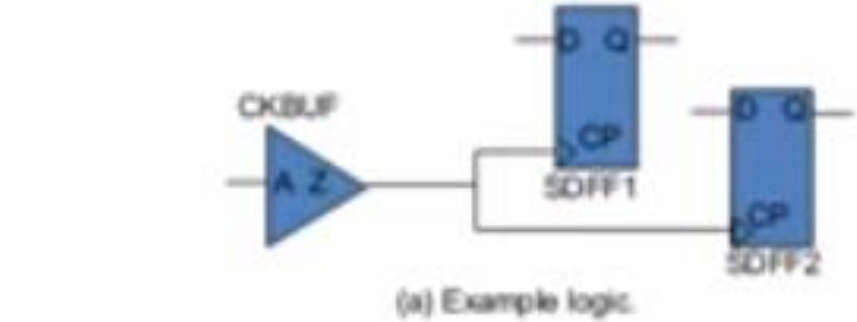
Detailed Standard Parasitic Format (DSPF)

- The detailed parasitics are represented in SPICE format
- DSPF file can be used as an input to a SPICE simulator
- Syntax is too detailed and verbose (total file size is very large)
- Used for relatively small group of nets

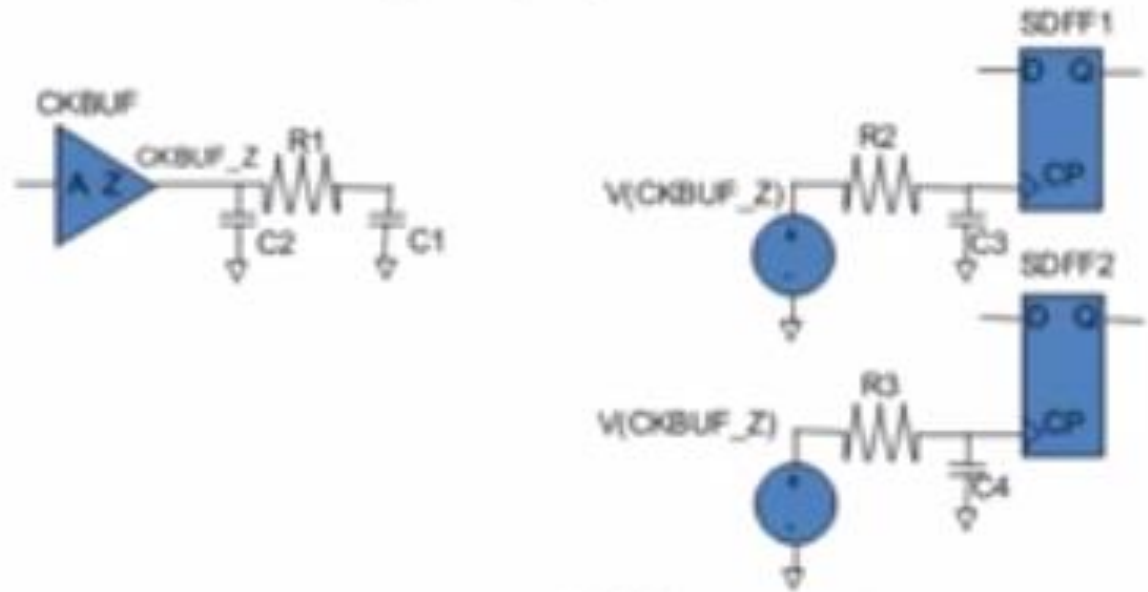
```
.SUBCKT TEST_EXAMPLE OUT IN
* Net Section
*|GROUND_NET VSS
*|NET IN 4.9E-02PF
*|P (IN I 0.0 0.0 4.1)
*|I (BUF1:A BUF A I 0.0 0.7 4.3)
C1 IN VSS 2.3E-02PF
C2 BUF1:A VSS 2.6E-02PF
R1 IN BUF1:A 4.8E00
*|NET OUT 4.47E-02PF
*|S (OUT:1 8.3 0.7)
*|P (OUT O 0.0 8.3 0.0)
*|I (BUF1:OUT BUF1 OUT O 0.0 4.9 0.7)
C3 BUF1:OUT VSS 3.5E-02PF
C4 OUT:1 VSS 4.9E-03PF
C5 OUT VSS 4.8E-03PF
R2 BUF1:OUT OUT:1 12.1E00
R3 OUT:1 OUT 8.3E00
*Instance Section
X1 BUF1:A BUF1:OUT BUF
.ENDS
```

Reduced Standard Parasitic Format (RSPF)

- The parasitics are represented in a reduced form (voltage and a controlled current sources)
- RSPF file can be used as an input to a SPICE simulator
- The bidirectional signal flow cannot be represented



(a) Example logic.



(b) RSPF representation.

Standard Parasitic Extraction Format (SPEF)

- Compact
- Representing detailed parasitics
- The units of the parasitics R and C are specified at the beginning of the SPEF file

```
*D_NET NET_27 0.77181
*CONN
*I *8:Q O *L 0 *D CELL1
*I *10:I I *L 12.3
*CAP
1 *9:0 0.00372945
2 *9:1 0.0206066
3 *9:2 0.035503
4 *9:3 0.0186259
5 *9:4 0.0117878
6 *9:5 0.0189788
7 *9:6 0.0194256
8 *9:7 0.0122347
9 *9:8 0.00972101
10 *9:9 0.298681
11 *9:10 0.305738
12 *9:11 0.0167775
```

```
*RES
1 *9:0 *9:1 0.0327394
2 *9:1 *9:2 0.116926
3 *9:2 *9:3 0.119265
4 *9:4 *9:5 0.0122066
5 *9:5 *9:6 0.0122066
6 *9:6 *9:7 0.0122066
7 *9:8 *9:9 0.142205
8 *9:9 *9:10 3.85904
9 *9:10 *9:11 0.142205
10 *9:12 *9:2 1.33151
11 *9:13 *9:6 1.33151
12 *9:1 *9:9 1.33151
13 *9:5 *9:10 1.33151
14 *9:12 *8:Q 0
15 *9:13 *10:I 0
*END
```