

Vellore Institute of Technology, Chennai

BECE407P - ASIC Design

Lab-2

Running the Basic Synthesis Flow using Cadence® Genus

Name of the Student: [REDACTED]

Roll Number: [REDACTED]

Date of the Lab. Class: 25/07/24

1. **Aim:** To run the basic synthesis flow of 4 bit up counter using genus.

2. **EDA Tools Used:**

Cadence® Genus

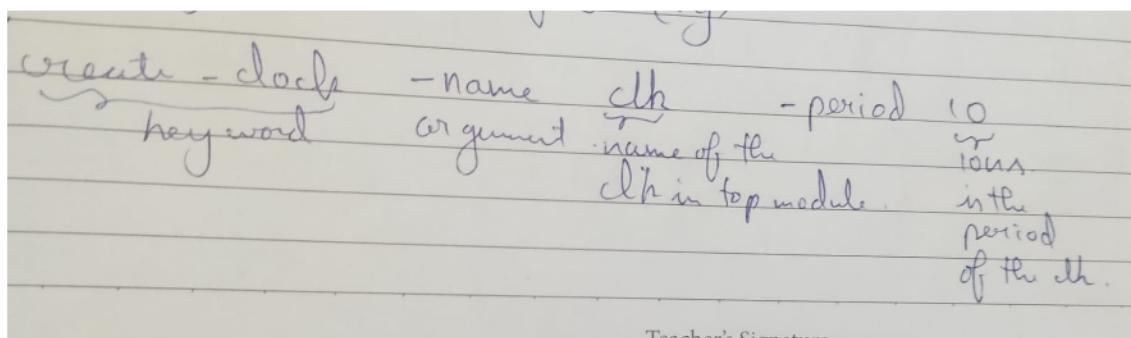
3. **Details of the Synthesis Flow:** (with clear snapshots)

(a) Method of writing a script file (.g) for input *Timing Constraints*:

1.) Create a file with .g extension in the synthesis folder.

2.) Open it and write the following commands and save it:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "rst"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "q"] -clock [get_clocks "clk"]
```



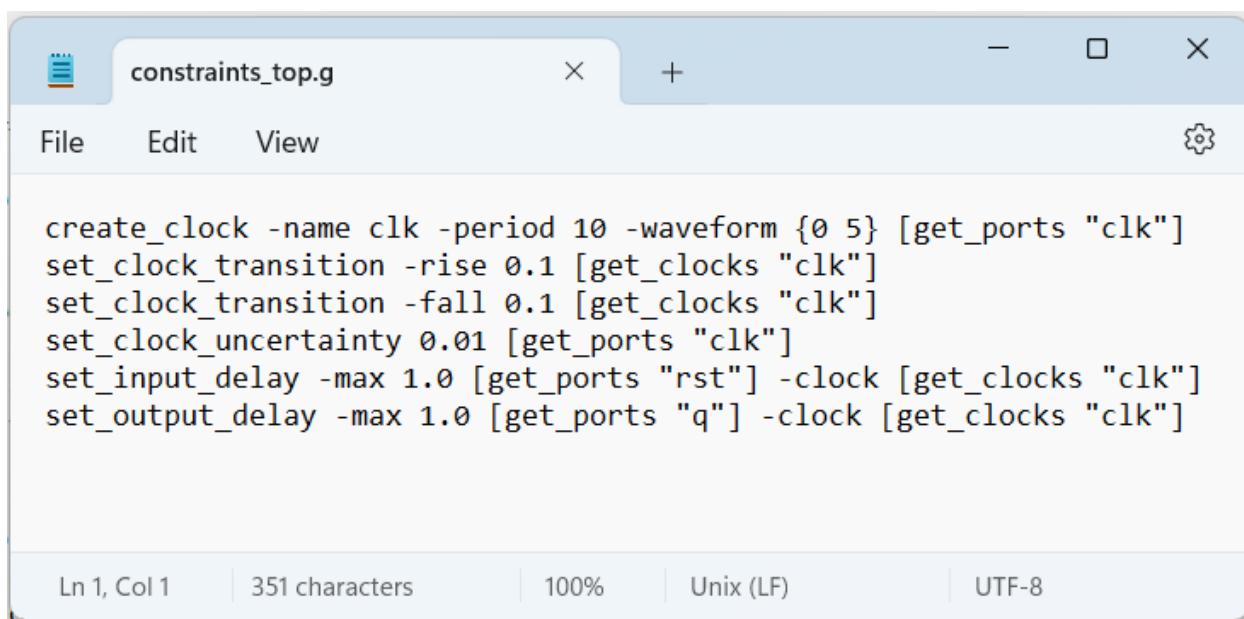
Teacher's Signature _____

- wave form $\{0\ 5\}$ [get_ports "clk"] //
 duty cycle.
 0 = start of pulse width
 5us = 1bp time of "

set_clock_transition -rise 0.1 [get_clocks "clk"]
 Keyword to define -fall 0.1us rise time.
 the rise & fall time
 of clk.

set_clock_uncertainty 0.01 [get_ports "clk"]
 defines the skew & jitter. clk.

set_input_delay -max(-min) 1.0 [get_ports "clk"]
 1.0 as default.



```

constraints_top.g

File Edit View
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "rst"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "q"] -clock [get_clocks "clk"]

Ln 1, Col 1 | 351 characters | 100% | Unix (LF) | UTF-8
  
```

(b) Steps to start Cadence® Genus:

- 1.) Open the synthesis folder terminal .
- 2.) run the following commands : 'csh' , 'source /home/install/cshrc' , 'genus -legacy -ui' .

(c) Steps to "load the required libraries, designs and synthesizing those designs":

- 1.) After opening the genus set the library and rtl folder path by using the

commands :

```
'set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/ '
'set_attribute init_rtl_search_path /home/student/Desktop/21BEC1033/rtl/ '
```

2.) Now load the library using the command :

```
'set_attribute library slow_vdd1v0_basicCells.lib '
```

3.) Now read the counter.v file by using the command : 'read_hdl counter.v'

4.) Elaborate the design by using the command: 'elaborate'.

5.) Now read the timing constraints file by using the command :

```
'read_sdc constraints_top.g'
```

6.) To synthesize the design run the command:

```
'set_attribute syn_generic_effort medium'
```

```
'syn_generic'
```

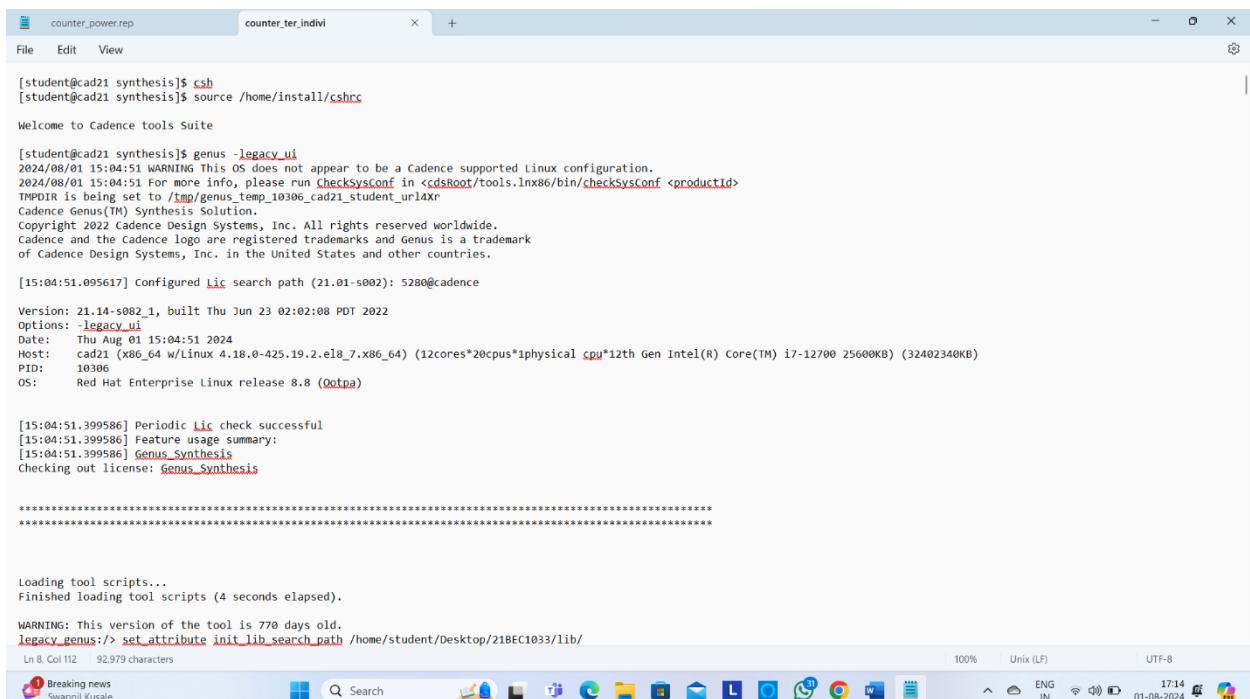
```
'set_attribute syn_map_effort high'
```

```
'set_attribute syn_opt_effort high'
```

```
'syn_map'
```

```
'syn_opt'
```

4. Cadence® Genus Legacy terminal after Synthesis: [Terminal](#)
(click the link for viewing entire terminal)



```
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc
Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -legacy_ui
2024/08/01 15:04:51 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/08/01 15:04:51 For more info, please run checkSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productid>
TMPDIR is being set to /tmp/genus_temp_10306_cad21_student_ur14xr
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[15:04:51.095617] Configured lic search path (21.01-s002): 5280@cadence
Version: 21.14-s002_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui
Date: Thu Aug 01 15:04:51 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64) (12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700 25600KB) (32402340KB)
PID: 10306
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

[15:04:51.399586] Periodic lic check successful
[15:04:51.399586] Feature usage summary:
[15:04:51.399586] Genus_Synthesis
Checking out license: Genus_Synthesis

*****
***** Loading tool scripts...
***** Finished loading tool scripts (4 seconds elapsed).

WARNING: This version of the tool is 770 days old.
legacy_genus:/> set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
Ln 8, Col 112    92.979 characters
100% Unix (LF)   UTF-8
Breaking news   Search   L   ENG IN   17:14 01-08-2024
```

File Edit View
counter_power.rep counter_ter.indivi +

Finished loading tool scripts (4 seconds elapsed).

WARNING: This version of the tool is 770 days old.
 legacy_genus:/> set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
 Setting attribute of root '/': 'init_lib_search_path' = /home/student/Desktop/21BEC1033/lib/
 legacy_genus:/> set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/
 Setting attribute of root '/': 'init_hdl_search_path' = /home/student/Desktop/21BEC1033/rtl/
 legacy_genus:/> set_attribute library slow_vddiv0_basicCells.lib

Threads Configured:3

Message Summary for Library slow_vddiv0_basicCells.lib:

 Missing a function attribute in the output pin definition. [LBR-518]: 1

Info : Created nominal operating condition. [LBR-412]
 : Operating condition '_nominal' was created for the PVT values (1.000000, 0.900000, 125.000000) in library 'slow_vddiv0_basicCells.lib'.
 : The nominal operating condition is represented, either by the nominal PVT values specified in the library source (via nom_process, nom_voltage and nom_temperature respectively), or by the default PVT values (1.0,1.0,1.0).
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'ANTENNA' must have an output pin.
 Warning : Library cell has no output pins(s), then reload the library. Else the library cell will be marked as timing model i.e. unusable. Timing_model means that the cell does not have any defined function. If there is no output pin, Genus will mark library cell as unusable i.e. the attribute 'usable' will be marked to 'false' on the libcell. Therefore, the cell is not used for mapping and it will not be picked up from the library for synthesis. If you query the attribute 'unusable_reason' on the libcell; result will be: 'Library cell has no output pins.' Note: The message LBR-9 is only for the logical pins and not for the power_ground pins. Genus will depend upon the output function defined in the pin group (output pin) of the cell, to use it for mapping. The pg_min will not have any function defined.
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'ANTENNA' must have an output pin.
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'DECAP10' must have an output pin.
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'DECAP10' must have an output pin.
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'DECAP10' must have an output pin.
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'DECAP2' must have an output pin.
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'DECAP2' must have an output pin.
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'DECAP3' must have an output pin.
 Warning : Library cell has no output pins defined. [LBR-9]
 : Library cell 'DECAP3' must have an output pin.

Ln 8, Col 112 92,979 characters

File Edit View
counter_power.rep counter_ter.indivi +

File Edit View
 - library cell 'DECAP9' must have an output pin.
 Setting attribute of root '/': 'library' = slow_vddiv0_basicCells.lib
 legacy_genus:/> read_hdl counter.v
 legacy_genus:/> elaborate
 Library has 324 usable logic and 128 usable sequential lib-cells.
 Info : Elaborating Design. [ELAB-1]
 : Elaborating top-level block 'counter' from file '/home/student/Desktop/21BEC1033/rtl/counter.v'.
 Info : Done Elaborating Design. [ELAB-3]
 : Done elaborating 'counter'.
 Checking for analog nets...
 Check completed for analog nets.
 Checking for source RTL...
 Check completed for source RTL.
 Running Unified Mux Engine Tricks...
 Completed Unified Mux Engine Tricks

Stage: post_elab

Trick	Accepts	Rejects	Runtime (ms)
ume_constant_bmux	0	0	0.00

Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: counter, recur: true)
 Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
 Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: counter, recur: true)
 Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab

Transform	Accepts	Rejects	Runtime (ms)
hlo_clip_mux_input	0	0	0.00
hlo_clip	0	0	0.00

/designs/counter

legacy_genus:/> read_sdc constraints_top.g
 Statistics for commands executed by read_sdc:
 "create_clock" - successful 1 , failed 0 (runtime 0.00)
 "get_clocks" - successful 4 , failed 0 (runtime 0.00)
 "get_ports" - successful 4 , failed 0 (runtime 0.00)
 "set_clock_transition" - successful 2 , failed 0 (runtime 0.00)
 "set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)
 "set_input_delay" - successful 1 , failed 0 (runtime 0.00)
 "set_output_delay" - successful 1 , failed 0 (runtime 0.00)
 read_sdc completed in 00:00:00 (hh:mm:ss)

Legacy_genus:/> set_attribute syn_generic_effort high
 Setting attribute of root '/': 'syn_generic_effort' = high
 legacy_genus:/> syn generic

Stage: pre_early_cg

Transform	Accepts	Rejects	Runtime (ms)
-----------	---------	---------	--------------

#Generic Timing Info for library domain: _default_ typical gate delay: 127.6 ps std_slew: 17.9 ps std_load: 1.0 ff
 Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: counter, recur: true)
 Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_to_gen_setup

Transform	Accepts	Rejects	Runtime (ms)
hlo_mux_reorder	0	0	0.00

Info : Synthesizing. [SYNTH-1]
 : Synthesizing 'counter' to generic gates using 'high' effort.
 PBS_Generic_Start - Elapsed_Time 0, CPU_Time 0.0
 stamp 'PBS_Generic_Start' being created for table 'pbs_debug'

Total Time (Wall)	Stage Time (Wall)	% (Wall)	Date - Time	Memory	Stage
00:00:06(00:01:57)	00:00:00(00:00:00)	0.0(0.0)	15:06:50 (Aug01)	437.0 MB	PBS_Generic_Start

Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
 Info: ("N") indicates data that was populated from previously saved time_info database
 Info: CPU time includes time of parent + longest thread

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counter_power.rep

```

File Edit View
| SYNTH-5 [Info] | 1 | Done mapping.
| SYNTH-7 [Info] | 1 | Incrementally optimizing.
-----
Info : Done incrementally optimizing. [SYNTH-8]
      : Done incrementally optimizing 'counter'.
legacy_genus:/> write_sdc > counter.sdc
legacy_genus:/> Finished SDC export (command execution time 00:00 (real) = 00:00).
legacy_genus:/> gui_show
legacy_genus:/> report_timing > counter_timing.rep
legacy_genus:/> report_area > counter_area.rep
legacy_genus:/> report_power > counter_power.rep
Info : Joules engine is used. [RPT-16]
      : Joules engine is being used for the command report_power.
Info : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
      : counter
Info : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info : ACTP-0001 Activity propagation ended for stim#0
Info : PWRA-0001 [PwrInfo] compute_power effective options
      : -mode : vectorless
      : -skip_propagation : 1
      : -frequency_scaling_factor : 1.0
      : -use_clock_freq : stim
      : -stim :stim#0
      : -fromGenus : 1
Info : ACTP-0001 Timing initialization started
Info : ACTP-0001 Timing initialization ended
Info : PWRA-0002 Skipping activity propagation due to -skip_ap
      : option...
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
      : flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
      : of power analysis, ignored this option.
Info : PWRA-0002 Started 'vectorless' power computation.
Info : PWRA-0002 Finished power computation.
Info : PWRA-0007 [PwrInfo] completed successfully.
      : Info=6, Warn=2, Error=0, Fatal=0
Output file: counter_power.rep
legacy_genus:/>

```

Ln 890, Col 74 92,979 characters

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Search

100% Unix (LF) UTF-8

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5. Generate & Read the Reports: (with clear snapshots)

For generating the report run the following commands:

`report_timing > counter_timing.rep`

`report_area > counter_area.rep`

`report_power > counter_power.rep`

counter_area.rep

```

File Edit View
-----
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Jul 31 2024 12:49:41 pm
Module: counter
Technology library: slow_vddiv0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
-----
Instance Module Cell Count Cell Area Net Area Total Area Wireload
-----  

counter 13 33.858 0.000 33.858 <none> (D)  

(D) = wireload is default in technology library

```

counter_power.rep

```

File Edit View
-----
Instance: /counter
Power Unit: W
PDB Frames: /stim#0/frame#0
-----
Category Leakage Internal Switching Total Row%
-----  

memory 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
register 4.08901e-10 7.84178e-07 2.12742e-08 8.05861e-07 81.49%
latch 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
logic 2.60590e-10 8.03513e-08 3.76844e-08 1.18296e-07 11.96%
bbox 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
clock 0.00000e+00 0.00000e+00 6.48000e-08 6.48000e-08 6.55%
pad 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
pm 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
-----
Subtotal 6.69491e-10 8.64529e-07 1.23759e-07 9.88957e-07 100.00%
Percentage 0.07% 87.42% 12.51% 100.00% 100.00%
-----  


```

counter_timing.rep

```

File Edit View
-----
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Jul 31 2024 12:49:41 pm
Module: counter
Technology library: slow_vddiv0 1.0
Operating conditions: PVT_0P9V_125C (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
-----
Pin Type Fanout Load Slew Delay Arrival
-----  

(clock clk) launch 0 R  

q_reg[0]/CK 100 +0 0 R  

q_reg[0]/Q DFFHQX1 4 1.0 37 +255 255 F  

q[0] << interconnect 37 +0 255 F  

(constraints_top.g_line_6_3_1) out port 0 +0 255 F  

(ext delay) +1000 1255 F  

-----  

(clock clk) capture 10000 R
-----  

Cost Group : 'clk' (path_group 'clk')
Timing slack : 8745ps
Start-point : q_reg[0]/CK
End-point : q[0]

```

Ln 12, Col 49 1,572 characters

90% Unix (LF) UTF-8

1 KB

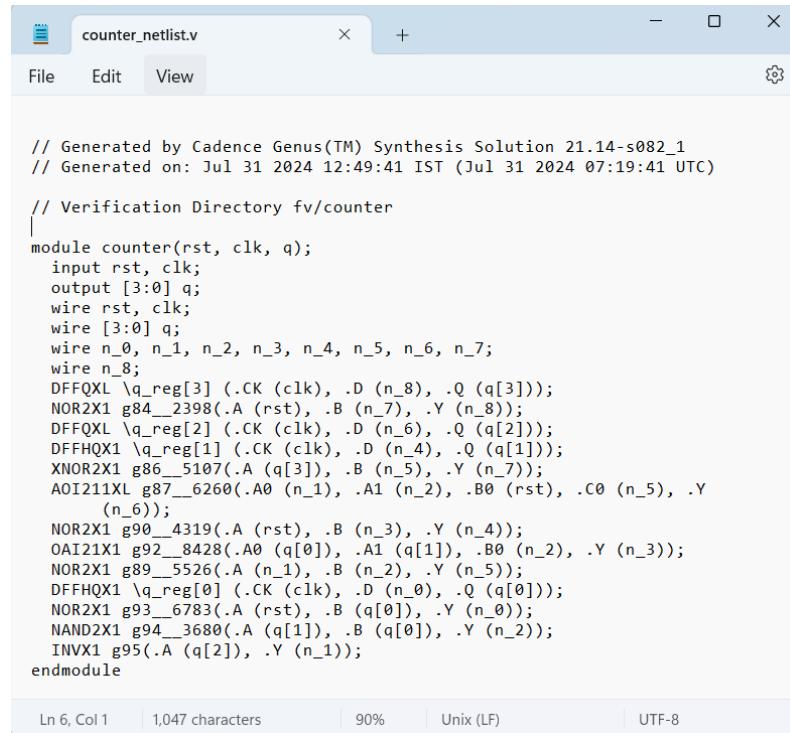
Cell Count=13
 Cell Area=33.858
 Power dissipated=0.67 nW

6. Writing the Output files: (with clear snapshots)

Run the following commands to write the output files:

```
write_netlist > counter_netlist.v
```

```
write_sdc > counter.sdc
```

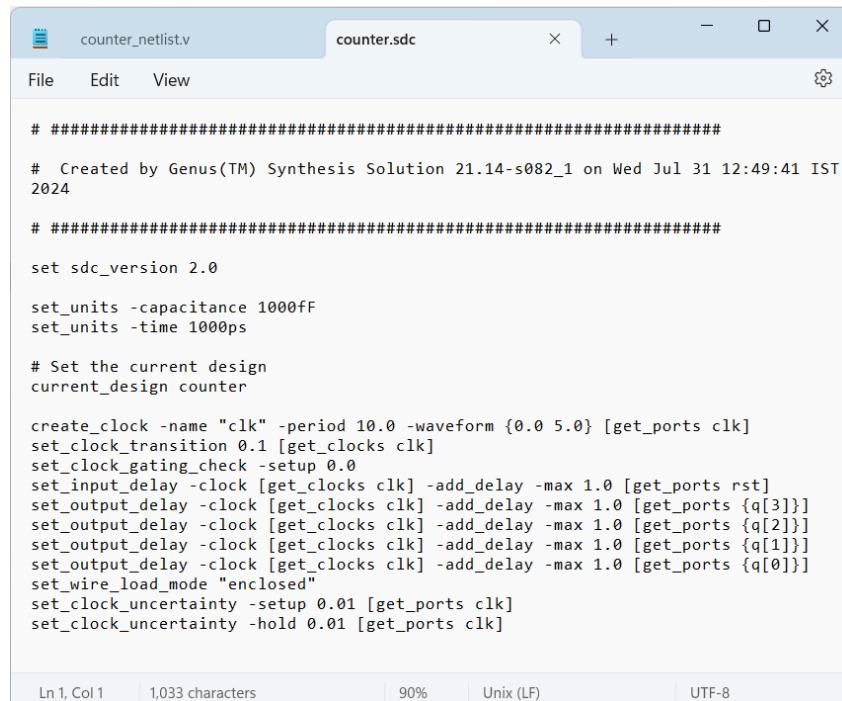


The screenshot shows a software interface with a title bar "counter_netlist.v". The main area contains the generated Verilog code for a counter module. The code includes declarations for inputs (rst, clk), outputs (q), and wires, along with various logic gates (DFQQXL, NOR2X1, DFFQXL, DFFHQX1, AOI211XL, NOR2X1, OAI21X1, NOR2X1, DFFHQX1, NOR2X1, NAND2X1, INVX1) used to implement the counter logic. The code is annotated with comments indicating it was generated by Cadence Genus Synthesis Solution 21.14-s082_1 on Jul 31 2024 at 12:49:41 IST.

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Jul 31 2024 12:49:41 IST (Jul 31 2024 07:19:41 UTC)

// Verification Directory fv/counter
module counter(rst, clk, q);
    input rst, clk;
    output [3:0] q;
    wire rst, clk;
    wire [3:0] q;
    wire n_0, n_1, n_2, n_3, n_4, n_5, n_6, n_7;
    wire n_8;
    DFQQXL \q_reg[3] (.CK (clk), .D (n_8), .Q (q[3]));
    NOR2X1 g84_2398(.A (rst), .B (n_7), .Y (n_8));
    DFFQXL \q_reg[2] (.CK (clk), .D (n_6), .Q (q[2]));
    DFFHQX1 \q_reg[1] (.CK (clk), .D (n_4), .Q (q[1]));
    XNOR2X1 g86_5107(.A (q[3]), .B (n_5), .Y (n_7));
    AOI211XL g87_6260(.A0 (n_1), .A1 (n_2), .B0 (rst), .C0 (n_5), .Y
        (n_6));
    NOR2X1 g90_4319(.A (rst), .B (n_3), .Y (n_4));
    OAI21X1 g92_8428(.A0 (q[0]), .A1 (q[1]), .B0 (n_2), .Y (n_3));
    NOR2X1 g89_5526(.A (n_1), .B (n_2), .Y (n_5));
    DFFHQX1 \q_reg[0] (.CK (clk), .D (n_0), .Q (q[0]));
    NOR2X1 g93_6783(.A (rst), .B (q[0]), .Y (n_0));
    NAND2X1 g94_3680(.A (q[1]), .B (q[0]), .Y (n_2));
    INVX1 g95(.A (q[2]), .Y (n_1));
endmodule
```

Ln 6, Col 1 | 1,047 characters | 90% | Unix (LF) | UTF-8



The screenshot shows a software interface with a title bar "counter.sdc". The main area contains the generated System Design Constraints (SDC) file. It includes header comments, a timestamp, and specific timing constraints for the "clk" clock port. These constraints include setting the clock period to 10.0 units, defining setup and hold times for the clock, and specifying wire load modes for the clock signal.

```
# #####
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Wed Jul 31 12:49:41 IST
# 2024
# #####
set sdc_version 2.0

set_units -capacitance 1000ff
set_units -time 1000ps

# Set the current design
current_design counter

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports rst]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {q[3]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {q[2]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {q[1]}]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports {q[0]}]
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.01 [get_ports clk]
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

Ln 1, Col 1 | 1,033 characters | 90% | Unix (LF) | UTF-8

7. Method of writing a script file (.tcl) for synthesis:

1.)Create a file with .tcl extension in synthesis folder and type the following commands and save it:

```
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {counter.v}

elaborate
read_sdc constraints_top.g

set_attribute syn_generic_effort high
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > counter_netlist.v
write_sdc > counter.sdc
gui_show

report_timing > counter_timing.rep
report_area > counter_area.rep
report_power > counter_power.rep
```

2.)After creating the .g and .tcl file open the terminal of synthesis folder and run the following commands:

```
'csh'
'source /home/install/cshrc'
'genus -legacy -ui -f counter.tcl' .
```

counter.tcl

```

set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {counter.v}

elaborate
read_sdc constraints_top.g

set_attribute syn_generic_effort high
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

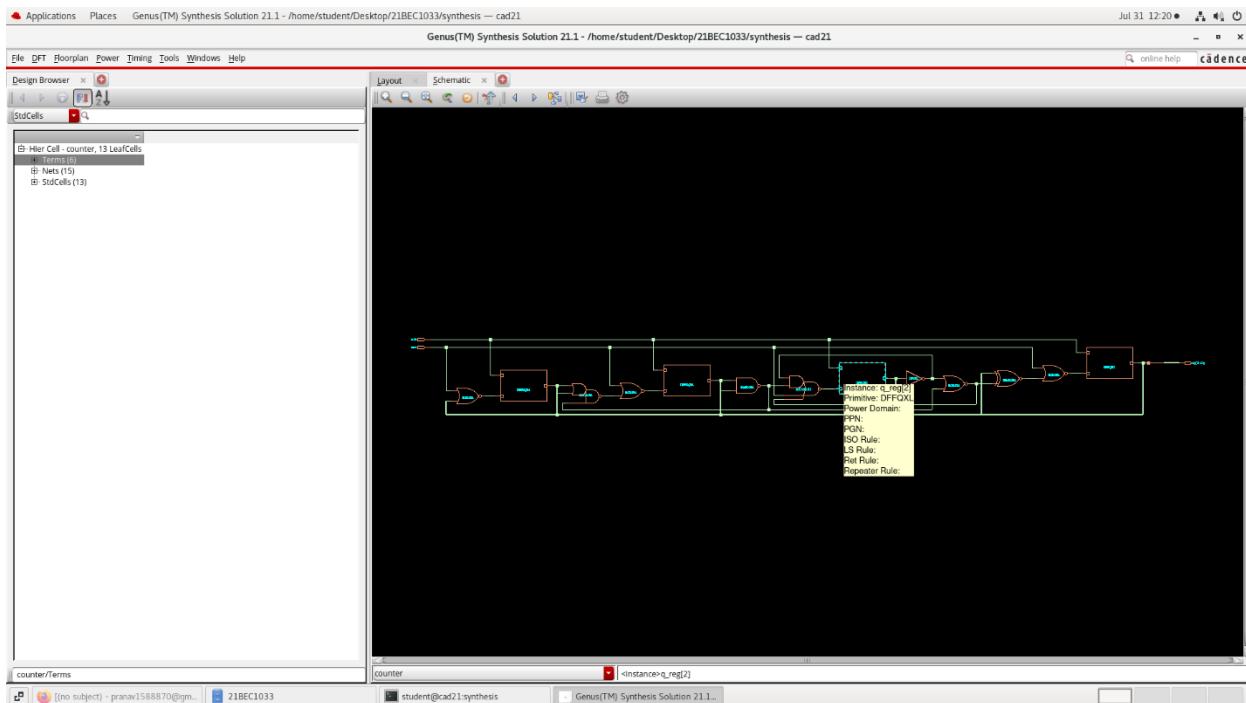
write_netlist > counter_netlist.v
write_sdc > counter.sdc
gui_show

report_timing > counter_timing.rep
report_area > counter_area.rep
report_power > counter_power.rep

```

Ln 15, Col 8 | 558 characters | 100% | Windows (CRLF) | UTF-8

8. Genus Schematic:



Vellore Institute of Technology, Chennai

BECE407P - ASIC Design

Lab-2

Running the Basic Synthesis Flow using Cadence® Genus

Name of the Student: PRANAV.G

Roll Number: 21BEC1033

Date of the Lab. Class: 25/07/24

1. Aim: To run the basic synthesis flow of half adder using genus.

2. EDA Tools Used:

Cadence® Genus

3. Details of the Synthesis Flow: (with clear snapshots)

(a) Method of writing a script file (.g) for input *Timing Constraints*:

1.) Create a file with .g extension in the synthesis folder.

2.) Open it and write the following commands and save it:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clk"]

set_output_delay -max 1.0 [get_ports "sum"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "carry"] -clock [get_clocks "clk"]
```

The screenshot shows a software window titled "half_adder_constraints_top.g". The menu bar includes "File", "Edit", "View", and a settings icon. The main area contains the following Verilog-like timing constraint code:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clk"]

set_output_delay -max 1.0 [get_ports "sum"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "carry"] -clock [get_clocks "clk"]
```

At the bottom of the window, status indicators show "Ln 11, Col 1", "491 characters", "100%", "Unix (LF)", and "UTF-8".

(b) Steps to start *Cadence® Genus*:

- 1.) Open the synthesis folder terminal .
- 2.) run the following commands : 'csh' , 'source /home/install/cshrc' , 'genus -legacy -ui' .

(c) Steps to “load the required libraries, designs and synthesizing those designs”:

- 1.) After opening the genus set the library and rtl folder path by using the commands :

```
'set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/ '
'set_attribute init_rtl_search_path /home/student/Desktop/21BEC1033/rtl/ '
```

- 2.) Now load the library using the command :

```
'set_attribute library slow_vdd1v0_basicCells.lib '
```

- 3.) Now read the counter.v file by using the command : 'read_hdl half_adder.v'
- 4.) Elaborate the design by using the command: 'elaborate'.
- 5.) Now read the timing constraints file by using the command :

```
'read_sdc half_adder_constraints_top.g'
```

- 6.) To synthesize the design run the command:

```
'set_attribute syn_generic_effort medium'
```

```
'syn_generic'
```

```
'set_attribute syn_map_effort high'
```

```
'set_attribute syn_opt_effort high'
```

'syn_map'
'syn_opt'

4. Cadence® Genus Legacy terminal after Synthesis: [Terminal](#)
(click the link for viewing entire terminal)

```
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -legacy_ui
2024/08/01 15:15:35 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/08/01 15:15:35 For more info, please run CheckSysConf in cdsroot/tools.lnx86/bin/checksysconf <productId>
TMPDIR is being set to /tmp/genus\_temp\_11733\_cad21\_student\_UKHKNK
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[15:15:35.095649] Configured Lic search path (21.01-s002): 5280@cadence

Version: 21.14-s082_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui
Date: Thu Aug 01 15:15:35 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64) (12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700 25600KB) (32402340KB)
PID: 11733
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

[15:15:35.407017] Periodic Lic check successful
[15:15:35.407025] Feature usage summary:
[15:15:35.407025] Genus_Synthesis
Checking out license: Genus\_Synthesis

*****
***** Loading tool scripts...
***** Finished loading tool scripts (4 seconds elapsed).

WARNING: This version of the tool is 770 days old.

half_adder_constraints_top.g half_ter.indi + File Edit View
Setting attribute of root '/': init\_hdl\_search\_path = /home/student/Desktop/21BEC1033/lib/
legacy\_genus:/set\_attribute init\_hdl\_search\_path /home/student/Desktop/21BEC1033/rtl/
Setting attribute of root '/': init\_hdl\_search\_path = /home/student/Desktop/21BEC1033/rtl/
legacy\_genus:/set\_attribute library slow_vddiv0_basiccells.lib

Threads Configured: 3

Message Summary for Library slow_vddiv0_basiccells.lib:
*****
Missing a function attribute in the output pin definition. [LBR-518]: 1
*****

Info : Created nominal operating condition. [LBR-412]
: Operating condition '_nominal_' was created for the PVT values (1.000000, 0.900000, 125.000000) in library 'slow_vddiv0_basiccells.lib'.
: The nominal operating condition is represented, either by the nominal PVT values specified in the library source (via nom\_process, nom\_voltage and nom\_temperature respectively), or by the default PVT values (1.0,1.0,1.0).
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "ANTENNA" must have an output pin.
: Add the missing output pin(s), then reload the library. Else the library cell will be marked as timing model i.e. unusable. Timing\_model means that the cell does not have any defined function. If there is no output pin, Genus will mark library cell as unusable i.e. the attribute 'usable' will be marked to 'false' on the libcell. Therefore, the cell is not used for mapping and it will not be picked up from the library for synthesis. If you query the attribute 'unusable\_reason' on the libcell, result will be: 'Library cell has no output pins'. Note: The message LBR-9 is only for the logical pins and not for the power\_ground pins. Genus will depend upon the output function defined in the pin group (output pin) of the cell, to use it for mapping. The pg_pin will not have any function defined.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "ANTENNA" must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "DECAP10" must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "DECAP10" must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "DECAP2" must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "DECAP2" must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "DECAP3" must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "DECAP3" must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "DECAP4" must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell "DFRAPA" must have an output pin.

Ln 23, Col 1 78,742 characters 100% Unix (LF) UFT-8
33°C Mostly cloudy Search L ENG IN 17:54 01-Aug-2024
```

```

half_adder_constraints_top.g half_termini.indi + - O X
File Edit View
Warning : Library cell has no output pins defined. [LBR-9]
: Library cell 'DECAPS' must have an output pin.
Setting attribute of root '/': 'library' = slow_vddive_basiccells.lib
legacy_genus:/> read_hdl [half_adder.v]
legacy_genus:/> elaborate
Library has 324 usable logic and 128 usable sequential lib-cells.
Info : Elaborating Design. [ELAB-1]
: elaborating top-level block 'half_adder' from file '/home/student/Desktop/21BEC1033/rtl/half_adder.v'.
Info : Done Elaborating Design. [ELAB-3]
: Done elaborating 'half_adder'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_elab
| Trick | Accepts | Rejects | Runtime (ms) |
| ume_constant_bmux | 0 | 0 | 0.00 |
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: half_adder, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: half_adder, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_clip_mux_input | 0 | 0 | 0.00 |
| hlo_clip | 0 | 0 | 0.00 |

/designs/half_adder
legacy_genus:/> read_sdc half_adder_constraints_top.sdc
Statistics for commands executed by read_sdc:
"create_clock" - successful 1 , failed 0 (runtime 0.00)
"get_clocks" - successful 6 , failed 0 (runtime 0.00)
"set_clocks" - successful 6 , failed 0 (runtime 0.00)
"set_nurts" - successful 6 , failed 0 (runtime 0.00)
Ln 110, Col 36 78.742 characters

```

```

half_adder_constraints_top.g half_termini.indi + - O X
File Edit View
legacy_genus:/> read_sdc half_adder_constraints_top.sdc
Statistics for commands executed by read_sdc:
"create_clock" - successful 1 , failed 0 (runtime 0.00)
"get_clocks" - successful 6 , failed 0 (runtime 0.00)
"get_ports" - successful 6 , failed 0 (runtime 0.00)
"set_clock_transition" - successful 2 , failed 0 (runtime 0.00)
"set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)
"set_input_delay" - successful 2 , failed 0 (runtime 0.00)
"set_output_delay" - successful 2 , failed 0 (runtime 0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
legacy_genus:/> set_attribute syn_generic_effort medium
Setting attribute of root '/': 'syn_generic_effort' = medium
legacy_genus:/> set_attribute syn_map_effort high
Setting attribute of root '/': 'syn_map_effort' = high
legacy_genus:/> set_attribute syn_opt_effort high
Setting attribute of root '/': 'syn_opt_effort' = high
legacy_genus:/> syn_generic

Stage: pre_early_cg
| Transform | Accepts | Rejects | Runtime (ms) |

##Generic Timing Info for library domain: _default_ typical gate delay: 127.6 ps std_slew: 17.9 ps std_load: 1.0 fF
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: half_adder, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_mux_reorder | 0 | 0 | 0.00 |

Info : Synthesizing. [SYNTH-1]
: Synthesizing 'half_adder' to generic gates using 'medium' effort.
PBS_Generic_Start - Elapsed Time 0, CPU Time 0.0
stamp 'PBS_Generic_Start' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
00:00:00(00:01:45) | 00:00:00(00:00:00) | 0.0% | 15:17:22 (AUG01) | 456.9 MR | PBS_Generic_Start
Ln 148, Col 1 78.742 characters

```

```

half_adder_constraints_top.g half_termini.indi + - O X
File Edit View
| SYNTH-5 | Info | 1 | Done mapping.
| SYNTH-7 | Info | 1 | Incrementally optimizing.
Info : Done incrementally optimizing. [SYNTH-8]
: Done incrementally optimizing 'half_adder'.
legacy_genus:/> write_netlist > half_adder_netlist.v
legacy_genus:/> write_sdc > half_adder.sdc
Finished SDC export. (command execution time mm:ss (real) = 00:00).
legacy_genus:/> gui_show
legacy_genus:/> report_timing > half_adder_timing.rep
legacy_genus:/> report_area > half_adder_area.rep
legacy_genus:/> report_power > half_adder_power.rep
Info : Joules engine is used. [REP-16]
: Joules engine is being used for the command report_power.
Info : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
: half_adder
Info : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info : ACTP-0001 Activity propagation ended for stim#0
Info : PWRRA-0001 [PwrInfo] compute_power effective options
: :mode :vectorless
: :skip_propagation : 1
: :frequency_scaling_factor : 1.0
: :use_clock_freq : stim
: :stim :/stim#0
: :fromGenus : 1
Info : ACTP-0001 Timing initialization started
Info : ACTP-0001 Timing initialization ended
Info : PWRRA-0002 [PwrInfo] Skipping activity propagation due to _skip_ap
: option...
Warning: PWRRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
: flow. Ignoring frequency scaling.
Warning: PWRRA-0304 [PwrWarn] stim option is not applicable with vectorless mode
: of power analysis, ignored this option.
Info : PWRRA-0002 Started 'vectorless' power computation.
Info : PWRRA-0002 Finished power computation.
Info : PWRRA-0007 [PwrInfo] Completed successfully.
: Info=6, Warn=2, Error=0, Fatal=0
Output file: half_adder_power.rep
legacy_genus:/>

Ln 429, Col 56 78.742 characters

```

5. Generate & Read the Reports: (with clear snapshots)

For generating the report run the following commands:

```
report_timing > half_adder_timing.rep
```

```
report_area > half_adder_area.rep
```

```
report_power > half_adder_power.rep
```

half_adder_timing.rep

```
=====
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Aug 01 2024 03:17:59 pm
Module: half_adder
Technology library: slow_vdd1v0 1.0
Operating conditions: PVT_O90V_125C (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====

Pin Type Fanout Load Slew Delay Arrival
(clock clk) launch 0 R
(half_adder constrain_line_6) ext delay +1000 1000 F
b in port 1 0.4 0 +0 1000 F
g44_2398/A 0 +0
g44_2398/S ADDHXI 1 0.3 24 +178 1178 R
sum_reg/D <<< DFFHXQ1 0 +0
sum_reg/CK setup 100 +89 1267 R
(clock clk) capture 10000 R
uncertainty -10 9990 R

Cost Group : 'clk' (path_group 'clk')
Timing slack : 8723ps
Start-point : b
End-point : sum_reg/D
Ln 1, Col 1 1,710 characters 100% Unix (LF) UTF-8
```

Cell Count=3
Cell Area=14.7 sq. units
Power dissipated=0.3 nW

half_adder_power.rep

```
=====
Instance: /half_adder
Power Unit: W
PDB Frames: /stim#0/frame#0

Category Leakage Internal Switching Total Row%
memory 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
register 2.04051e-10 4.03290e-07 0.00000e+00 4.03494e-07 82.54%
latch 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
logic 9.66040e-11 4.00906e-08 1.27575e-08 5.29447e-08 10.83%
bbox 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
clock 0.00000e+00 0.00000e+00 3.24000e-08 3.24000e-08 6.63%
pad 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%
pm 0.00000e+00 0.00000e+00 0.00000e+00 0.00000e+00 0.00%

Subtotal 3.00655e-10 4.43380e-07 4.51575e-08 4.88838e-07 100.00%
Percentage 0.06% 90.70% 9.24% 100.00% 100.00%
```

half_adder_area.rep

```
=====
Generated by: Genus(TM) Synthesis Solution 21.14-s082_1
Generated on: Aug 01 2024 03:18:05 pm
Module: half_adder
Technology library: slow_vdd1v0 1.0
Operating conditions: PVT_O90V_125C (balanced_tree)
Wireload mode: enclosed
Area mode: timing library
=====

Instance Module Cell Count Cell Area Net Area Total Area Wireload
half_adder 3 14.706 0.000 14.706 <none> (D)
(D) = wireload is default in technology library
Ln 1, Col 1 734 characters 100% Unix (LF) UTF-8
```

6. Writing the Output files: (with clear snapshots)

Run the following commands to write the ouput files:

```
write_netlist > half_adder_netlist.v
```

```
write_sdc > half_adder.sdc
```

```

half_adder.sdc

# ##### Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Aug 01 15:17:46 IST 2024 #####
# Set the current design
current_design half_adder

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports a]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports b]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports sum]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports carry]
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.01 [get_ports clk]
set_clock_uncertainty -hold 0.01 [get_ports clk]

Ln 11, Col 1 | 944 characters | 100% | Unix (LF) | UTF-8

```

```

half_adder.sdc          half_adder_netlist.v      +      -      ×
File   Edit   View   ⚙

|
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Aug 1 2024 15:17:38 IST (Aug 1 2024 09:47:38 UTC)

// Verification Directory fv/half_adder

module half_adder(a, b, clk, sum, carry);
    input a, b, clk;
    output sum, carry;
    wire a, b, clk;
    wire sum, carry;
    wire n_0, n_1;
    DFFHQX1 sum_reg(.CK (clk), .D (n_1), .Q (sum));
    DFFQXL carry_reg(.CK (clk), .D (n_0), .Q (carry));
    ADDHX1 g44_2398(.A (b), .B (a), .CO (n_0), .S (n_1));
endmodule

Ln 1, Col 1 | 486 characters | 100% | Unix (LF) | UTF-8

```

7. Method of writing a script file (.tcl) for synthesis:

- 1.) Create a file with .tcl extension in synthesis folder and type the following commands and save it:

```

set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {half_adder.v}

elaborate

```

```

read_sdc half_adder_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > half_adder_netlist.v
write_sdc > half_adder.sdc
gui_show

report_timing > half_adder_timing.rep
report_area > half_adder_area.rep
report_power > half_adder_power.rep

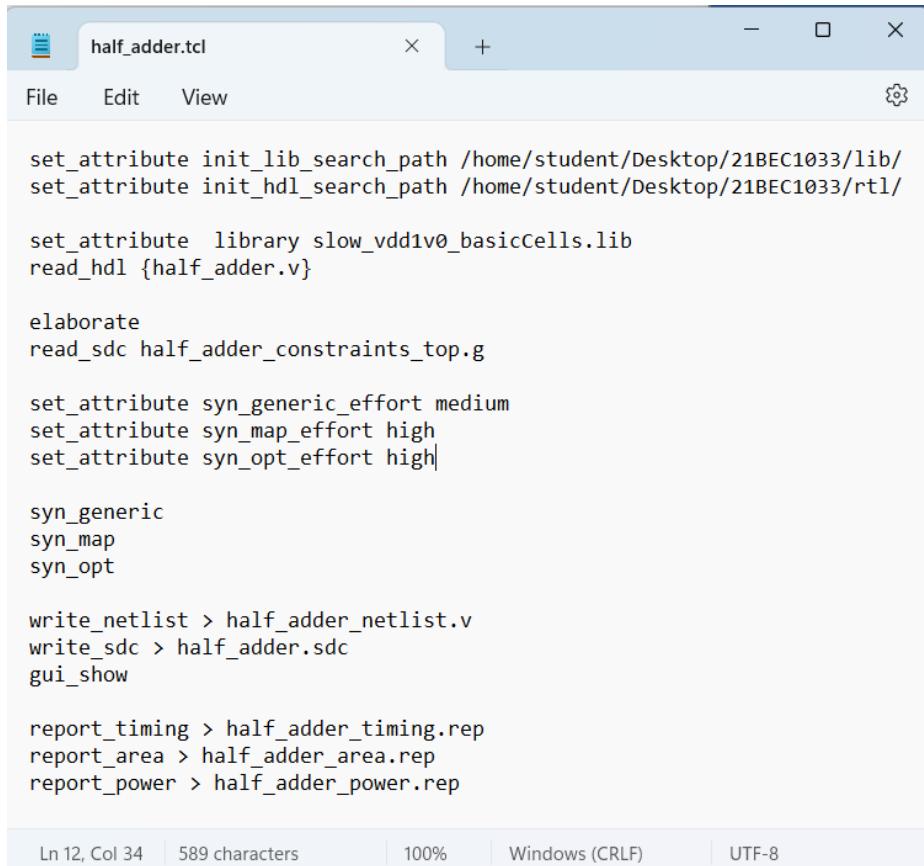
```

2.) After creating the .g and .tcl file open the terminal of synthesis folder and run the following commands:

```

'csh'
'source /home/install/cshrc'
'genus -legacy -ui -f half_adder.tcl' .

```



```

half_adder.tcl
File Edit View
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {half_adder.v}

elaborate
read_sdc half_adder_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

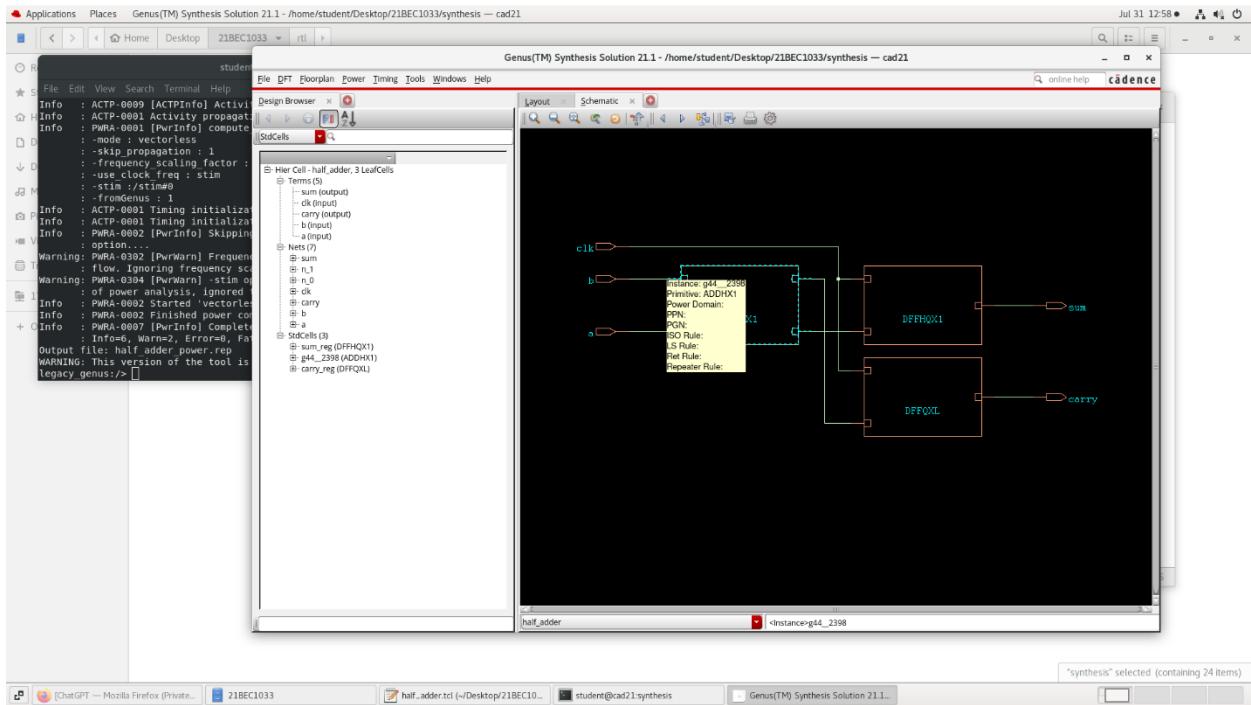
write_netlist > half_adder_netlist.v
write_sdc > half_adder.sdc
gui_show

report_timing > half_adder_timing.rep
report_area > half_adder_area.rep
report_power > half_adder_power.rep

```

Ln 12, Col 34 | 589 characters | 100% | Windows (CRLF) | UTF-8

8. Genus Schematic:



Vellore Institute of Technology, Chennai

BECE407P - ASIC Design

Lab-2

Running the Basic Synthesis Flow using Cadence® Genus

Name of the Student: PRANAV.G

Roll Number: 21BEC1033

Date of the Lab. Class: 25/07/24

1. Aim: To run the basic synthesis flow of full adder using genus.

2. EDA Tools Used:

Cadence® Genus

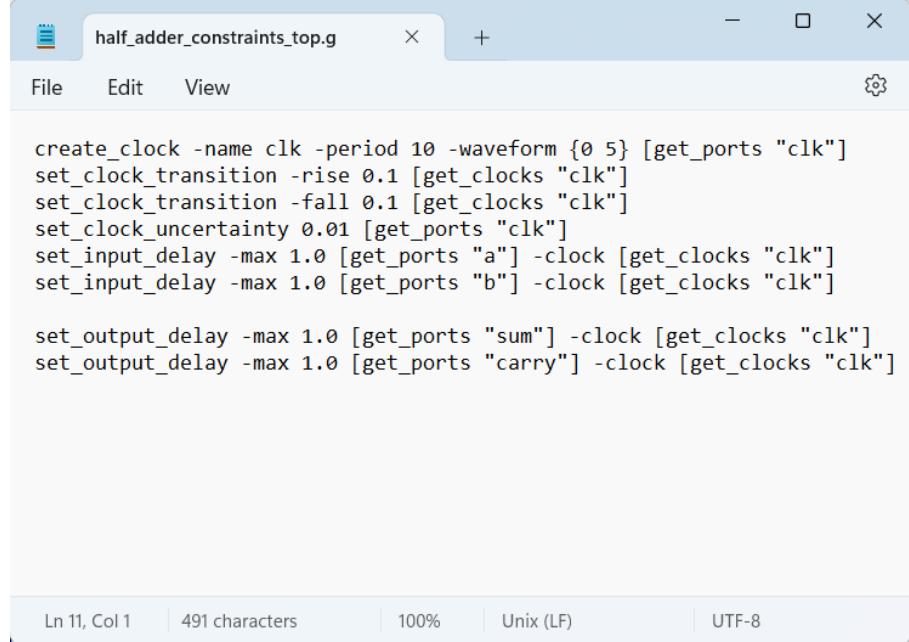
3. Details of the Synthesis Flow: (with clear snapshots)

(a) Method of writing a script file (.g) for input *Timing Constraints*:

1.) Create a file with .g extension in the synthesis folder.

2.) Open it and write the following commands and save it:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "c"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "s"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "c_out"] -clock [get_clocks "clk"]
```



The screenshot shows a terminal window titled "half_adder_constraints_top.g". The window contains a script for setting up timing constraints. The script includes commands for creating a clock, setting clock transitions, input delays, output delays, and uncertainty. The bottom status bar indicates the script is at line 11, column 1, with 491 characters, at 100% zoom, in Unix (LF) mode, and using UTF-8 encoding.

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "a"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "b"] -clock [get_clocks "clk"]

set_output_delay -max 1.0 [get_ports "sum"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "carry"] -clock [get_clocks "clk"]
```

Ln 11, Col 1 | 491 characters | 100% | Unix (LF) | UTF-8

(b) Steps to start *Cadence® Genus*:

- 1.) Open the synthesis folder terminal .
- 2.) run the following commands : 'csh' , 'source /home/install/cshrc' , 'genus -legacy -ui' .

(c) Steps to “load the required libraries, designs and synthesizing those designs”:

- 1.) After opening the genus set the library and rtl folder path by using the commands :

```
'set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/ '
'set_attribute init_rtl_search_path /home/student/Desktop/21BEC1033/rtl/ '
```

- 2.) Now load the library using the command :

```
'set_attribute library slow_vdd1v0_basicCells.lib '
```

- 3.) Now read the counter.v file by using the command : 'read_hdl full_adder.v'
- 4.) Elaborate the design by using the command: 'elaborate'.
- 5.) Now read the timing constraints file by using the command :

```
'read_sdc full_adder_constraints_top.g'
```

- 6.) To synthesize the design run the command:

```
'set_attribute syn_generic_effort medium'
```

```
'syn_generic'
```

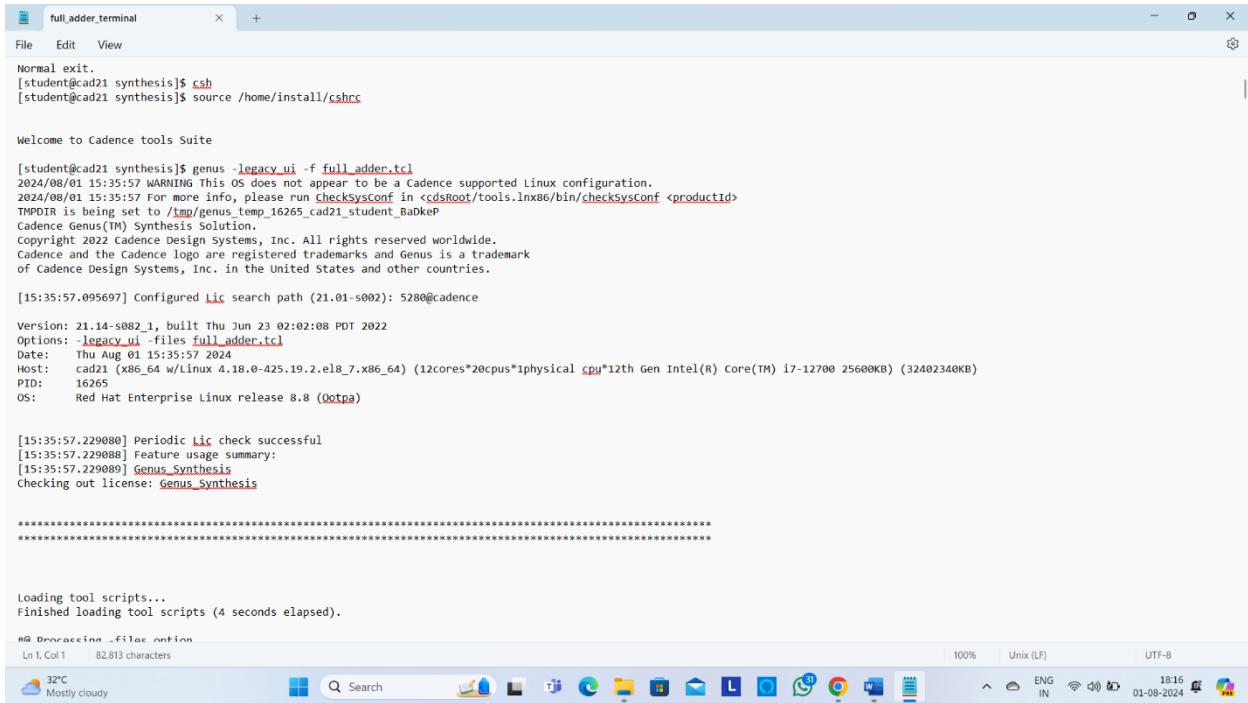
```
'set_attribute syn_map_effort high'
```

```
'set_attribute syn_opt_effort high'
```

```
'syn_map'
```

'syn_opt'

4. Cadence® Genus Legacy terminal after Synthesis: [Terminal](#) (click the link for viewing entire terminal)



```
Normal exit.
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc

Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -legacy_ui -f full_adder.tcl
2024/08/01 15:35:57 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/08/01 15:35:57 For more info, please run checksysConf in <cdsroot>/tools.lnx86/bin/checksysConf <productid>
TMPDIR is being set to /tmp/genus_temp_16265_cad21_student_BdKpe
Cadence Genus(TM) Synthesis Solution.
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of Cadence Design Systems, Inc. in the United States and other countries.

[15:35:57.095697] Configured Lic search path (21.01-s002): 5280@cadence
Version: 21.14-s082.1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files full_adder.tcl
Date: Thu Aug 01 15:35:57 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.e18.7.x86_64) (12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700 25600KB) (32402340KB)
PID: 16265
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

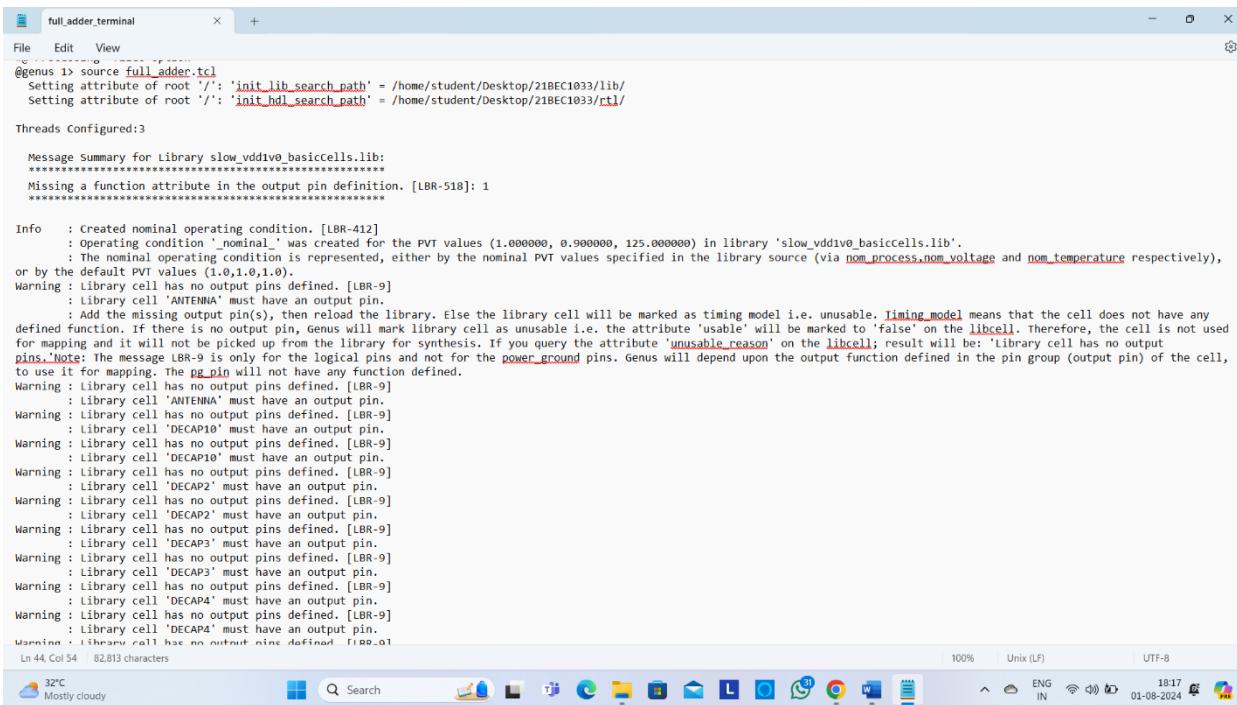
[15:35:57.229080] Periodic Lic check successful
[15:35:57.229080] Feature usage summary:
[15:35:57.229080] Genus_Synthesis
Checking out license: Genus_Synthesis

*****
```

Loading tool scripts...
finished loading tool scripts (4 seconds elapsed).

#@ Deactivation _file option
Ln 1, Col 1 82,813 characters

32°C Mostly cloudy Search L Q T E C M W L 100% Unix (LF) UTF-8 ENG IN 18:16 01-08-2024



```
@genus > source full_adder.tcl
Setting attribute of root '/': 'init_lib_search_path' = /home/student/Desktop/21BEC1033/lib/
Setting attribute of root '/': 'init_hdl_search_path' = /home/student/Desktop/21BEC1033/rtl/
Threads Configured:

Message Summary for Library slow_vddio_basicCells.lib:
*****
Missing a function attribute in the output pin definition. [LBR-518]: 1
*****

Info   : Created nominal operating condition. [LBR-412]
        : Operating condition '_nominal_' was created for the PVT values (1.000000, 0.900000, 125.000000) in library 'slow_vddio_basicCells.lib'.
        : The nominal operating condition is represented, either by the nominal PVT values specified in the library source (via nom_process,nom_voltage and nom_temperature respectively), or by the default PVT values (1.0,1.0,1.0).
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'ANTENNA' must have an output pin.
        : Add the missing output pin(s), then reload the library. Else the library cell will be marked as timing model i.e. unusable. Timing_model means that the cell does not have any defined function. If there is no output pin, Genus will mark library cell as unusable i.e. the attribute 'usable' will be marked to 'false' on the libcell. Therefore, the cell is not used for mapping and it will not be picked up from the library for synthesis. If you query the attribute 'unusable_reason' on the libcell; result will be: 'Library cell has no output pins.' Note: The message LBR-9 is only for the logical pins and not for the power_ground pins. Genus will depend upon the output function defined in the pin group (output pin) of the cell, to use it for mapping. The pg_pin will not have any function defined.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'ANTENNA' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP10' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP10' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP2' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP2' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP3' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP3' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP4' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP4' must have an output pin.
Warning : Library cell has no output pins defined. [LBR-9]
        : Library cell 'DECAP5' must have an output pin.
Ln 44, Col 54 82,813 characters
```

32°C Mostly cloudy Search L Q T E C M W L 100% Unix (LF) UTF-8 ENG IN 18:17 01-08-2024

full_adder_terminal

```

File Edit View
: library cell 'DECAP9' must have an output pin.
Setting attribute of root '/': 'library' = slow_vddive0/basicCells.lib
Library has 324 usable logic and 128 usable sequential lib-cells.
Info : Elaborating Design. [ELAB-1]
: Elaborating top-level block 'full_adder' from file '/home/student/Desktop/21BEC103/rtl/full_adder.v'.
Warning : In legacy_Ui mode, Genus creates a blackbox as description for a module is not found. Black boxes represent unresolved references in the design and are usually not expected.
Another possible reason is, some libraries are not read and the tool could not get the content for some macros or lib_cells. [CDFG-428]
: A blackbox was created for instance 'ui' in file '/home/student/Desktop/21BEC103/rtl/full_adder.v' on line 5.
: Check the kind of module a black box is. If it is a lib_cell or a macro, check why the corresponding .lib was not read in. This could be either due to a missing or faulty file or
due to an incomplete init_lib_search_path attribute value making restricting access to the missing file. If it is a module of your design, verify whether the path to this module is a part
of the files you read or else check that the init_hdl_search_path attribute is not missing some paths.
Info : Done Elaborating Design. [ELAB-3]
: Done elaborating "full_adder".
Warning : Black-boxes are represented as unresolved references in the design. [TUI-273]
: Cannot resolve reference to 'half_adder'.
: Run check_design to get all unresolved instances. To resolve the reference, either load a technology library containing the cell by appending to the 'library' attribute, or read
in the .hdl file containing the module before performing elaboration. As the design is incomplete, synthesis results may not correspond to the entire design.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_elab
| Trick | Accepts | Rejects | Runtime (ms) |
| none_constant_bmux | 0 | 0 | 0.00 |
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: full_adder, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: full_adder, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
| Transform | Accepts | Rejects | Runtime (ms) |
| blo_clip_mux_input | 0 | 0 | 0.00 |
| blo_clip | 0 | 0 | 0.00 |
Ln 81, Col 59 82.813 characters
100% Unix (LF) UTF-8
```

full_adder_terminal

```

File Edit View
| Transform | Accepts | Rejects | Runtime (ms) |
| blo_clip_mux_input | 0 | 0 | 0.00 |
| blo_clip | 0 | 0 | 0.00 |
Statistics for commands executed by read_sdc:
"create_clock" - successful 1 , failed 0 (runtime 0.00)
"get_clocks" - successful 7 , failed 0 (runtime 0.00)
"get_ports" - successful 7 , failed 0 (runtime 0.00)
"set_clock_transition" - successful 2 , failed 0 (runtime 0.00)
"set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)
"set_input_delay" - successful 3 , failed 0 (runtime 0.00)
"set_output_delay" - successful 2 , failed 0 (runtime 0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
Setting attribute of root '/': 'syn_generic_effort' = medium
Setting attribute of root '/': 'syn_map_effort' = high
Setting attribute of root '/': 'syn_opt_effort' = high

Stage: pre_early_cg
| Transform | Accepts | Rejects | Runtime (ms) |

##Generic Timing Info for library domain: default_typical_gate_delay: 127.6 ps std_slew: 17.9 ps std_load: 1.0 fF
Starting mux data reorder optimization [v1.0] (stage: pre_to_gen_setup, startdef: full_adder, recur: true)
Completed mux data reorder optimization (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: pre_to_gen_setup
| Transform | Accepts | Rejects | Runtime (ms) |
| blo_mux_reorder | 0 | 0 | 0.00 |
Info : Synthesizing. [SYNTH-1]
: Synthesizing 'full_adder' to generic gates using 'medium' effort.
PBS_Generic_Start - Elapsed Time 0, CPU Time 0.0
stamp 'PBS_Generic_Start' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
-----+-----+-----+-----+-----+-----+
00:00:00(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 15:36:01 (Aug01) | 241.8 MB | PBS_Generic_Start
Ln 160, Col 32 82.813 characters
100% Unix (LF) UTF-8
```

full_adder_terminal

```

File Edit View
| CPI-506 | Warning | 1 | Command 'commit_power_intent' cannot proceed as
| | | there is no power intent loaded.
| PA-7 | Info | 4 | Resetting power analysis results.
| | | All computed switching activities are removed.
| SYNTH-5 | Info | 1 | Done mapping.
| SYNTH-7 | Info | 1 | Incrementally optimizing.

Info : Done incrementally optimizing. [SYNTH-8]
: Done incrementally optimizing 'full_adder'.
Finished SDC export (command execution time rmss (real) = 00:00).
Info : Joules engine is used. [RPT-16]
Info : Joules engine is being used for the command report_power.
Info : ACTP-0001 [ACTPInfo] Activity propagation started for stim#0 netlist
: full_adder
Info : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%
Info : ACTP-0001 Activity propagation ended for stim#0
Info : PWRA-0001 [PwrInfo] compute_power effective options
: -mode : vectorless
: -skip_propagation : 1
: -frequency_scaling_factor : 1.0
: -use_clock_freq : stim
: -stim : /stim#0
: -fromGenus : 1
Info : ACTP-0001 timing initialization started
Info : ACTP-0001 timing initialization ended
Info : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap
: option...
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
: flow. Ignoring frequency scaling.
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with vectorless mode
: of power analysis, ignored this option.
Info : PWRA-0002 Started 'vectorless' power computation.
Info : PWRA-0002 Finished power computation.
Info : PWRA-0007 [PwrInfo] Completed successfully.
: Info=6, Warn=2, Error=0, Fatal=0
Output file: full_adder_power.rep
WARNING: This version of the tool is 770 days old.
legacy_genus:/>
Lic Summary:
[15:36:32.077672] CdsLmd servers: cadence
[15:36:32.077681] Feature usage summary:
Ln 1253, Col 2 82.813 characters
100% Unix (LF) ENG IN 18:19 01-08-2024
```

5. Generate & Read the Reports: (with clear snapshots)

For generating the report run the following commands:

```
report_timing > full_adder_timing.rep
```

```
report_area > full_adder_area.rep
```

```
report_power > full_adder_power.rep
```

The screenshot shows three Microsoft Word documents side-by-side, each containing a synthesis report for a full adder.

- full_adder_timing.rep**: This document contains timing analysis data. It includes a table of pin details and a summary section:
 - Cell Count=3
 - Cell Area=12.3 sq. units
 - Power dissipated=0.2 nW
- full_adder_area.rep**: This document contains area analysis data. It includes a table of instance details and a summary section:
 - Cell Count=3
 - Cell Area=12.3 sq. units
 - Power dissipated=0.2 nW
- full_adder_power.rep**: This document contains power analysis data. It includes a table of category details and a summary section:
 - Cell Count=3
 - Cell Area=12.3 sq. units
 - Power dissipated=0.2 nW

6. Writing the Output files: (with clear snapshots)

Run the following commands to write the output files:

```
write_netlist > full_adder_netlist.v
```

```
write_sdc > full_adder.sdc
```

```
# #####  
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Aug 01 15:36:03 IST 2024  
# #####  
set sdc_version 2.0  
set_units -capacitance 1000ff  
set_units -time 1000ps  
# Set the current design  
current_design full_adder  
create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]  
set_clock_transition 0.1 [get_clocks clk]  
set_clock_gating_check -setup 0.0  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports a]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports b]  
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports c]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports s]  
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports c_out]  
set_wire_load_mode "enclosed"  
set_clock_uncertainty -setup 0.01 [get_ports clk]  
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1  
// Generated on: Aug 1 2024 15:36:03 IST (Aug 1 2024 10:06:03 UTC)  
  
// Verification Directory fv/full_adder  
  
module full_adder(a, b, c, clk, s, c_out);  
    input a, b, c, clk;  
    output s, c_out;  
    wire a, b, c, clk;  
    wire s, c_out;  
    wire n_0, \w[0] , \w[1] , \w[2] , \w[3] ;  
    half_adder u1(a, b, clk, \w[0] , \w[1] );  
    half_adder u2(\w[0] , c, clk, \w[2] , \w[3] );  
    DFFQXL c_out_reg(.CK (clk), .D (n_0), .Q (c_out));  
    DFFQXL s_reg(.CK (clk), .D (\w[2] ), .Q (s));  
    OR2X1 g17_2398(.A (\w[1] ), .B (\w[3] ), .Y (n_0));  
endmodule
```

7. Method of writing a script file (.tcl) for synthesis:

- 1.) Create a file with .tcl extension in synthesis folder and type the following commands and save it:

```
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/  
  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl {full_adder.v}
```

```

elaborate
read_sdc full_adder_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > full_adder_netlist.v
write_sdc > full_adder.sdc
gui_show

report_timing > full_adder_timing.rep
report_area > full_adder_area.rep
report_power > full_adder_power.rep

```

2.) After creating the .g and .tcl file open the terminal of synthesis folder and run the following commands:

```

'csh'
'source /home/install/cshrc'
'genus -legacy -ui -f full_adder.tcl' .

```

```

full_adder_netlist.v          full_adder.tcl      x  +  -  □  ×
File   Edit   View
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/
set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {full_adder.v}

elaborate
read_sdc full_adder_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

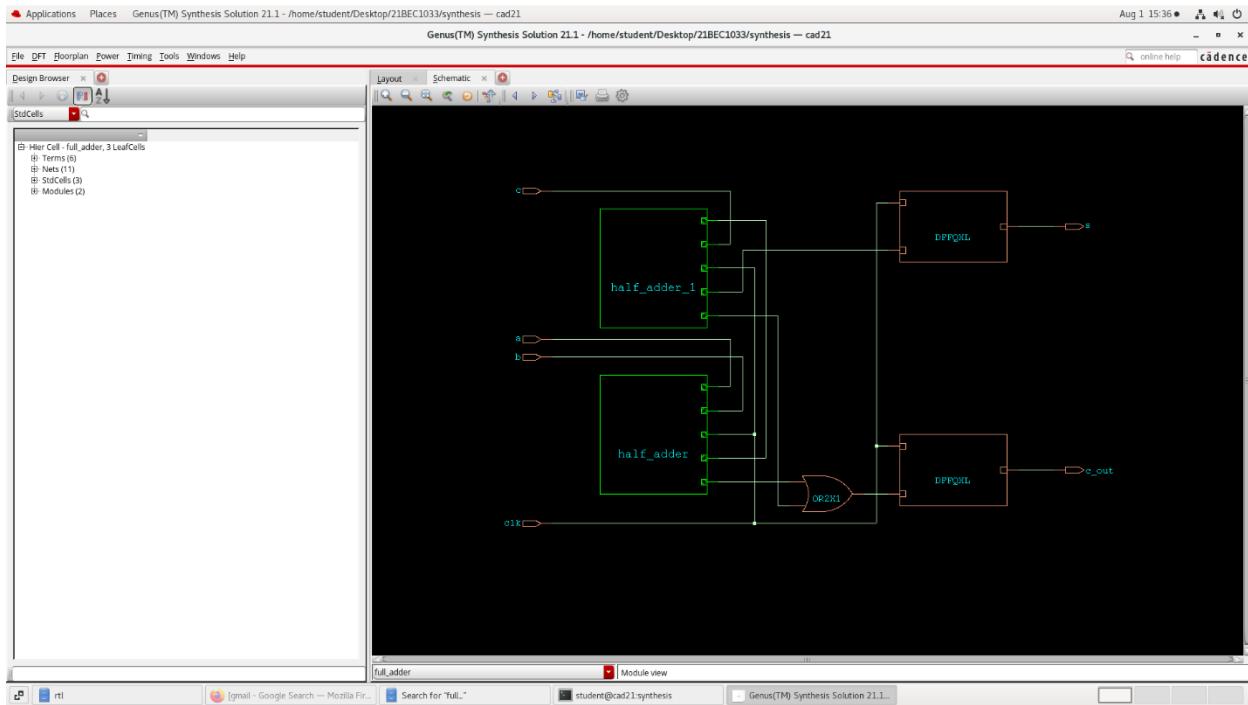
write_netlist > full_adder_netlist.v
write_sdc > full_adder.sdc
gui_show

report_timing > full_adder_timing.rep
report_area > full_adder_area.rep
report_power > full_adder_power.rep

```

Ln 14, Col 12 | 589 characters | 100% | Windows (CRLF) | UTF-8

8. Genus Schematic:



Vellore Institute of Technology, Chennai

BECE407P - ASIC Design

Lab-2

Running the Basic Synthesis Flow using Cadence® Genus

Name of the Student: PRANAV.G

Roll Number: 21BEC1033

Date of the Lab. Class: 25/07/24

1. Aim: To run the basic synthesis flow of sr flip flop using genus.

2. EDA Tools Used:

Cadence® Genus

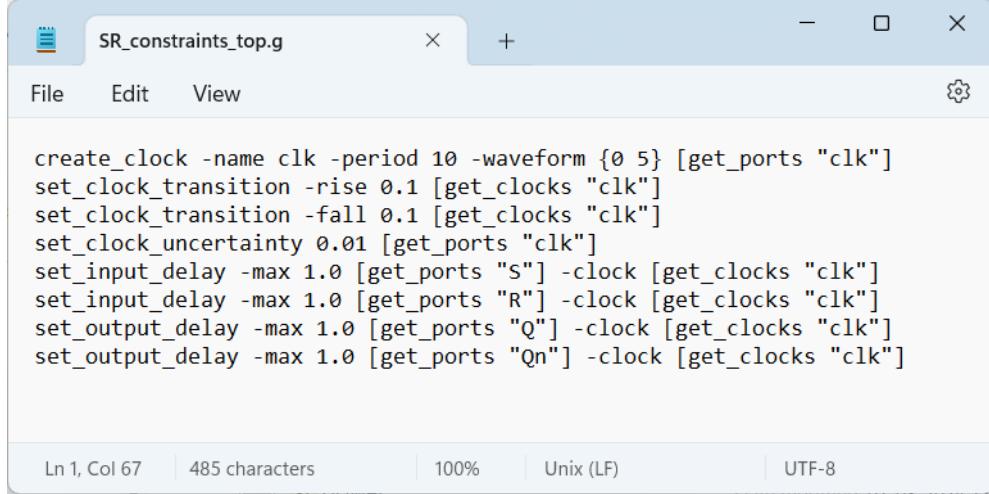
3. Details of the Synthesis Flow: (with clear snapshots)

(a) Method of writing a script file (.g) for input *Timing Constraints*:

1.) Create a file with .g extension in the synthesis folder.

2.) Open it and write the following commands and save it:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "S"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "R"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "Q"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "Qn"] -clock [get_clocks "clk"]
```



The screenshot shows a Cadence Genus editor window titled "SR_constraints_top.g". The code in the editor is a timing constraints file (SDC) containing the following commands:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]
set_input_delay -max 1.0 [get_ports "S"] -clock [get_clocks "clk"]
set_input_delay -max 1.0 [get_ports "R"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "Q"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "Qn"] -clock [get_clocks "clk"]
```

The status bar at the bottom of the window displays: Ln 1, Col 67 | 485 characters | 100% | Unix (LF) | UTF-8.

(b) Steps to start *Cadence® Genus*:

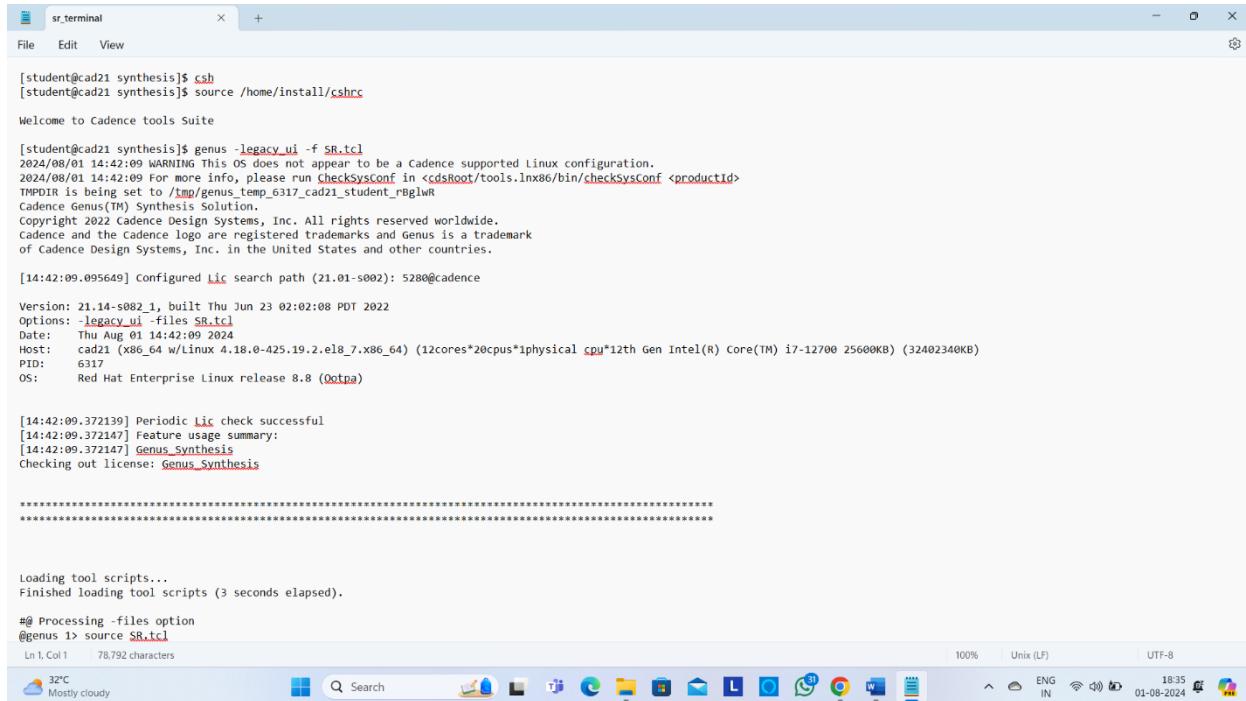
- 1.) Open the synthesis folder terminal .
- 2.) run the following commands : 'csh' , 'source /home/install/cshrc' , 'genus -legacy -ui' .

(c) Steps to “load the required libraries, designs and synthesizing those designs”:

- 1.) After opening the genus set the library and rtl folder path by using the commands :
`'set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/ '`
`'set_attribute init_rtl_search_path /home/student/Desktop/21BEC1033/rtl/ '`
- 2.) Now load the library using the command :
`'set_attribute library slow_vdd1v0_basicCells.lib '`
- 3.) Now read the counter.v file by using the command : 'read_hdl sr_flip_flop.v'
- 4.) Elaborate the design by using the command: 'elaborate'.
- 5.) Now read the timing constraints file by using the command :
`'read_sdc SR_constraints_top.g'`
- 6.) To synthesize the design run the command:
`'set_attribute syn_generic_effort medium'`
`'syn_generic'`
`'set_attribute syn_map_effort high'`
`'set_attribute syn_opt_effort high'`

`'syn_map'`
`'syn_opt'`

4. Cadence® Genus Legacy terminal after Synthesis: [Terminal](#) (click the link for viewing entire terminal)



```
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc
Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -f SR.tcl
2024/08/01 14:42:09 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/08/01 14:42:09 For more info, please run checkSysConf in <cdsRoot/tools.lnx86/bin/checkSysConf <productid>
TMPDIR is being set to /tmp/genus_temp_6317_cad21_student_rBglwR
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[14:42:09.095649] Configured Lic search path (21.01-s002): 5280@cadence
Version: 21.14-s082_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files SR.tcl
Date: Thu Aug 01 14:42:09 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64) (12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700 25600KB) (32402340KB)
PID: 6317
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

[14:42:09.372139] Periodic Lic check successful
[14:42:09.372147] Feature usage summary:
[14:42:09.372147] Genus_Synthesis
Checking out license: Genus_Synthesis

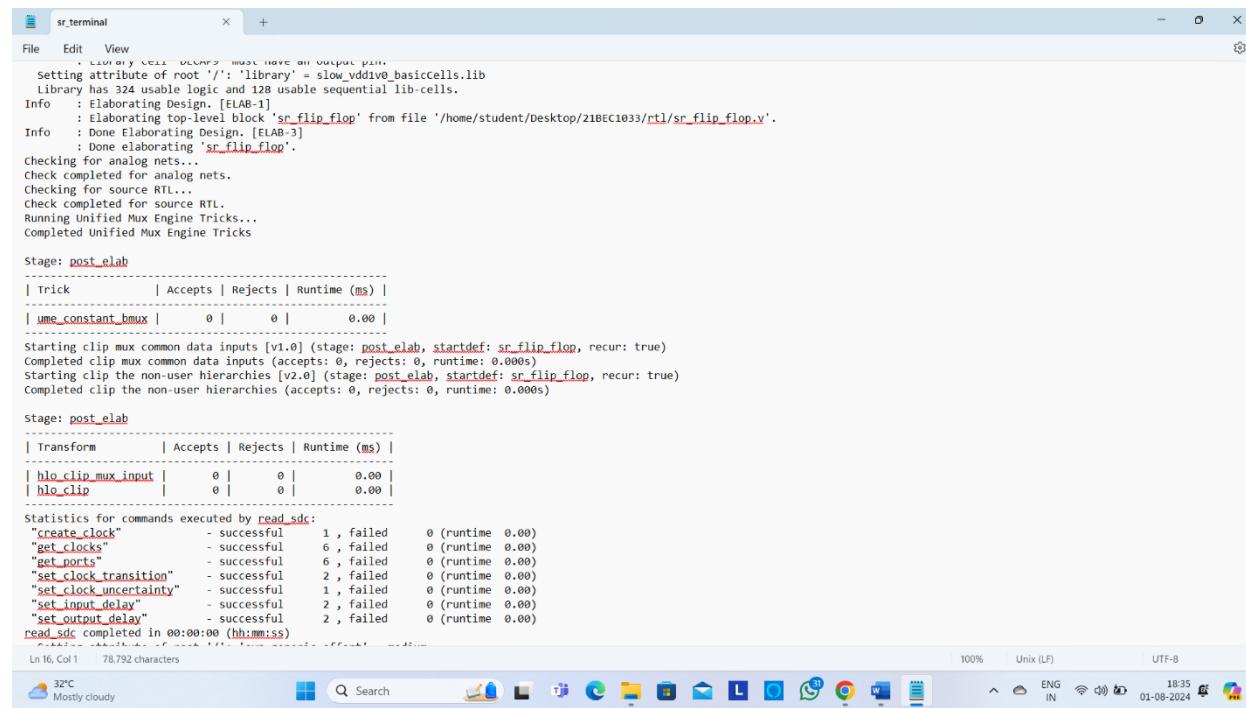
*****
```

Loading tool scripts...
Finished loading tool scripts (3 seconds elapsed).

#@ Processing -files option
@genus 1> source SR.tcl
Ln 1, Col 1 78.792 characters

100% Unix (LF) UTF-8

32°C Mostly cloudy Search L E M W 18:35 IN 01-08-2024



```
. Library cell DEOPS must have an output pin.
Setting attribute of root '/': 'library' = slow_vddio_basiccells.lib
Library has 324 usable logic and 128 usable sequential lib-cells.
Info : Elaborating Design. [ELAB-1]
      : Elaborating top-level block 'sr_flip_flop' from file '/home/student/Desktop/21BEC1033/rtl/sr_flip_flop.v'.
Info : Done Elaborating Design. [ELAB-3]
      : Done elaborating 'sr_flip_flop'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_elab
-----| Trick | Accepts | Rejects | Runtime (ms) |
| ume_constant_bmux | 0 | 0 | 0.00 |
-----Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: sr_flip_flop, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: sr_flip_flop, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
-----| Transform | Accepts | Rejects | Runtime (ms) |
| hlo_clip_mux_input | 0 | 0 | 0.00 |
| hlo_clip | 0 | 0 | 0.00 |
-----Statistics for commands executed by read_sdc:
"create_clock" - successful 1 , failed 0 (runtime 0.00)
"get_clocks" - successful 6 , failed 0 (runtime 0.00)
"get_ports" - successful 6 , failed 0 (runtime 0.00)
"set_clock_transition" - successful 2 , failed 0 (runtime 0.00)
"set_clock_uncertainty" - successful 1 , failed 0 (runtime 0.00)
"set_input_delay" - successful 2 , failed 0 (runtime 0.00)
"set_output_delay" - successful 2 , failed 0 (runtime 0.00)
read_sdc completed in 00:00:00 (hh:mm:ss)
Ln 16, Col 1 78.792 characters
```

100% Unix (LF) UTF-8

32°C Mostly cloudy Search L E M W 18:35 IN 01-08-2024

```

File Edit View
Trick Calls Accepts Attempts Time(secs)
-----
hi_fo_buf 0 ( 0 / 0 ) 0.00

Incremental optimization status
=====
Group
Tot WRST Total - - DRC Totals -
Operation Area Weighted Slacks Slack Neg Max Max
init_delay 19 0 0 0 0 0 Cap
-----
Trick Calls Accepts Attempts Time(secs)
-----
crit_upsz 0 ( 0 / 0 ) 0.00
plc_bal_star 0 ( 0 / 0 ) 0.00
drc_buf_timb 0 ( 0 / 0 ) 0.00
plc_st 0 ( 0 / 0 ) 0.00
plc_st_fence 0 ( 0 / 0 ) 0.00
plc_star 0 ( 0 / 0 ) 0.00
plc_laf_st 0 ( 0 / 0 ) 0.00
plc_laf_st_fence 0 ( 0 / 0 ) 0.00
drc_buf_tims 0 ( 0 / 0 ) 0.00
fopt 0 ( 0 / 0 ) 0.00
plc_laf_lo_st 0 ( 0 / 0 ) 0.00
plc_lo_st 0 ( 0 / 0 ) 0.00
mb_split 0 ( 0 / 0 ) 0.00

Local TNS optimization status
=====
Group
Tot WRST Total - - DRC Totals -
Operation Area Weighted Slacks Slack Neg Max Max
init_tns 19 0 0 0 0 0 Cap
-----
Trick Calls Accepts Attempts Time(secs)
-----
```

sr_terminal

File	Edit	View	Message Text
	Id	<u>Severity</u>	count
CFM-1 Info 1 Wrote dofile.			
CFM-5 Info 1 Wrote formal verification information.			
CPI-506 Warning 1 Command 'commit_power_intent' cannot proceed as there is no power intent loaded.			
PA-7 Info 4 Resetting power analysis results. All computed switching activities are removed.			
SYNTH-5 Info 1 Done mapping.			
SYNTH-7 Info 1 Incrementally optimizing.			
Info : Done incrementally optimizing. [SYNTH-8]			
: Done incrementally optimizing 'sr_flip_flop'.			
Finished SDC export (command execution time mm:ss (real) = 00:00).			
Info : Joules engine is used. [RPT-16]			
: Joules engine is being used for the command report_power.			
Info : ACTP-0001 [ACPIInfo] Activity propagation started for stim#0 netlist : sr_flip_flop			
Info : ACTP-0009 [ACTPInfo] Activity Propagation Progress Report : 100%			
Info : ACTP-0001 Activity propagation ended for stim#0			
Info : PWRA-0001 [PwrInfo] compute_power effective options : -mode : vectorless : -skip_propagation : 1 : -frequency_scaling_factor : 1.0 : -user_clock_freq : stim : -stim : /stim#0 : -fromGenus : 1			
Info : ACTP-0001 Timing initialization started			
Info : ACTP-0002 Timing initialization ended			
Info : PWRA-0002 [PwrInfo] Skipping activity propagation due to -skip_ap option....			
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for <u>vectorless</u> flow. Ignoring frequency scaling.			
Warning: PWRA-0304 [PwrWarn] -stim option is not applicable with <u>vectorless</u> mode of power analysis, ignored this option.			
Info : PWRA-0002 Started <u>vectorless</u> power computation.			
Info : PWRA-0002 Finished power computation.			
Info : PWRA-0007 [PwrInfo] Completed successfully. : Info=6, Warn=2, Error=0, Fatal=0			
Output file: sr_power.rep			
WARNING: This version of the tool is 770 days old.			

Ln 707, Col 54 78,792 characters

100% Unix (LF) UTF-8

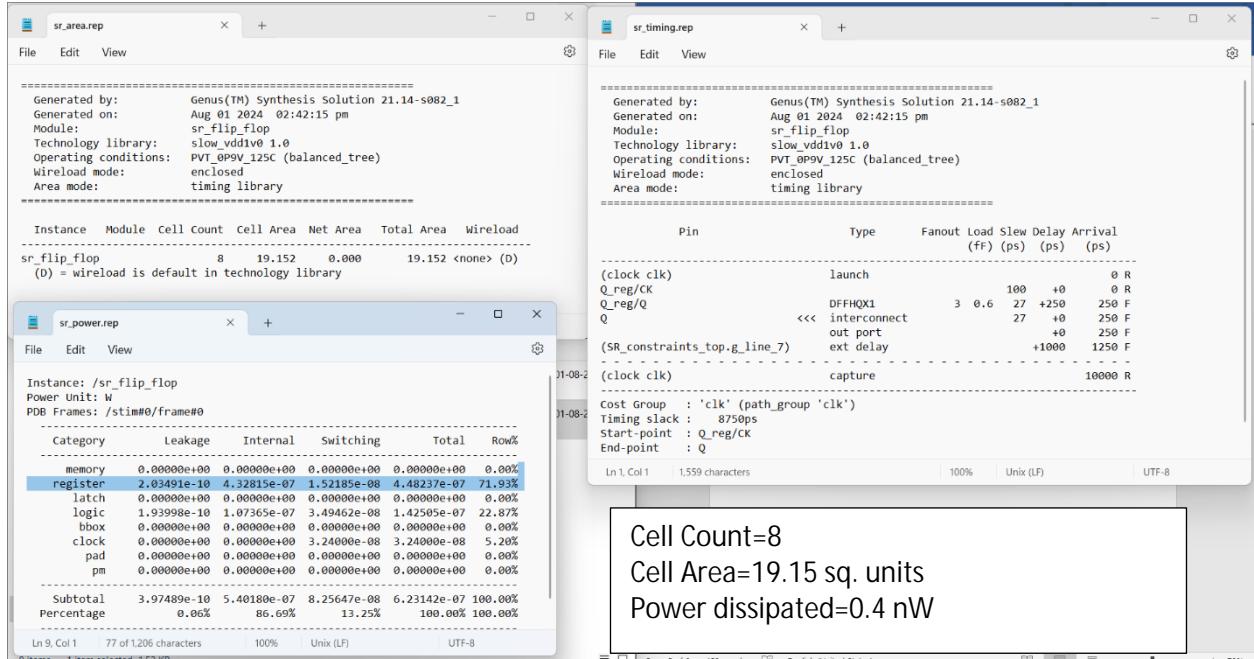
5. Generate & Read the Reports: (with clear snapshots)

For generating the report run the following commands:

```
report_timing > sr_timing.rep
```

```
report_area > sr_area.rep
```

```
report_power > sr_power.rep
```



6. Writing the Output files: (with clear snapshots)

Run the following commands to write the output files:

```
write_netlist > sr_netlist.v
```

```
write_sdc > sr.sdc
```

```

sr.sdc

# ######
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Aug 01 14:42:14 IST 2024
# #####
set sdc_version 2.0

set_units -capacitance 1000fF
set_units -time 1000ps

# Set the current design
current_design sr_flip_flop

create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]
set_clock_transition 0.1 [get_clocks clk]
set_clock_gating_check -setup 0.0
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports S]
set_input_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports R]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports Q]
set_output_delay -clock [get_clocks clk] -add_delay -max 1.0 [get_ports Qn]
set_wire_load_mode "enclosed"
set_clock_uncertainty -setup 0.01 [get_ports clk]
set_clock_uncertainty -hold 0.01 [get_ports clk]

```

Ln 1, Col 1 | 941 characters | 100% | Unix (LF) | UTF-8

```

sr_netlist.v

// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1
// Generated on: Aug 1 2024 14:42:14 IST (Aug 1 2024 09:12:14 UTC)

// Verification Directory fv/sr_flip_flop

module sr_flip_flop(S, R, clk, Q, Qn);
    input S, R, clk;
    output Q, Qn;
    wire S, R, clk;
    wire Q, Qn;
    wire n_0, n_1, n_2, n_3, n_4, n_5;
    DFFQXL Qn_reg(.CK (clk), .D (n_4), .Q (Qn));
    DFFHQX1 Q_reg(.CK (clk), .D (n_5), .Q (Q));
    OAI21X1 g168_2398(.A0 (R), .A1 (n_2), .B0 (n_0), .Y (n_5));
    OAI2BB1X1 g169_5107(.A0N (R), .A1N (n_1), .B0 (n_3), .Y (n_4));
    NAND2BX1 g170_6260(.AN (S), .B (Qn), .Y (n_3));
    NOR2X1 g171_4319(.A (S), .B (Q), .Y (n_2));
    NAND2BXL g172_8428(.AN (Qn), .B (S), .Y (n_1));
    NAND2X1 g173_5526(.A (S), .B (Q), .Y (n_0));
endmodule

```

Ln 6, Col 1 | 755 characters | 100% | Unix (LF) | UTF-8

7. Method of writing a script file (.tcl) for synthesis:

- 1.) Create a file with .tcl extension in synthesis folder and type the following commands and save it:

```

set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {sr_flip_flop.v}

```

```

elaborate
read_sdc SR_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > sr_netlist.v
write_sdc > sr.sdc
gui_show

report_timing > sr_timing.rep
report_area > sr_area.rep
report_power > sr_power.rep

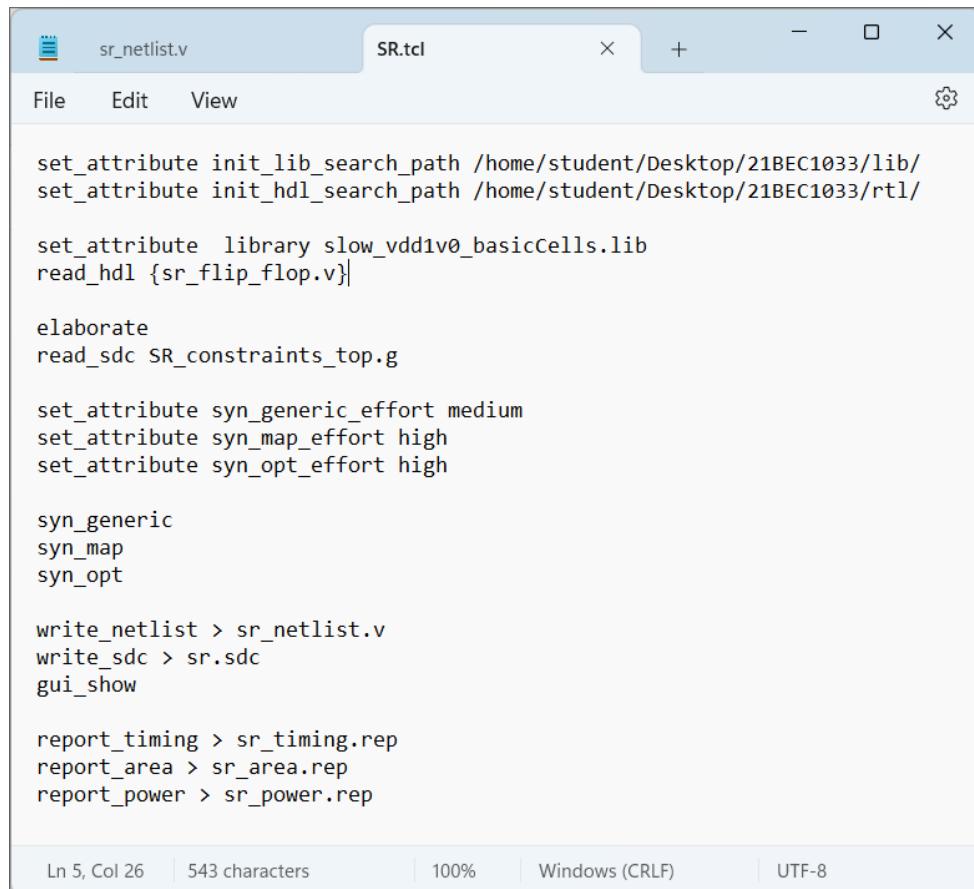
```

2.) After creating the .g and .tcl file open the terminal of synthesis folder and run the following commands:

```

'csh'
'source /home/install/cshrc'
'genus -legacy -ui -f SR.tcl'.

```



```

sr_netlist.v SR.tcl × + − □ ×
File Edit View ⚙
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {sr_flip_flop.v}

elaborate
read_sdc SR_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

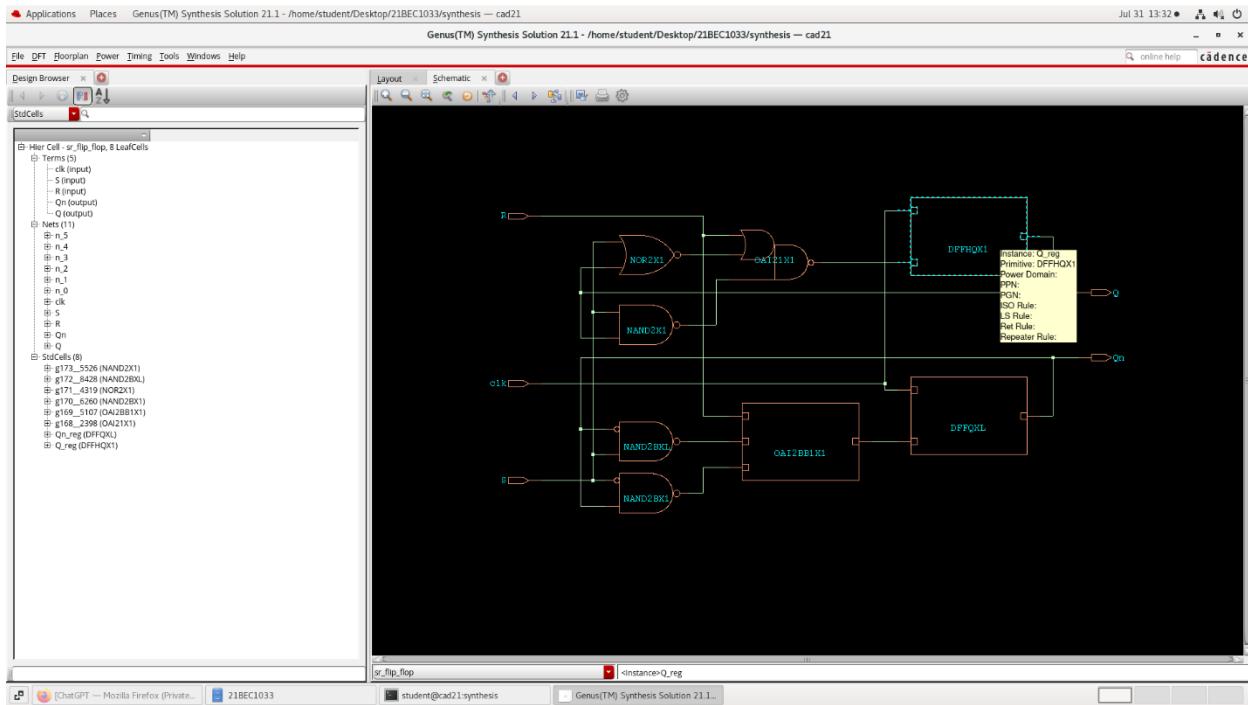
write_netlist > sr_netlist.v
write_sdc > sr.sdc
gui_show

report_timing > sr_timing.rep
report_area > sr_area.rep
report_power > sr_power.rep

```

Ln 5, Col 26 | 543 characters | 100% | Windows (CRLF) | UTF-8

8. Genus Schematic:



Vellore Institute of Technology, Chennai
BECE407P - ASIC Design
Lab-2

Running the Basic Synthesis Flow using Cadence® Genus

Name of the Student: PRANAV.G

Roll Number: 21BEC1033

Date of the Lab. Class: 25/07/24

1. Aim: To run the basic synthesis flow of d flip flop using genus.

2. EDA Tools Used:

Cadence® Genus

3. Details of the Synthesis Flow: (with clear snapshots)

(a) Method of writing a script file (.g) for input *Timing Constraints*:

1.) Create a file with .g extension in the synthesis folder.

2.) Open it and write the following commands and save it:

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "D"] -clock [get_clocks "clk"]

set_output_delay -max 1.0 [get_ports "Q"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "Qn"] -clock [get_clocks "clk"]
```

The screenshot shows a window titled "d_constraints_top.g" containing Verilog-like timing constraint code. The code includes commands like "create_clock", "set_clock_transition", "set_input_delay", and "set_output_delay". The window has a standard OS X-style interface with a menu bar (File, Edit, View) and status bar (Ln 6, Col 59, 419 characters, 100%, Unix (LF), UTF-8).

```
create_clock -name clk -period 10 -waveform {0 5} [get_ports "clk"]
set_clock_transition -rise 0.1 [get_clocks "clk"]
set_clock_transition -fall 0.1 [get_clocks "clk"]
set_clock_uncertainty 0.01 [get_ports "clk"]

set_input_delay -max 1.0 [get_ports "D"] -clock [get_clocks "clk"]

set_output_delay -max 1.0 [get_ports "Q"] -clock [get_clocks "clk"]
set_output_delay -max 1.0 [get_ports "Qn"] -clock [get_clocks "clk"]
```

(b) Steps to start *Cadence® Genus*:

- 1.) Open the synthesis folder terminal .
- 2.) run the following commands : 'csh' , 'source /home/install/cshrc' , 'genus -legacy -ui' .

(c) Steps to “load the required libraries, designs and synthesizing those designs”:

- 1.) After opening the genus set the library and rtl folder path by using the commands :

```
'set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/ '
'set_attribute init_rtl_search_path /home/student/Desktop/21BEC1033/rtl/ '
```

- 2.) Now load the library using the command :

```
'set_attribute library slow_vdd1v0_basicCells.lib '
```

- 3.) Now read the counter.v file by using the command : 'read_hdl d_flip_flop.v'
- 4.) Elaborate the design by using the command: 'elaborate'.
- 5.) Now read the timing constraints file by using the command :

```
'read_sdc d_constraints_top.g'
```

- 6.) To synthesize the design run the command:

```
'set_attribute syn_generic_effort medium'
'syn_generic'
'set_attribute syn_map_effort high'
'set_attribute syn_opt_effort high'
```

```
'syn_map'
'syn_opt'
```

4. Cadence® Genus Legacy terminal after Synthesis: [Terminal](#) (click the link for viewing entire terminal)

```
[student@cad21 synthesis]$ csh
[student@cad21 synthesis]$ source /home/install/cshrc
Welcome to Cadence tools Suite

[student@cad21 synthesis]$ genus -legacy_ui -f D.tcl
2024/08/01 14:44:22 WARNING This OS does not appear to be a Cadence supported Linux configuration.
2024/08/01 14:44:22 For more info, please run checkSysConf in <cdsRoot>/tools.lnx86/bin/checkSysConf <productId>
TMPDIR is being set to /tmp/genus-temp_7596_cad21_student_NrxdjC
Cadence Genus(TM) Synthesis Solution.
Copyright 2022 Cadence Design Systems, Inc. All rights reserved worldwide.
Cadence and the Cadence logo are registered trademarks and Genus is a trademark
of Cadence Design Systems, Inc. in the United States and other countries.

[14:44:23.095633] Configured Lic search path (21.01-s002): 5280@cadence
Version: 21.14-s082_1, built Thu Jun 23 02:02:08 PDT 2022
Options: -legacy_ui -files D.tcl
Date: Thu Aug 01 14:44:23 2024
Host: cad21 (x86_64 w/Linux 4.18.0-425.19.2.el8_7.x86_64) (12cores*20cpus*1physical cpu*12th Gen Intel(R) Core(TM) i7-12700 25600KB) (32402340KB)
PID: 7596
OS: Red Hat Enterprise Linux release 8.8 (Ootpa)

[14:44:23.207474] Periodic Lic check successful
[14:44:23.207475] Feature usage summary:
[14:44:23.207475] Genus_Synthesis
Checking out license: Genus_Synthesis

*****
***** Loading tool scripts...
***** Finished loading tool scripts (3 seconds elapsed).

#@ Processing -files option
@genus 1> source D.tcl
Ln 1, Col 1     81,848 characters
100% Unix (LF) UTF-8
32°C Mostly cloudy  Search  L  C  W  18:48 IN 01-08-2024
```

```
File Edit View
Setting attribute of root '/': 'library' = slow_vddive_basicCells.lib
Library has 324 usable logic and 128 usable sequential lib-cells.
Info : Elaborating Design. [ELAB-1]
      : Elaborating top-level block 'd_flip_flop' from file '/home/student/Desktop/21BEC1033/rtl/d_flip_flop.v'.
Info : Done Elaborating Design. [ELAB-3]
      : Done elaborating 'd_flip_flop'.
Checking for analog nets...
Check completed for analog nets.
Checking for source RTL...
Check completed for source RTL.
Running Unified Mux Engine Tricks...
Completed Unified Mux Engine Tricks

Stage: post_elab
| Trick           | Accepts | Rejects | Runtime (ms) |
| ume_constant_bmux |    0 |    0 |      0.00 |
Starting clip mux common data inputs [v1.0] (stage: post_elab, startdef: d_flip_flop, recur: true)
Completed clip mux common data inputs (accepts: 0, rejects: 0, runtime: 0.000s)
Starting clip the non-user hierarchies [v2.0] (stage: post_elab, startdef: d_flip_flop, recur: true)
Completed clip the non-user hierarchies (accepts: 0, rejects: 0, runtime: 0.000s)

Stage: post_elab
| Transform        | Accepts | Rejects | Runtime (ms) |
| hio_clip_mux_input |    0 |    0 |      0.00 |
| hio_clip          |    0 |    0 |      0.00 |

Warning : Could not find requested search value, [SOC-208] [get_ports]
      : The 'get_ports' command on line '6' of the SDC file 'd_constraints_top.sdc' cannot find any ports named 'D'
      : Use get_*_commands to find the objects along with a wild card entry in the name of the object to check if the object is existing with different naming style.
Error : Invalid SDC command option combination. [SOC-204] [set_io_delay]
      : The 'set_io_delay' command does not accept empty ports lists
      : This option is not valid for the indicated SDC command. Check the SDC command and contact Cadence customer support if you believe this option combination should be supported.
Error : could not interpret SDC command. [SOC-202] [read_sdc]
      : The 'read_sdc' command encountered an error while processing this command on line '6' of the SDC file 'd_constraints_top.sdc': set_input_delay -max 1.0 [get_ports 'D'] -clock [get_clocks 'clk']
      : The 'read_sdc' command encountered a problem while trying to evaluate an SDC command. This SDC command will be added to the Tcl variable $::de::sdc failed commands.
Ln 56, Col 416 81,848 characters
100% Unix (LF) UTF-8
32°C Mostly cloudy  Search  L  C  W  18:48 IN 01-08-2024
```

```

d_terminal x +
File Edit View
Group
Tot Wst Total - - DRC Totals - -
Operation Total Weighted Area Slacks Slack Trans Max Max Cap
init_tns 12 0 0 0 0 0 0 0

Trick Calls Accepts Attempts Time(secs)
--- plc_bal_star 0 ( 0 / 0 ) 0.00
drc_buftimb 0 ( 0 / 0 ) 0.00
drc_buftims 0 ( 0 / 0 ) 0.00
crit_upsz 0 ( 0 / 0 ) 0.00
plc_laf_lo_st 0 ( 0 / 0 ) 0.00
plc_lo_st 0 ( 0 / 0 ) 0.00
fopt 0 ( 0 / 0 ) 0.00
crit_dnsz 0 ( 0 / 0 ) 0.00
dup 0 ( 0 / 0 ) 0.00
setup_dn 0 ( 0 / 0 ) 0.00
mb_split 0 ( 0 / 0 ) 0.00

PBS_TechMap-Postmap Cleanup - Elapsed Time 0, CPU Time -2.0000000000131024e-5
stamp 'PBS_TechMap-Postmap Cleanup' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
--- 00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Generic-start
00:00:03(00:00:02) | 00:00:00(00:00:00) | -0.1( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Generic_Opt-Post
00:00:03(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Generic_Postgen HBO Optimizations
00:00:04(00:00:02) | 00:00:01(00:00:00) | 100.2( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_TechMap-start
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_TechMap_Premap HBO Optimizations
00:00:04(00:00:02) | 00:00:00(00:00:00) | -0.1( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Techmap_Global Mapping
00:00:04(00:00:03) | 00:00:00(00:00:01) | 0.0(100.0) | 14:44:28 (Aug01) | 247.0 MB | PBS_TechMap-Datapath Postmap Operations
00:00:04(00:00:03) | -01:59:59(00:00:00) | -0.0( 0.0) | 14:44:28 (Aug01) | 247.0 MB | PBS_TechMap_Postmap HBO Optimizations

Ln 619, Col 50 81.848 characters
100% Unix (LF) UTF-8
ENG IN 18:48 01-08-2024

```

```

d_terminal x +
File Edit View
- Scan type 0 0.0
- No suitable cell 0 0.0
State Retention instances 0 0.0

INFO: skipping constant propagation
PBS_Techmap-Global Mapping - Elapsed Time 0, CPU Time -0.000536000000000314
stamp 'PBS_Techmap-Global Mapping' being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
--- 00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Generic-start
00:00:03(00:00:02) | 00:00:00(00:00:00) | -0.1( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Generic_Opt-Post
00:00:03(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Generic-Postgen HBO Optimizations
00:00:04(00:00:02) | 00:00:01(00:00:00) | 100.1( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_TechMap-start
00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_TechMap_Premap HBO Optimizations
00:00:04(00:00:02) | 00:00:00(00:00:00) | -0.1( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Techmap-Global Mapping

Number of threads: 8 * 1 (id: pbs_debug, time_info v1.57)
Info: (*) indicates data that was populated from previously saved time_info database
Info: CPU time includes time of parent + longest thread
Warning: Command 'commit_power_intent' cannot proceed as there is no power intent loaded. [CPI-506]
Info : Command 'commit_power_intent' requires a valid power_intent to be loaded.
Info : Wrote formal verification information. [CFM-5]
Info : Wrote 'fv/d_flip_flop/fv_map fv.json' for netlist 'fv/d_flip_flop/fv_map.v.gz'.
Info : Existing file found, Copied as fv/d_flip_flop/rtl_to_fv_map.dv~.
Info : Wrote dofile. [CFM-1]
: Dofile is 'fv/d_flip_flop/rtl_to_fv_map.dv'.
: Alias mapping flow is enabled.
PBS_TechMap-Datapath Postmap Operations - Elapsed Time 1, CPU Time 0.0
stamp 'PBS_TechMap-Datapath Postmap' Operations being created for table 'pbs_debug'

Total Time (Wall) | Stage Time (Wall) | % (Wall) | Date - Time | Memory | Stage
--- 00:00:04(00:00:02) | 00:00:00(00:00:00) | 0.0( 0.0) | 14:44:27 (Aug01) | 247.0 MB | PBS_Generic-start

Ln 113, Col 49 81.848 characters
100% Unix (LF) UTF-8
32°C Mostly cloudy
ENG IN 18:48 01-08-2024

```

```

d_terminal x +
File Edit View
| Id | Sev | Count | Message Text |
| CFM-1 | Info | 1 | Wrote dofile.
| CFM-5 | Info | 1 | Wrote formal verification information.
| CPI-506 | Warning | 1 | Command 'commit_power_intent' cannot proceed as
| | | | there is no power intent loaded.
| PA-7 | Info | 4 | Resetting power analysis results.
| | | | All computed switching activities are removed.
| SYNTH-5 | Info | 1 | Done mapping.
| SYNTH-7 | Info | 1 | Incrementally optimizing.

Info : Done incrementally optimizing. [SYNTH-8]
: Done incrementally optimizing 'd_flip_flop'.
Finished SDC export (command execution time mmiss (real) = 00:00).
Info : Joules engine is used. [RPT-16]
: Joules engine is being used for the command report_power.
Info : ACTP-0001 [ACTInfo] Activity propagation started for stim#0 netlist
: d_flip_flop
Info : ACTP-0009 [ACTInfo] Activity Propagation Progress Report : 100%
Info : ACTP-0000 Activity propagation ended for stim#0
Info : PWRA-0002 [PwrInfo] compute_power effective options
: -mod : vectorless
: -skip_propagation : 1
: -frequency_scaling_factor : 1.0
: -use_clock_freq : stim
: -stim : stim#0
: -fromGenus : 1
Info : ACTP-0001 Timing initialization started
Info : ACTP-0001 Timing initialization ended
Info : PWRA-0002 [PwrInfo] skipping activity propagation due to -skip_ap
: option...
Warning: PWRA-0302 [PwrWarn] Frequency scaling is not applicable for vectorless
: flow. Ignoring frequency scaling.
Warning: PWRA-0303 [PwrWarn] -stim option is not applicable with vectorless mode
: of power analysis, ignored this option.
Info : PWRA-0002 Started 'vectorless' power computation.
Info : PWRA-0002 Finished power computation.
Info : PWRA-0007 [PwrInfo] Completed successfully.
: Info=6, Warn=2, Error=0, Fatal=0
Output file: d_power.rep
WARNING: This version of the tool is 770 days old.

Ln 776, Col 52 81.848 characters
100% Unix (LF) UTF-8
32°C Mostly cloudy
ENG IN 18:49 01-08-2024

```

5. Generate & Read the Reports: (with clear snapshots)

For generating the report run the following commands:

```
report_timing > d_timing.rep
```

```
report_area > d_area.rep
```

```
report_power > d_power.rep
```

The screenshot shows three terminal windows side-by-side:

- d_power.rep**: Power consumption report for instance /d_flip_flop. It includes a detailed breakdown of leakage, internal, and switching power by category (memory, register, latch, logic, bbox, clock, pad, pm) and a summary table.
- d_timing.rep**: Timing report for instance /d_flip_flop. It lists timing parameters for pins (clock clk, q_bar_reg/CK, q_bar_reg/Q, q_bar) including launch, fanout, load, slew, delay, and arrival times.
- d_area.rep**: Area report for instance /d_flip_flop. It provides a summary of cell counts, areas, and wireloads.

A callout box highlights the following metrics from the timing report:

Cell Count=3
Cell Area=11.63 sq. units
Power dissipated=0.25 nW

6. Writing the Output files: (with clear snapshots)

Run the following commands to write the output files:

```
write_netlist > d_netlist.v
```

```
write_sdc > d.sdc
```

```
# #####  
# Created by Genus(TM) Synthesis Solution 21.14-s082_1 on Thu Aug 01 14:44:28 IST 2024  
# #####  
  
set sdc_version 2.0  
  
set_units -capacitance 1000fF  
set_units -time 1000ps  
  
# Set the current design  
current_design d_flip_flop  
  
create_clock -name "clk" -period 10.0 -waveform {0.0 5.0} [get_ports clk]  
set_clock_transition 0.1 [get_clocks clk]  
set_clock_gating_check -setup 0.0  
set_wire_load_mode "enclosed"  
set_clock_uncertainty -setup 0.01 [get_ports clk]  
set_clock_uncertainty -hold 0.01 [get_ports clk]
```

Ln 1, Col 1 641 characters 100% Unix (LF) UTF-8

```
// Generated by Cadence Genus(TM) Synthesis Solution 21.14-s082_1  
// Generated on: Aug 1 2024 14:44:28 IST (Aug 1 2024 09:14:28 UTC)  
  
// Verification Directory fv/d_flip_flop  
  
module d_flip_flop(clk, d, q, q_bar);  
    input clk, d;  
    output q, q_bar;  
    wire clk, d;  
    wire q, q_bar;  
    wire n_0;  
    DFFHQX1 q_bar_reg(.CK (clk), .D (n_0), .Q (q_bar));  
    DFFHQX1 q_reg(.CK (clk), .D (d), .Q (q));  
    INVXL g6(.A (d), .Y (n_0));  
endmodule
```

Ln 18, Col 1 436 characters 100% Unix (LF) UTF-8

7. Method of writing a script file (.tcl) for synthesis:

- 1.) Create a file with .tcl extension in synthesis folder and type the following commands and save it:

```
set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/  
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/  
  
set_attribute library slow_vdd1v0_basicCells.lib  
read_hdl {d_flip_flop.v}
```

```

elaborate
read_sdc d_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > d_netlist.v
write_sdc > d.sdc
gui_show

report_timing > d_timing.rep
report_area > d_area.rep
report_power > d_power.rep

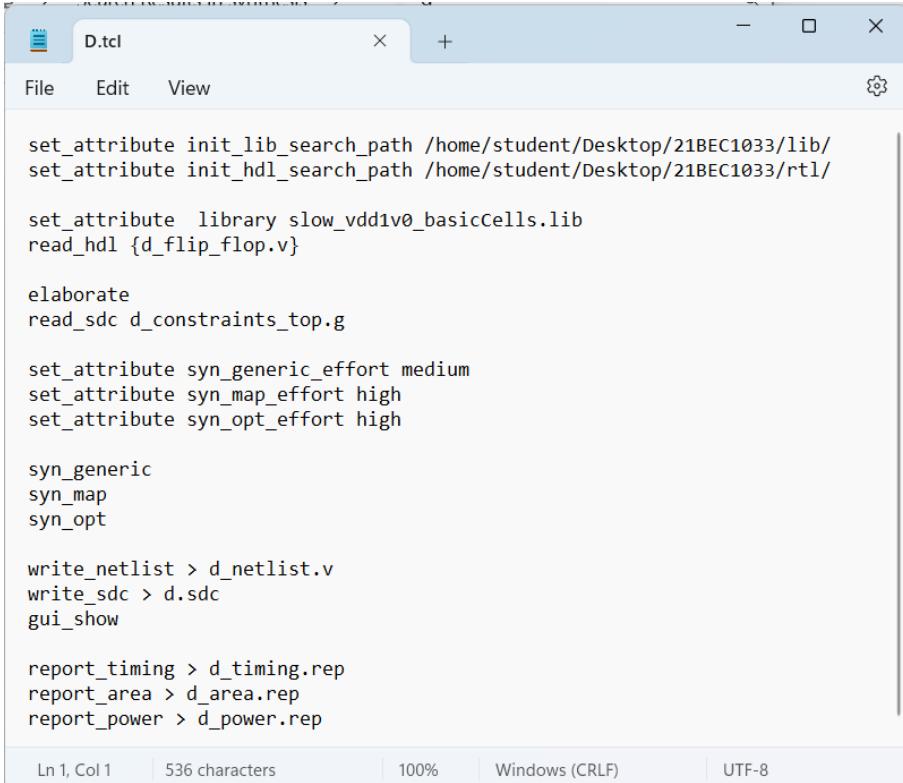
```

2.) After creating the .g and .tcl file open the terminal of synthesis folder and run the following commands:

```

'csh'
'source /home/install/cshrc'
'genus -legacy -ui -f D.tcl' .

```



```

D.tcl

File Edit View

set_attribute init_lib_search_path /home/student/Desktop/21BEC1033/lib/
set_attribute init_hdl_search_path /home/student/Desktop/21BEC1033/rtl/

set_attribute library slow_vdd1v0_basicCells.lib
read_hdl {d_flip_flop.v}

elaborate
read_sdc d_constraints_top.g

set_attribute syn_generic_effort medium
set_attribute syn_map_effort high
set_attribute syn_opt_effort high

syn_generic
syn_map
syn_opt

write_netlist > d_netlist.v
write_sdc > d.sdc
gui_show

report_timing > d_timing.rep
report_area > d_area.rep
report_power > d_power.rep

```

Ln 1, Col 1 | 536 characters | 100% | Windows (CRLF) | UTF-8

8. Genus Schematic:

