BECE407E ASIC DESIGN

Timing Analysis

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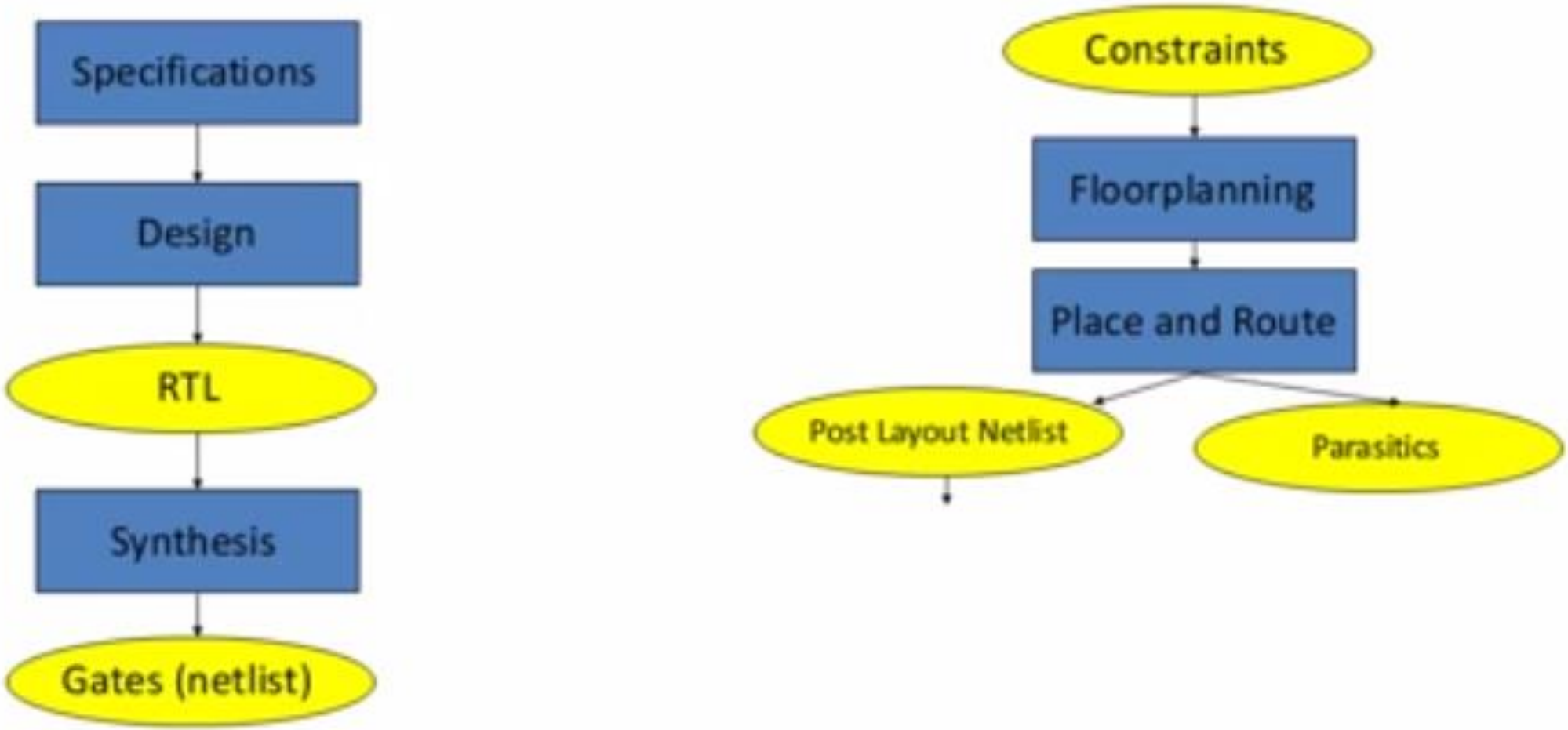
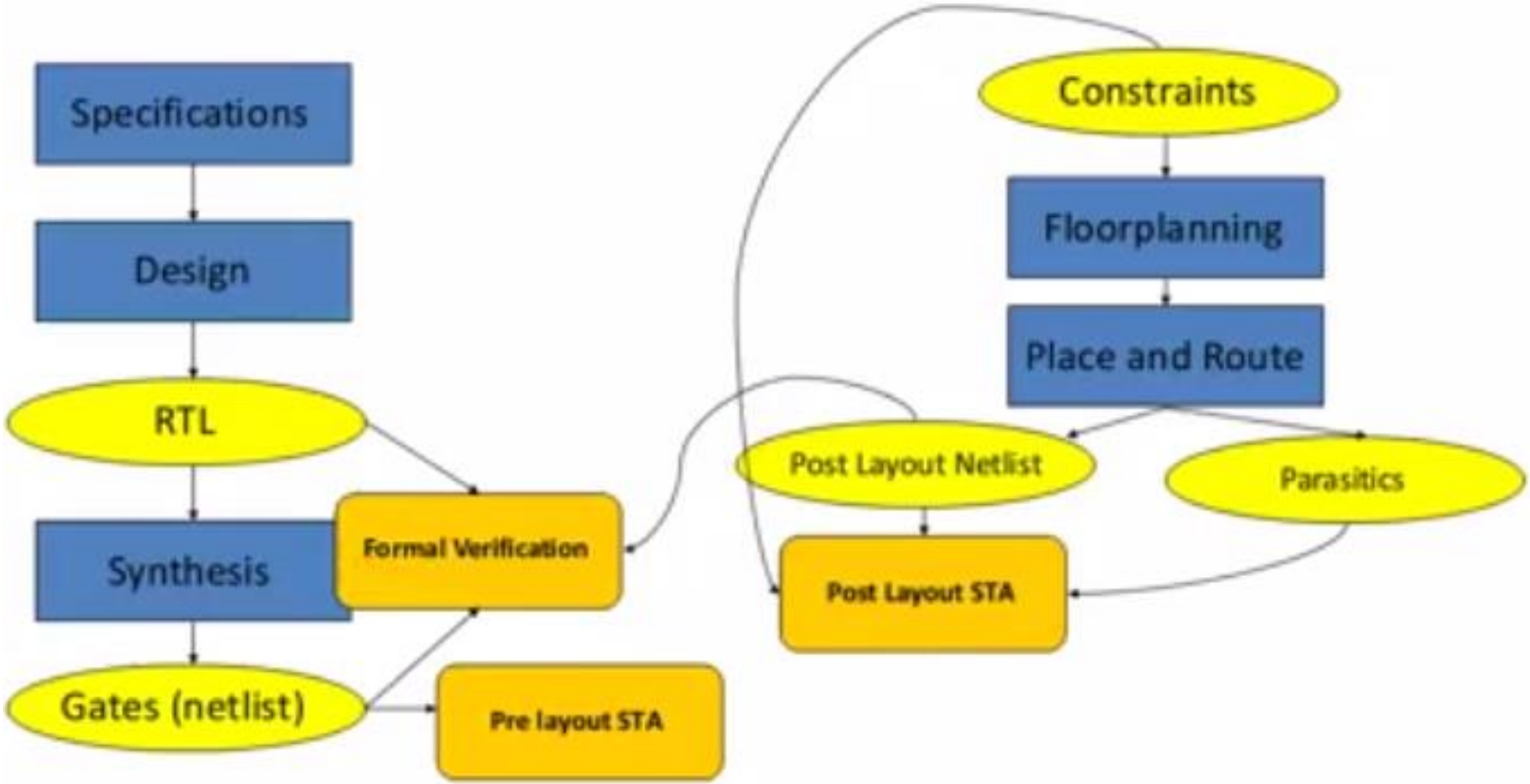
Static Timing Analysis

- STA in ASIC Design Flow
- Operating Conditions
- Timing Paths
- Constraints
  - Setup
  - Hold
  - Recovery
  - Removal
- Clocks
- Exceptions
- STA Flow

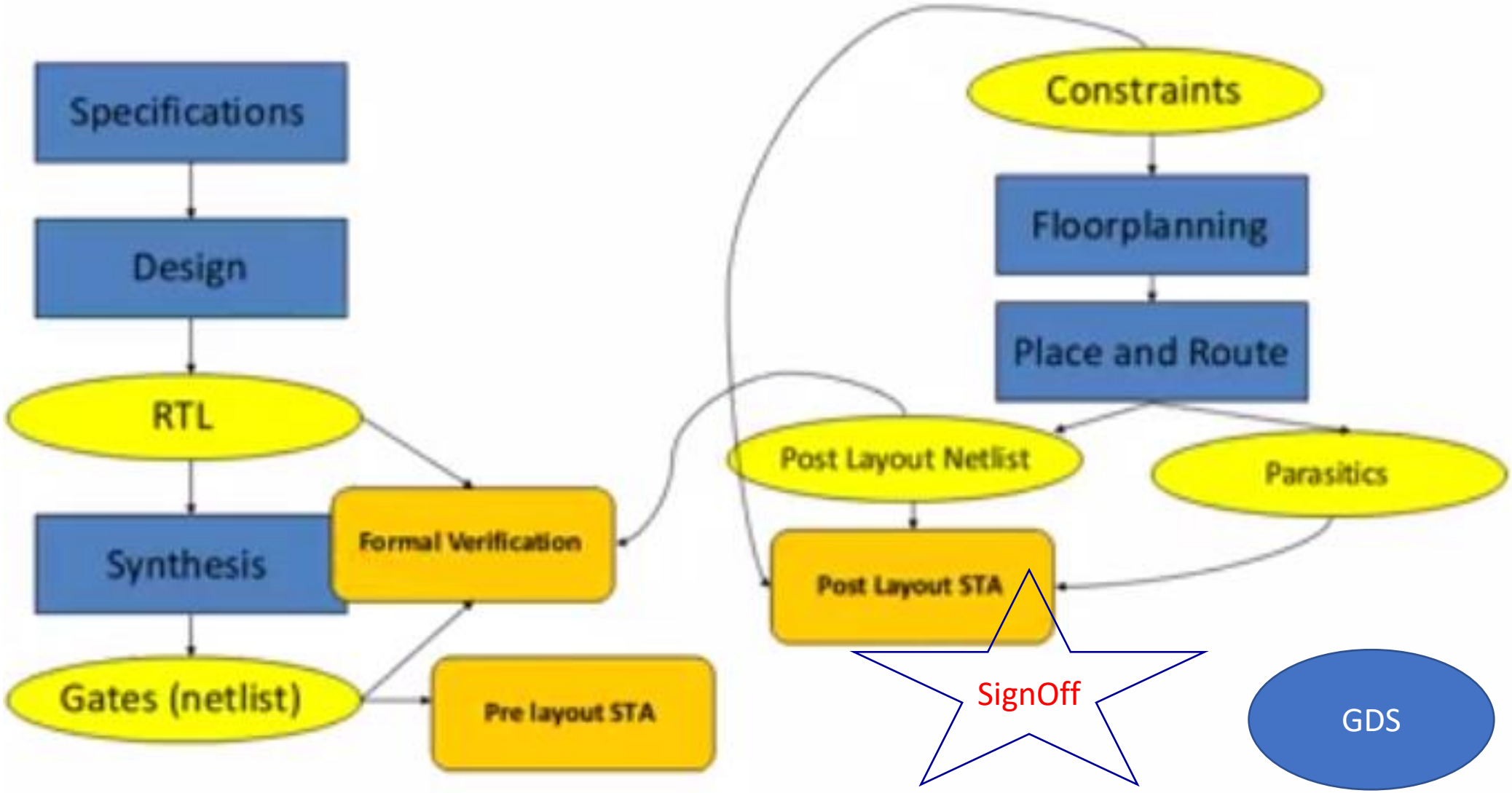
ASIC Design Flow



ASIC Design Flow



ASIC Design Flow



What STA checks

- Salient points
  - Checks all the possible paths. Not vector driven
  - Checking quite fast compared to dynamic timing simulation. However does not replace simulation completely.
  - Does not check functionality
  - STA = Delay Calculation + Timing Checks
- Types of checking performed
  - Setup, hold, recovery, and removal constraints
  - User-specified data-to-data timing constraints
  - Clock-gating setup and hold constraints
  - Minimum period and minimum pulse width for clocks
  - Design rules (minimum/maximum transition time, capacitance and fanout)

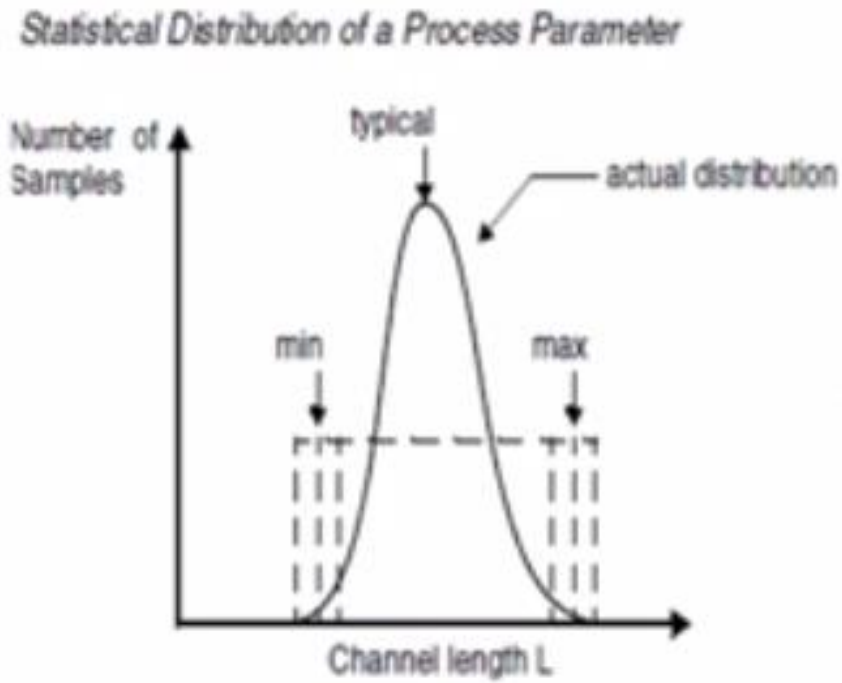
Operating Conditions (P, V, T)

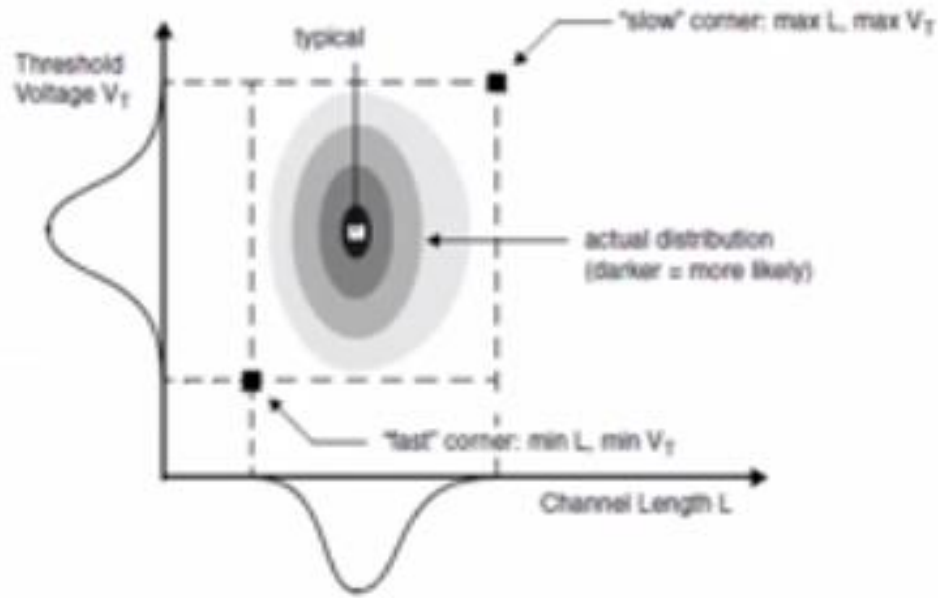
- P for Process
  - Systematic variation --- corrections needed in Fabrication flow
  - Random variation --- modeled by Gaussian distribution
- V for Voltage
  - All cells don't get same voltage (IR drop in rails)
  - Variation in power supply
- T for Temperature
  - Chip heats up during operation
  - All cells don't heat up by same degree

STA should guarantee that chip works across different corners

Corner Based STA

- Remember *delay = f1(slew_in, load, P, V, T)*





Operating Conditions

Condition	Process type	Voltage	Temperature	Cell Delay
Worst case	Worst	Low	High	High (Setup critical)
Best Case	Best	High	Low	Low (Hold critical)

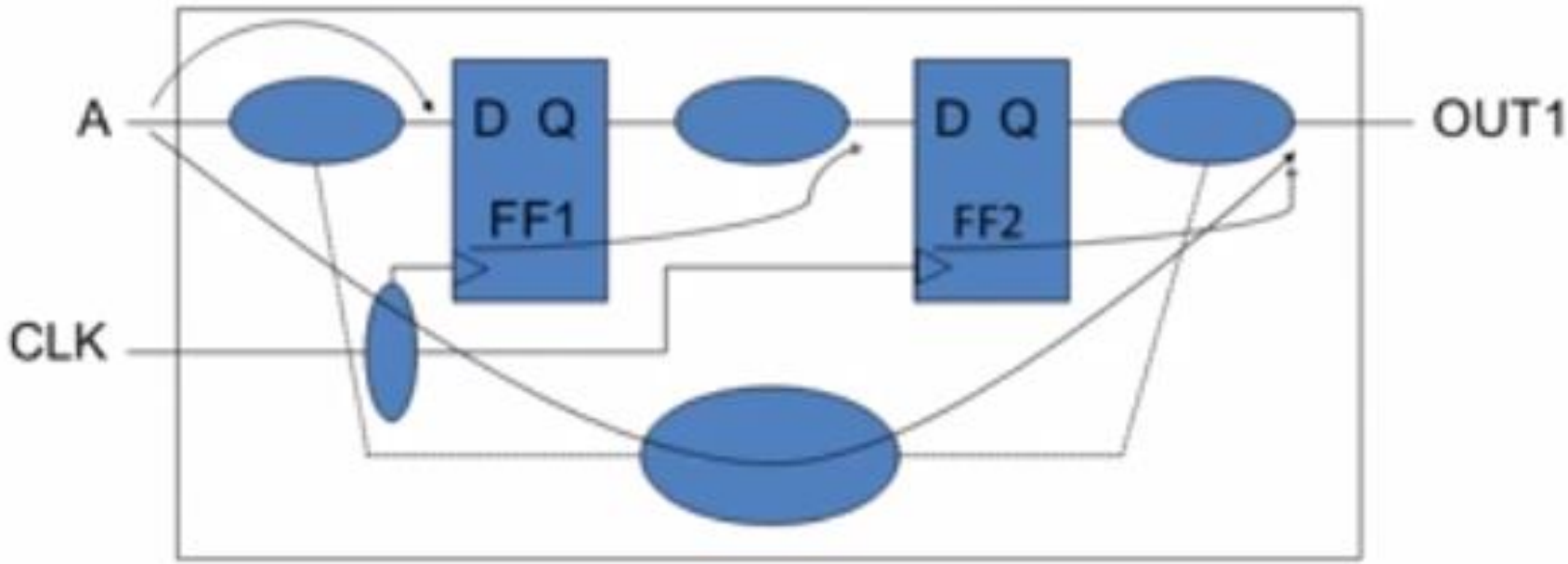
For 65nm typical operating condition can be 1.0V, 85C
Worst Case corner -> Worst process, 0.9V, 125C
Best Case corner -> Best process, 1.1V, 0 C

Pre and Post Layout STA

- Pre-Layout STA
  - No information about the nets
  - Estimated net delays
  - Used for resolving bottlenecks and finalizing STA strategy
  - Choose the worst corner (same as Synthesis)
  - Clocks ideal

- Post-Layout STA
  - Uses back annotated net information (SPEF / DSPF)
  - Done at various corners for Sign-Off
  - Clock network fully implemented

General Steps of STA



- Three general steps in Static Timing Analysis
  - Circuit is broken down into sets of timing paths
  - Delay of each path is calculated
  - Path delays are checked to make sure timing constraints have been met

Timing – few things to note

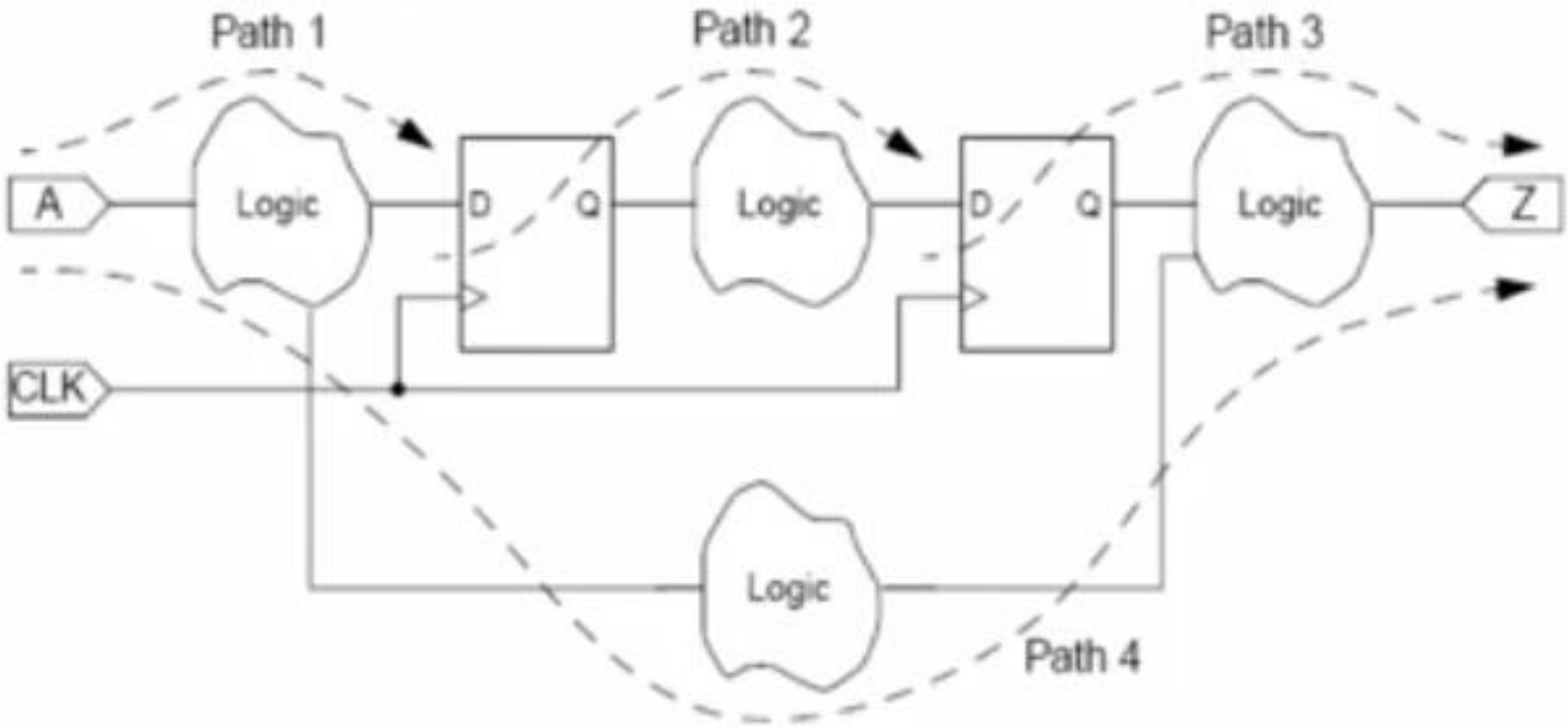
- Combinational cells
  - Propagation delay – function of output load and input slope
- Sequential cells
  - + Timing Checks – function of constrained pin transition and related pin transition

Delay Calculation

- Delay
  - Gate delay – from libraries
  - Net Delays – from post layout data (DSPF / SPEF)

- Calculation
  - Gate delays – Interpolated from the NLDM lookup tables
  - Net delays --- calculated using algorithms (matched with spice)

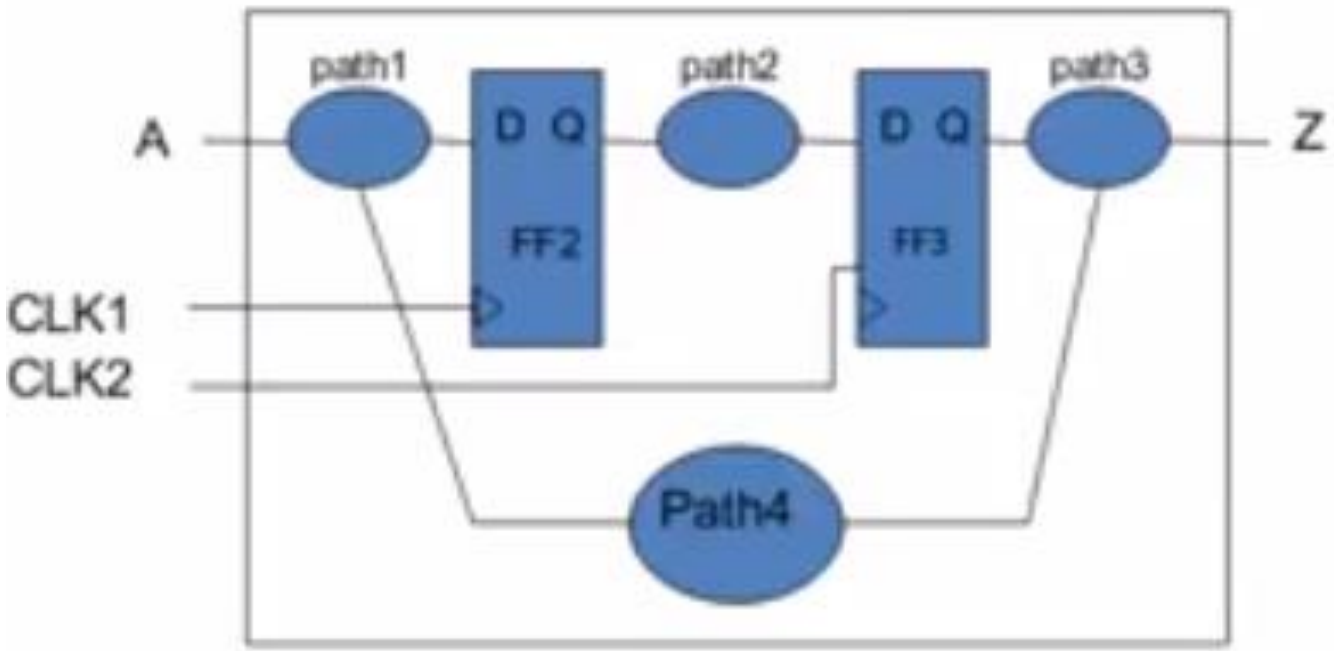
Timing Paths

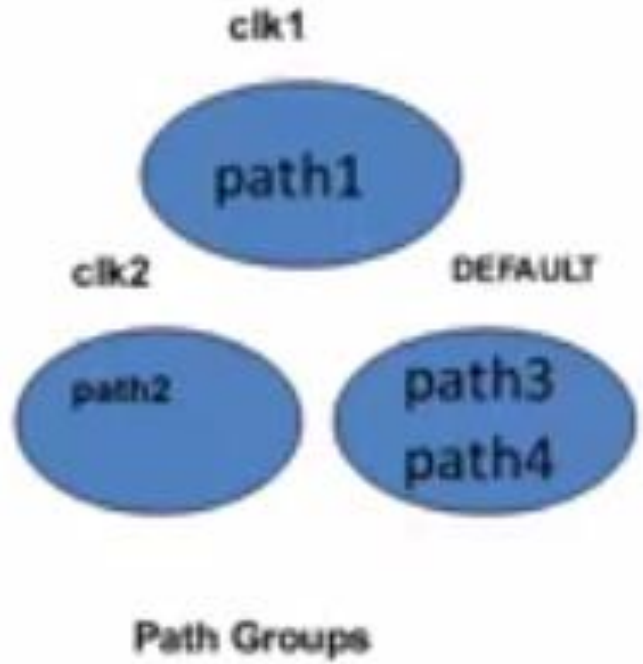


Timing Paths

- Path startpoint (Launch)
  - Input pin or
  - Clock pin of a Sequential element
- Path endpoint (Capture)
  - Output pin or
  - Data pin of a Sequential element
- Checking done at the capture point
- Launch part forms the data path

Grouped Timing Paths





- Timing paths are grouped into path groups by the clocks controlling their endpoints
- STA tools like PrimeTime generates timing reports by path groups

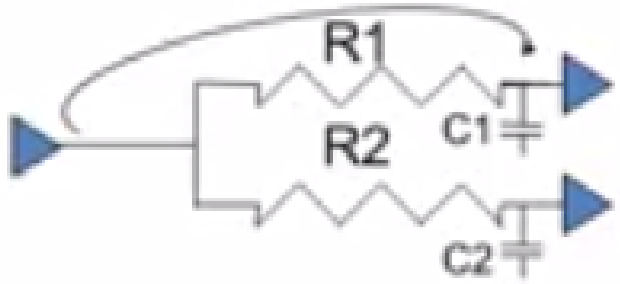
Timing Paths – Complete List

- Register-Register path
  - Constrained by clock only
- Input to register path
  - Clock ,Input delay (time given to external world on input side)
- Register to output path
  - Clock, Output delay (time given to external world on output side)
- Input to output path
  - Fully combinational path
  - Max_delay, min_delay or virtual clocks
- Clock Gating
- Async default – recovery and removal check

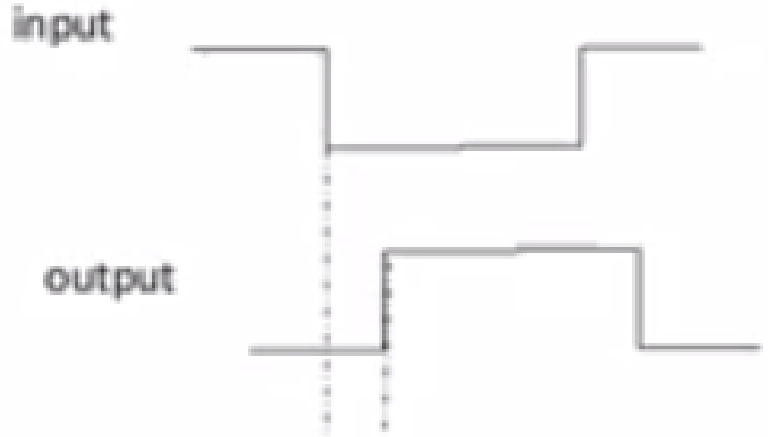
Timing Path Delay

The path delay is the sum of net and cell delays along the timing path

- Net Delay is the total time which needs to charge or discharge all parasitic capacitances of a given net



- Cell Delay shows a timing difference between output change and input change

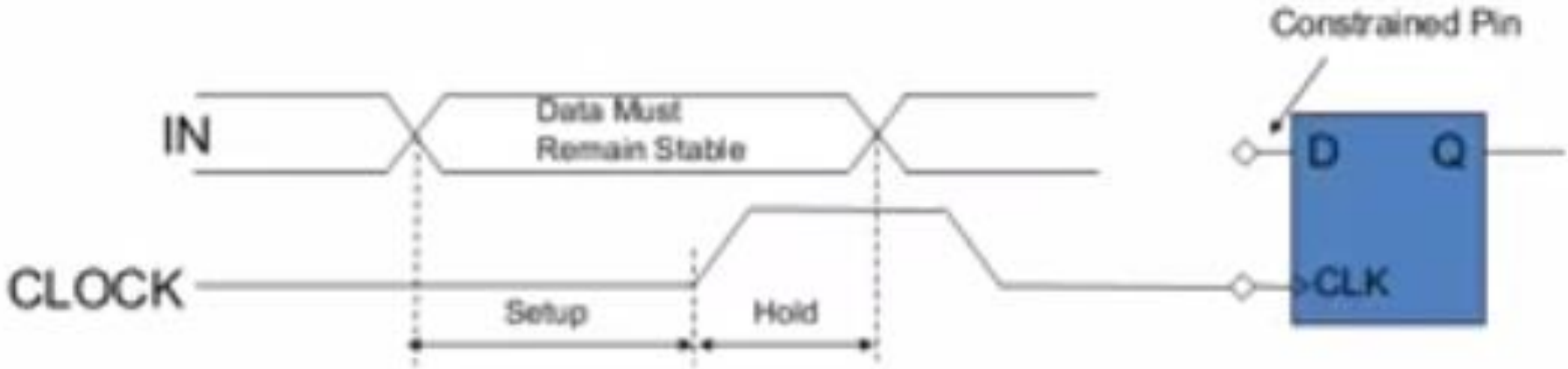


Basic Terminologies

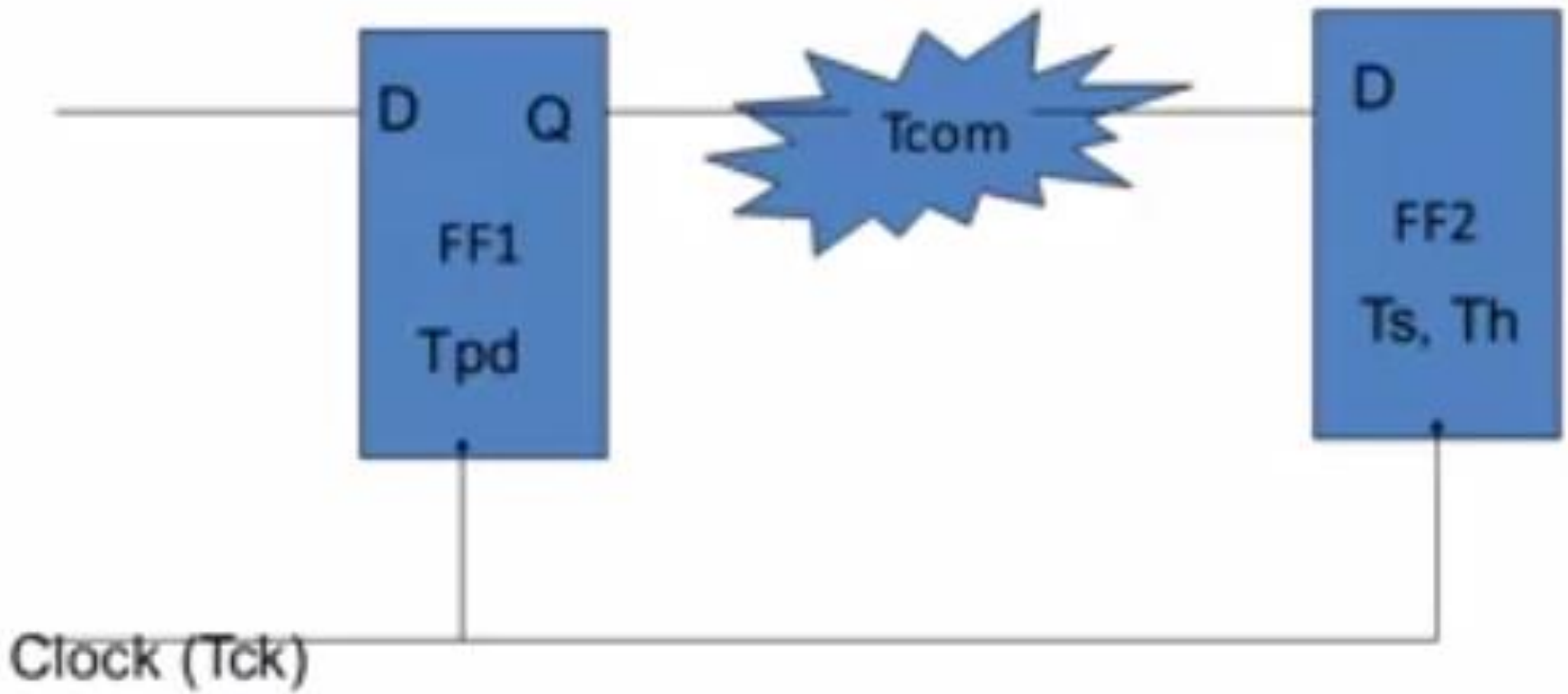
- Setup and Hold times
- Recovery and Removal times
- Pulse width
- Signal slew
- Clock latency
- Clock skew
- Slack and Critical path
- False path
- Multi-cycle path
- Input arrival time
- Output required time

Setup and Hold Times

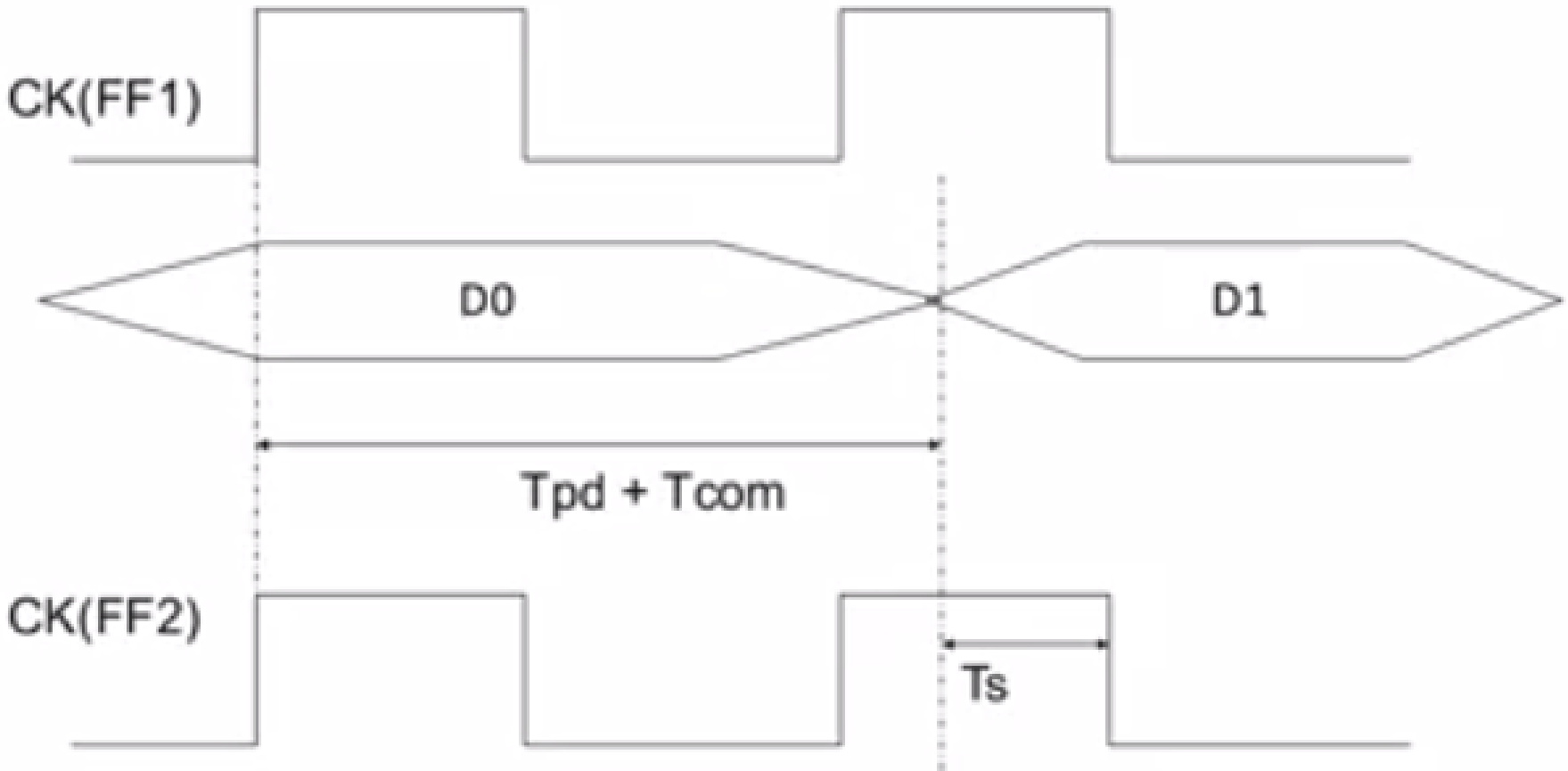
- For an edge triggered element, the time interval before the active clock edge during which the data should be unchanged, is called Setup Time
- The time interval after the active clock edge during which the data should be unchanged is called Hold Time



Classic Timing Problem



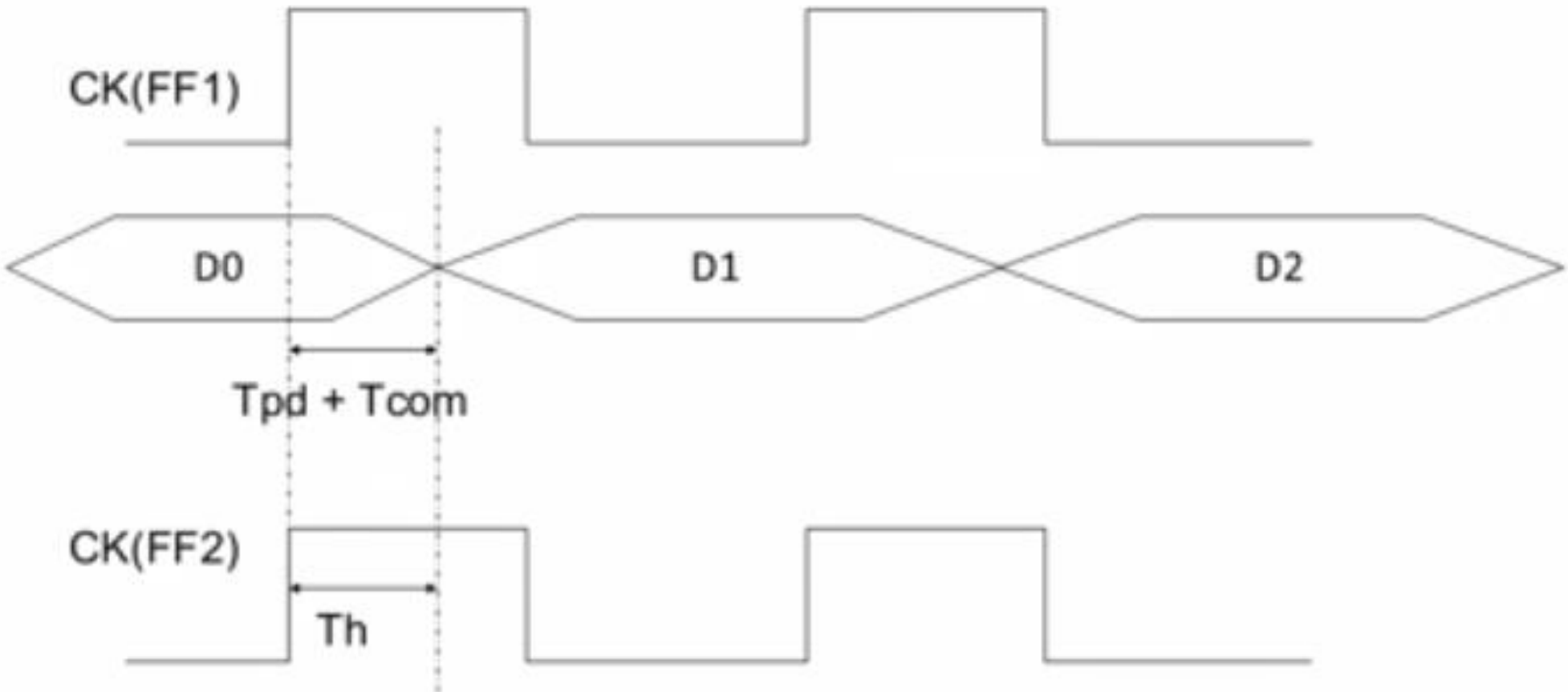
Setup Check



Setup Check

- Tpd + Tcom < Tck –Ts
- Total Data path delay = Tpd + Tcom
- Setup check limits the data path to a maximum value
- This check is also called “max delay check”
- Slack = Constraint – Delay
- What happens if setup violates on chip??

Hold Check

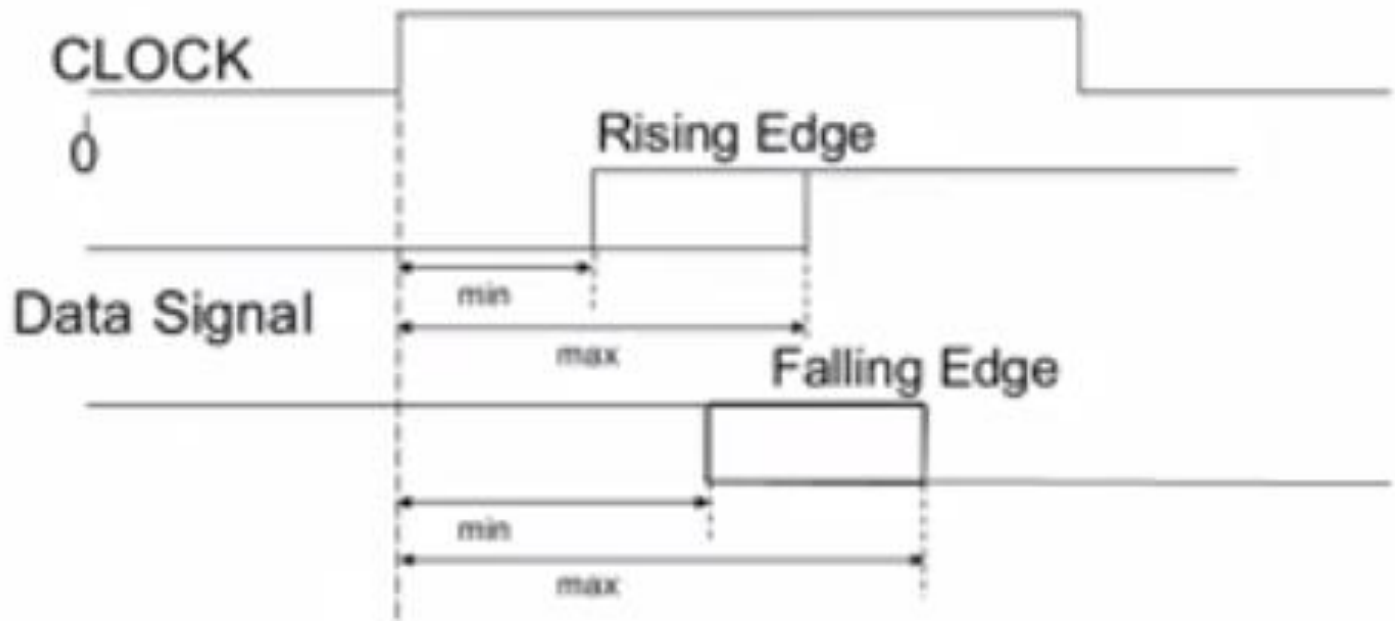


Hold Check

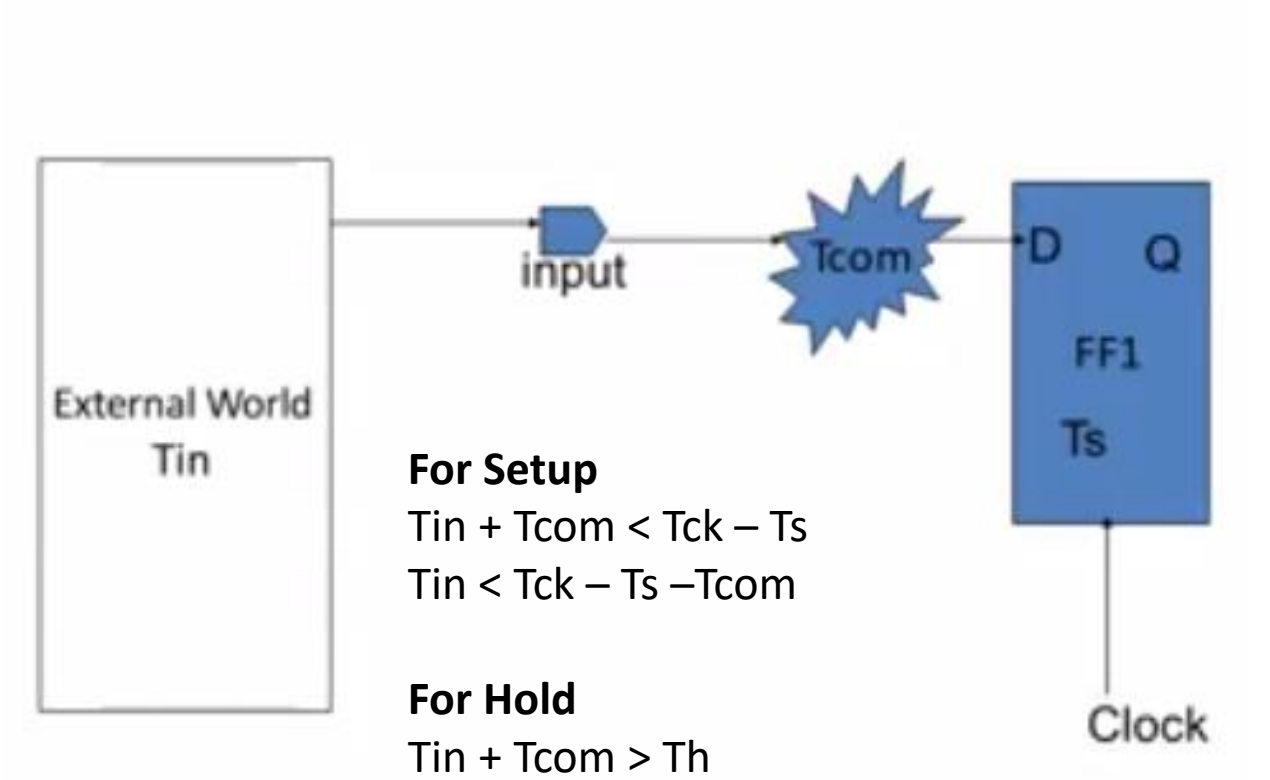
- Tpd + Tcom > Th
- Total Data path delay = Tpd + Tcom
- Hold check limits the data path to a minimum value
- This check is also called “min delay check”
- What happens if hold violates on chip??

Input Arrival Time

Arrival time defines the time interval during which a data signal can arrive at a pin in relation to the nearest edge of the clock signal that triggers the data transition



Input Delay



For Setup

Tin + Tcom < Tck – Ts

Tin < Tck – Ts –Tcom

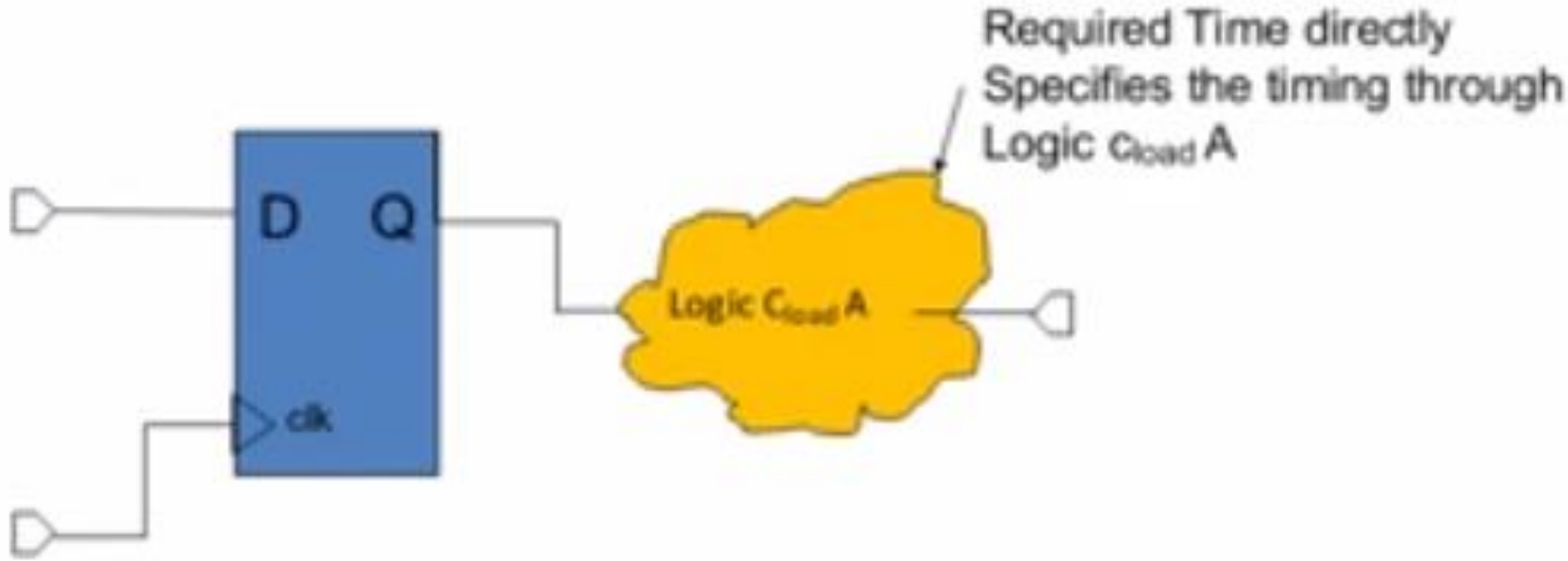
For Hold

Tin + Tcom > Th

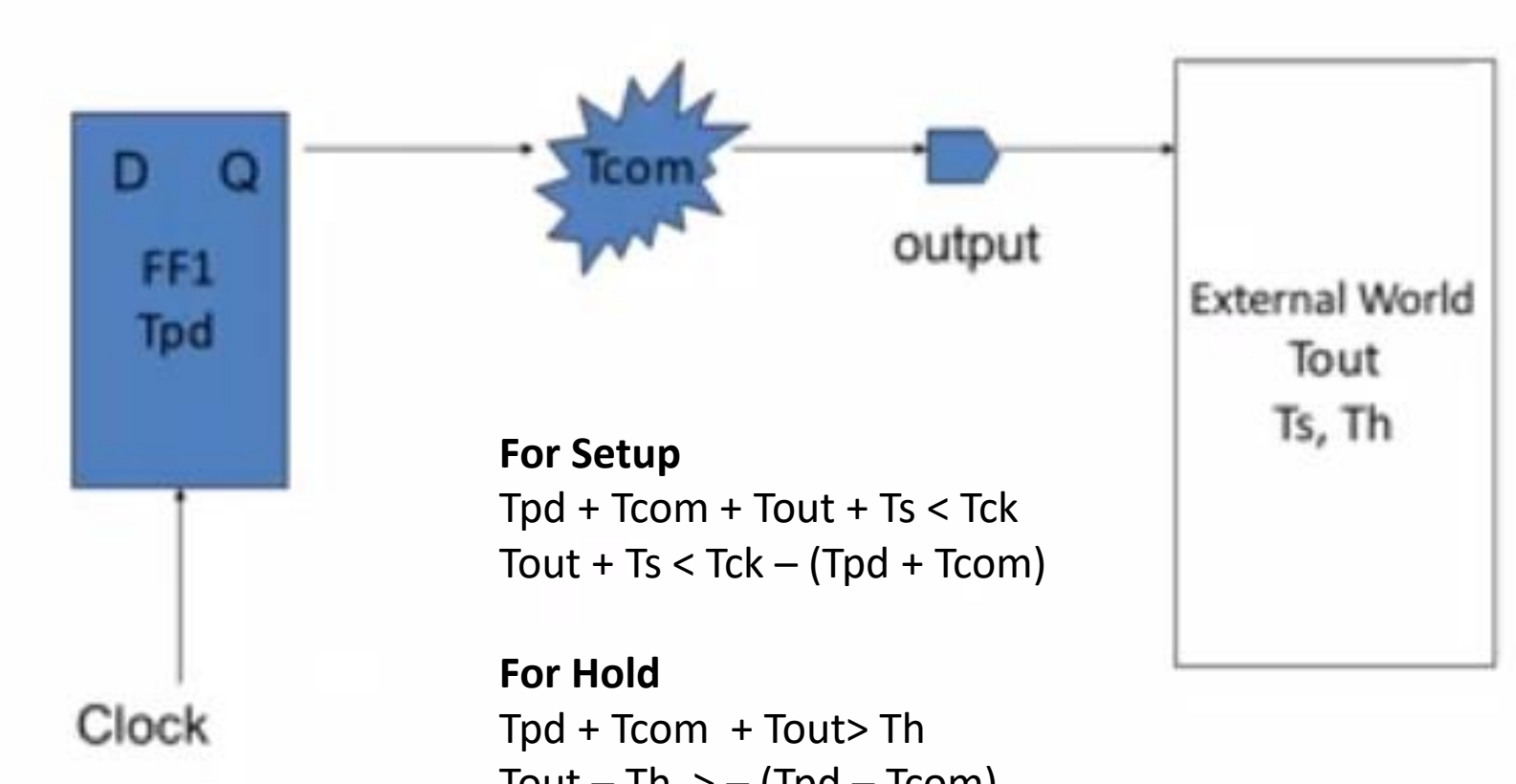
Tin > Th - Tcom

Output Required Time

- Output required time specifies the data required time on output ports



Output Delay



For Setup

Tpd + Tcom + Tout + Ts < Tck

Tout + Ts < Tck – (Tpd + Tcom)

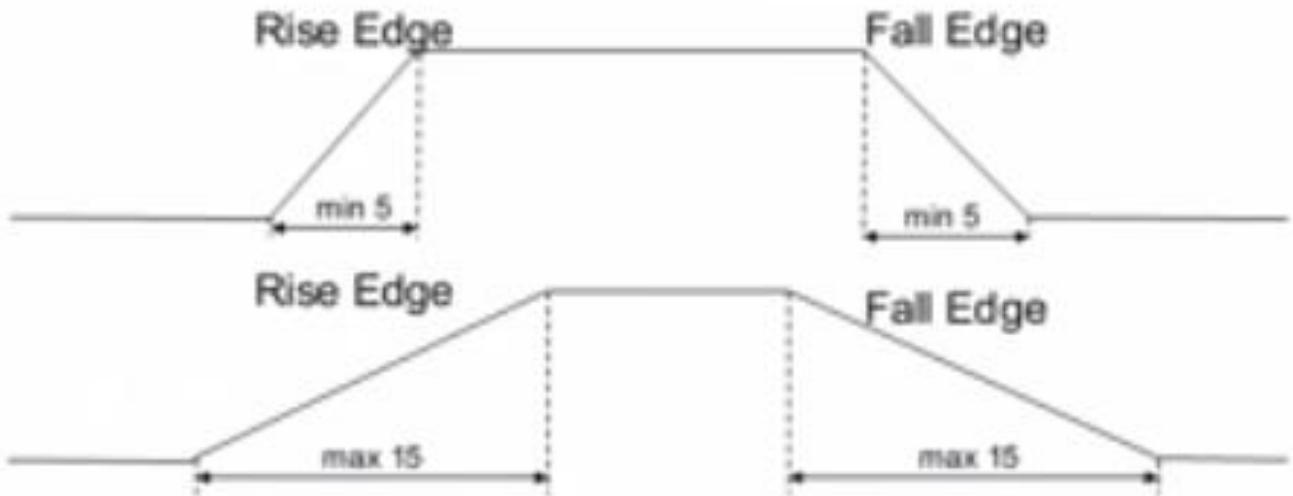
For Hold

Tpd + Tcom + Tout> Th

Tout – Th > – (Tpd – Tcom)

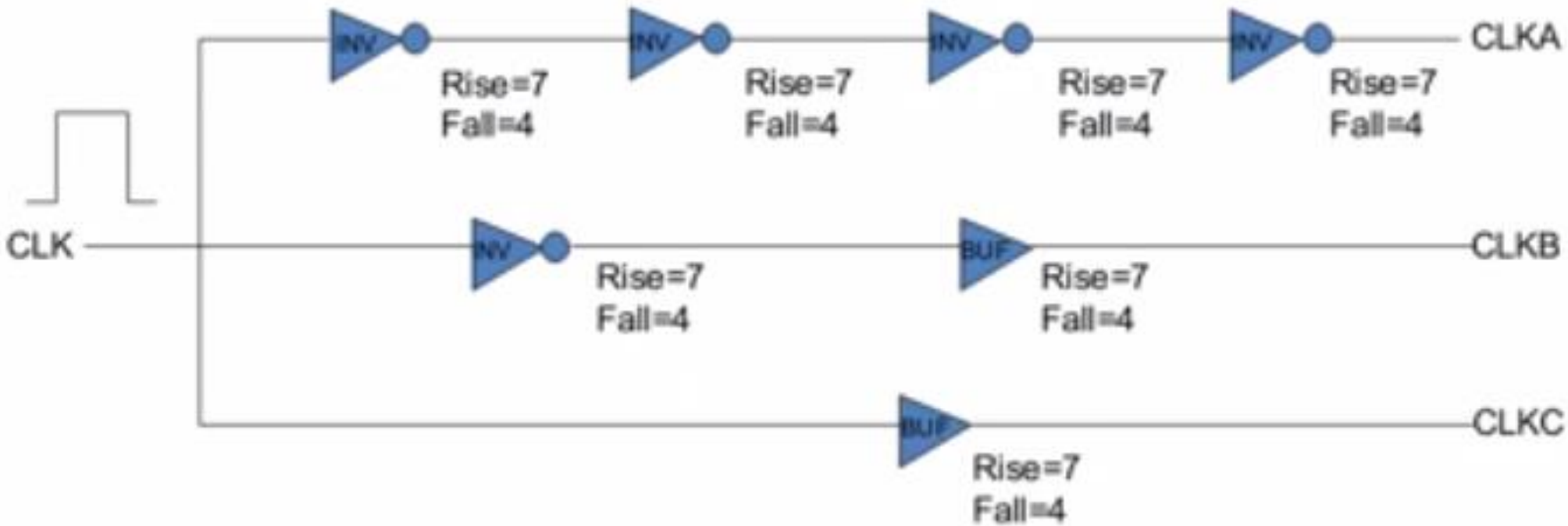
Pulse Width, Signal Slew

- Pulse width is the time between the active and inactive states of the same signal
- Signal Slew: Amount of time it takes for a signal transition to occur accounts for uncertainty in rise and fall times of the signal. Slew rate measurement is volts/sec



Clock Latency

Clock Latency is the difference between the reference (source) clock slew to the clock tree endpoint signal slew values. Rise and fall latency are specified below.



Clock Skew

- Clock skew is a measure of the difference in latency between two leaf pins in a clock tree

  For example, CLKA and CLKB

  rise = 22 – 8 = 14

  fall = 22 – 14 = 8

  or CLKB and CLKC

  rise = 8 – 7 = 1

  fall = 14 – 4 = 10

  or between CLKA and CLKC

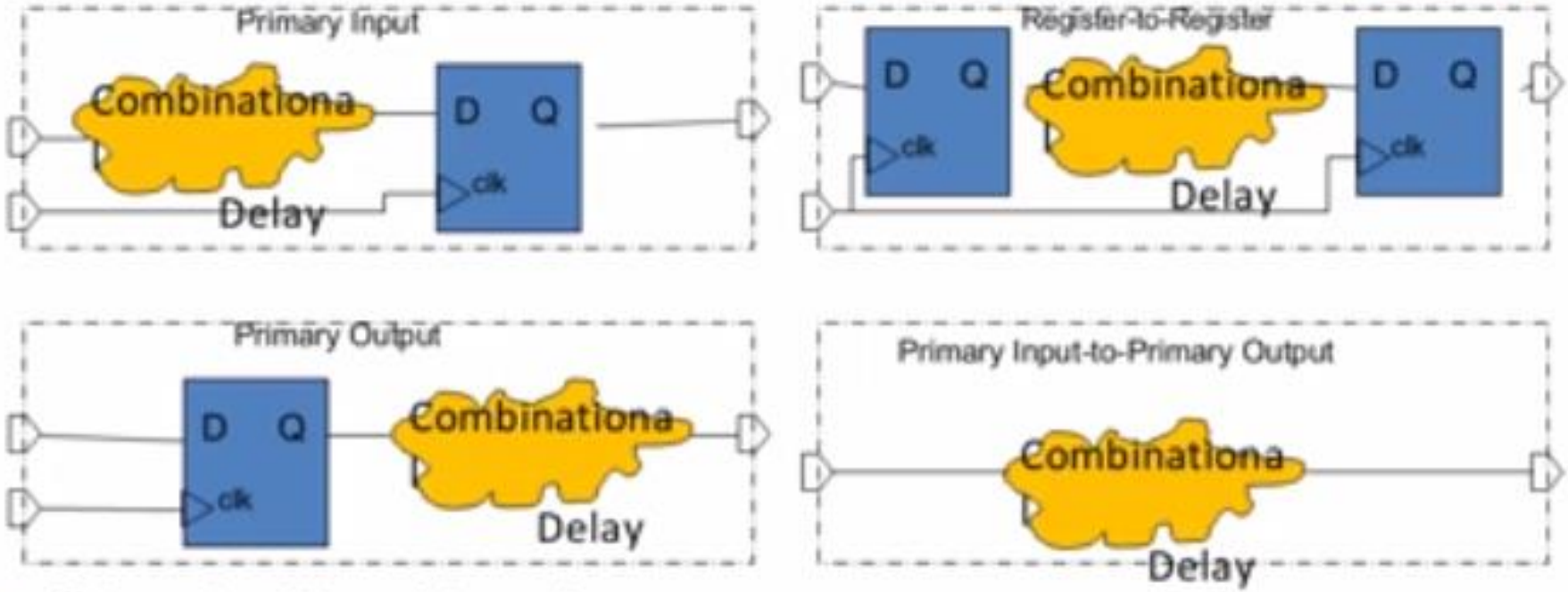
  rise = 22 – 7 = 15

  fall = 22 – 4 = 18

Slack and Critical Path

- Slack is the difference between the constraint required time and the arrival time (inputs and delays)
  - Negative slack specifies that the constraints have not been satisfies, while positive slack indicates that constraints have been met
  - Static timing analysis tool calculates the slack of each logic path, in order to find critical path
- Critical path is any logical path in the design that violates the timing constraints
- Any path with negative slack

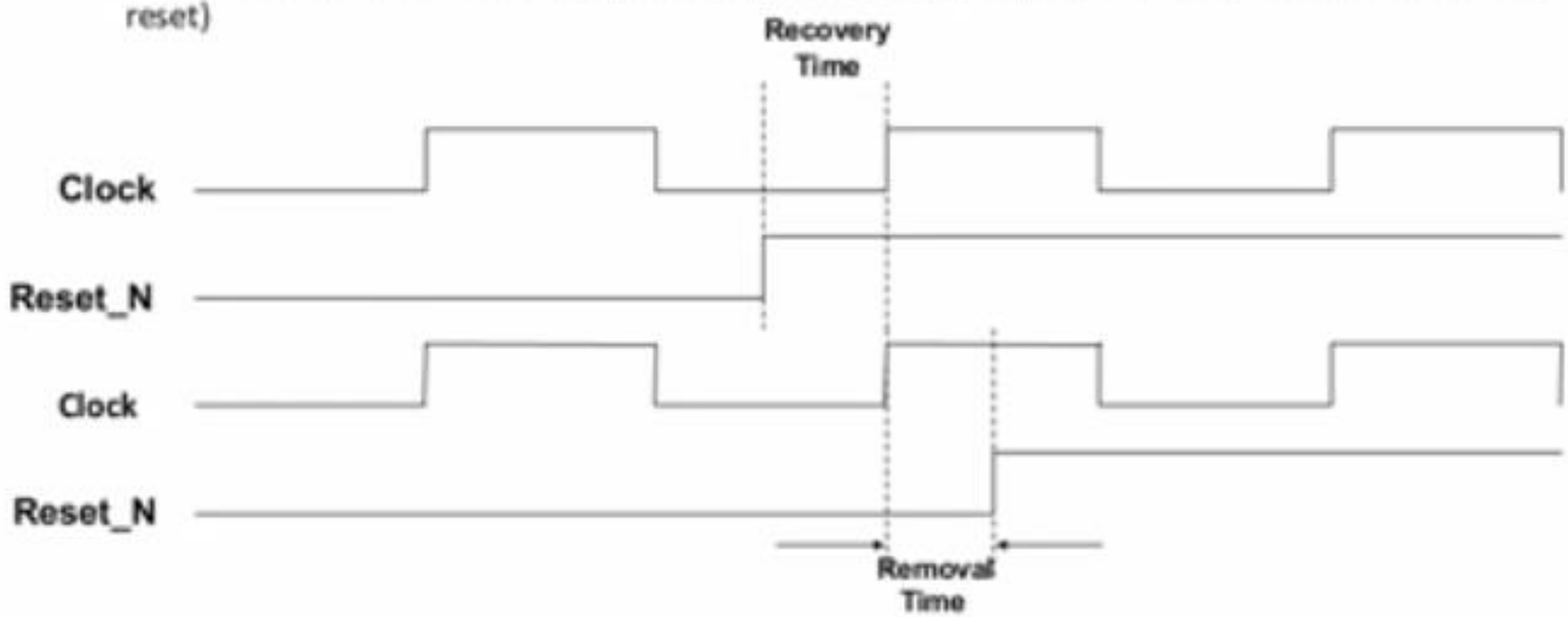
Slack Calculation



- Primary input to register path
  - Delays of input nets and combinational logic, up to the first sequential device
- Register to primary output paths
  - Start at a sequential device and CLK to Q transition delay + the combinational logic delay + external delays
- Register-to register paths
  - Delay and setup/hold times between sequential devices for synchronous clocks + source and destination clock propagation times
- Primary input to primary output paths
  - Delays of input nets + combinational logic delays + external delay

Recovery and Removal Times

- Recovery time
  - The time available between the asynchronous signal going inactive to the active clock edge (like setup time for set/reset)
- Removal time
  - The time between active clock edge and asynchronous signal going inactive (like hold time for set reset)

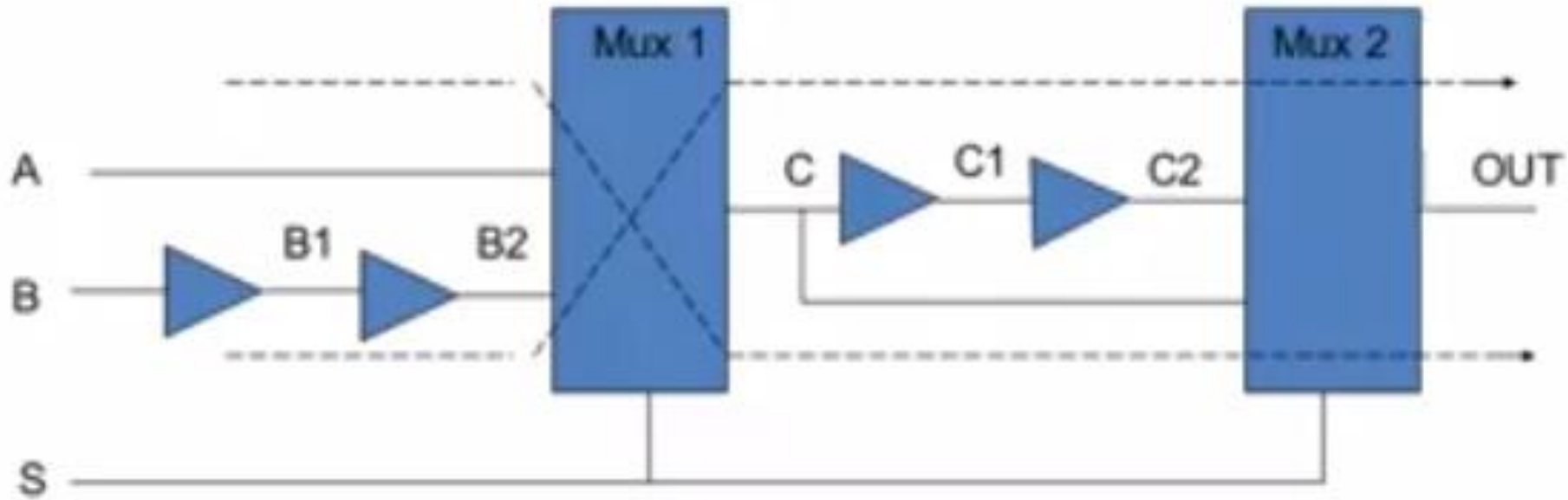


Timing Exceptions

- False paths
- Multicycle paths
- Case analysis
- Disable Timing
- Max / Min delays

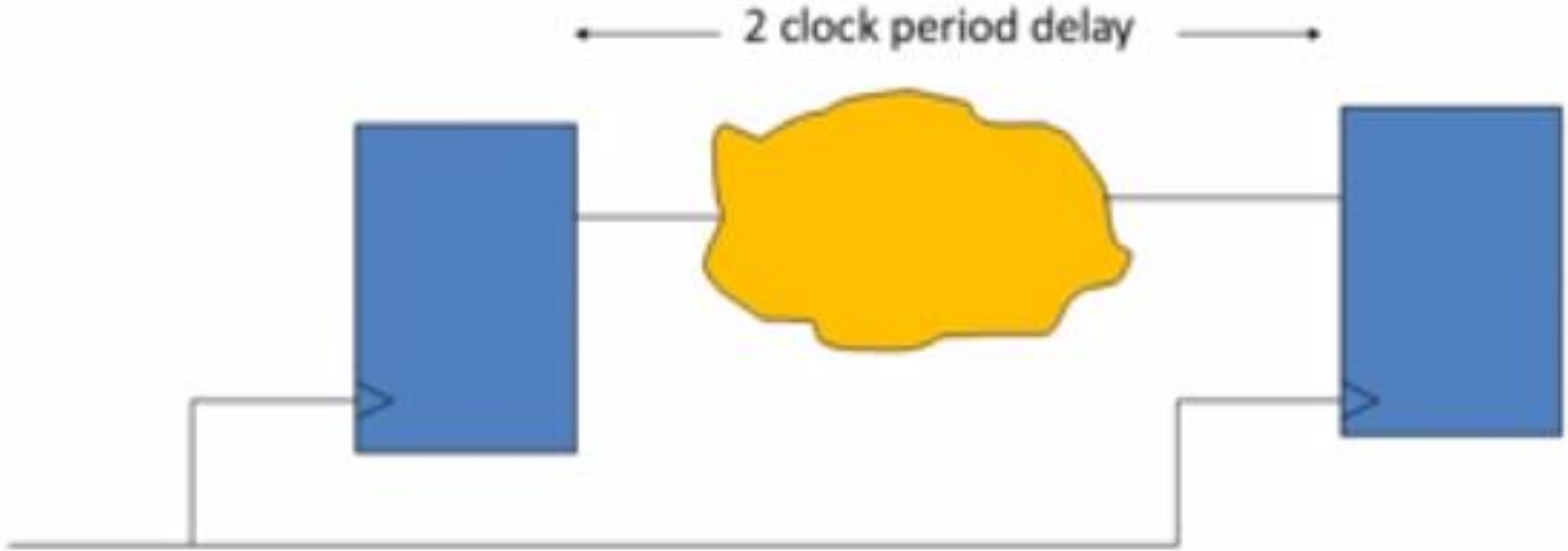
False Paths

Paths which physically exist in a design but are not logic paths.
These paths never get sensitized under any input condition



Multi-cycle Paths

- There are data paths that require more than one clock period for execution



Boundary Conditions

- *set_load*
  - Set a lumped capacitance value on an output port
- *set_driving_cell*
  - Set the external driver to be a particular cell (usually a common standard cell with a nominal drive strength)
- *set_input_transition*
  - Specify transition times of input signals
  - **Prefer to use this for top-level and set_driving_cell for block-level constraints**

STA Flow

- Read design data
  - Library, design, parasitics
- Apply constraints
  - Clocks, input delays, output delays etc
- Check
  - Design is properly and fully constrained
  - DRC violations (What happens if it violates?)
- Report
  - Max paths in worst corners
  - Min paths in best corners

Exercise

Assume
Clock Period = 20ns
Setup = 2ns
Hold = 2ns
Combinational Delay Max = 5ns
Combinational Delay Min = 3ns
Clock -> Q delay max = 3ns
Clock -> Q delay min = 1ns

Lets
1. Calculate Setup slack
2. Calculate Hold slack
3. Estimate input delay
4. Estimate output delay